G300
TECHNICAL DESCRIPTION

A). GENERAL DESCRIPTION

The G300 GMRS radio is a self-contained transceiver unit with integral antenna intended for use as a general communication tool. It is designed to operate on all 22 channels allocated by the FCC. This model also features user selectable sub-audible tones for channel quieting. The useable range, while dependent upon terrain and other radio propagation principles, is typically two miles. The G300 uses the maximum transmit power allowed to help ensure the maximum communication range.

Features include: 22 GMRS Channels, Digital Receive Volume Control, Channel Monitor, Page and LCD Display. The unit is equipped with an external Headset option connector. Four AAA alkaline batteries that are readily available in retail outlets supply operating power. An automatic power savings feature allows the typical standby battery life to extend to more than 10 days.

B). FREQUENCY DETERMINING CIRCUITS

The fundamental frequency for both the transmitter and the receiver local oscillators are controlled by a phase lock loop (PLL) circuit IC201 (Toshiba TB31202, or equipvalent). The frequency of operation of the FRS voltage controlled oscillator (VCO), composed of Q301 and Q302 operating in cascade is phase locked to a voltage controlled crystal reference (VCXO) operating at 20.95MHz (X202).

The VCO is locked to the fundamental of the transmit signal in the transmit mode and is locked to the receive 1st LO (Fundamental channel frequency minus 21.4MHz) in the receive mode. The crystal reference frequency is shared with the 2nd LO of 20.95MHz.

C). TRANSMITTER CIRCUITS

The transmitter amplifies the 0 dBm signal from the VCO to approximately 27dBm that is fed to the antenna. The transmitter is a three stage amplifier composed of Q1,3 and Q11. The first two stages are operated class A and the final is operated class B in full saturation to help prevent unwanted amplitude modulation. The fundamental transmit signal is fed through an elliptical low pass filter (5-pole, 2 zero) in order to suppress the harmonics to below –50 dBc. The desired frequency modulation of the carrier is accomplished by modulating the current in the VCO directly with the microphone audio signal. The microphone audio is conditioned with a three-pole high pass filter at 300 Hz (IC5C,D), a hard clipper circuit (IC5B) to limit maximum deviation to +/- 2.5 kHz and a three-pole low pass or splatter filter at

2.8 kHz (IC5A). The low pass filter insures that the occupied bandwidth of the FM modulated signal meets FCC requirements under all input conditions.

D). RECEIVER CIRCUITS

The received signal from the antenna is band limited to 600 Mhz by the transmitter harmonic filter. The desired signal is fed to a low noise amplifier (LNA – Q6) centered from 460 to 470 MHz that provides approximately 10 dB of gain. The output of the LNA is filtered with a Band Pass filter (C41,L16,C43,L17,C15,L5) with pass-band of 460 to 470 MHz and stopband attenuation of 10 dB. The filtered receive signal is one input to the 1st mixer (Q8), the other mixer input (1st LO) is the output of the VCO at the desired channel frequency minus 21.4MHz. The output of the mixer is tuned to the 1st IF of 21.4 MHz.

The 1st IF is transformer coupled for impedance matching to a X-tal filter centered at 21.4MHz with a bandwidth of +/-3.75Hz. The filtered 1st IF is then amplified by Q9 and fed to the 2nd mixer input of the multi-function receiver IC (IC1). The 2nd LO (20.95 MHz) is generated by VCXO that is the reference frequency for the PLL. The 2nd mixer output of 450 kHz is filtered through a 4 section ceramic filter that in combination with the 21.4MHz X-tal filter provides approximately 50 dB of adjacent channel attenuation. The 450 kHz 2nd IF is then amplified, limited and fed to a quadrature detector for FM demodulation. The resulting audio output signal is bandpass filtered from 300 to 3 kHz (Q22) and amplified to provide 150mW of audio power (IC2). A squelch circuit is provided (IC1 pins 10 through 11) to mute the receiver noise under low signal conditions. The squelch circuit amplifies and detects noise in a narrow bandwidth at approximately 5 kHz. When the detected noise exceeds a threshold set to trigger at approximately 9 dB SINAD receive signal strength, the audio output is muted.

E). TRANSMIT/RECEIVE SWITCH

When the radio is in the transmit mode, pin diode switches D13 and D1 are both turned on (representing less than 0.7 ohms). D13 allows the transmit signal to pass to the antenna and D1 shorts one leg of a T matching network (L3, L15 and C4) to ground in the receive path. This results in a parallel tuned circuit high impedance being presented to the transmit signal so that the receive path does not load the transmit signal. In the receive mode, both D13 and D1 are off, resulting in the antenna signal being coupled into the receive LNA through the 50 ohm T matching network and the unwanted load of the transmit final amplifier is reduced to less than 1 pF by D1.

F). RADIO CONTROL CIRCUIT

A microprocessor (CPU1) is used to control the transceiver. User stimuli is provided through a tack switch for PTT (push to talk), along with the keypad for channel selection, channel monitor, receive volume, and page. Pressing

the PTT switch instructs CPU1 to switch to the transmit mode. This is accomplished by loading the proper channel counter information through a 3-wire serial link to the PLL IC (IC201), turning on power to the PLL and VCO, microphone and transmit audio circuits and the transmit RF amplifiers. Pressing the call switch causes the microcontroller to transmit a warbling tone for approximately 3 seconds on the current channel selected that is used to notify another person with FRS radio that you wish to communicate. Pressing the channel Up/Down buttons (active in receive mode only) instructs CPU1 to increment or decrement respectively the channel frequency by one channel from the channel previously selected.

In receive mode the microcontroller periodically switches on the VCO and receiver power and checks for a valid received signal by monitoring the squelch circuit output. If a valid signal is present, the audio output is turned on and receive power is maintained for the duration of the valid signal. If the valid signal is removed or no valid signal was present, the microcontroller removes power from the VCO and receiver, waits for approximately 100 ms and then checks again. This periodic cycling of the power to the receiver circuits results in a much longer battery life vs. leaving power on continuously. The total period of the cycling is selected such that the worst case delay in 'seeing' a valid receive signal is not disruptive to normal two-way voice communications.