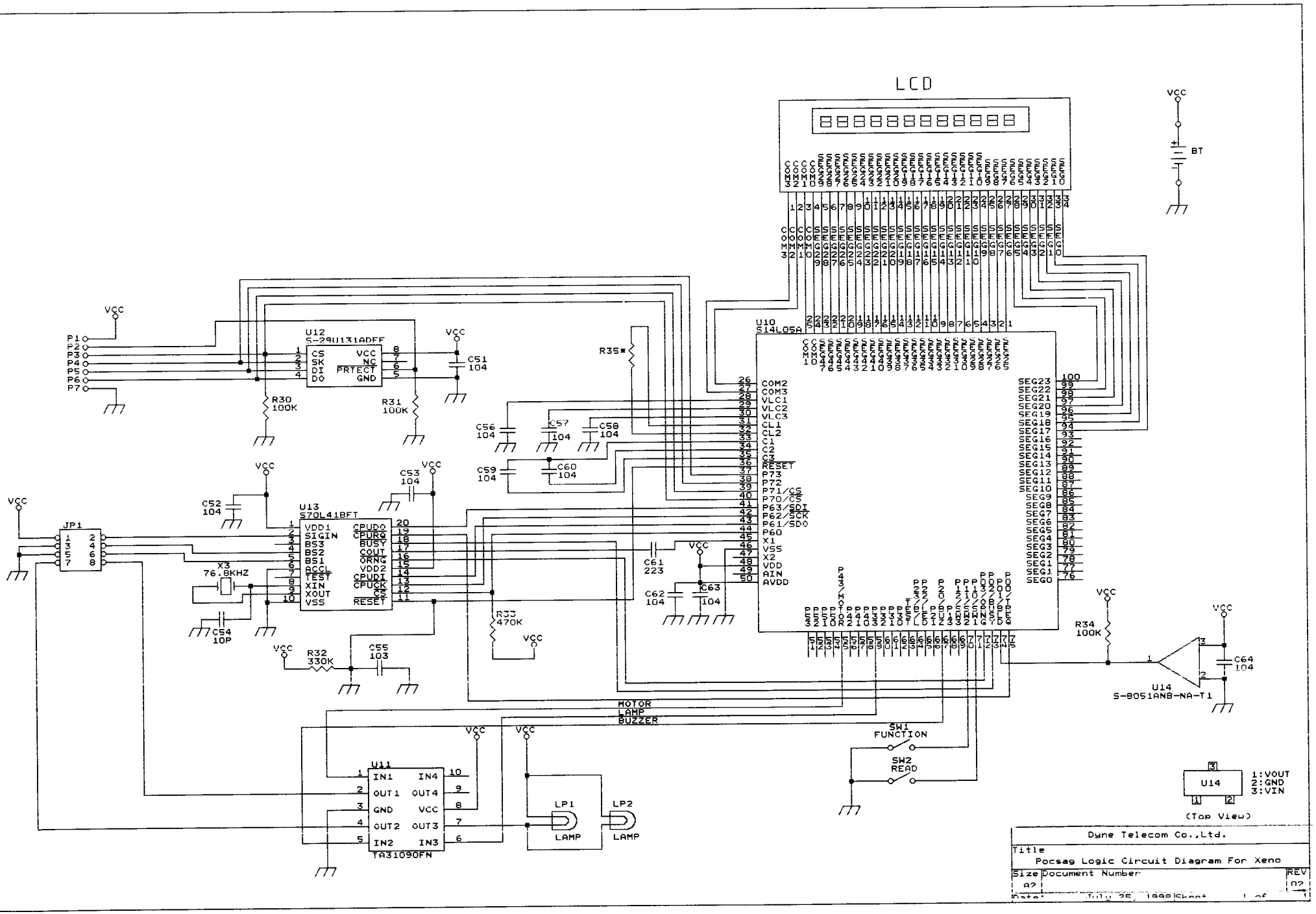
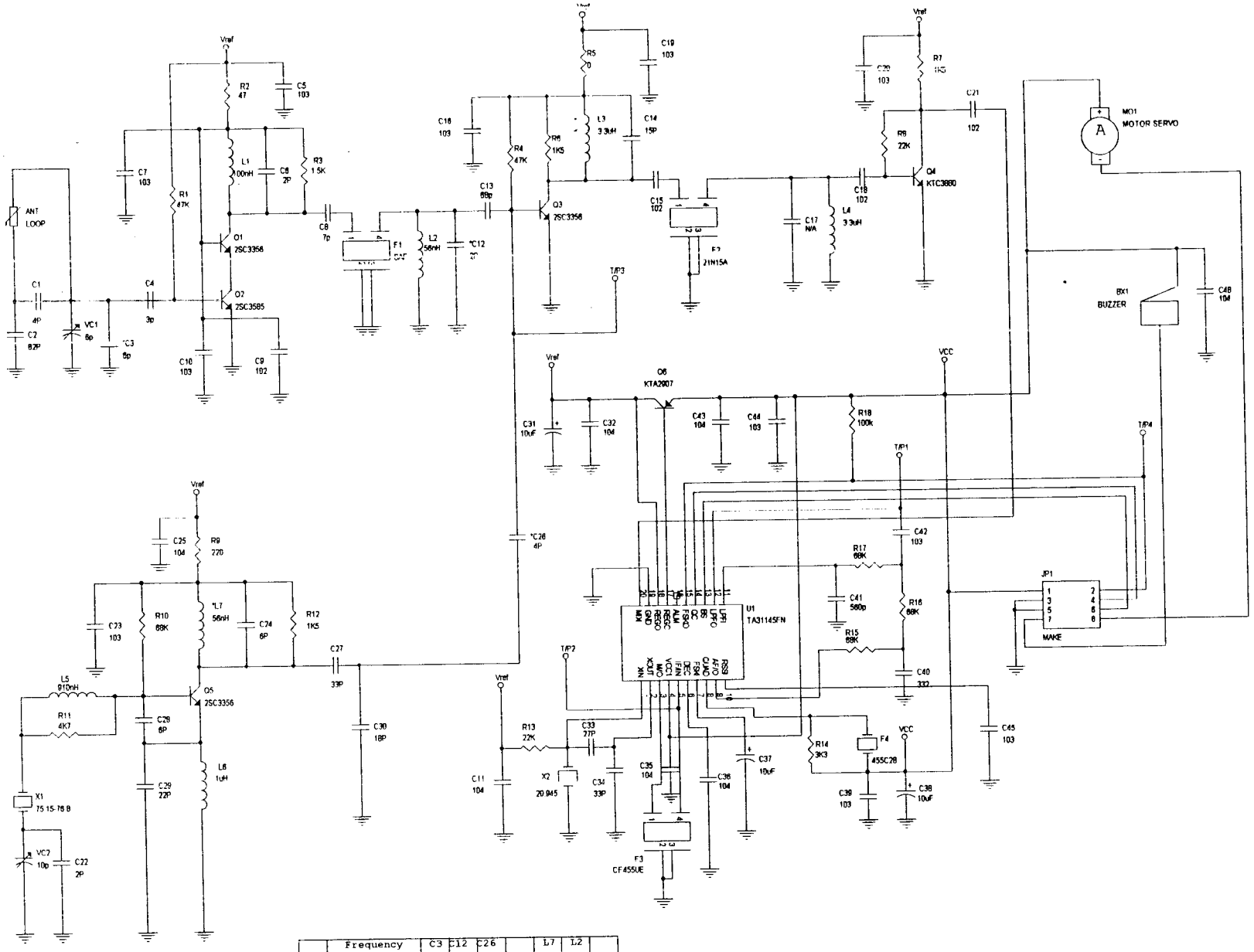

LCD
U10
S14L05A
U12
S-29U131ADFF
U13
S70L41BFT
U11
TA31090FN
U14
S-8051ANB-NA-T1
JP1
X3
76.8KHZ
BT
SW1
FUNCTION
SW2
READ
LP1
LAMP
LP2
LAMP
MOTOR
LAMP
BUZZER
VCC
P1
P2
P3
P4
P5
P6
P7
R30
100K
R31
100K
R32
330K
R33
470K
R34
100K
R35*
C51
104
C52
104
C53
104
C54
10P
C55
103
C56
104
C57
104
C58
104
C59
104
C60
104
C61
223
C62
104
C63
104
C64
104
1:VOUT
2:GND
3:VIN
(Top View)
Dyne Telecom Co.,Ltd.
Title
Pocsag Logic Circuit Diagram For Xeno
Size
A2
Document Number
REV
02
Date:
July 25, 1998
Sheet
1 of
1



	Frequency	C3	C12	C26		L7	L2
A	137-143Mhz	15p	4p	9p		68nH	56nH
B	143-151Mhz	10p	4p	4p		56nH	56nH
C	151-159Mhz	8p	2p	4p		68nH	68nH
D	159-167Mhz	6p	2p	4p		56nH	56nH
E	167-175Mhz	6p	2p	4p		56nH	56nH

Title: Pocsag Logic Circuit Diagram For Xeno

Size: A3 | Document Number: 150Mhz RF | Rev

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