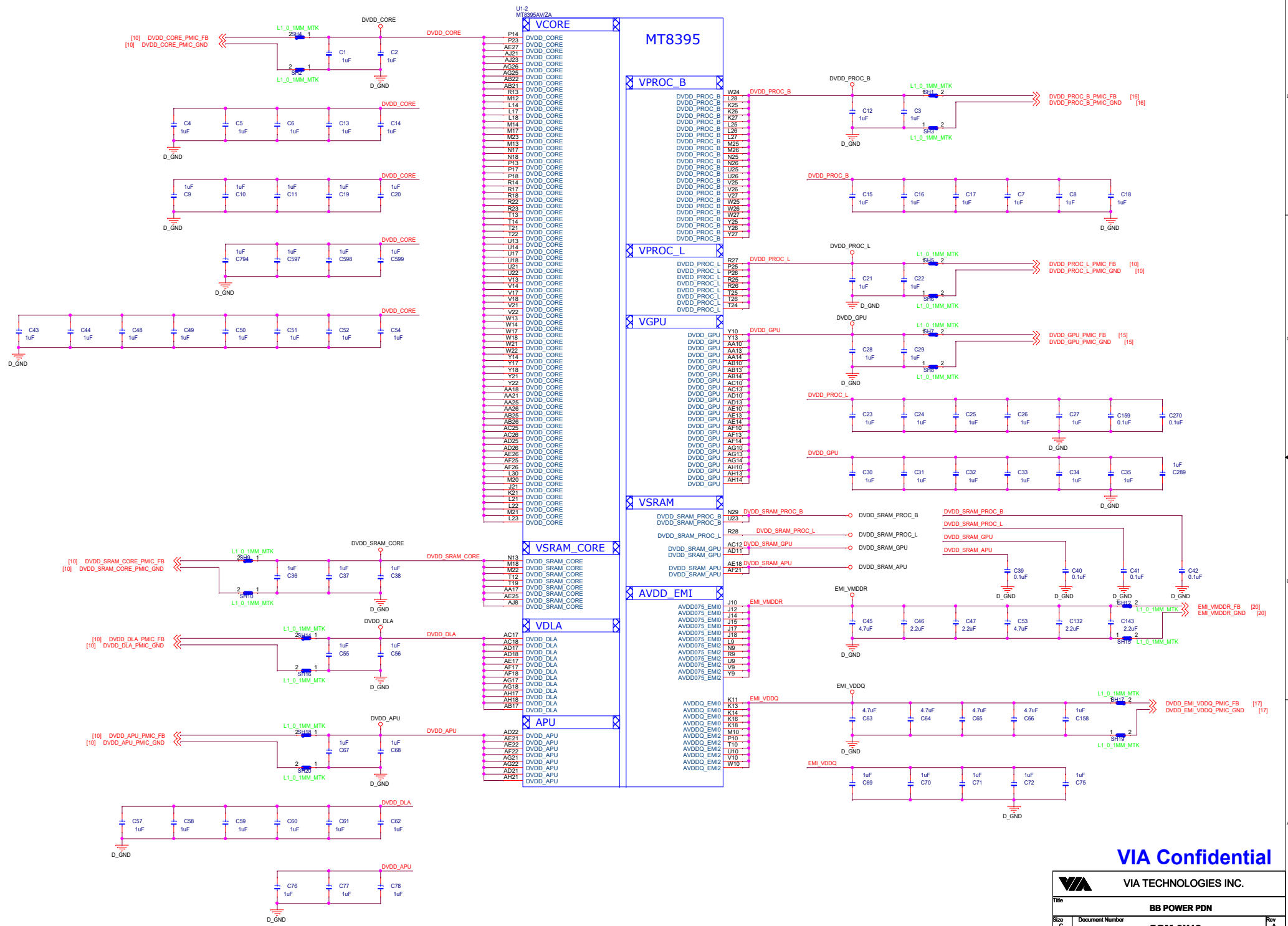
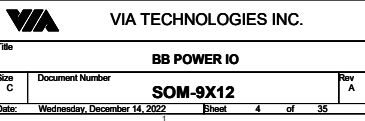
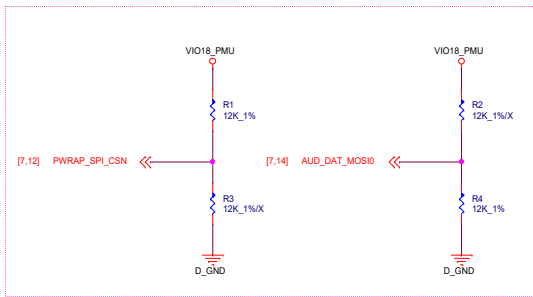


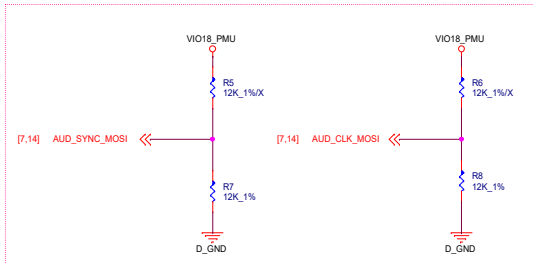


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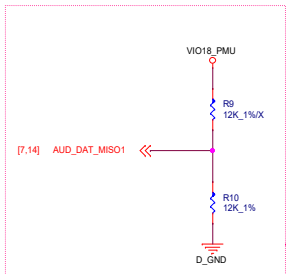




Note: 1



Note: 2



Note: 3

Schematic design notice:

Note 1: "PWRAP_SPI_CSN" and "AUD_DAT_MOSI0" pin features in trapping pin to enable JTAG.

PWRAP_SPI0_CSN	AUD_DAT_MOSI0	AP JTAG	ADSP or SCP JTAG
H (Default)	L (Default)	N/A	N/A
H	H (by external PU)	DMIC2_SCK, PCM_DO PCM_CLK, PCM_DI PCM_SYNC	N/A
L (by external PD)	L	MSDC1_CLK, MSDC1_CMD, MSDC1_DAT0, MSDC1_DAT1, MSDC1_DAT2	ADSP JTAG: PCIE_WAKE_N, PCIE_PERESET_N, PCIE_CLKREQ_N CMMRST, CMMPDN
L (by external PD)	H (by external PU)	MSDC1_CLK, MSDC1_CMD, MSDC1_DAT0, MSDC1_DAT1, MSDC1_DAT2	SCP JTAG: SPIM1_CSB, SPIM1_CLK SPIM1_MO, SPIM1_MI USB_DRV_VBUS_1P

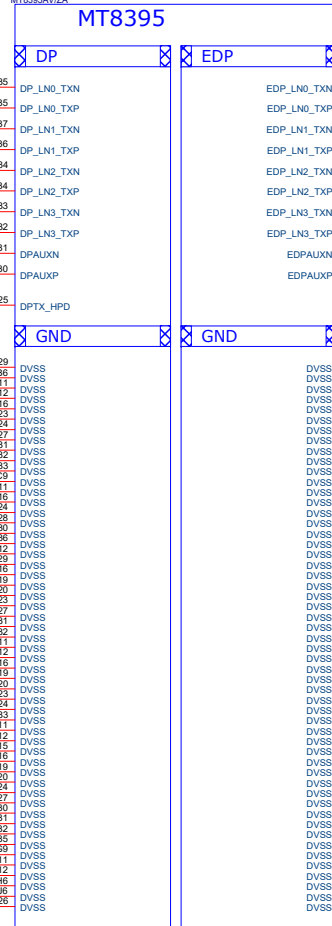
Note 2: "AUD_SYNC_MOSI" and "AUD_CLK_MOSI" pin features in trapping pin to booting (eMMC/UFS/SPI NOR).

AUD_SYNC_MOSI	AUD_CLK_MOSI	Storage Booting
L (Default)	L (Default)	Only eMMC boot
L	H (by external PU)	Only UFS boot
H (by external PD)	L	Only SPI NAND boot
H (by external PD)	H (by external PU)	Only SPI NOR boot

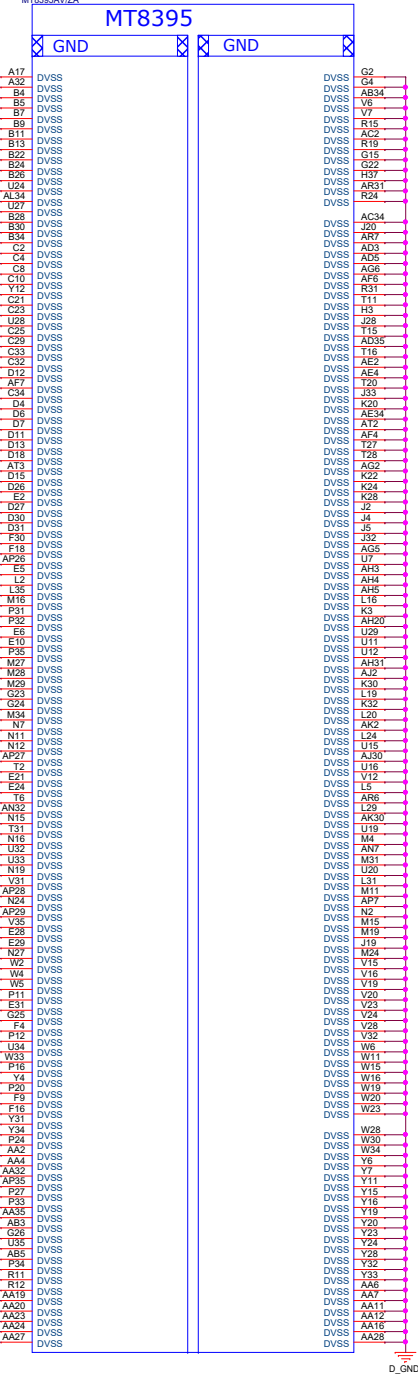
Note 3: "AUD_DAT_MISO1" is trapping pin to select VEMC Voltage.

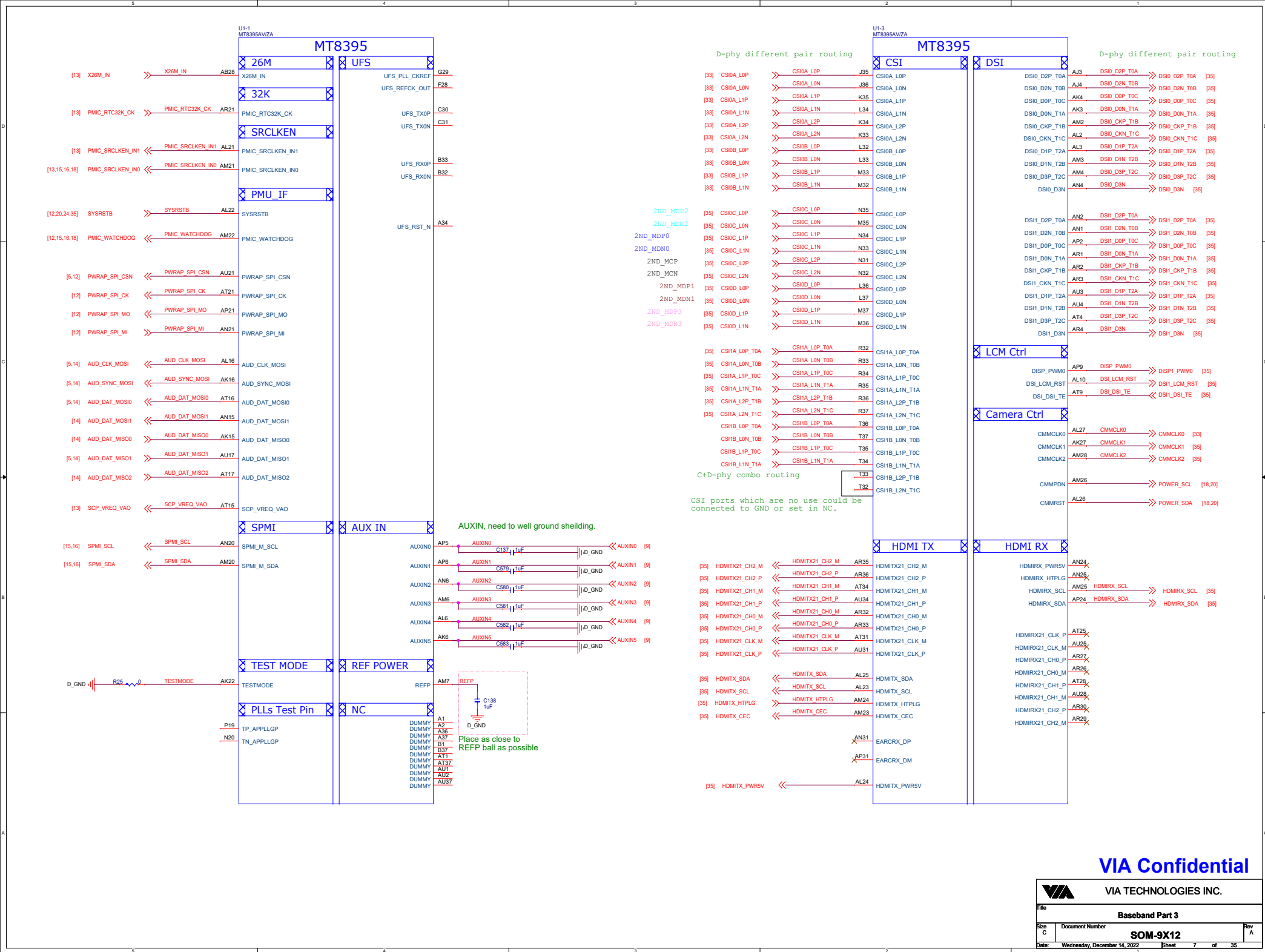
AUD_DAT_MISO1	VEMC Voltage
L (Default)	VEMC=3.0V
H (by external PU)	VEMC=2.5V

U1-7
MT8395AV/ZA

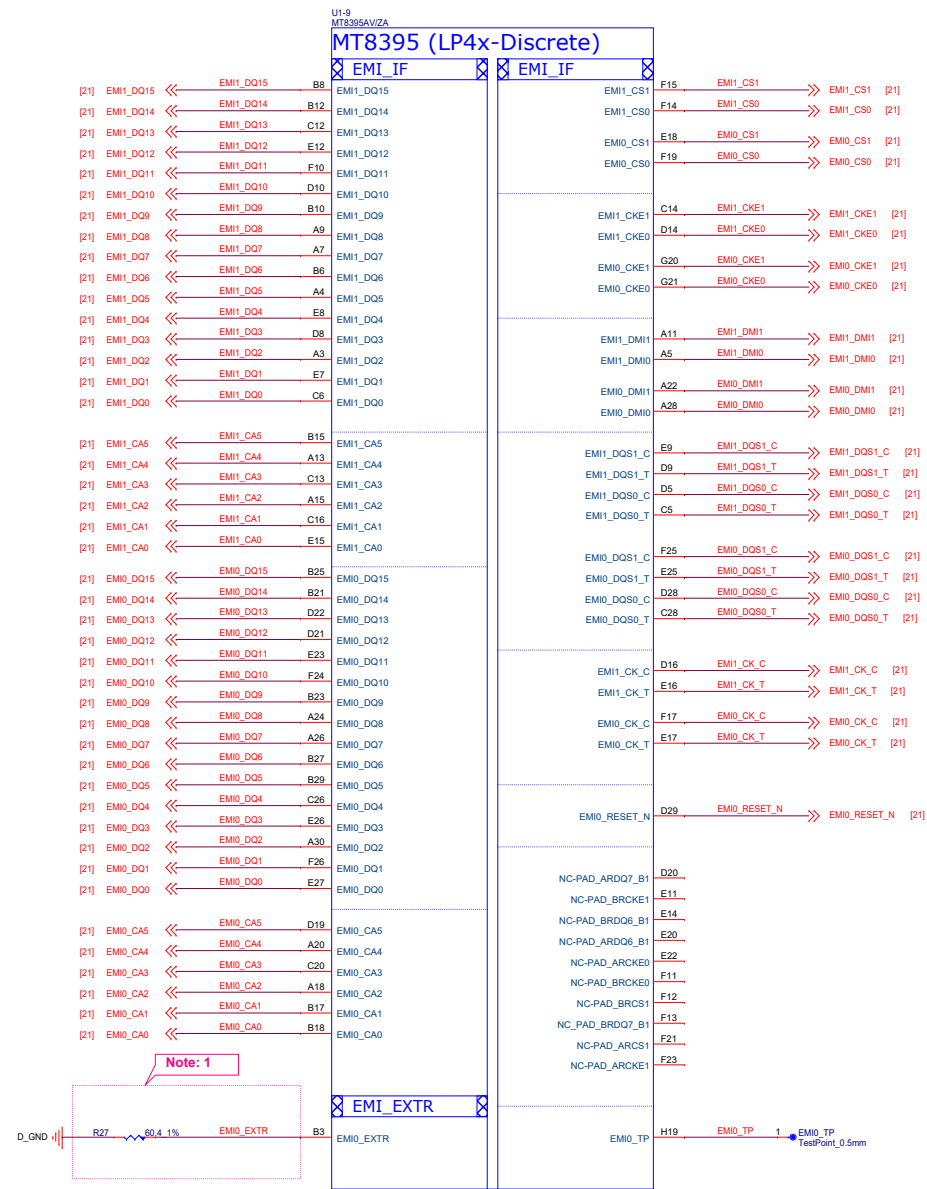
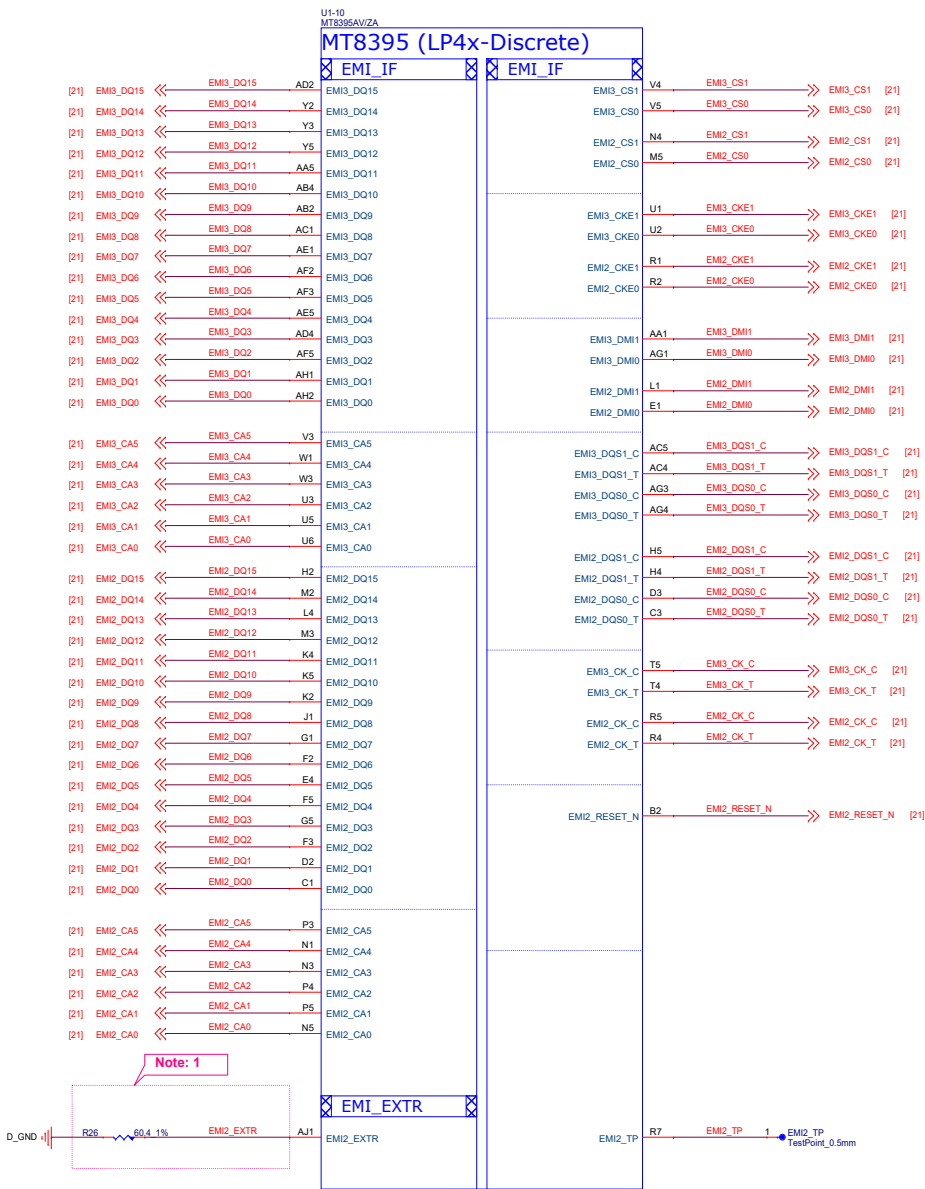


U1-8
MT8395AV/ZA





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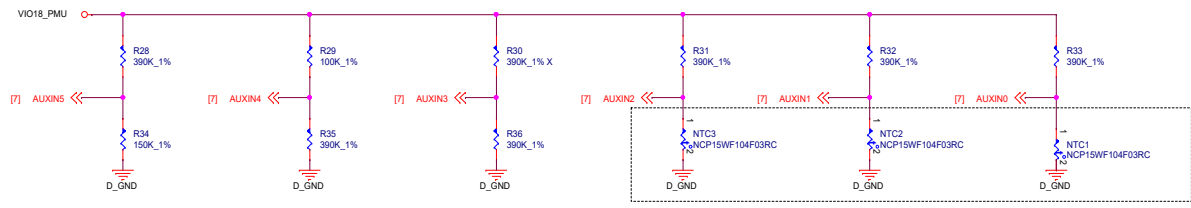


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Baseband Part 4			
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Schematic design notice of "BB_4_Interface" page:

Note 1: R26, R27 please select 60.4 ohm (1%) resistor



AUX5 for eMMC/DRAM Config. Table

<0.7v 4CH, DSC
0.7~1.2v 2CH, eMCP
>1.2v 2CH, DSC

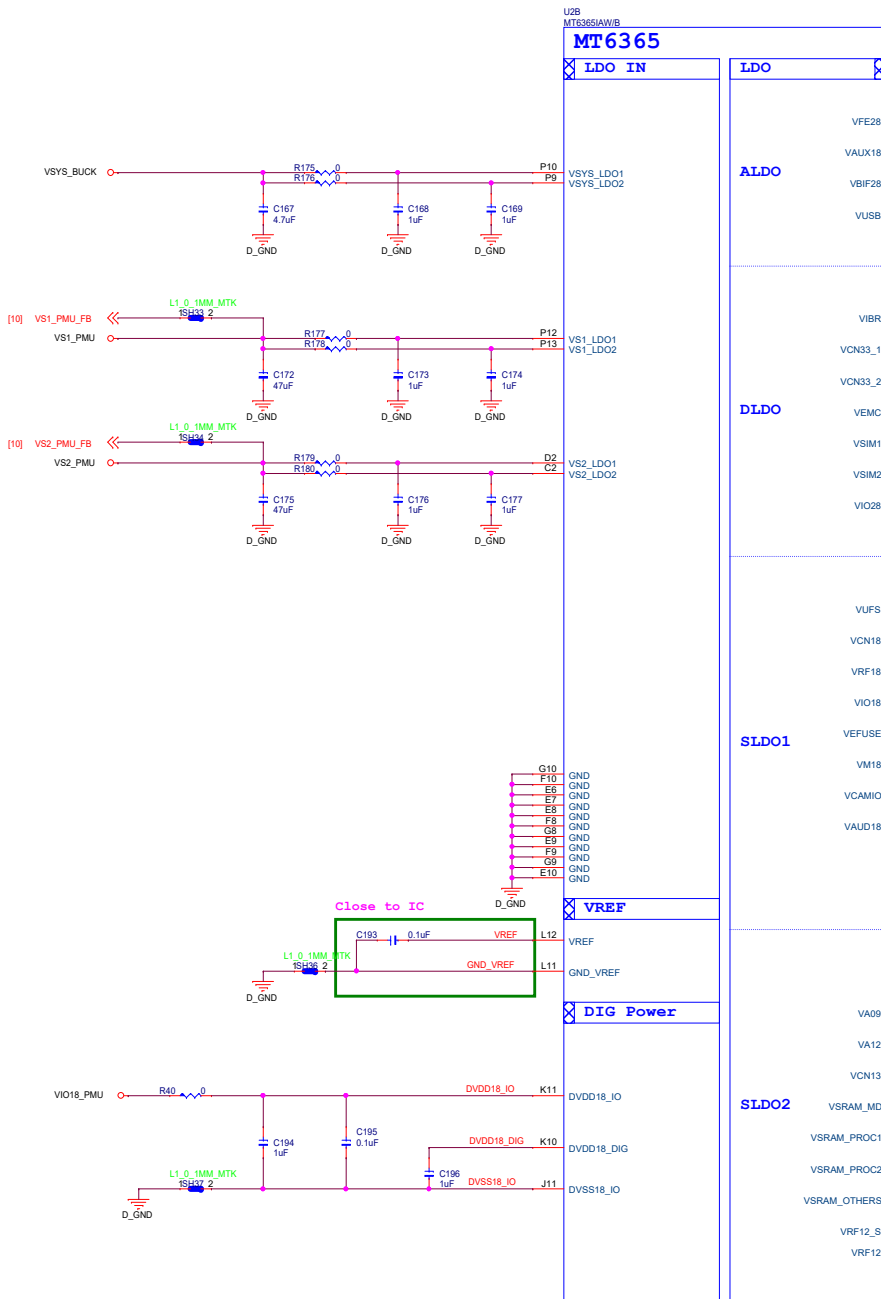
AUX4 for DemoBoard SKU

<0.2V SMT0
0.2~0.7V SMT1 (default ICE)
0.7~1.2V SMT2 (default SD)
>1.2V SMT3 (default SD)

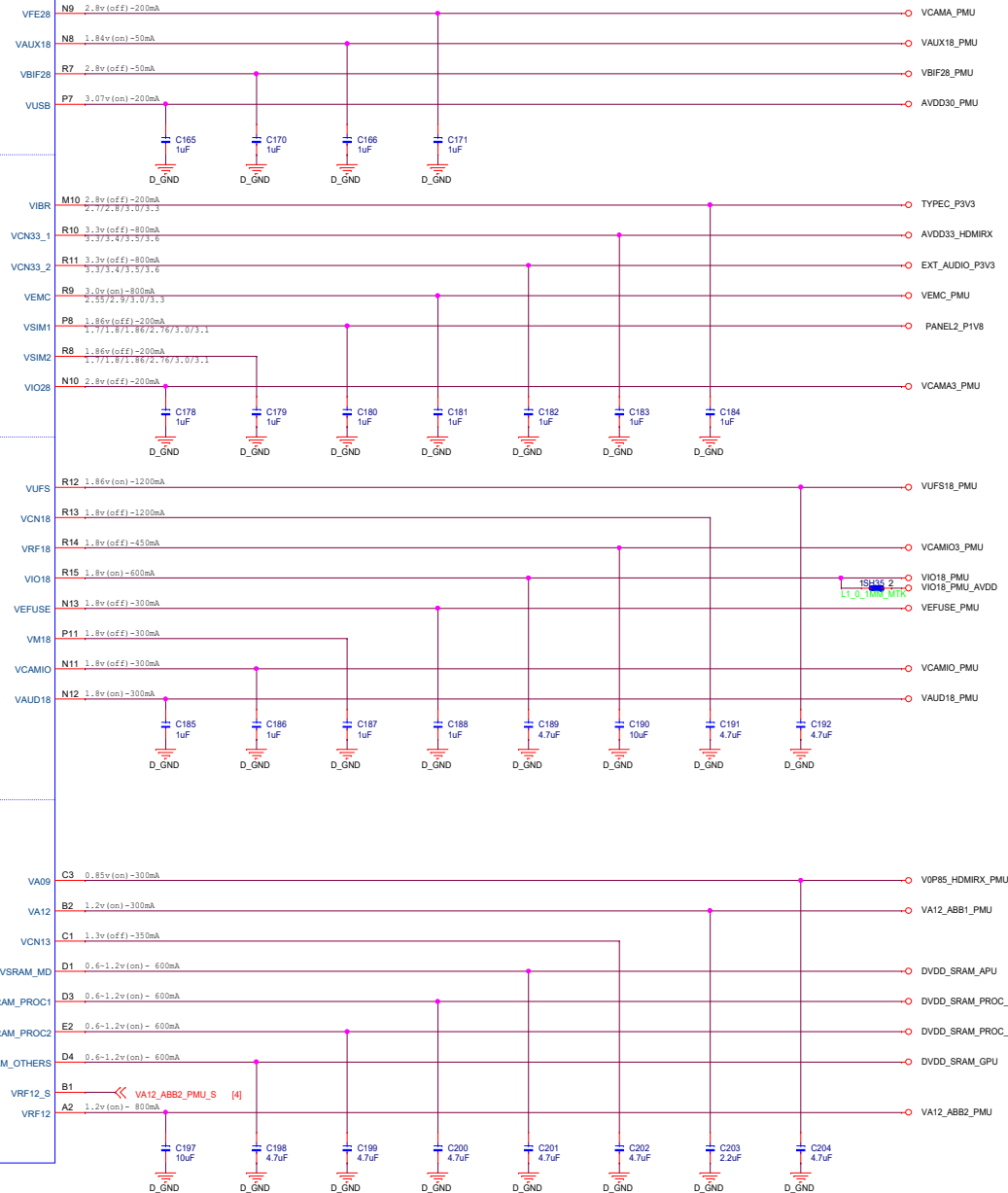
Thermistor to sense AP temperature

- 1. NTC1 must keep a distance about 6~8 mm away from AP and far from other heat sources 10 mm at least.
- 2. The distance is the shortest distance from package edge to edge.

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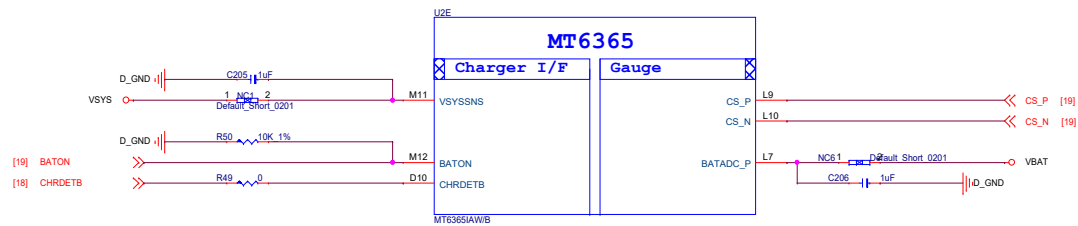
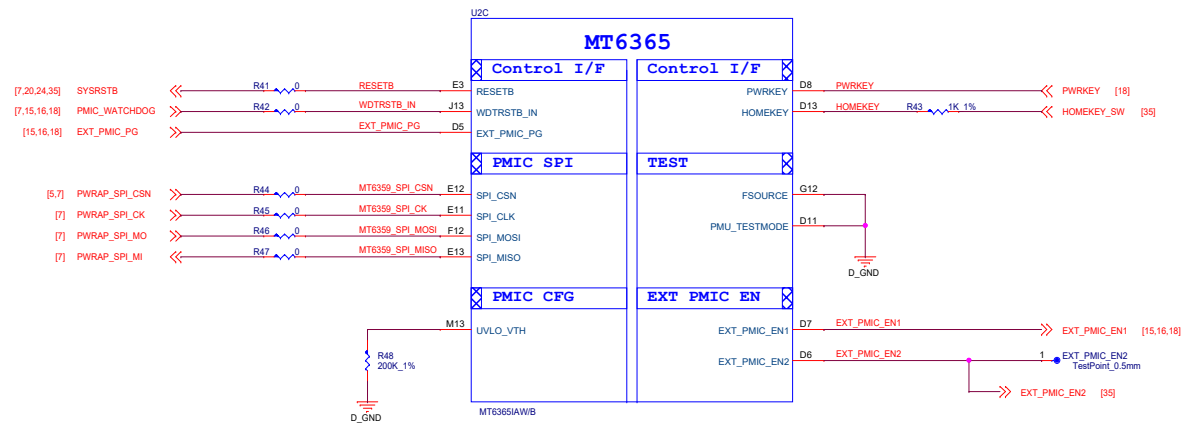


1. "Typical Cap" defined in design notice is the minimum cap. to LDO Cout.
 2. NC cap can move to application, if (PCB L<20nH, PCB R<0.2mohm)
- => value and placement of Cap, please refer design notice



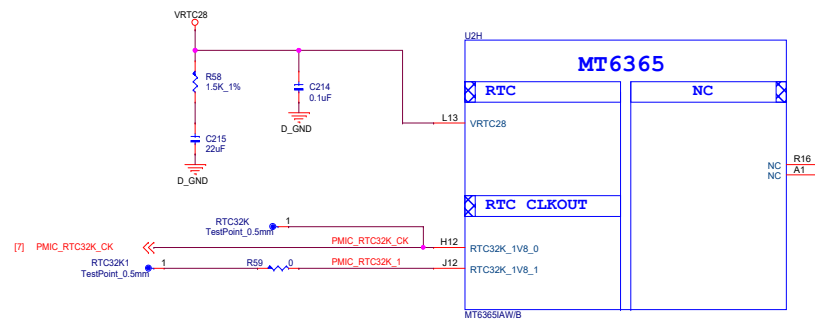
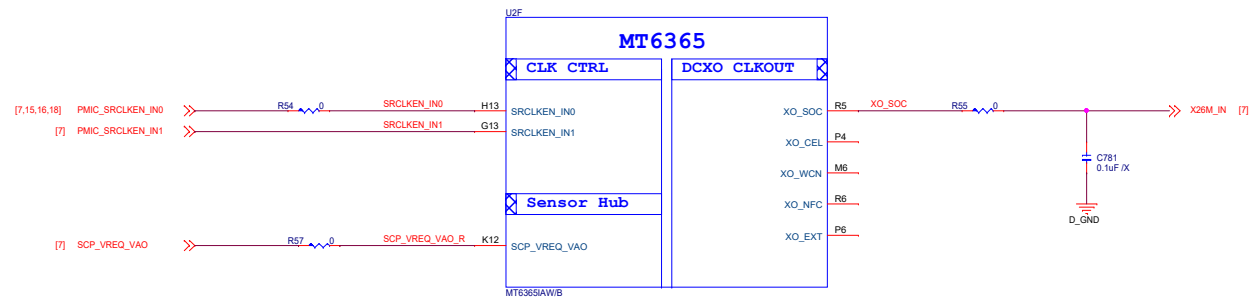
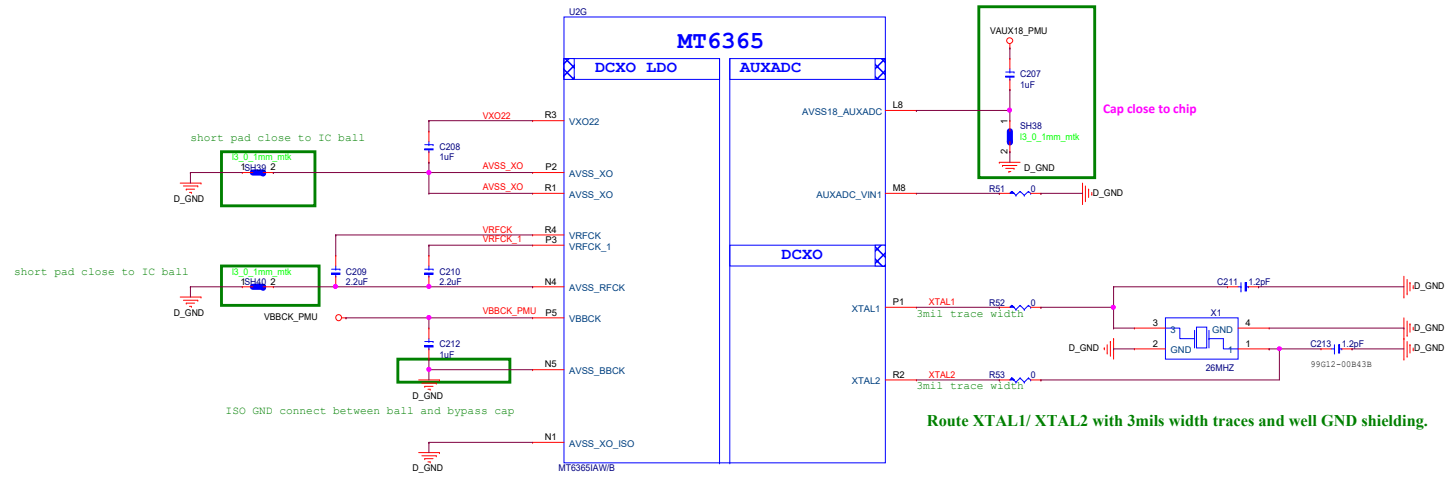
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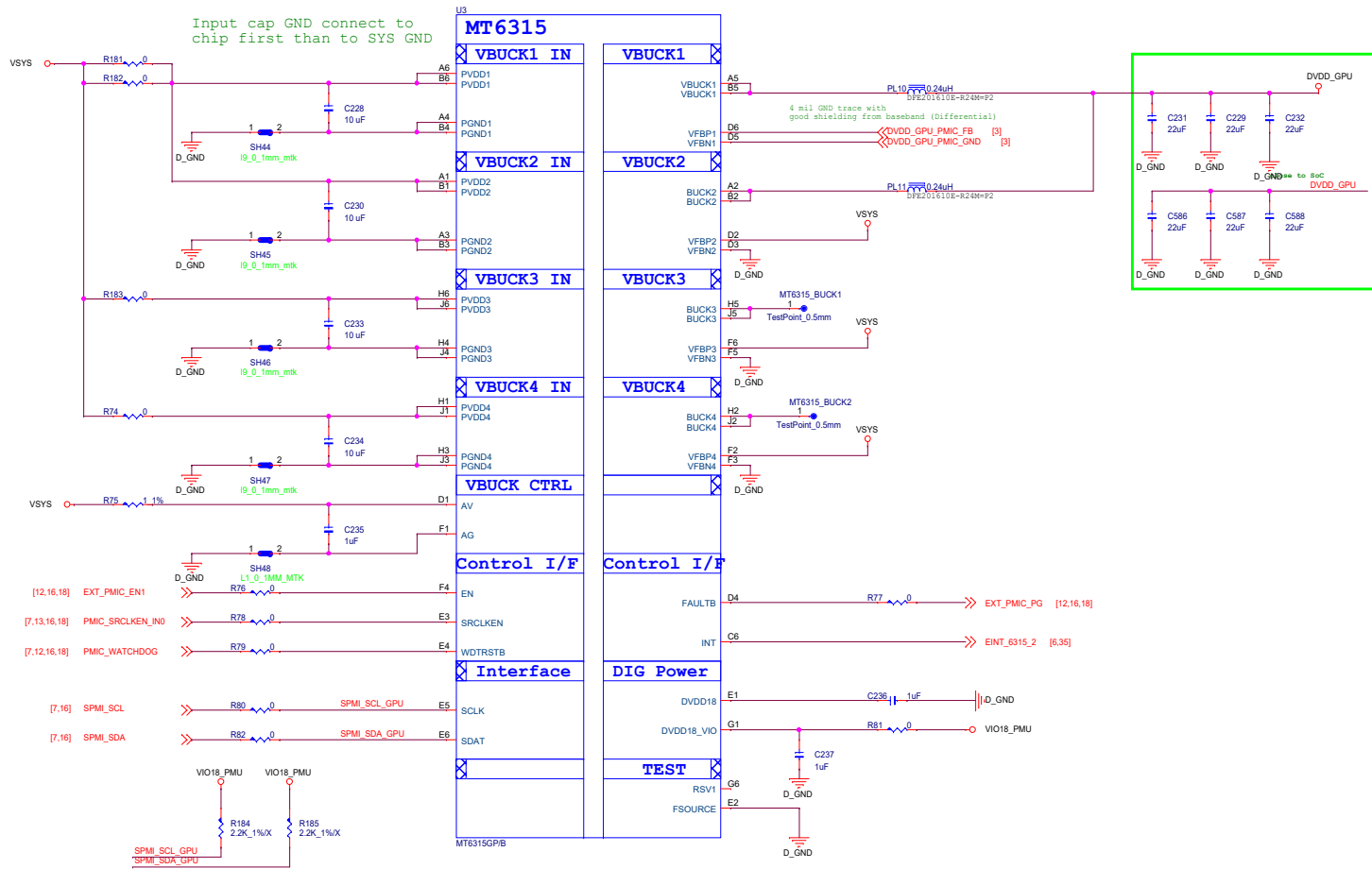
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MT6365 Clock	
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MT6315 4-Phase Buck



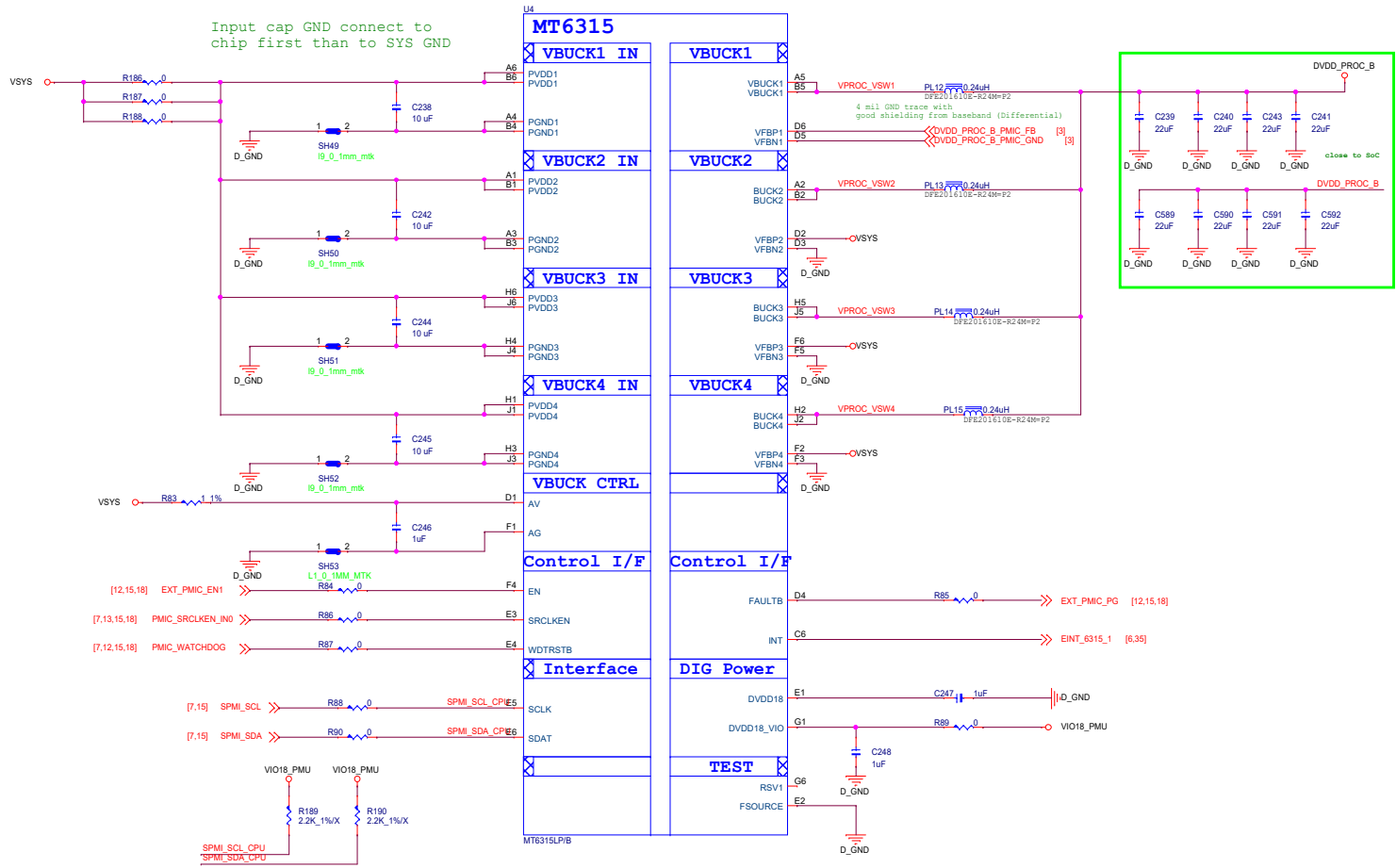
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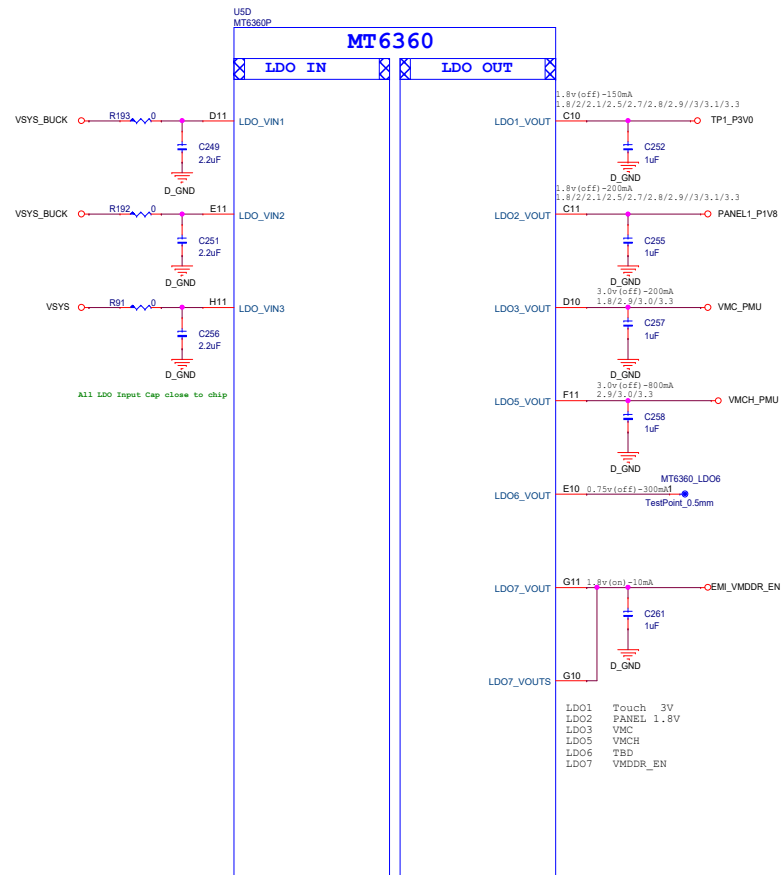
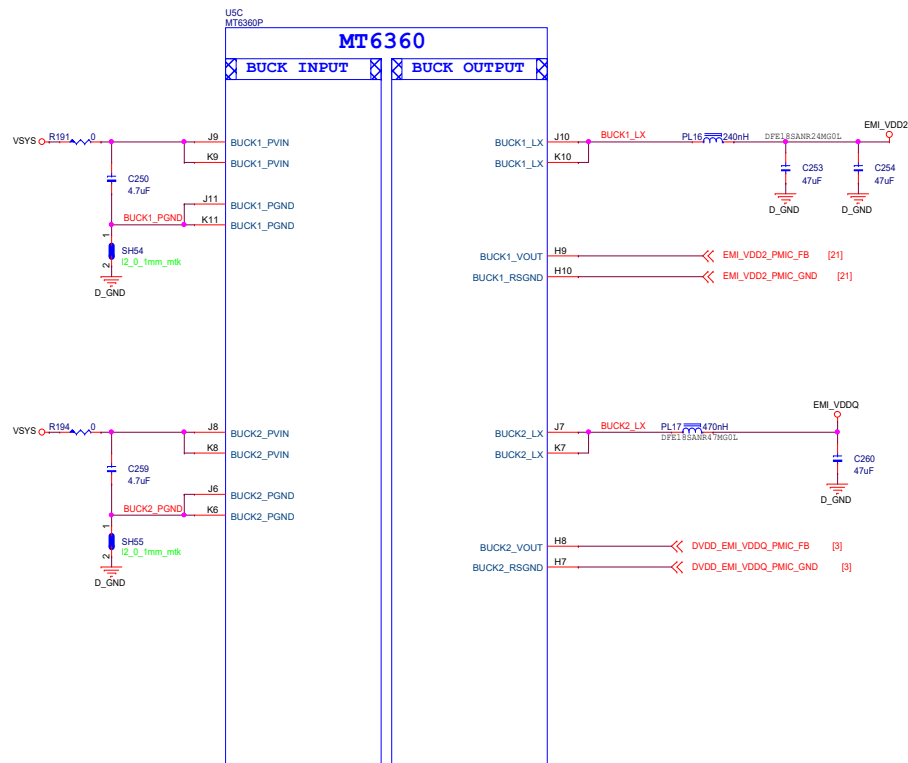
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Title			
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MT6315 4-Phase Buck



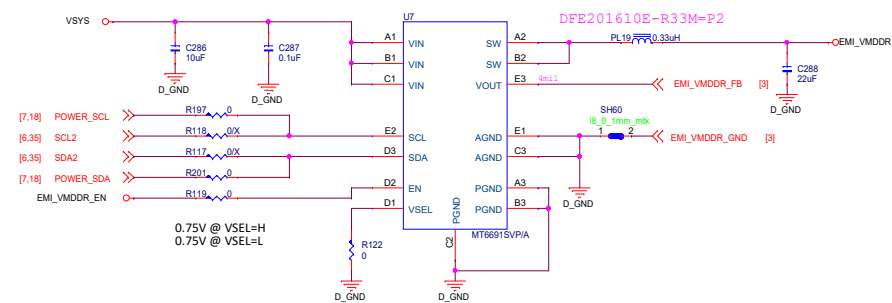
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MT6360 BUCK & LDO	
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LP4X DRAM: VMDDR(0.75V)

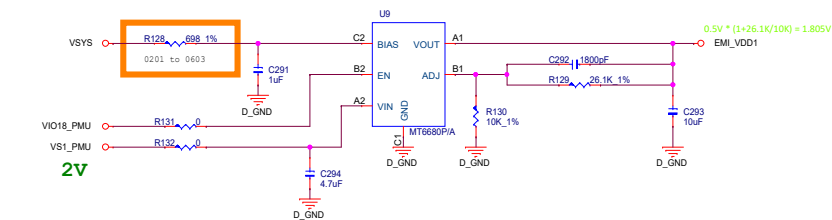


Bypass/Boost for VSYS@LV (Reserve)

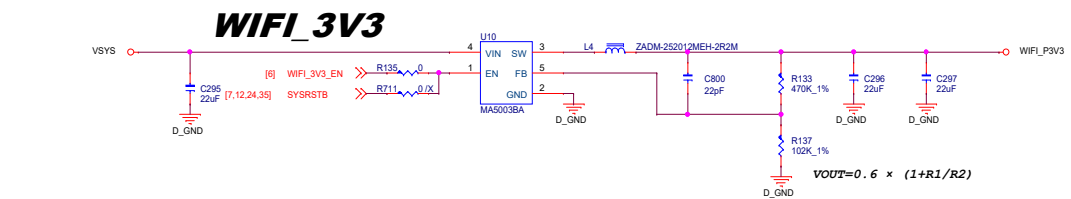
RT4803WSC I2C address: 0X75 (Write:0xEA, Read:0xEB)



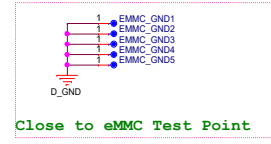
LP4X DRAM: VDD1 (1.8V)



WIFI_3V3 2A



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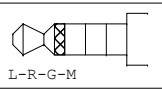
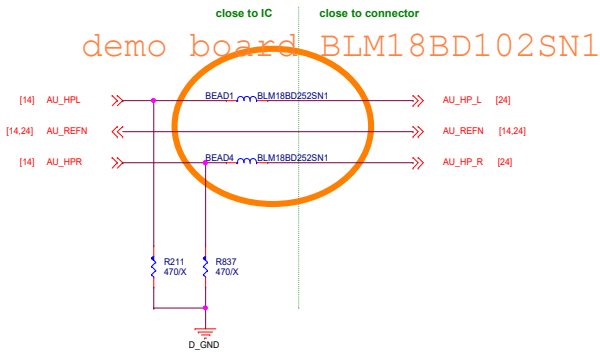


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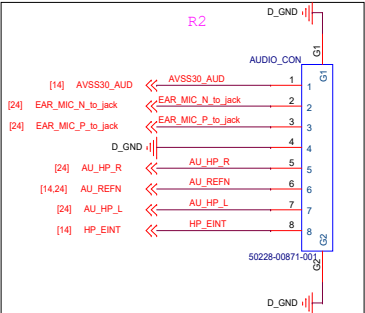
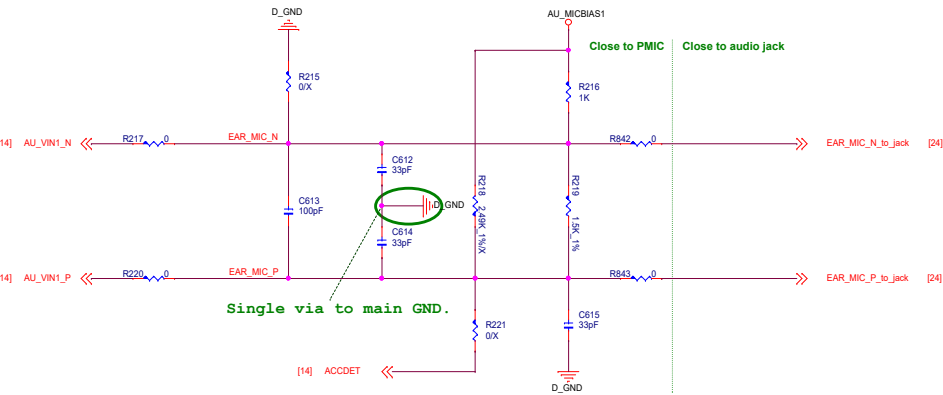
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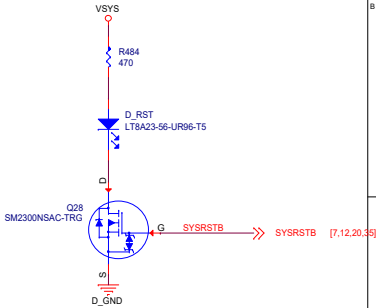
Earphone Audio (PMIC)



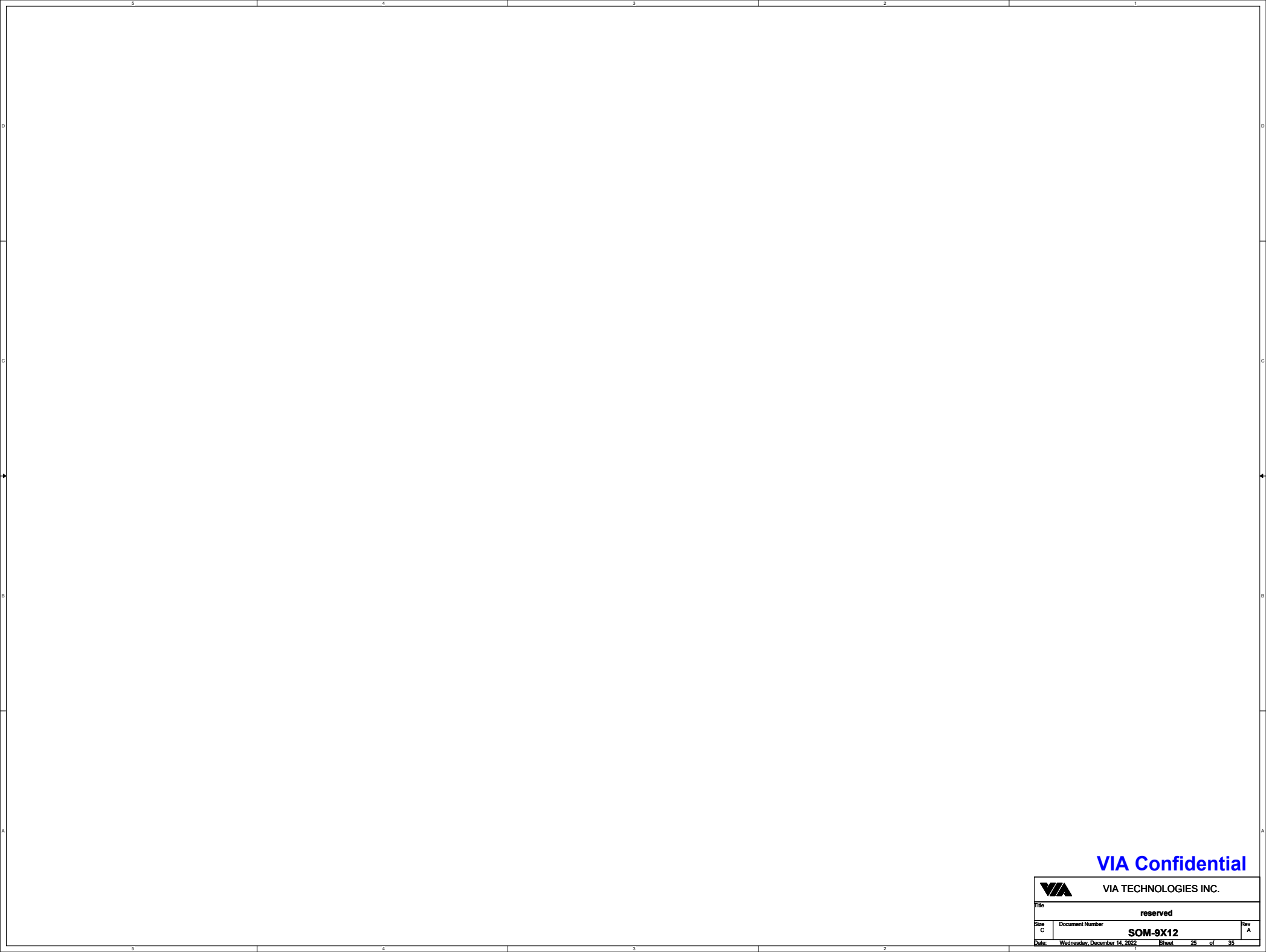
Earphone Microphone (PMIC)



Reset LED

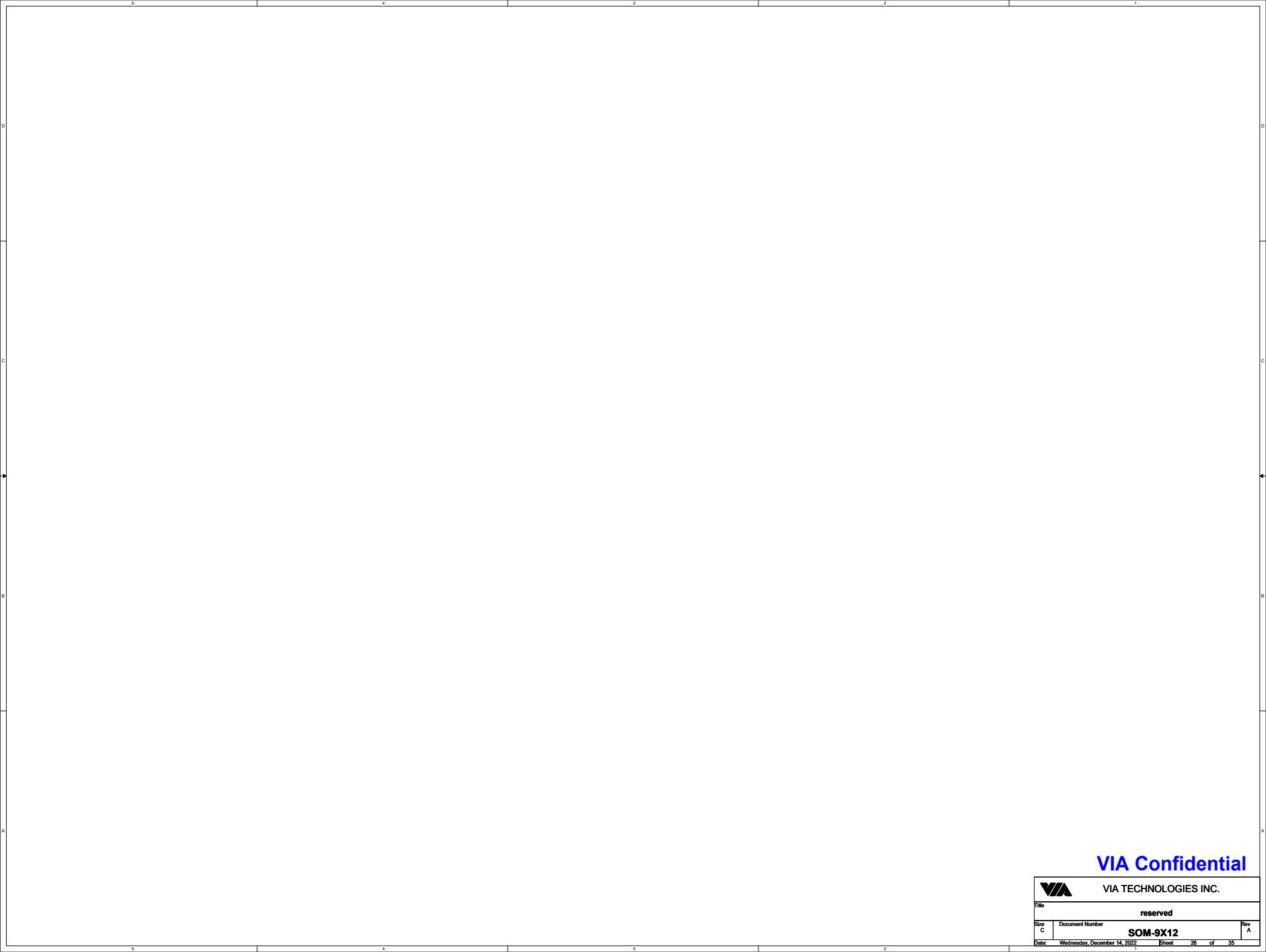


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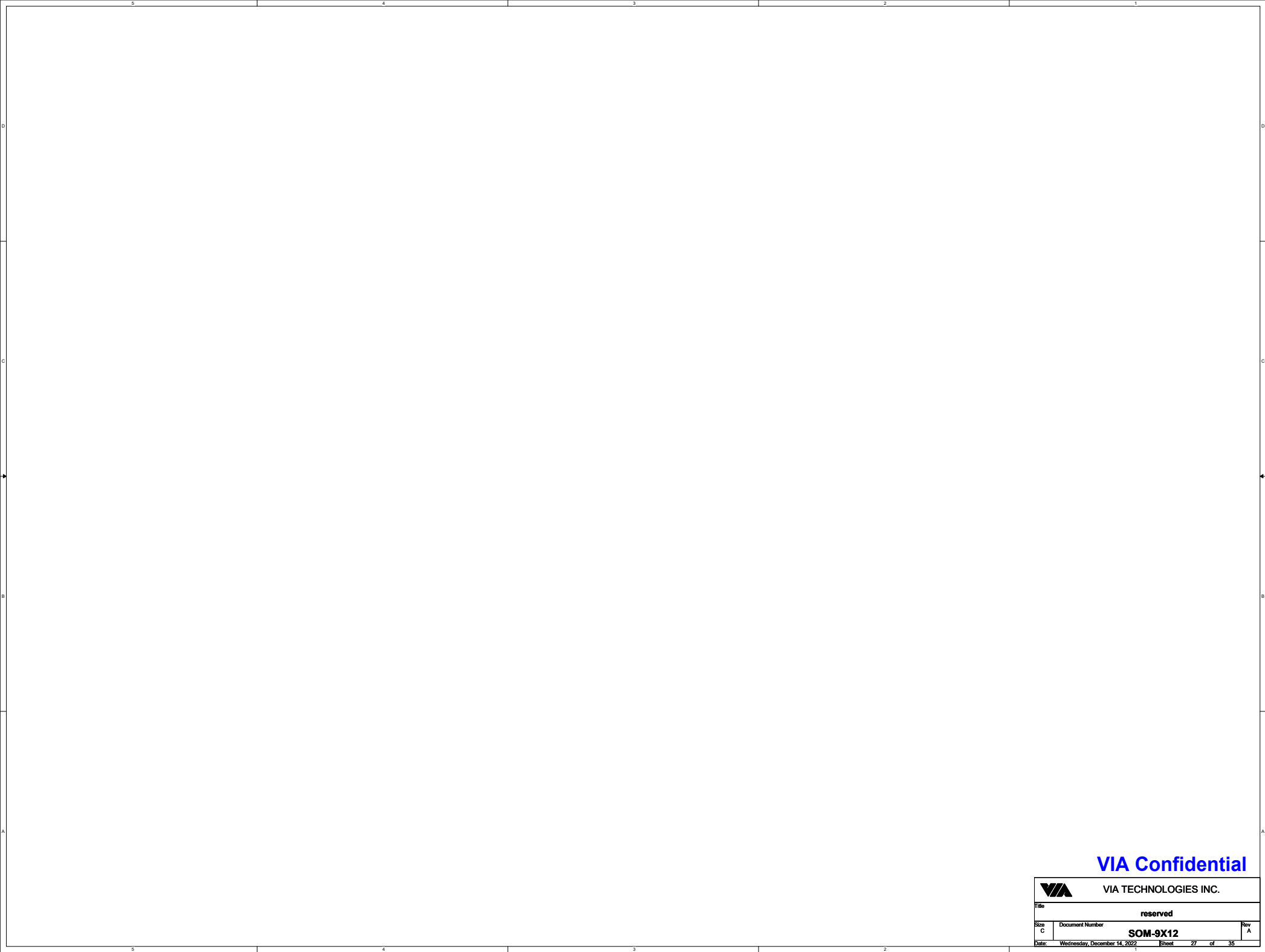
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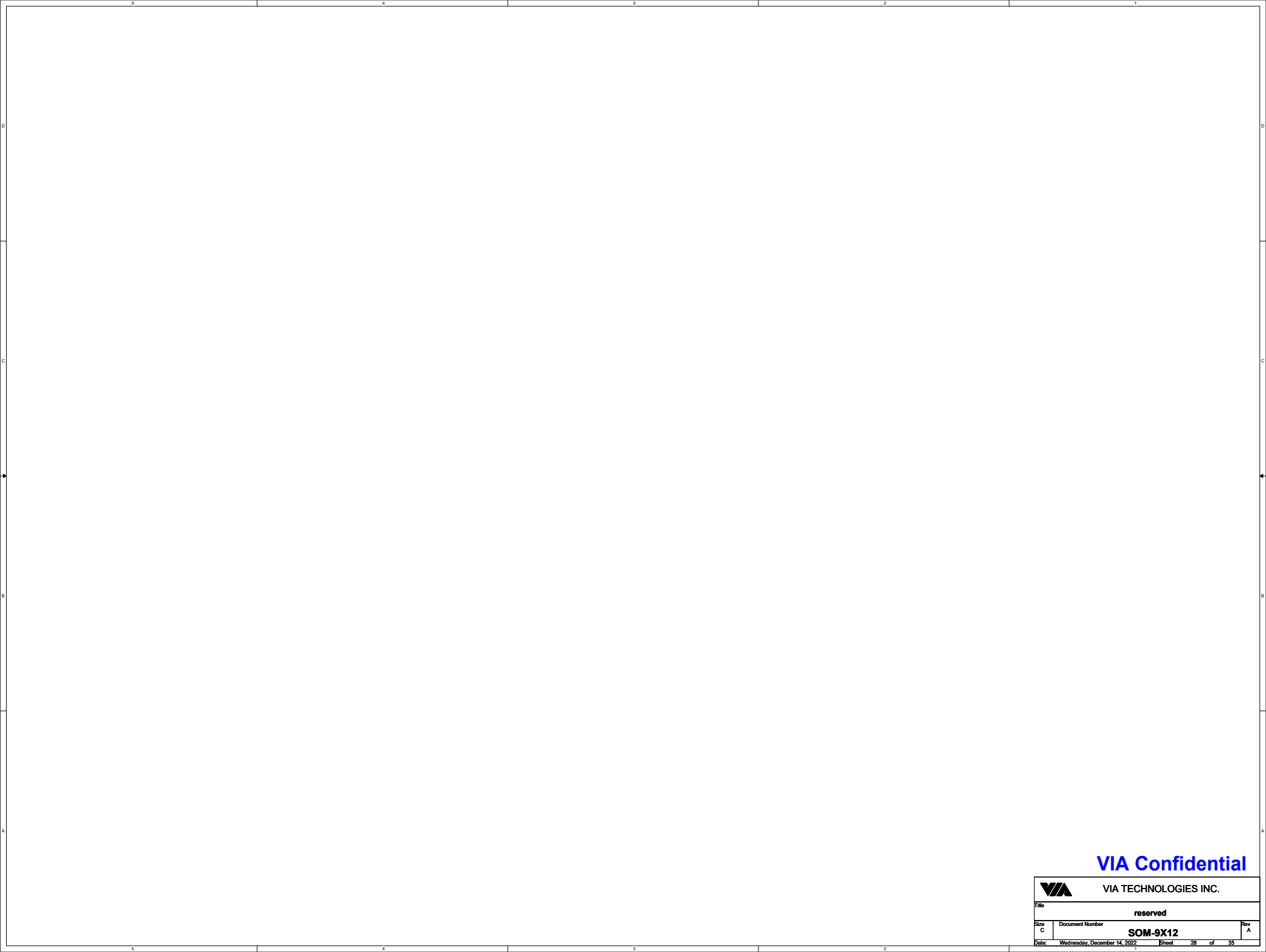
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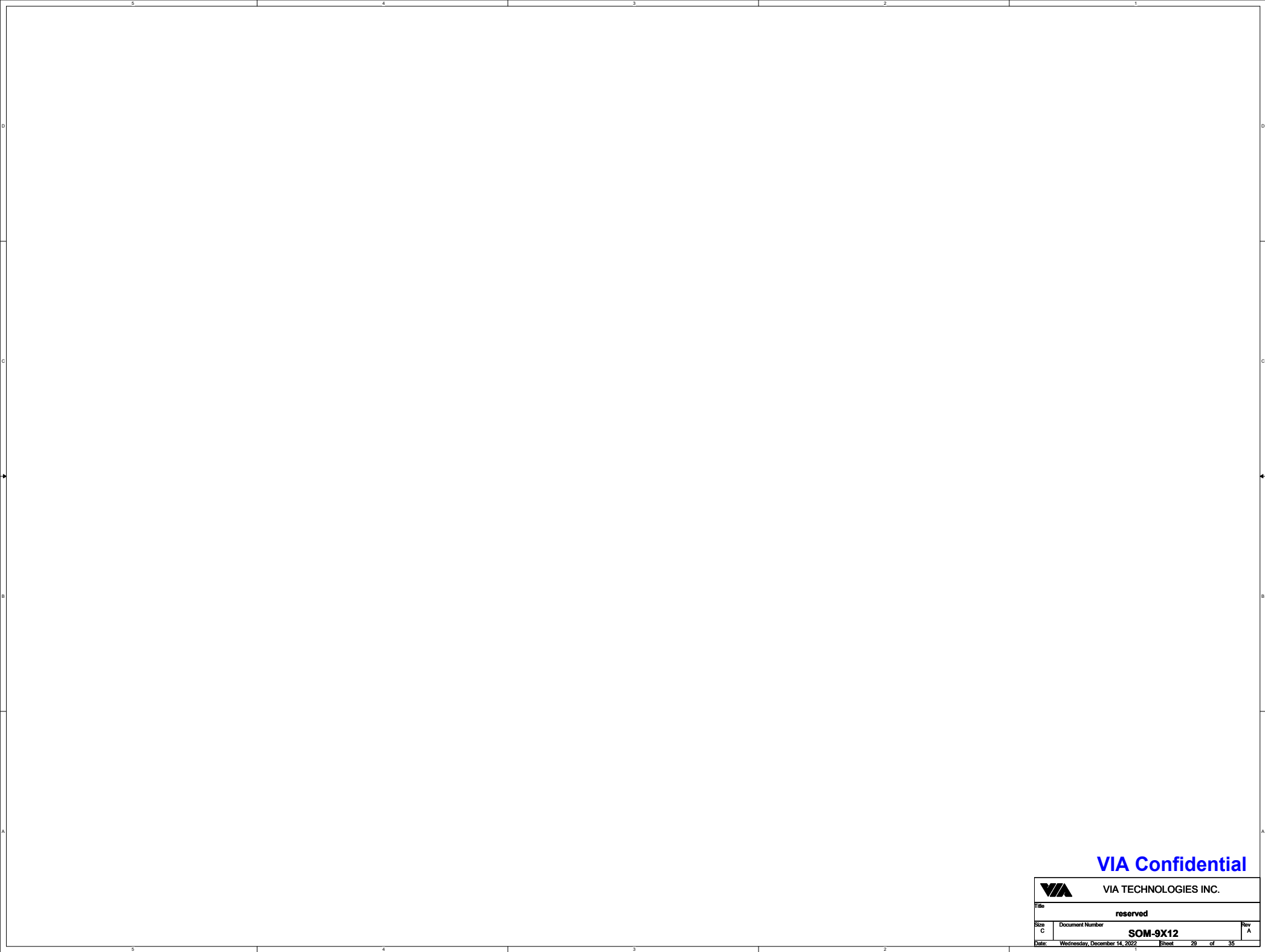
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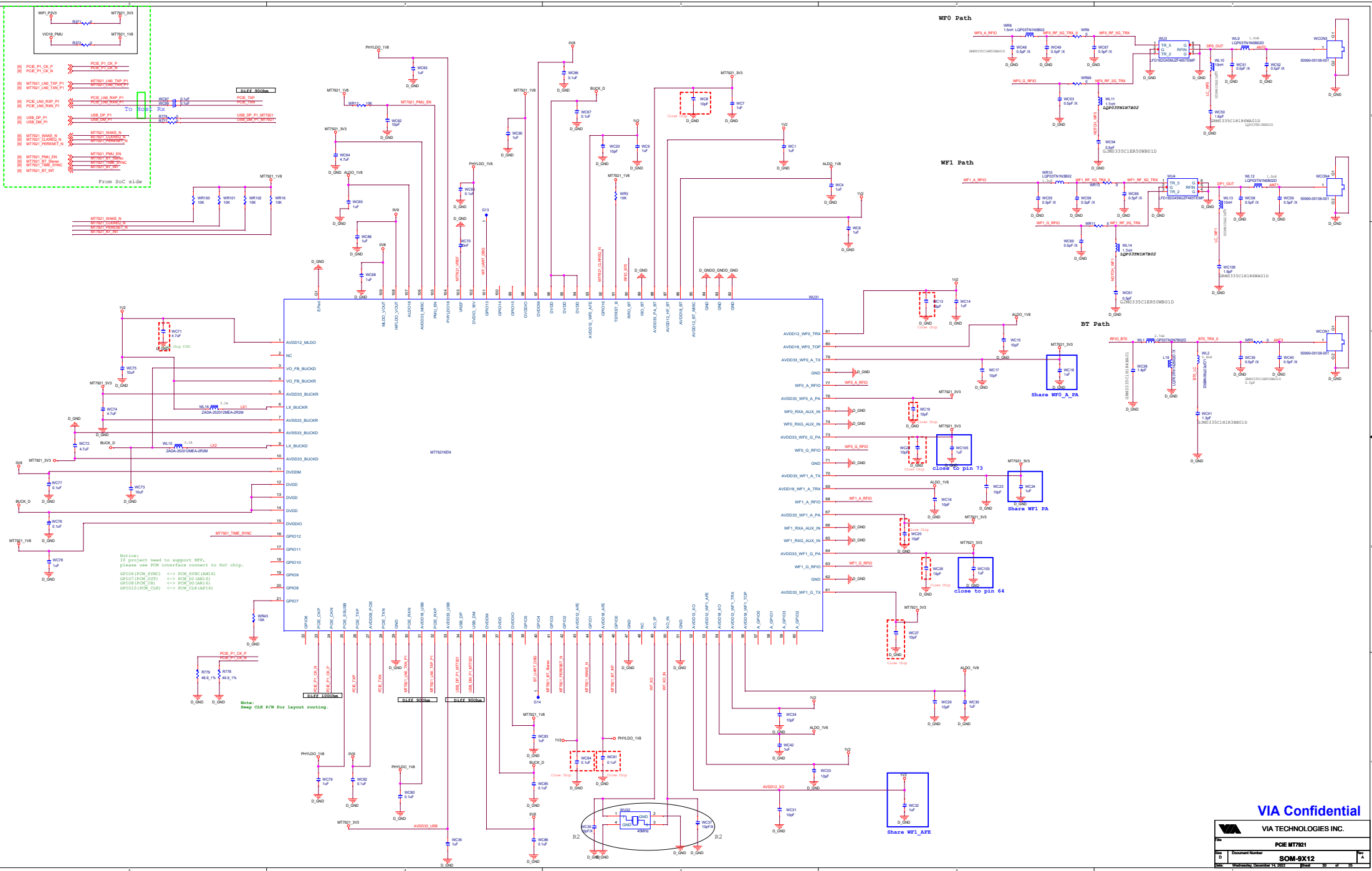
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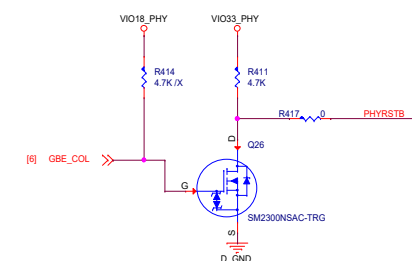
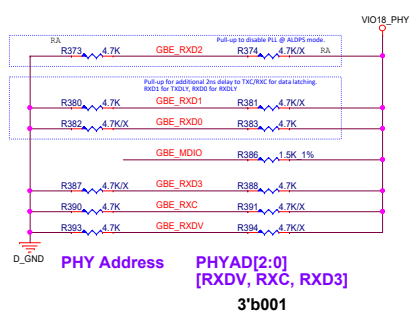
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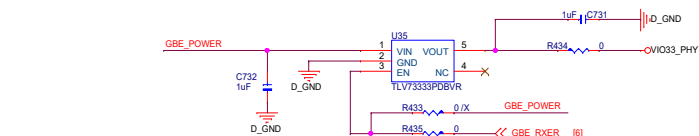
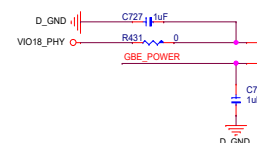
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PCE MT7921			
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D	1.0	1.0	1.0

RGMII PHY



VSYS



Set as GPIO

RGMII Power Source	CFG_EXT LED0	CFG_LDO{1:0} (LED0, LED1)
External 3.3V	1'b1	2'b00
External 2.5V	1'b1	2'b01
External 1.8V(default)	1'b1	2'b10
External 1.5V	1'b1	2'b11
Internal 2.5V	1'b0	2'b01
Internal 1.8V	1'b0	2'b10
Internal 1.5V	1'b0	2'b11

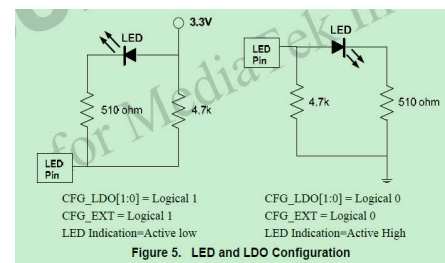
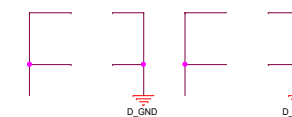
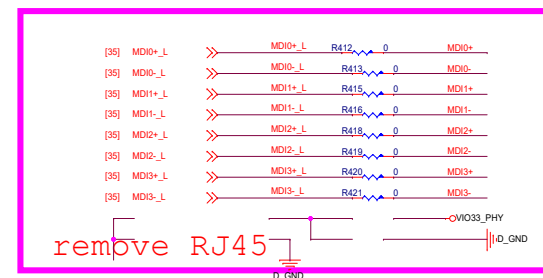
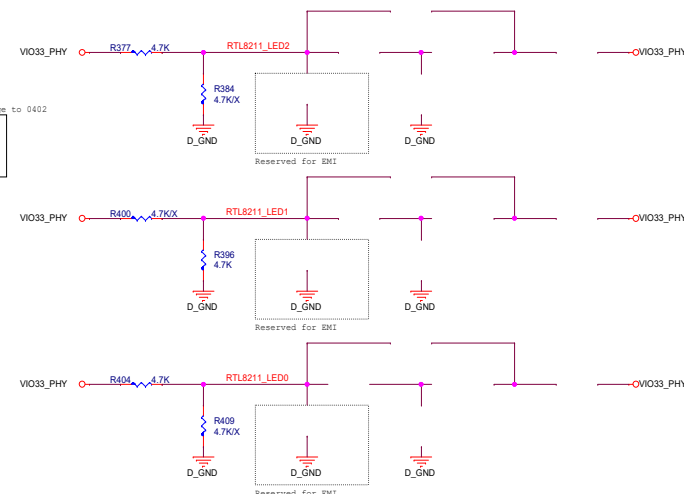
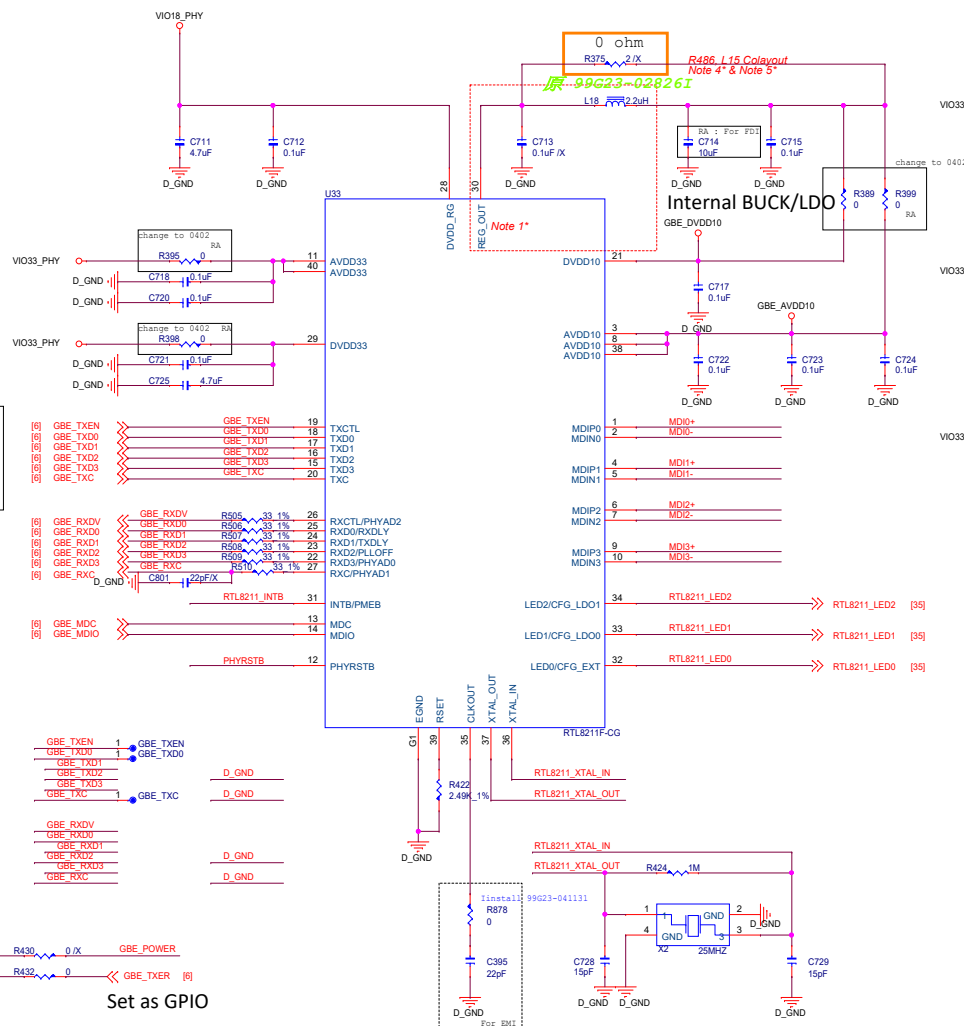


Figure 5. LED and LDO Configuration

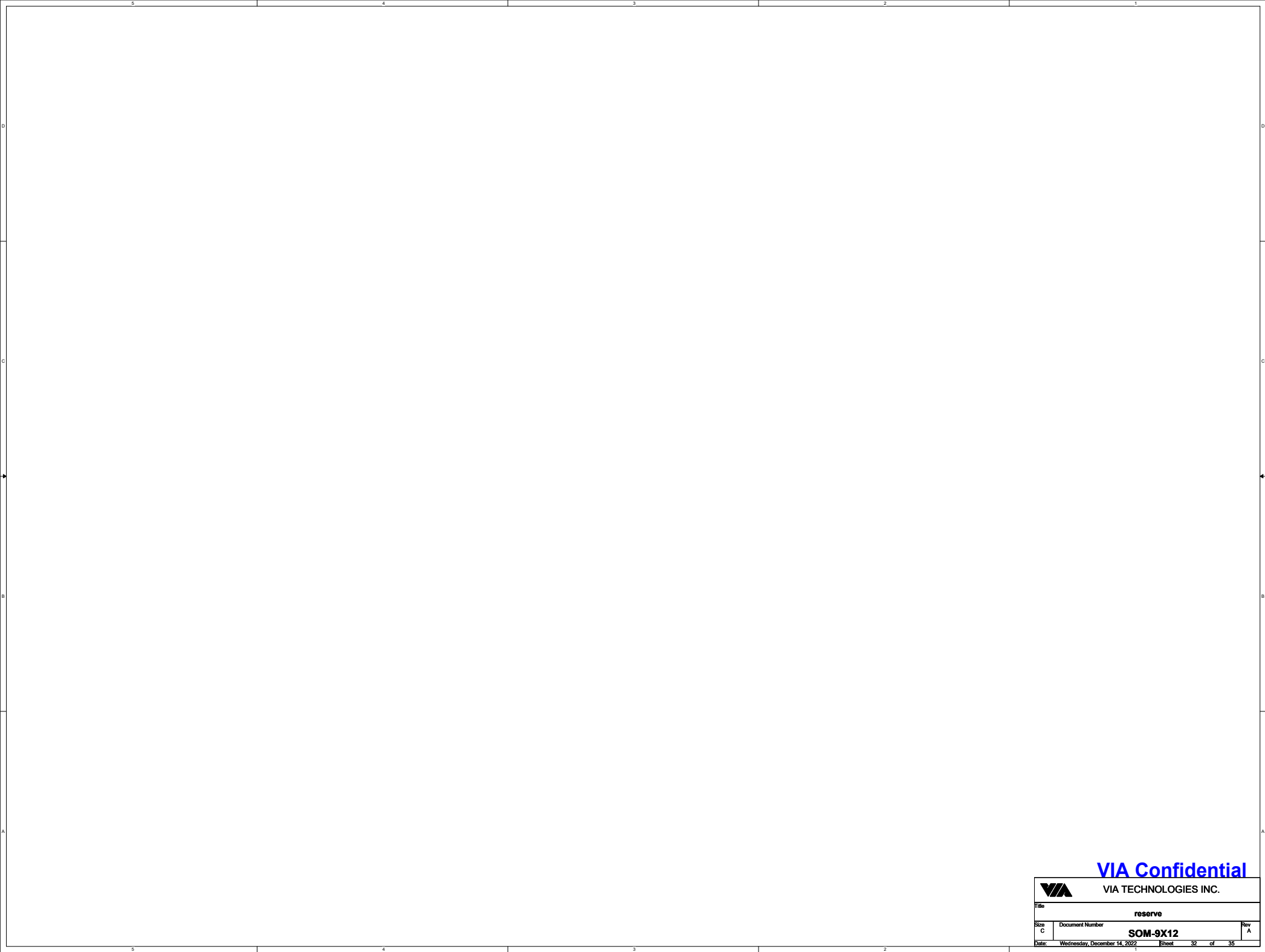


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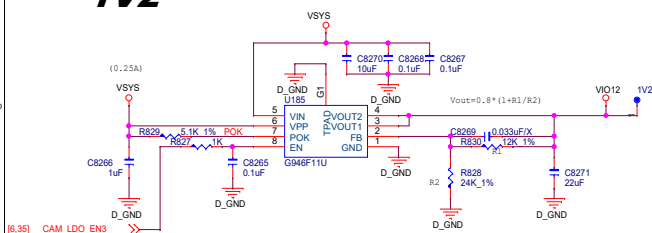
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1V2

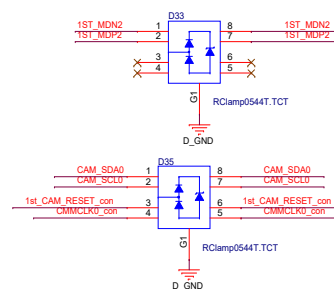
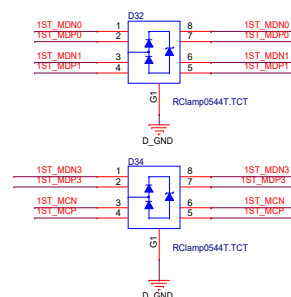
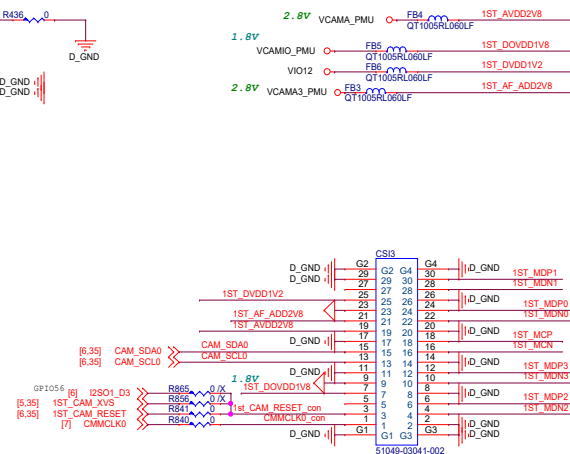
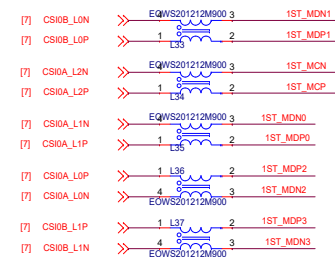


1T1_AVDD02V8
1T1_DVDD01V2
1T1_D0V001V8

C738 0.1uF
C739 0.1uF
C740 2.2uF
C741 0.1uF

D_GND
D_GND
D_GND
D_GND

D_GND
D_GND

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