ACE9030

HELPFUL INFORMATION AND ERRATA:

1. **Using DACs 1 and 2 for controlling Xtal oscillator.**

DACs 1 and 2 are intended to drive varactor diodes for the crystal oscillator circuit. The internal series resistors form an RC LPF circuit with the varactors. The LPF helps suppress internal noise generated by the DACs. The resistor variation specified is due to operating temperature range and production tolerances.

DAC3 does not have internal series resistors. Its output can source or sink 1 Ma. This DAC, in conjunction with one of the LF op-amps may be used as an ALC loop reference for a PA power control circuit.

2. **Programming the 9030 synthesizer to reduce phase noise:**

As mentioned in the ACE9030 data sheet, the 9030 can be set up to minimize phase noise on the synthesizers due to the data clock. Latch C (LATCH [3] ACE9050) must be held high. The ACE9050 has provisions to maintain LATCH [3] high via the PRORT3 Bit 6 [ONRAD] (see ACE 9050 data sheet). The ONRAD bit is ORed with LATCH [3].

The procedure is to set the LATCH [3] low after programming the synthesizer for the desired channel. Then, send a dummy command latched with a long LATCH[3]. Next, set the ONRAD bit high to maintain LATCH[3] high after the long latch has timed out. Make sure the programmed long latch length is sufficiently long enough to set the ONRAD bit before the latch length time out.

3. **ADC input impedance**

Please take note. The ADC inputs are multiplexed to one ADC. During polling, a voltage spike may be present at the ADC inputs. The spike amplitude is dependent on the source impedance of the input signal. Normally a 1000 pF capacitor to ground at the ADC inputs is sufficient to minimize these spikes.

4. **8MHz clock**

Loop Filter:

Please take note. The suggested loop filter component values (figure 17 in data sheet) for the 8 MHz PLL is as follows:

R8F = 12Kohms
C8F = 10 nF

Power supply sensitivity:

Care should be taken to isolate the 8MHz clock signal from potential noise interference. The signal level generated out of the ACE9030 is about 800 mV. The ACE9050 is designed to accept this clock level signal. Remember, the clock must be AC coupled to the ACE9050. The VDDA supply should also be appropriately decoupled from excessive noise and transients.

Excessive noise on the VDD supply has been attributable to observed jitter. Excessive jitter on the 8 MHz clock may reduce the ACE9050 data modem performance.

FAQ:

What is the mechanism for determining lock status?

Lock detect circuitry is included within the ACE9030 and is interrogated via the serial interface. This information is available on every word read back from the ACE9030.

ACE9030 DATA SHEET

GEC PLESSEY
SEMICONDUCTORS

FEBRUARY 1997

DS4288 - 1.4

ACE9030

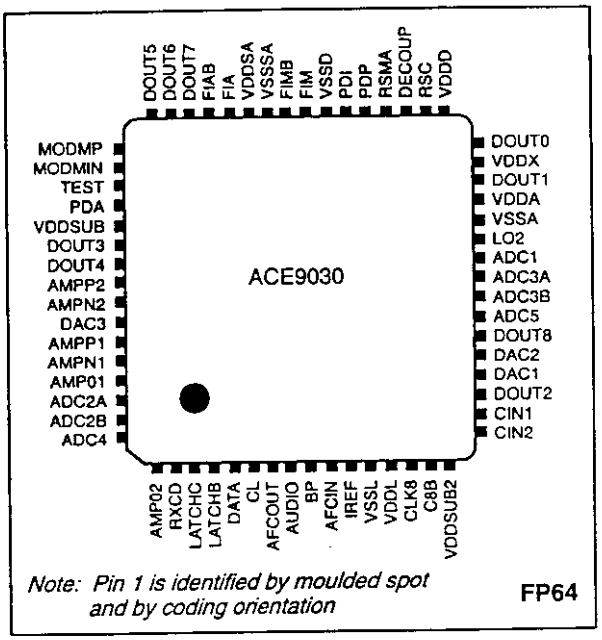
RADIO INTERFACE AND TWIN SYNTHESISER

ACE9030 is a combined radio interface circuit and twin synthesiser, intended for use in a cellular telephone.

The radio interface section contains circuits to monitor and control levels such as transmit power in the telephone, circuits to demodulate the frequency modulated signal to audio, and a crystal oscillator with a frequency multiplier.

The Main synthesiser has normal and fractional-N modes both with optional speed-up to select the desired channel. The Auxiliary synthesiser is used for the transmit-receive offset and for modulation.

Both sections are controlled by a serial bus and have software selected power saving modes for battery economy. The circuit techniques used have been chosen to minimise external components and at the same time give very high performance.



Note: Pin 1 is identified by moulded spot and by coding orientation

FP64

Fig.1 Pin connections - top view

FEATURES

- Low Power Low Voltage (3·6 to 5·0 V) Operation
- Serial Bus Controlled Power Down Modes
- Simple Programming Format
- Reference Crystal Oscillator
- Frequency Multiplier for LO2 Signal
- 8·064 MHz Output for External Microcontroller
- Main Synthesiser with Fractional-N Option
- Auxiliary Synthesiser
- Main Synthesiser Speed-up Options
- FM Discriminator for 450 kHz or 455 kHz I.F. Signal
- Radio System Control Interface
- Part of the ACE Integrated Cellular Phone Chipset
- TQFP 64 pin 0·4 mm and 0·5 mm pitch packages

RELATED PRODUCTS

ACE9030 is part of the following chipset:

- ACE9010 R.F. Front End with VCO
- ACE9020 Receiver and Transmitter Interface
- ACE9040 Audio Processor
- ACE9050 System Controller and Data Modem

APPLICATIONS

- AMPS and TACS Cellular Telephone
- Two-way Radio Systems

ORDERING INFORMATION

Industrial temperature range
TQFP 64 lead 10 x 10 mm, 0·5 mm pitch
ACE9030/IG/FP1N - shipped in trays and dry packed
ACE9030/IG/FP1Q - tape & reel and dry packed
TQFP 64 lead 7 x 7 mm, 0·4 mm pitch
ACE9030/IG/FP2N - shipped in trays and dry packed
ACE9030/IG/FP2Q - tape & reel and dry packed

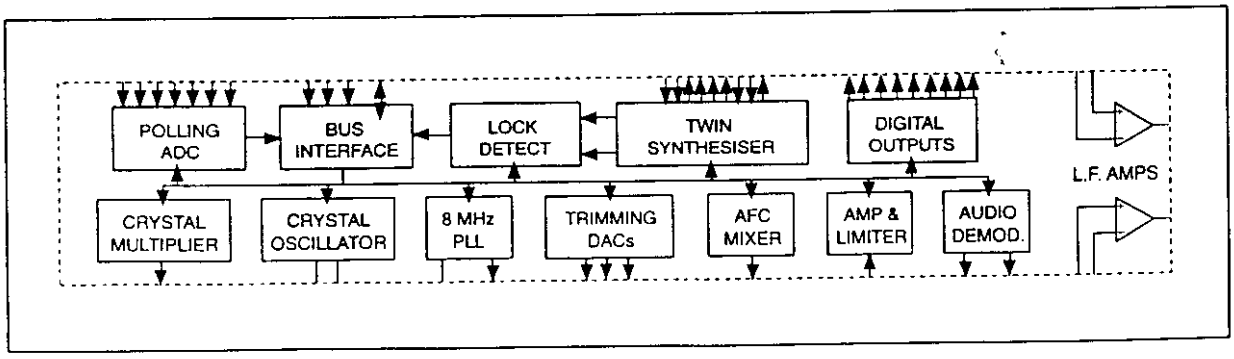


Fig. 2 ACE9030 Simplified Block Diagram

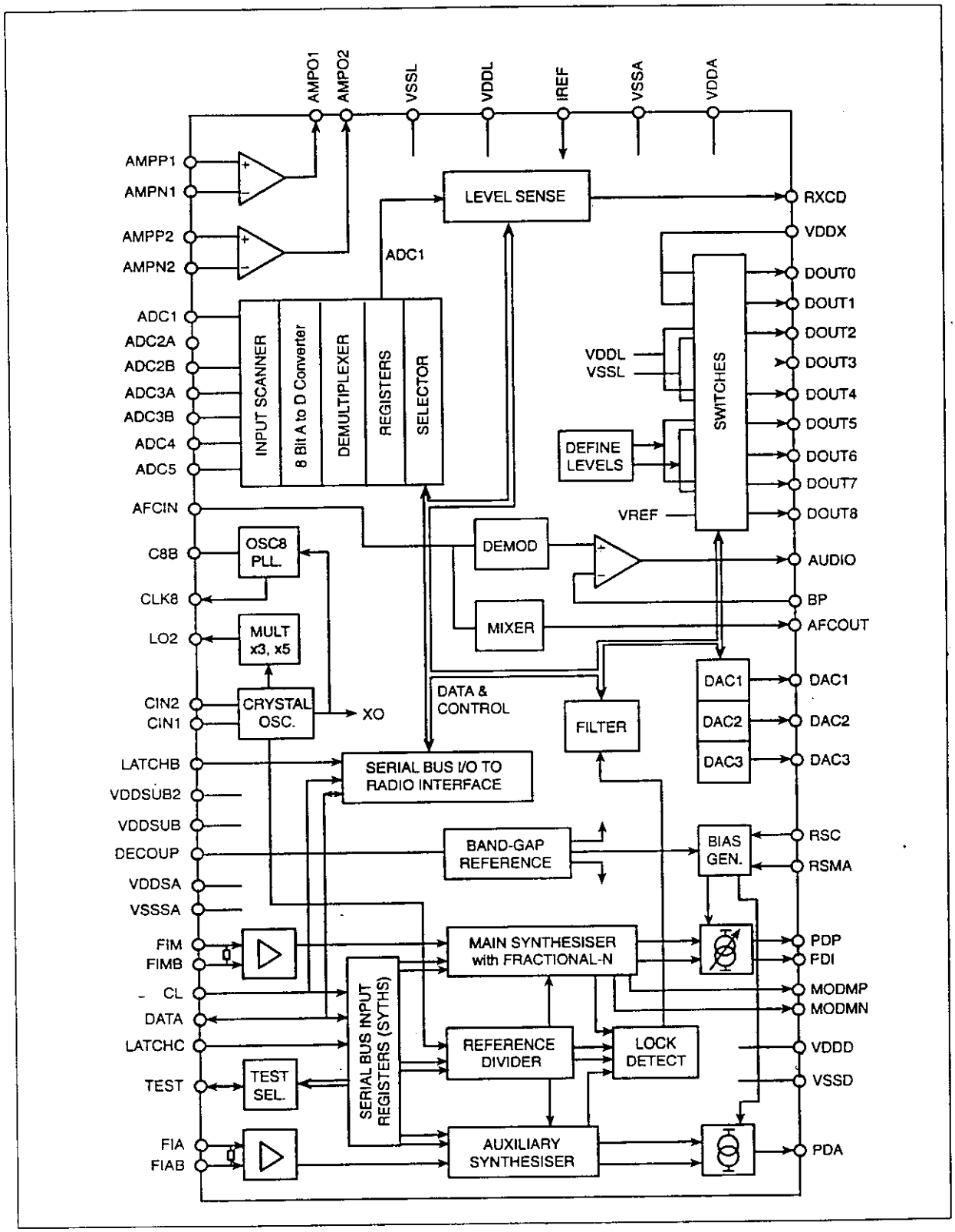


Fig.3 ACE9030 Block diagram

PIN DESCRIPTIONS

The relevant supplies (V_{DD}) and grounds (V_{SS}) for each circuit function are listed. All V_{DD} and V_{SS} pins should be used.

Pin No.	Name	Description	VDD	VSS
1	AMPO2	LF amplifier 2 output.	VDDA	VSSA
2	RXCD	Receive carrier detect (ADC1 comparator) output.	VDDL	VSSL
3	LATCHC	Synthesiser programme enable input.	VDDL	VSSL
4	LATCHB	Radio interface programme enable input.	VDDL	VSSL
5	DATA	Serial data; programming input, results output.	VDDL	VSSL
6	CL	Clock input for programming bus and for I.F. sampling.	VDDL	VSSL
7	AFCOUT	Output from AFC amplifier after sampling.	VDDL	VSSL
8	AUDIO	Output from f.m. discriminator after filtering.	VDDA	VSSA
9	BP	Feedback input to audio bandpass filter.	VDDA	VSSA
10	AFCIN	Input to AFC amplifier and f.m. discriminator.	VDDL	VSSL
11	IREF	Bias current input for radio interface, connect setting resistor to ground.	–	VSSA
12	VSSL	Ground for radio interface logic.	–	–
13	VDDL	Power supply to radio interface logic.	–	–
14	CLK8	Output clock at 8·064 MHz, locked to crystal.	VDDL	VSSL
15	C8B	8·064 MHz oscillator charge pump output and control voltage input.	VDDA	VSSA
16	VDDSUB2	Second connection for clean positive supply to bias substrate.	VDDA	VSSA
17	CIN2	Connection for crystal oscillator.	VDDL	VSSL
18	CIN1	Connection for crystal oscillator.	VDDL	VSSL
19	DOUT2	Digital control output 2.	VDDL	VSSL
20	DAC1	Analog control output 1.	VDDA	VSSA
21	DAC2	Analog control output 2.	VDDA	VSSA
22	DOUT8	Digital control output 8.	VDDA	VSSA
23	ADC5	Analog to digital converter input 5.	VDDA	VSSA
24	ADC3B	Analog to digital converter input 3B.	VDDA	VSSA
25	ADC3A	Analog to digital converter input 3A.	VDDA	VSSA
26	ADC1	Analog to digital converter input 1.	VDDA	VSSA
27	LO2	Output from crystal frequency multiplier.	VDDA	VSSA
28	VSSA	Ground for radio interface analog parts.	–	–
29	VDDA	Power supply to radio interface analog parts.	–	–
30	DOUT1	Digital control output 1.	VDDX	–
31	VDDX	Power supply to DOUT1 and DOUT2 switches.	–	–
32	DOUT0	Digital control output 0.	VDDX	–
33	VDDD	Power supply to synthesisers, except input buffers and the bandgap.	–	–
34	RSC	Fractional-N compensation bias current, resistor to ground.	–	VSSSA
35	DECOUP	Bandgap reference decoupling capacitor connection.	VDDSA	VSSSA
36	RSMA	Bias current for synthesiser charge pumps, resistor to ground.	–	VSSSA
37	PDP	Main synthesiser proportional charge pump output.	VDDD	VSSD
38	PDI	Main synthesiser integral charge pump output.	VDDD	VSSD
39	VSSD	Ground for synthesisers, except input buffers and the bandgap.	–	–
40	FIM	Main synthesiser positive input from prescaler.	VDDSA	VSSSA
41	FIMB	Main synthesiser negative input from prescaler.	VDDSA	VSSSA
42	VSSSA	Ground for FIM and FIA input buffers and the bandgap.	–	–
43	VDDSA	Power for FIM and FIA input buffers and the bandgap.	–	–
44	FIA	Auxiliary synthesiser positive input from VCO.	VDDSA	VSSSA
45	FIAB	Auxiliary synthesiser negative input from VCO.	VDDSA	VSSSA
46	DOUT7	Digital control output 7.	VDDD	VSSD
47	DOUT6	Digital control output 6.	VDDD	VSSD
48	DOUT5	Digital control output 5.	VDDD	VSSD
49	MODMP	Modulus control output to prescaler - positive sense.	VDDD	VSSD
50	MODMN	Modulus control output to prescaler - negative sense.	VDDD	VSSD
51	TEST	Test input and output for synthesisers.	VDDD	VSSD
52	PDA	Auxiliary synthesiser charge pump output.	VDDD	VSSD
53	VDDSUB	Clean positive supply to bias substrate.	–	–
54	DOUT3	Digital control output 3.	VDDL	VSSL
55	DOUT4	Digital control output 4.	VDDL	VSSL
56	AMPP2	LF amplifier 2 positive input.	VDDA	VSSA
57	AMPN2	LF amplifier 2 negative input.	VDDA	VSSA
58	DAC3	Analog control output 3.	VDDL	VSSL
59	AMPP1	LF amplifier 1 positive input.	VDDA	VSSA
60	AMPN1	LF amplifier 1 negative input.	VDDA	VSSA
61	AMPO1	LF amplifier 1 output.	VDDA	VSSA
62	ADC2A	Analog to digital converter input 2A.	VDDA	VSSA
63	ADC2B	Analog to digital converter input 2B.	VDDA	VSSA
64	ADC4	Analog to digital converter input 4.	VDDA	VSSA

ABSOLUTE MAXIMUM RATINGS

Supply voltage from ground (any V_{DD} to any V_{SS})	−0·3 V to +6·0 V
Supply voltage difference (any V_{DD} to any other V_{DD})	−0·3 V to +0·3 V
Input voltage (any input pin to its local V_{SS} and V_{DD})	V_{SS} −0·3 V to V_{DD} +0·3 V
Output voltage (any output pin to its local V_{SS} and V_{DD})	V_{SS} −0·3 V to V_{DD} +0·3 V
Storage temperature	−55 °C to +150 °C
Operating temperature	−40 °C to +85 °C

These are not the operating conditions, but are the absolute limits which if exceeded even momentarily may cause permanent damage. To ensure sustained correct operation the device should be used within the limits given under Electrical Characteristics.

To avoid any possibility of latch-up the substrate connections V_{DDSUB} and V_{DDSUB2} must be the most positive of all V_{DD}'s at all times including during power on and off ramping. As the current taken through these V_{DD}'s is significantly less than through the other V_{DD}'s this requirement can be easily met by directly connecting all V_{DD} pins to a common point on the circuit board but with the decoupling capacitors distributed to minimise cross-talk caused by common mode currents. If low value series resistors are to be included in the V_{DD} connections, with decoupling capacitors by the ACE9030 pins to further reduce interference, the V_{DDSUB} and V_{DDSUB2} pins should not have such a resistor in order to guarantee that their voltage is not slowed down at power-on. Power switches to DOUT0 and DOUT1 are supplied from V_{DDX} and are specified for a total current of up to 40 mA so any resistor in the V_{DDX} connection must be very low, around 1Ω, in order to avoid excessive voltage drop; it is recommended that this supply has no series resistor. These two methods are shown in circuit diagrams, figures 4 and 5. In both circuits the main V_{DD} must also have good decoupling.

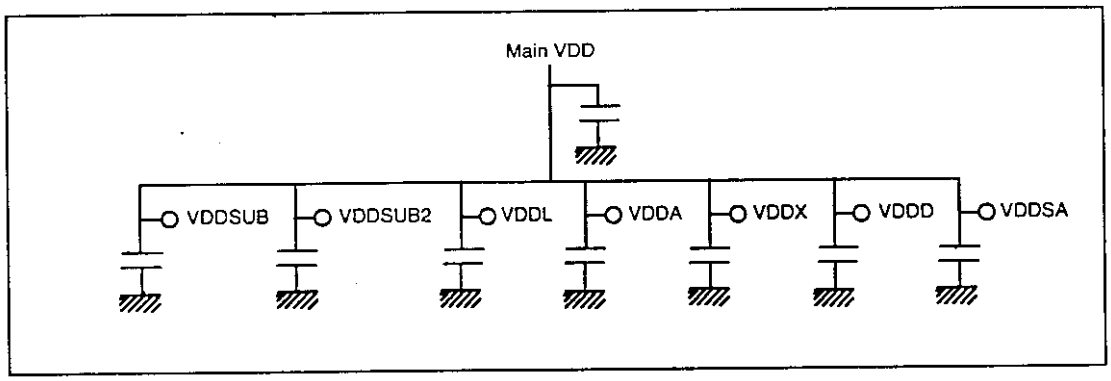


Fig.4 Typical VDD local decoupling networks without series resistors

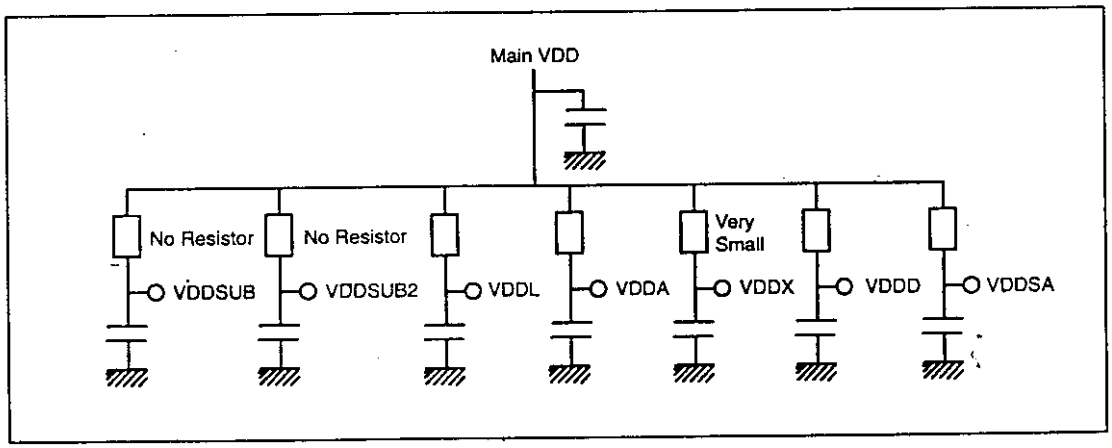


Fig.5 Typical VDD local decoupling networks with series resistors

ELECTRICAL CHARACTERISTICS

These characteristics apply over these ranges of conditions (unless otherwise stated):

T_{AMB} = – 40 °C to + 85 °C, V_{DD} = + 3·6 to + 5·0 V, GND ref. = V_{SS}

D.C. Characteristics

Parameter	Min.	Typ.	Max.	Unit	Conditions
Power supply					
Supply current, Radio Interface: Sleep mode Fully operating (excluding I_{DDX})		2.3	 2·7 7	 mA mA	 XO, OSC8 on (see Note 1)
Supply current, Synthesisers: V_{DD}=5V Main and Auxiliary ON Main ON and Auxiliary in Standby Main in Standby and Auxiliary ON Main and Auxiliary in Standby, with Bandgap off			 5 3.7 3 100	 mA mA mA µA	f_{REF} = 10 MHz f_{MAIN} = 10 MHz f_{AUX} = 10 MHz (see Note 2)
Supply current, Synthesisers: Main and Auxiliary ON Main ON and Auxiliary in Standby Main in Standby and Auxiliary ON Main and Auxiliary in Standby		 3 2 2	 100	 mA mA mA µA	f_{REF} = 15 MHz f_{MAIN} = 16 MHz f_{AUX} = 90 MHz (see Note 2)
Input and output signals					
Logic input HIGH (LATCHC, LATCHB, DATA, CL, and TEST)	0·7 x V_{DD}		V_{DD} + 0·3	V	
Logic input LOW (LATCHC, LATCHB, DATA, CL, and TEST)	– 0·3		+ 0·8	V	
Input capacitance (signal pins) Input leakage (signal pins)			10 1	pF µA	Pin voltage V_{SS} to V_{DD}
Logic output HIGH (RXCD, DATA, AFCOUT, TEST and DOUT2, 3 and 4)	V_{DD} – 0·5			V	External load: 20 kΩ & 30 pF
Logic output LOW (RXCD, DATA, AFCOUT, TEST and DOUT2, 3 and 4)			0·4	V	
Output ON level, DOUT0 and DOUT1	V_{DDX} – 0·2			V	I_{OH} = 20 mA.
Output HIGH level, DOUT5, 6 and 7	2·3		2·9	V	I_{OH} = 80 µA
Output LOW level, DOUT5, 6 and 7			0·3	V	I_{OL} = 0.2 µA
Trimmed output level ON, DOUT8	3·35		3·55	V	I_{OH} = 135 to 400 µA.
Level difference, DOUT8 ON – ADC reference	– 5		+ 15	mV	
Output level OFF, DOUT8			0.4	V	
MODMP, MODMN output HIGH	V_{DD}/2 + 0·35		V_{DD}/2 + 1·0	V	I_{OH} = 10 µA
MODMP, MODMN output LOW	V_{DD}/2 – 1·0		V_{DD}/2 – 0·35	V	I_{OL} = – 10 µA
Input Schmitt Hysteresis, pins CL, LATCHB, LATCHC, DATA.	0·3			V	
Analog circuits bias resistor on I_{REF}		68 100		kΩ kΩ	V_{DD} @ 3·75 V V_{DD} @ 4·85 V

Notes

1. The sleep current is specified with the crystal oscillator (XO) and the OSC8 oscillator and PLL running as these are normally needed to provide the clock to the system controller.

2. The terms f_{REF}, f_{MAIN}, and f_{AUX} refer to the frequencies of the Reference inputs (Crystal oscillator, pins CIN1 and CIN2), the Main synthesiser inputs (pins FIM and FIMB) and the Auxiliary synthesiser inputs (pins FIA and FIAB) respectively.

ELECTRICAL CHARACTERISTICS

These characteristics apply over these ranges of conditions (unless otherwise stated):

T_{AMB} = – 40 °C to + 85 °C, V_{DD} = + 3·6 to + 5·0 V, GND ref. = V_{SS}

D.C. Characteristics (continued)

Parameter	Min.	Typ.	Max.	Unit	Conditions
Synthesiser charge pump current					
Current setting resistor R_{SMA}	19	39	78	kΩ	Note 3
Current setting resistor R_{SC}	19	39	78	kΩ	Note 3
External capacitance on pin R_{SMA}			5	pF	Ensures stable
External capacitance on pin R_{SC}			5	pF	bias current.
Bias current I_{RSMA} (nominally 1·25V / R_{SMA})	28·8	32	35·2	µA	R_{SMA} = 39 kΩ
Bias current I_{RSC} (nominally 1·25V / R_{SC})	28·8	32	35·2	µA	R_{SC} = 39 kΩ
Iprop(0) scaling accuracy, pin PDP	–10		+10	%	@ 200µA. Note 4
Iprop(1) scaling accuracy, pin PDP	–10		+10	%	@ 800µA. Note 4
Iint scaling accuracy, pin PDI	–10		+10	%	@ 4 mA. Note 4
Icomp(0) scaling accuracy, pin PDP	–10		+10	%	@ ACC x 0·2µA Note 4
Icomp(1) scaling accuracy, pin PDP	–10		+10	%	@ ACC x 0·8µA Note 4
Icomp(2) scaling accuracy, pin PDI	–10		+10	%	@ ACC x 4µA Note 4
Iauxil scaling accuracy, pin PDA	–5		+5	%	@ 256µA. Note 4
Auxiliary Charge Pump, Up or Down I_{AUX} current variation	–10		+10	%	Note 5
Main Charge Pumps, Up or Down I_{MAIN} or $I_{INTEGRAL}$ current variation	–10		+10	%	Note 6
Iprop(0) or Iprop(1) setting from PDP pin			1·0	mA	
Iint setting from PDI pin			5	mA	
Icomp(0) or Icomp(1) setting from PDP pin			12	µA	
Icomp(2) setting from PDI pin			180	µA	
Iauxil setting from PDA pin			512	µA	

Notes

3. The circuit is defined with resistors R_{SMA} and R_{SC} connected from pins RSMA and RSC to V_{SSSA} but in most practical applications all V_{SS} pins. will be connected to a ground plane so R_{SMA} and R_{SC} should then also be connected to this ground plane.

4. The charge pump currents are specified to this accuracy when the relevant output pin is at a potential of $V_{DD}/2$ and with R_{SMA} = 39 kΩ, CN = 200, L= 1, K = 5, R_{SC} = 19 kΩ. The nominal value is set by external resistors and by programming registers, as defined in Table 6. Tolerances in the internal Bandgap voltage and bias circuits are within the limits given for I_{RSMA} and I_{RSC}, the scaling accuracy of the multiplying DAC's is within these limits given for Iprop(0), Iprop(1), Iint, Icomp(0), Icomp(1), Icomp(2), and auxil.

5. The Auxiliary charge pump output voltage is referred to as V_{PDA} and the output current I_{AUX} is the Up or Down current measured when $V_{PDA} = V_{DD}/2$.
   The conditions for the variation limits for the Up current are:
   either I_{AUX} = 128 or 256 µA and $0 < V_{PDA} < V_{DD} - 0{\cdot}5$ V
   or I_{AUX} = 512 µA and $0 < V_{PDA} < V_{DD} - 0{\cdot}65$ V
   The conditions for the variation limits for the Down current are:
   either I_{AUX} = 128 or 256 µA and $0{\cdot}5\text{ V} < V_{PDA} < V_{DD}$
   or I_{AUX} = 512 µA and $0{\cdot}65\text{ V} < V_{PDA} < V_{DD}$

6. The Main charge pump output voltage at pin PDP is referred to as V_{PDP} and at pin PDI as V_{PDI}. The output currents I_{MAIN} and $I_{INTEGRAL}$ are the up or down current Iprop(0), Iprop(1) or Iint measured when V_{PDP} or $V_{DPI} = V_{DD}/2$.
   The conditions for the variation limits for the Up current are :
   I_{MAIN} = 100 to 1000 µA or $I_{INTEGRAL}$ = 1 to 5 mA and $0 < V_{PDP} < V_{DD} - 0{\cdot}45$ V
   The conditions for the variation limits for the Down current are:
   I_{MAIN} = 100 to 1000 µA or $I_{INTEGRAL}$ = 1 to 5 mA and $0{\cdot}45\text{ V} < V_{PDP} < V_{DD}$

ELECTRICAL CHARACTERISTICS

These characteristics apply over these ranges of conditions (unless otherwise stated):

T_{AMB} = – 40 °C to + 85 °C, V_{DD} = + 3·6 to + 5·0 V, GND ref. = V_{SS}

A.C. Characteristics

Parameter	Min.	Typ.	Max.	Unit	Conditions
CONTROL BUS					
Clock rate CL input		1008		kHz	
Clock duty cycle CL input	40	50	60	%	
t_{DS}, input data set-up time	80			ns	See Fig. 7
t_{DH}, input data hold time	80			ns	See Fig. 7
t_{CWL}, t_{CWH}, CL input pulse width (to bus logic)	400		600	ns	See Fig. 7
t_{CL}, delay time, clock to latch	440			ns	See Fig. 7
t_{LW}, latch pulse high time	230			ns	See Fig. 7
t_{LH}, delay time, latch to clock	220			ns	See Fig. 7
t_{DSO}, output data set-up time	80			ns	See Fig. 8
t_{DHO}, output data hold time	80			ns	See Fig. 8
t_{ZS}, DATA line available to ACE9030	80		1200	ns	See Fig. 8
t_{ZH}, DATA line released by ACE9030	80		1200	ns	See Fig. 8
t_{CD}, delay from received message to transmitted response	4		4	cycles of CL	See Figs. 8 and 10
Rise and Fall times, all digital inputs:			50	ns	
DIGITAL OUTPUTS					
DOUT0 and 1 On time to V_{DD} – 0·2 V			100	µs	100 nF load and from LATCHB rising edge
DOUT0 and 1 Off time to > 1 MΩ			100	µs	
DOUT5, 6 and 7 rise and fall times			10	µs	30 pF load and to D.C. specification noise
DOUT8 rise and fall time			10	µs	
A to D CONVERTER					
Lowest transition, 0000 0000 to 0000 0001	0·07	0·15	0·23	V	Bandgap multiplier correctly trimmed
Highest transition, 1111 1110 to 1111 1111	3·35	3·45	3·55	V	
ADC conversion time (20 cycles of CL)		20		µs	CL = 1008 kHz
Input scanning rate (CL ÷ 40)		25·2		kHz	CL = 1008 kHz
Integral Non-linearity	– 1		+ 1	LSB	
Differential Non-linearity	– 0·8		+ 0·8	LSB	
Power supply sensitivity			3	LSB/0.3V	0 to 10 kHz
CRYSTAL OSCILLATOR					
Start-up time of crystal oscillator			5	ms	
Crystal effective series resistance (ESR)			25	Ω	
Power dissipation in crystal		50	150	µW	
D to A CONVERTERS					
Full scale output level, DAC1, DAC2 & DAC3	3·35	3·45	3·55	V	Bandgap multiplier trimmed to nominal reference voltage
Zero scale output level, DAC1	1·0		1·2	V	
Zero scale output level, DAC2 & DAC3	0·3		0·5	V	
Integral Non-linearity	– 1		+ 1	LSB	
Differential Non-linearity	– 0·5		+ 0·5	LSB	
Output wideband and clock noise: 50 Hz to 1·1 MHz, flat integration			3	mV_{rms}	
Power supply rejection ratio	30			dB	50 Hz to 25 kHz.
Settling time to within 10% of end of step (DAC3 with external 15 kΩ resistor)			6	µs	DAC1 and DAC2 10 pF load
Output load capacitance, DAC1 and DAC2			100	nF	
Output load capacitance, DAC3			30	pF	To guarantee stability
Internal series resistor, DAC1 and DAC2	7	15	40	kΩ	
DAC3 output current, sink or source	1·0			mA	

ELECTRICAL CHARACTERISTICS

These characteristics apply over these ranges of conditions (unless otherwise stated):

T_{AMB} = – 40 °C to + 85 °C, all V_{DD} = + 3·6 to + 5·0 V, GND ref. = V_{SS}

A.C. Characteristics (continued)

Parameter	Min.	Typ.	Max.	Unit	Conditions
LOW FREQUENCY AMPLIFIERS (1 and 2)					
Voltage Gain	1200	2800			
Input Offset		10	20	mV	
Open loop input resistance		1		MΩ	
Open loop output resistance		8		kΩ	
Unity Gain bandwidth		2		MHz	
Input bias current, inverting input			200	nA	
Power supply rejection at 120 Hz, 10 kHz	40	50		dB	
Output voltage maximum	V_{DDA} – 0·2			V	10 kΩ to 6ND
Output voltage maximum, as a comparator	V_{DDA} – 0·1			V	10 kΩ to 6ND
Output voltage minimum level			0·2	V	10 kΩ to 6ND
Output voltage minimum level			0·1	V	10 kΩ to 6ND
Common mode input range (LF1 1)	V_{SSA}		2.5	V	
Common mode input range (LF1 2)	V_{SSA}		V_{DDA}		
Output slew rate	0.15	0.25		V/µs	
Output load capacitance			30	pF	
8 MHz OSCILLATOR and PLL					
OSC8 centre frequency		8·064		MHz	
OSC8 VCO sensitivity		25		MHz/V	
OSC8 charge pump output current		50		µA	
CLK8 output load, resistive: capacitive:	15 15	25 25	100 30	kΩ pF	
CLK8 output amplitude	0·8	1·0	2·4	V_{pk-pk}	
CLK8 total output jitter			500	Hz	0 - 3 kHz
Start-up time at power-on, to default settings			15	ms	With a loop filter as described in fig. 17
Lock time to within 125 ppm, after reprogramming set-ups			15	ms	
AFCIN F.M. DISCRIMINATOR and AFC					
AFCIN input signal level	0·05		2·5	V_{pk-pk}	
AFCIN input impedance, resistive: capacitive:	50		 10	kΩ pF	
Input frequency	400		500	kHz	
Input signal to integrated noise ratio	10			dB	I.F. ± 15 kHz.
Input Schmitt Hysteresis	8			mV	
AUDIO signal SINAD, psophometric, note 7 AUDIO signal hum and noise, note 7 AUDIO output signal level, note 7	40 195	45 260	 – 46 	dB dB mV_{rms}	1 kHz tone at 3 kHz peak deviation on AFCIN input at I.F.
AFCOUT load			30	pF	
AFCOUT duty cycle	37		63	%	
AFCOUT rise and fall times			75	ns	

Note

7. AUDIO signal quality is measured with feedback components as shown in figure 18 and with 500 mV peak to peak input to AFCIN. Discriminator gain is set with D = 3 and M = 40 and V_{DD} = 3·75 V and a crystal at 14·85 MHz. SINAD is defined as the ratio of wanted signal to all unwanted output, measured simultaneously with filters. The hum and noise figure is defined as the ratio of output power at AUDIO when AFCIN is unmodulated to the output power when AFCIN is driven as specified above.

ELECTRICAL CHARACTERISTICS

These characteristics apply over these ranges of conditions (unless otherwise stated):

T_{AMB} = – 40 °C to + 85 °C, all V_{DD} = + 3·6 to + 5·0 V, GND ref. = V_{SS}

A.C. Characteristics (continued)

Parameter	Min.	Typ.	Max.	Unit	Conditions
LO2 Multiplier					
Amplitude	235		500	mV_{rms}	Circuit as in fig. 15,
Reference frequency content of output			-10.5	dBc	
2nd, 4th harmonic content of output			-13.5	dBc	
5th harmonic of output			-15	dBc	
6th and higher harmonics in output			-20	dBc	
SYNTHESISERS					
Reference divider					
Reference divider input frequency	5		30	MHz	
Drive level into CIN1 from external oscillator	400			mV_{pk-pk}	With crystal oscillator powered down
CIN1 input capacitance			10	pF	
CIN1 input resistance	10			kΩ	
Auxiliary synthesiser					
FIA input frequency	10		135	MHz	May be a sinewave
Rise and fall times of inputs			10	ns	
Timing Skew between FIA and FIAB			± 2 or ± 10%	ns signal period	See Fig. 6 Both maxima must be met
FIA, FIAB differential signal level with both sides driven	180 100			mV_{pk-pk} mV_{pk-pk}	Each input, 5 to 50 & 99 to 135 MHz Each input, 50 to 99 MHz
FIA single input drive level with FIAB decoupled to V_{SS}	360 200			mV_{pk-pk} mV_{pk-pk}	One input, 5 to 50 & 99 to 135 MHz One input, 50 to 99 MHz
FIA, FIAB common mode range	V_{DD} – 1·7		V_{DD} – 0·7	V	V_{DD} = 3.6V
FIA, FIAB common mode range	2.8		V_{DD} – 0·85	V	V_{DD} = 5V
FIA, FIAB input capacitance			10	pF	
FIA, FIAB differential input resistance	10			kΩ	Note 8
Auxiliary Synthesiser comparison frequency			2	MHz	
Main Synthesiser					
FIM input frequency	4		20	MHz	
Rise and fall times of inputs			50	ns	
FIM - FIMB Timing Skew			± 2 or ± 10%	ns signal period	See Fig. 6 Both maxima must be met
FIM, FIMB differential signal level with both sides driven.	100			mV_{pk-pk}	Each input, 4 to 20 MHz
FIM single input drive level with FIMB decoupled to V_{SS}	200		1000	mV_{pk-pk}	One input, 4 to 20 MHz
FIM, FIMB common mode range	V_{DD} – 1·7		V_{DD} – 0·7	V	V_{DD} =3.6V
FIM, FIMB common mode range	2·8		V_{DD} – 0·85	V	V_{DD} =5V
FIM, FIMB input capacitance			10	pF	
FIM, FIMB differential input resistance	10			kΩ	Note 8
Delay FIM rising to MODMP/MODMN changing			30	ns	
Main Synthesiser comparison frequency			2	MHz	

Note

8. To simplify single ended drive there is a resistor between FIA and FIAB and another between FIM and FIMB. In this mode the inputs should drive FIA or FIM with D.C. coupling and the other inputs FIAB and FIMB should be decoupled to ground by external capacitors.

TIMING WAVEFORMS

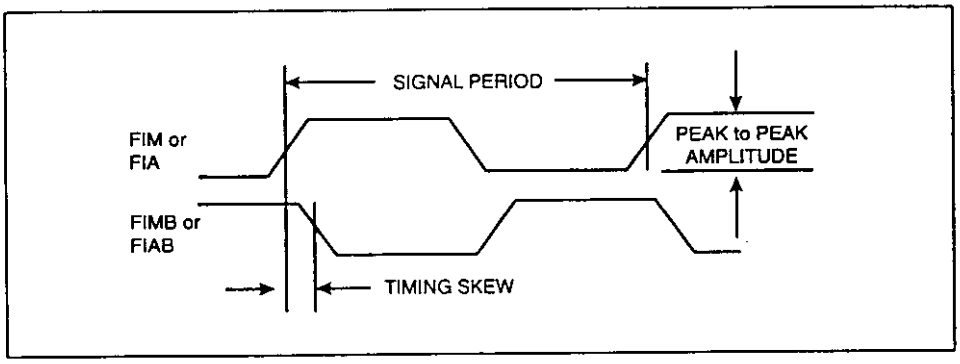


Fig. 6 Synthesiser Inputs

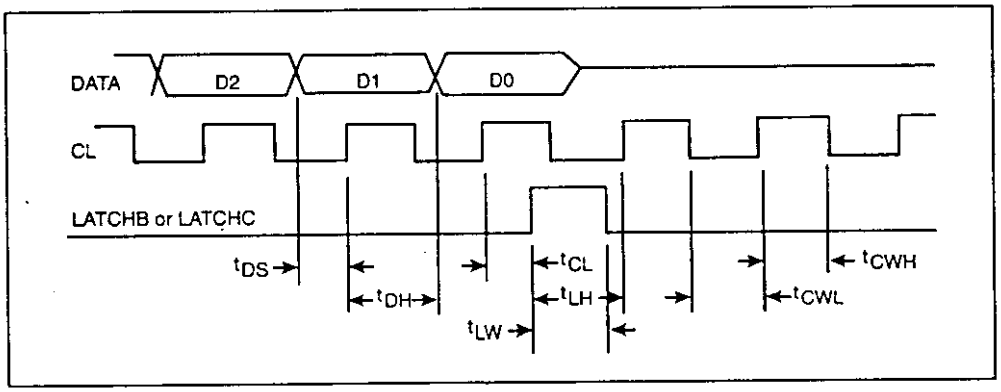


Fig. 7 Control Bus input timing

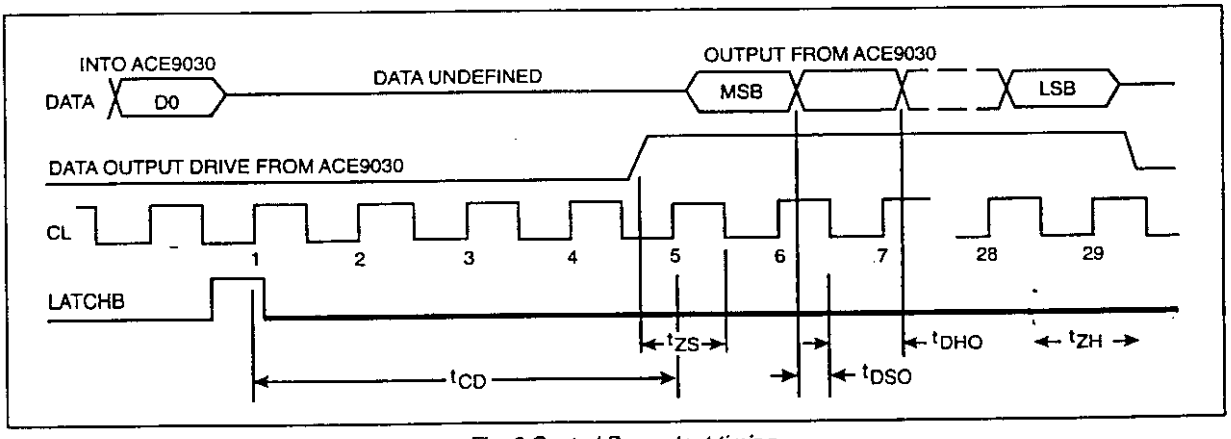


Fig. 8 Control Bus output timing

FUNCTIONAL DESCRIPTION - CONTROL BUS

The functions of the ACE9030 fall into two separate groups, the Radio Interface and the Synthesisers.

The common control bus splits the input strings differently for these two sections so this bus operation is described first as an introduction to the available features.

All functions are controlled by a serial bus; DATA is a bi-directional data line, to input all control data and to output the results of measurements in the Radio Interface section, CL is the clock, and LATCHB and LATCHC are the latch signals at the end of each control word for either the Radio Interface or the Synthesiser section respectively.

CL is a continuously running clock at typically 1·008 MHz, and all incoming and output data are latched on rising edges of this clock. The controller should clock data in and out on falling clock edges. For bus control purposes the frequency of CL may be widely varied and this clock does not need to be continuous, however, the sampled I.F. signal AFCOUT, the Polling ADC, and the Lock Detect Filter also use CL as the sampling clock. In systems where any of these are required the clock CL is constrained to be 1·008 MHz and to be continuous.

To ensure clean initialisation the clock CL should give at least 8 cycles before the power-up command and similarly to set the control logic to known states there should be 8 cycles of CL after a power-down command.

During normal operation there should be at least 30 cycles of CL between latch pulses, 24 for the data bits (see figures 9,10 & 11) plus 6 extra. This minimum becomes 36 cycles if the extended synthesiser programming command (A2) is used.

Radio Interface Bus - Receive

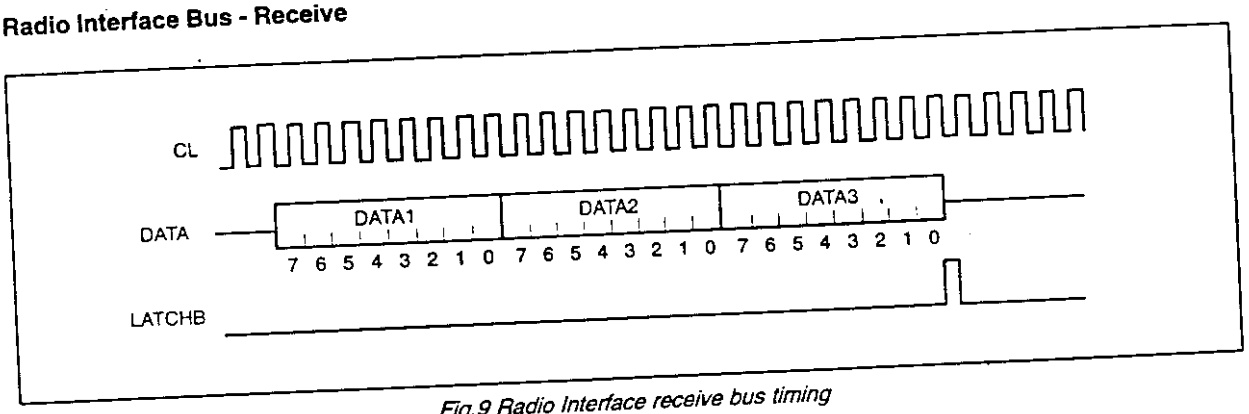


Fig.9 Radio Interface receive bus timing

The received data is split into three bytes, where DATA1 normally contains a value to be loaded into a destination set by DATA2 and DATA3. When a command does not need to put any information into byte DATA1 a preamble xx1010xx is recommended to fill this byte. It is possible to set-up several features in one bus operation and to allow this the decoding only acts on single or selected bits; the others are given as "x" in the block descriptions. Two bits of DATA2 also set the type of command, with four options:

DATA2 bit 7	DATA2 bit 6	Type of Command	Comment
0	0	SLEEP	No reply
0	1	NORMAL	Send requested data
1	0	SET-UP	No reply
1	1	TEST	No reply

Sleep mode is selected to put the cellular terminal into a very low power state for when it is "Off" and neither waiting for, nor setting up a call. In Sleep only the crystal and 8·064 MHz oscillators, DAC1 and DAC2, the OSC8 phase locked loop, and the CLK8 output driver will be active, and are used to clock the microcontroller. To reduce the supply current to its minimum in Sleep the synthesisers must also be powered down, by a Word D message with DA and DM both set HIGH as described under **Synthesiser Bus - Receive Only**. During Sleep all set-up values are retained unless changed by a Set-up command. The exit from Sleep is by any Normal command.

Normal commands will end Sleep mode but are primarily used to change the operating mode of the cellular terminal or to request ADC data. The ACE9030 will output data onto the serial bus after a Normal command.

Set-up commands are used to adjust various operating parameters but can also initiate a logic restart if DATA3 bits 1 and 0 are both "1" so for routine changes of set-ups these bits should always be 00.

Test mode is included only for use during chip manufacture.

The Sleep Command - DATA2 bits 7, 6 = 00

DATA1	DATA2	DATA3
xx1010xx	00xxxxxx	xxxxxxxx

Summary of Normal Commands - DATA2 bits 7, 6 = 01

Normal commands are always a request for data; the ADC registers to be read are defined by Y1 and Y0 in DATA3. A normal command will also end Sleep mode.

BIT	EFFECT when at 0	EFFECT when at 1
DATA2:		
7	With DATA2:6 defines command type	-
6	-	With DATA2:7 defines command type
5	Discriminator powered down	Discriminator active.
4	-	Load Lock threshold register from DATA1:7-1
3	DAC3 powered down	DAC3 active
2	-	Load DOUT7-0 from DATA1:7-0
1	-	Load DAC3 from DATA1:7-0
0	Not used	Not used
DATA3:		
7	Not used	Not used
6	LO2 multiplier powered down	LO2 multiplier active
5	Set DOUT8 to OFF	Set DOUT8 to ON, to output the ADC reference voltage
4	-	Load ADC1 comparator from DATA1:7-0
3	-	Load DAC1 from DATA1:7-0
2	-	Load DAC2 from DATA1:7-0
1	Y1 Decode with DATA3:0 for Polling ADC register read	
0	Y0 Decode with DATA3:1 for Polling ADC register read	

Summary of Set-up Commands - DATA2 bits 7, 6 = 10

BIT	EFFECT when at 0	EFFECT when at 1
DATA2:		
7	-	With DATA2:6 defines command type
6	With DATA2:7 defines command type	-
5	Not used	Not used
4	-	Set OSC8 VCO range from DATA1:5-0
3	-	Set OSC8 VCO offset from DATA1:5-0
2	Select input A for ADC3	Select input B for ADC3
1	Select input A for ADC2	Select input B for ADC2
0	OSC8 off	OSC8 on
DATA3:		
7	Crystal oscillator off	Crystal oscillator on
6	Bandgap off - use external reference	Bandgap on
5	-	Set discriminator divisors from DATA1:7,6 and lock detect period from DATA1:5 and OSC8 divisors from DATA1:2-0
4	-	Set bandgap trim from DATA1:7-0
3	Not used	Not used
2	Not used	Not used
1	-	Do a restart if both DATA3 bits 1 and 0 are at 1
0	-	Do a restart if both DATA3 bits 1 and 0 are at 1

Radio Interface Bus - Transmit

The ACE9030 only drives the bus in response to a request for data by a Normal command as described above. To avoid any bus contention, there is a delay from the end of a data request to the start of the response, see figure 10. The data will start on the fifth rising edge of CL after the rising edge of LATCHB.

The output Preamble word begins with a fixed pattern 1 0 1 0 and then includes the source code number (Y1, Y0) for the Result words and the status of the Lock Detect from the synthesiser, all as described in the section Polling A to D Converter.

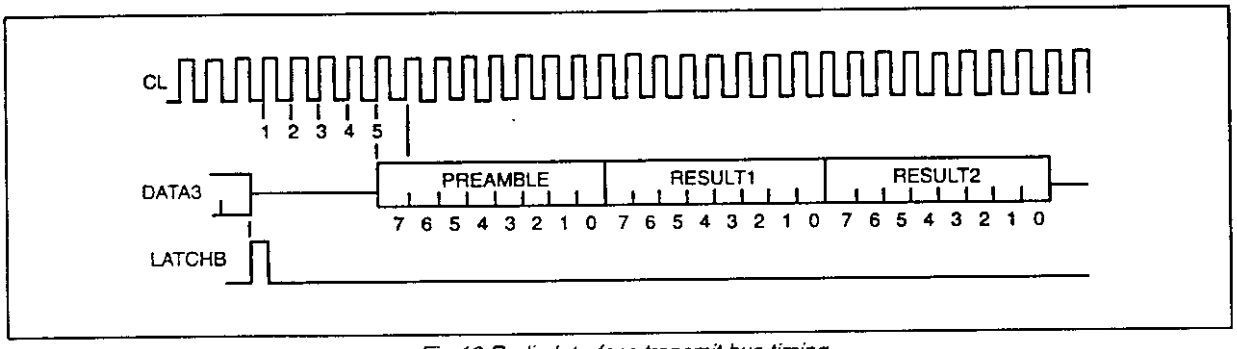


Fig. 10 Radio Interface transmit bus timing

Synthesiser Bus - Receive Only

The overall format to control the synthesiser is basically the same as for the Radio Interface. There is an option of a 32 bit sequence for the A word. The width of the LATCHC pulse is used to set the duration of speed-up mode when changing channels.

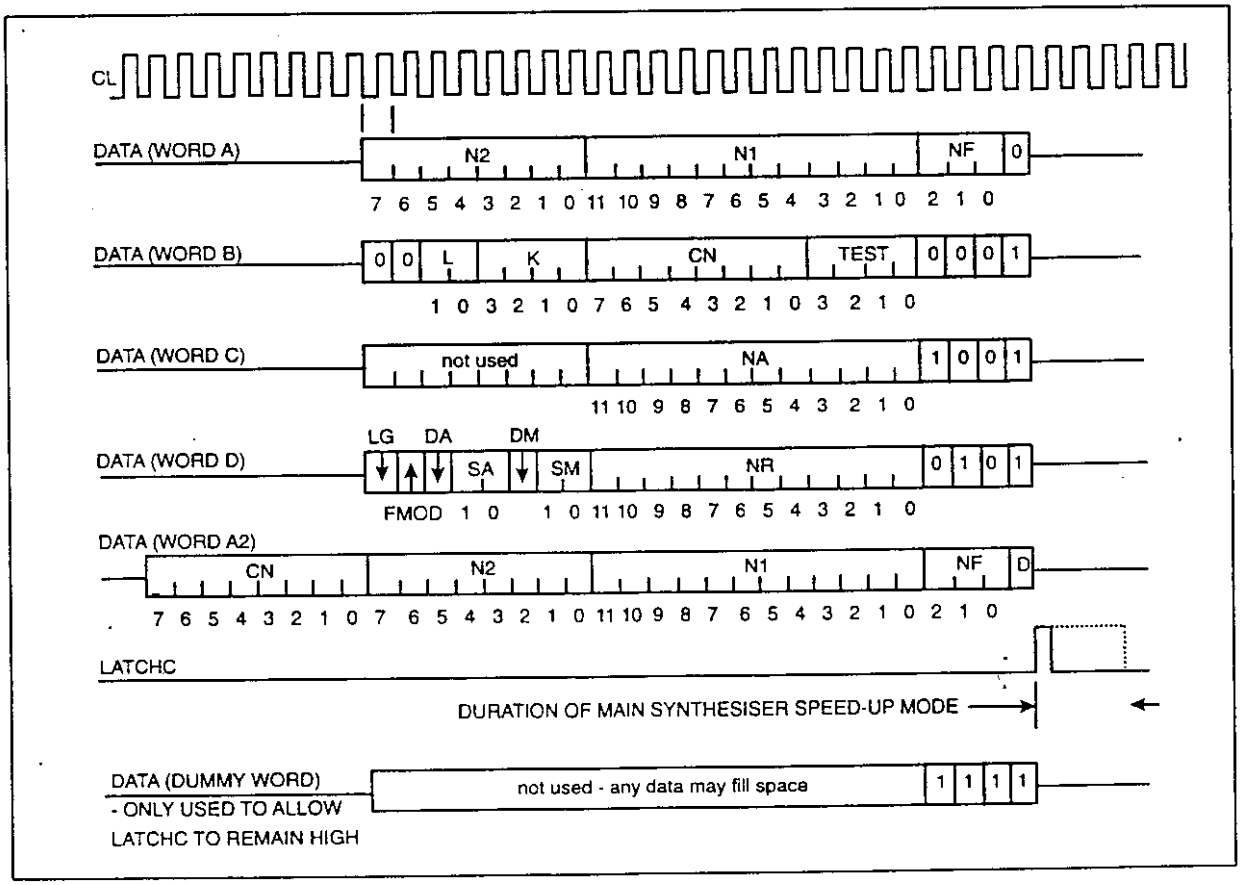


Fig. 11 Synthesiser bus timing

Data is accepted by the circuit on the rising edge of LATCHC. Programmable divider ratios will be changed at their next re-load, at up to a whole comparison period after the LATCHC edge.

Normal channel changes require only word A but if it is necessary to maintain exactly uniform loop dynamics the parameter CN (see Main Synthesiser - Normal Mode) must also change. This can be achieved by either sending a word B for the CN parameter before word A for the frequency or alternatively the extended command A2 can be used to combine both in one long word. This A2 mode is not supported by the ACE9050 as it is not necessary for most cellular terminals.

If Word B is reprogrammed, the new values do not become effective until the next Word A is written. This prevents any spurious conditions during a channel change.

The LG bit in Word D sets whether A or A2 mode is to be used, 0 for A and 1 for A2.

Speed-up drive is active for the duration of the LATCHC pulse that loads the A or A2 word and if it is required the pulse will typically be hundreds of cycles of CL in duration.

In some applications the system performance can be improved by holding LATCHC at HIGH to minimise clock noise on the synthesisers. LATCHC also controls Speed-up mode and so to exit speed-up mode after a channel change the LATCHC must be driven LOW and then a dummy command can be added to get LATCHC back to HIGH. This dummy command should be a non-functional word formed by setting the last four bits to 1111 as in figure 11; the value or the number of the data bits before the four 1's are of no significance so the typical schemes are to send either a standard 24 bit message ending 1111 or a special 4 bit only message of 1111 and in both cases the LATCHC is kept HIGH until the next channel change.

The TEST bits in Word B must be set to 0000 for normal operation and the first two bits in Word B should be set to 00 to be sure of compatibility with future variants.

Summary of Synthesiser Programming

BIT STRING	Range of values	FUNCTION
N1	3 - 4095	Main synthesiser down count; prescaler at lower modulus.
N2	1 - 255	Main synthesiser up count; prescaler at higher modulus.
NF	0 - 7	Main synthesiser fractional increment numerator.
TEST	0000	This state must be selected in every Word B for normal operation. TEST pin will be held LOW to screen adjacent PDA pin. Other test modes are for use during chip manufacture only.
CN	0 - 255	Main charge pump current scaling coefficient.
K	0 - 15	Integral charge pump speed-up mode multiplying factor.
L	0 - 3	Proportional charge pump speed-up mode exponent, giving x 2, x4, x 8 or x 16 current.
NA	3 - 4095	Auxiliary synthesiser VCO divider ratio.
NR	8 - 4095	Reference divider ratio.
SM	0 - 3	Main synthesiser comparison frequency select.
DM	0, 1	Main synthesiser in standby mode if DM set HIGH.
SA	0 - 3	Auxiliary synthesiser comparison frequency select.
DA	0, 1	Auxiliary synthesiser in standby mode if DA set HIGH.
FMOD	0, 1	Fractional-N denominator, $^1/_5$'s when at "0" or $^1/_8$'s when at "1".
LG	0, 1	Control bus mode select - Word A if LOW or Word A2 if HIGH.

FUNCTIONAL DESCRIPTION - BLOCKS IN THE RADIO INTERFACE

Power-On Reset Generator

To ensure a tidy start-up there is an internal power-on detector to initialise various registers.

This initialisation leaves the Radio Interface in Sleep mode with the crystal and 8·064 MHz oscillators running. The 8·064 MHz PLL will be set up for a 15·36 MHz crystal as a default to ensure the microprocessor is not clocked too fast during the start up sequence. Any Normal command can be used to change to active operation.

A software Restart command can be sent to force the Radio Interface to the power-on reset state. This command is:

DATA1	DATA2	DATA3
xxxxxxxx	10xxxxxx	xxxxxx11

Digital Outputs

The nine digital outputs, DOUT8 to DOUT0, are used to control the status or function of radio subsections external to the ACE9030 and are controlled by a Normal type command with a logic "1" setting the output to HIGH or ON and a logic "0" giving LOW or OFF.

Outputs DOUT0 and DOUT1 are power switches from V_{DDX} to supply Front-End circuits. Both are forced to OFF in Sleep mode.

Outputs DOUT2 to DOUT4 are logic level outputs to control various functions in the cellphone. DOUT2 and DOUT3 are forced to HIGH and DOUT4 is forced to high impedance in Sleep mode.

Outputs DOUT5 to DOUT7 are low current outputs with reduced voltage swing to control power down in the ACE9010 and ACE9020. All three are forced to LOW in Sleep mode.

Output DOUT8 can be driven by the buffered Band-gap based ADC reference voltage and is included for test and setting-up purposes, as well as for driving a temperature sensing thermistor read through one of the ADC channels. DOUT8 is forced to high impedance in Sleep mode.

The control formats are Normal commands:

DATA1	DATA2	DATA3
$D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1\ D_0$	01xxx1xx	xxxxxxxx

where DATA1 bits 7 to 0 control DOUT7 to DOUT0 respectively when enabled by DATA2 bit 2, and:

DATA1	DATA2	DATA3
xxxxxxxx	01xxxxxx	xx D5 xxxxx

where DATA3 bit 5 controls DOUT8 directly.

Lock Detect Filter

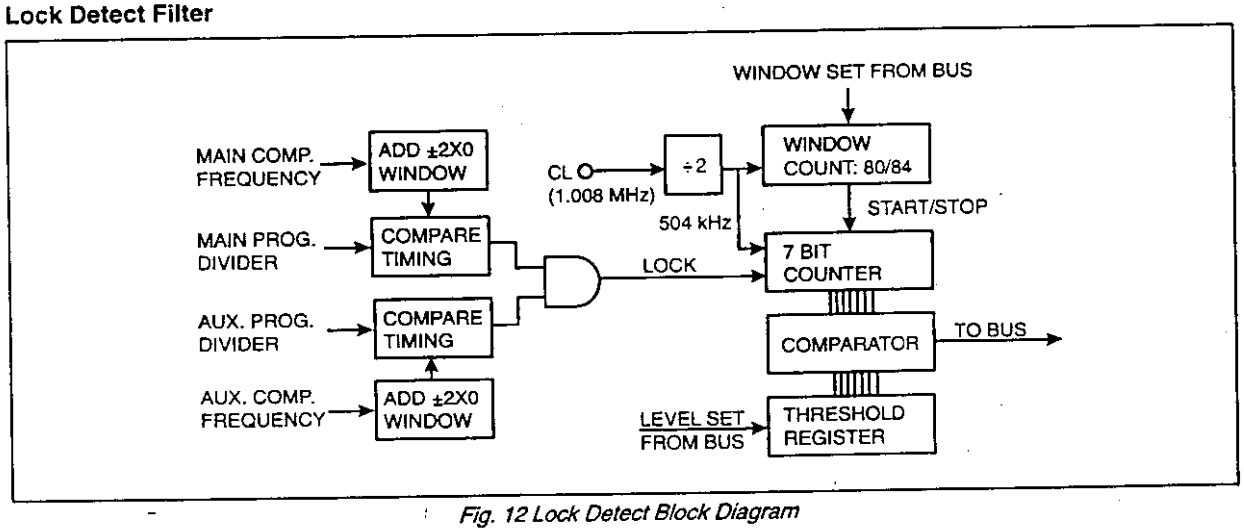


Fig. 12 Lock Detect Block Diagram

The Lock Detect Filter processes the phase errors in both synthesisers to give a clean signal to put onto the bus as a single bit added to the ADC read response.

In the synthesiser section of the ACE9030 the time differences between the active edges of the outputs of the programmable dividers and of the reference divider are compared with a window of two cycles of the reference clock, XO, from the crystal oscillator. If a loop has a time difference, or phase error, larger than this window then that loop is deemed unlocked and its lock signal is held low for a whole comparison period, giving a Main Lock and an Auxiliary Lock signal. When both synthesisers are active the error signals are combined by an AND function to give the internal signal LOCK. If either synthesiser is powered down its lock is disregarded and if both are powered down the ACE9030 will always give LOCK at LOW, the unlocked state, to be output on the bus. This final signal LOCK is normally HIGH to indicate locked loops but will pulse low for one or more comparison periods when an active synthesiser is unlocked.

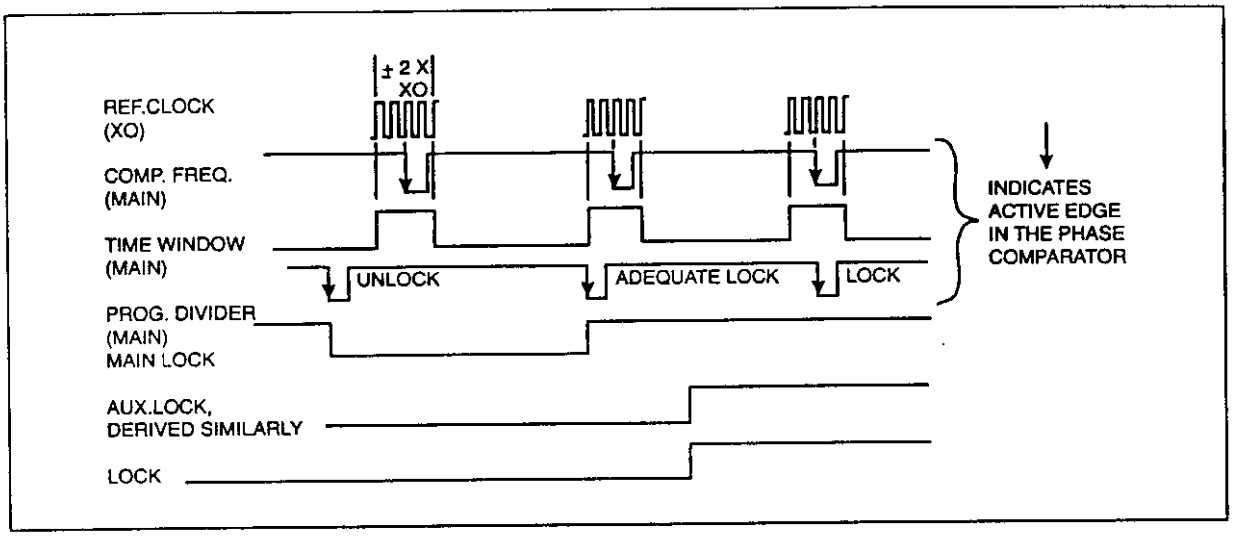


Fig. 13 Typical Lock Detect Waveforms

Pulses can occur on the LOCK signal at a rate up to the higher of the Main and Auxiliary comparison frequencies, and typically either 12·5 kHz for ETACS (50 kHz if Fractional-N is used) or 30 kHz for AMPS so some extra filtering is needed to get a clean lock indicator.

LOCK is filtered by first sampling at 504 kHz (the bus clock CL divided by two) and then counting the number of HIGH samples in a pre-determined period. There are two selections available for this counting period, approximately 160 µs (2 periods of 12·5 kHz or 8 of 50 kHz) or approximately 167µs (5 periods of 30 kHz) which are set by a second counter, also running at 504 kHz and with a fixed modulus of 80 or 84. LOCK is stable for each comparison period so the counts for each comparison frequency are always in blocks of 40 for 12·5 kHz, 10 for 50 kHz or 16 for 30 kHz.

The value in the LOCK sample counter is compared with a threshold previously set by another bus command, to determine if the loops are locked, the result is then output as the last bit in the pre-amble word in the response to a Normal command, before the ADC levels are given, as described in the section Polling A to D converter.

The filter period is selected by the following Set-up command where DATA1 bit D_5 sets the period to one of the two values to suit whichever cellular system is to be used:

DATA1	DATA2	DATA3
xx D_5 xxxxx	10xxxxxx	xx1xxx00

DATA1:5 = 0 sets 160 µs for ETACS (Window count = 80) and DATA1:5 = 1 sets 167 µs for AMPS (Window count = 84).

The threshold is set by a Normal command:

DATA1 bits D_7 to D_1 form a 7 bit binary number in the range

DATA1	DATA2	DATA3
D_7 D_6 D_5 D_4 D_3 D_2 D_1 x	01x1xxxx	xxxxxxxx

0 to 127, which is the threshold value to be loaded. The window period of 80 or 84 clock cycles sets the maximum count value that can be found; the effect of unlock is to reduce the actual count by at least one comparison period's worth of samples 40, 10, or 16 so a suitable threshold can easily be chosen. Assuming that the maximum sensitivity is required the threshold should be set at just above the maximum count (80 or 84) minus the effect of one unlock count (40, 10, or 16), to give suggested thresholds of at least 42 (for 12·5 kHz) or 72 (for 50 kHz) or 70 (for 30 kHz). In each case any convenient number between these suggestions and the maximum count may be used as the selection is not critical.

Polling A To D Converter

A five channel polling Analog to Digital Converter is used to monitor various analog levels, such as Received Signal Strength, Transmitter Power, Temperature and Battery Voltage. The 8 bit ADC has a nominal range of 0·15 V to 3·45 V for codes 00 to FF and is connected to each input channel, ADC1 to ADC5, in turn by the scanning logic. The results are put into individual registers for reading by the microcontroller. The successive approximation technique is used, with the bus clock CL controlling both the timing of the conversion and also the polling around the inputs. The voltage reference for the ADC is shared with the three DAC's and is derived from the bandgap voltage through a trimming multiplier which can be monitored on DOUT8 and is described in the section Band-Gap Reference. Some channels are scanned more frequently than others, with the pattern:

5, 1, 5, 2, 5, 1, 5, 3, 5, 1, 5, 4,

which repeats continuously. With clock CL at its normal 1008 kHz frequency, the scanning rates are 12·6 kHz for ADC5, 6·3 kHz for ADC1 and 2·1 kHz for ADC2, 3 and 4.

Channels 2 and 3 each have two options, 2A, 2B and 3A, 3B as pins to connect to alternative points to monitor. The selection is by a Set-up command:

DATA1	DATA2	DATA3
xxxxxxxx	10xxx D_2 D_1 x	xxxxxx00

where DATA2 bit D_2 selects ADC3B when HIGH or ADC3A when LOW for measurement by channel 3, and DATA2 bit D_1 selects ADC2B when HIGH or ADC2A when LOW for measurement by channel 2.

The ADC data in the five registers is read in response to a Normal command, with the two results to be output being selected by two bits of DATA3:

DATA1	DATA2	DATA3
xxxxxxxx	01xxxxxx	xxxxxxY_1Y_0

where Y_1 Y_0 are decoded to select:

Y_1	Y_0	Data requested
0	0	ADC5 & ADC1
0	1	ADC5 & ADC2A/B
1	0	ADC5 & ADC3A/B
1	1	ADC5 & ADC4

The requested data is then clocked out after a fixed delay, with a preamble followed by the two results:

PREAMBLE	RESULT 1	RESULT 2
1010 Y_1 Y_0 0 L	RRRRRRRR	RRRRRRRR

The Y_1 Y_0 code is output to confirm the data selection and is the same as in the Normal command that requested the data, detailed above, L is the Lock Detect status from the Lock Detect Filter, and the two results are in the order ADC5 in RESULT 1 and ADC1, 2, 3, or 4 in RESULT 2.

The level in the ADC1 register is continuously compared with a threshold number such that if ADC1 is above this threshold the output pin RXCD is driven HIGH and can be used to indicate the presence of a received carrier. The threshold is set by a Normal command on the bus, with the value in DATA1:

DATA1	DATA2	DATA3
DDDDDDDD	01xxxxxx	xxx1xxxx

IREF Bias Circuit

To set the operating current for several blocks in the Radio Interface there is a bias pin I_{REF} which should be connected to the ground plane (V_{SS} pins) via a resistor whose value depends on the supply voltage, 68 or 100 kΩ for 3·75 V or 4·85 V nominal V_{DD}. The current into this pin is then mirrored to the various functional blocks. To reduce the noise on this bias a capacitor can be added from the IREF pin preferably to the supply or alternatively to a good ground. A value of 82 nF offers a good compromise between noise rejection and power-up time.

D to A Converters

There are three 8-bit DAC's with buffered outputs in the ACE9030.

DAC1 and DAC2 have a high zero offset, a nominally 15 kΩ output series resistor, and are stable when driving up to a 100 nF load capacitance.

DAC3 has a low zero offset and no output resistor. In order to guarantee stability the capacitance of the load on DAC3 must be no more than 30 pF.

The output resistors on DAC1 and DAC2 are used to form part of a low pass filter and these DAC's are intended to be used to adjust the crystal frequency as given below under Crystal Oscillator.

The level for each DAC is set by a Normal command:

DATA1	DATA2	DATA3
DDDDDDDD	01xxxx D_1 x	xxxx D_3 D_2 xx

where the data in DATA1 is loaded into DAC1 if DATA3 bit D_3 is HIGH, into DAC2 if DATA3 bit D_2 is HIGH, or into DAC3 if DATA2 bit D_1 is HIGH.

DAC1 and DAC2 remain active during Sleep mode but the outputs are driven with reduced current capability; this will slightly reduce the accuracy and will significantly increase the settling time to any level change. DAC3 is powered down in Sleep mode.

To power down DAC3 outside of Sleep mode, a Normal command may be used:

DATA1	DATA2	DATA3
xxxxxxxx	01xx D_3 xxx	xxxxxxxx

where DAC3 is active if DATA2 bit D_3 is HIGH or powered down if DATA2 bit D_3 is LOW.

L.F. Amplifiers

Two identical low frequency amplifiers are provided; one has inputs AMPP1 and AMPN1 driving output AMPO1, the other has inputs AMPP2 and AMPN2 driving output AMPO2.

A typical use for AMP1 is as a linear amplifier to buffer the DAC3 output to drive the transmit power control in a software controlled loop with a power sensor input to ADC5.

AMP2 is typically used as a comparator to detect transmit power independent of the software as a system integrity check. The System Controller can then gate the presence of transmitter power on AMPO2 with the absence of received carrier on RXCD to detect a non-valid status and re-initialise the system.

Crystal Oscillator

A crystal oscillator maintaining circuit is provided on pins CIN1 and CIN2 for use with a crystal at 12·8, 14·85 or 15·36 MHz depending on the cellular system chosen. The circuit is designed for a crystal cut for a 20 pF load and with an ESR less than 25 Ω. To ensure reliable fast start times for this oscillator the bias current is increased significantly for the first 2047 cycles of oscillation after power-up, a restart command or after an oscillator ON command and then automatically changes to the lower normal level. The normal level has been chosen to still guarantee start-up if the circuit should be stopped by some external interference but to consume less power than the fast start mode.

The buffered internal output of this oscillator is used in several sections of the chip and is referred to as XO in this data sheet. This oscillator can be trimmed by using DAC1 and DAC2 to control varicap diodes and so to pull the frequency, the two DAC's may be used to give separate AFC and temperature compensation. A typical external circuit is shown in figure 14. Each DAC provides typically 30ppm tuning range.

If preferred, an external oscillator can be used by driving into CIN1 with CIN2 left open circuit. To allow this external drive the internal oscillator should be shut down by using a Set-up command with DATA3 bit D_7 at LOW. The internal oscillator is switched on at power-up, at restart, and by a Set-up command with DATA3 bit D_7 at HIGH:

DATA1	DATA2	DATA3
xxxxxxxx	10xxxxxx	D_7 xxxxx00

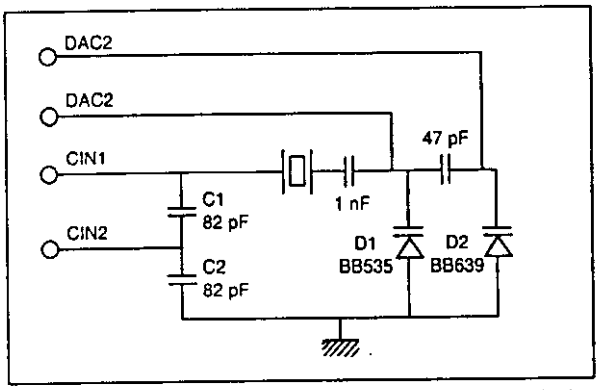


Fig. 14 Crystal Oscillator Trimming Circuit with Typical Component Values

Crystal Multiplier for LO2

To mix the first intermediate frequency signal down to the second IF a second local oscillator is needed. In the ACE9030 there is a crystal frequency multiplier to generate this signal by squaring the crystal oscillator waveform and selecting the desired harmonic. To multiply the crystal frequency by 3 or 5 output LO2 is driven at the reference frequency with a 1:1 mark space ratio. This ratio of 1:1 is chosen to minimise the even harmonics, especially the second and fourth. A tuned circuit will pick off the required harmonic. ACE9030 is specified with the external components shown in Figure 15 giving 44.55 MHz derived from 14.85 MHz crystal. The 6.8kΩ resistor and 5.6pF capacitor represent the input impedance of a typical IF amplifier LO input.

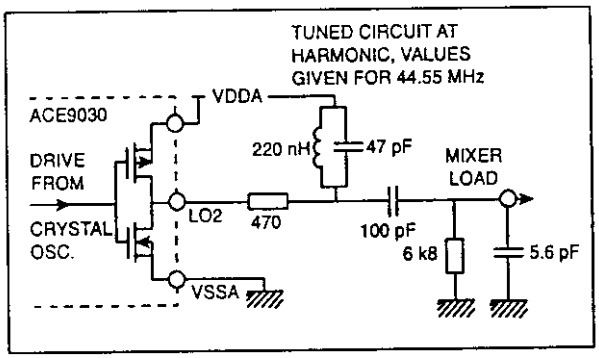


Fig. 15 Basic Circuit of the Crystal Multiplier

Typical frequencies generated by the multiplier are:

Crystal	Multiplier	LO2	1st I.F.	2nd I.F.
14·85 MHz	x 3	44·55 MHz	45·00 MHz	450 kHz
15·36 MHz	x 5	76·80 MHz	77·25 MHz	450 kHz

Typical performance for noise power measured in the adjacent channels, 16 kHz wide at 25 kHz offset is – 70 dBc.

To power down the multiplier if it is not required, a Normal command can be used with DATA3 bit D6 set to LOW, to set the multiplier power on DATA3 bit D6 should be set to HIGH:

DATA1	DATA2	DATA3
xxxxxxxx	01xxxxxx	x 1 xxxxxx

Band-Gap Reference

A band-gap voltage reference is used to set levels in the ADC, in the DAC's and the currents in the synthesiser charge pumps. This voltage is smoothed by an external decoupling capacitor on the DECOUP pin.

The voltage derived for the ADC full range reference can be monitored through pin DOUT8. The Radio Interface DAC reference is nominally the same as the ADC reference and it can be monitored independantly of DOUT8 by setting DAC3 (the low output impedance DAC) to full scale.

To power down the band-gap reference to allow the use of an external reference voltage on pin DECOUP the following Set-up command can be used:

DATA1	DATA2	DATA3
xxxxxxxx	10 xxxxxx	x 1 xxxx00

where the band-gap is powered down if DATA3 bit D6 is LOW or is active if DATA3 bit D6 is HIGH.

The band-gap voltage multiplier for the ADC and DAC reference (nominally 3·45 V) can be adjusted by a Set-up command to correct for production spreads:

DATA1	DATA2	DATA3
DDDDDDDD	10xxxxxx	xxx1xx00

where the value in DATA1, G_{BG}, sets the gain from band-gap to output voltage according to the approximate equation:

$$\frac{V_{OUT}}{V_{BG}} = \frac{(430 \times G_{BG} + 355 \times 10^3)}{(145 \times 10^3)}$$

For a typical V_{BG} of 1·2 V the number is approximately 144 (= 90_{HEX}) and for a typical V_{BG} of 1·3 V the number is approximately 70 (= 46_{HEX}) and a suitable trimming pattern can be chosen.

8·064 MHz Oscillator

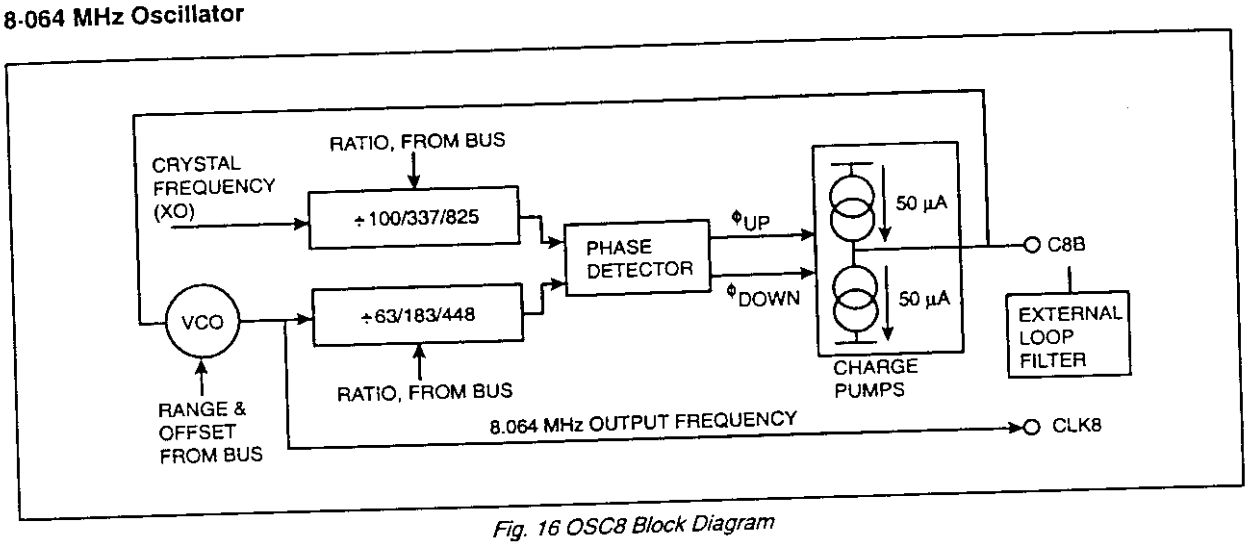


Fig. 16 OSC8 Block Diagram

An 8·064 MHz oscillator OSC8 is provided to drive the ACE9050 System Controller through pin CLK8. ACE9050 further drives the ACE9040 Audio Processor and the CL bus clock via a ÷ 8 divider. OSC8 is locked to the crystal oscillator by a phase locked loop with an external filter on pin C8B.

This loop can be programmed by a Set-up command to give the correct output frequency with any of the normally used crystals. Note that the same Set-up command uses DATA1 bit D_5 for the lock logic and bits D_7 and D_6 for the Discriminator programming:

DATA1	DATA2	DATA3
xxxxx D_2 D_1 D_0	10xxxxxx	xx1xxx00

where D_2 D_1 D_0 act as in table 2. At power-on reset the setting is D_2 D_1 D_0 = 110, the values for a 15·36 MHz crystal, so that the microcontroller is never clocked too fast with any of the crystals and can then send the Set-up message to set D_2 D_1 D_0 to the correct levels.

With a 14·85 MHz crystal it is not possible to both use a high comparison frequency and get the exact 8·064 MHz output, so two options are provided. The lower comparison frequency will give the output exactly correct but will need larger capacitors in the loop filter and the higher option allows smaller capacitors and can improve close-in phase noise by having a larger loop bandwidth, but gives a very small frequency error - this error should have no effect in a practical cellular terminal.

A Sleep command will not change the status of OSC8; if enabled it will remain active when put into Sleep mode and when returning to Normal mode. If the OSC8 oscillator is not required it can be switched off by a Set-up command:

DATA1	DATA2	DATA3
xxxxxxxx	10xxxxx D_0	xxxxxx00

where DATA2 bit D0 at LOW gives OSC8 OFF or DATA2 bit D_0 at HIGH gives OSC8 ON.

To allow for design and manufacturing tolerances the VCO can be trimmed by two set-up commands, each of which loads a 6 bit value in DATA1 into a control register. One sets frequency "Range" (effectively the VCO gain but also with an effect on the centre frequency):

DATA1	DATA2	DATA3
xx D_5 D_4 D_3 D_2 D_1 D_0	10x1xxxx	xxxxxx00

The other sets frequency "Offset" (effectively the VCO centre frequency but also with an effect on the gain):

DATA1	DATA2	DATA3
xx D_5 D_4 D_3 D_2 D_1 D_0	10xx1xxx	xxxxxx00

The default values loaded by the power-on reset are Offset = $0A_{HEX}$ and Range = 21_{HEX} and were chosen to help ensure that the output clock on CLK8 does not run faster than 8·064 MHz while better values are to be loaded. These default values can usually be left unchanged for normal operation.

The output of the phase comparator charge pump is on pin C8B so that an external loop filter can be connected. This loop filter then drives the VCO control voltage, also through

Command Data D2 D1 D0	Crystal frequency	Crystal divider	PLL comp. freq. (kHz)	OSC8 divider	Exact CLK8 output (MHz)	Error (ppm)
1 0 0	12·8 MHz	+100	128	+63	8·064	0
0 1 1	14·85 MHz	+825	18	+448	8·064	0
1 0 1	14·85 MHz	+337	44·065281	+183	8·0639466	−7
1 1 0*	15·36 MHz	+120	128	+63	8·064	0

* Power up default

Table 2

C8B to close the loop. An integration is needed to set the VCO onto the correct frequency and other components can then ensure loop stability. Enough filtering must be provided to give a clock output suitable for all of its uses - microprocessor clock and audio filtering. A typical loop filter is shown in figure 17.

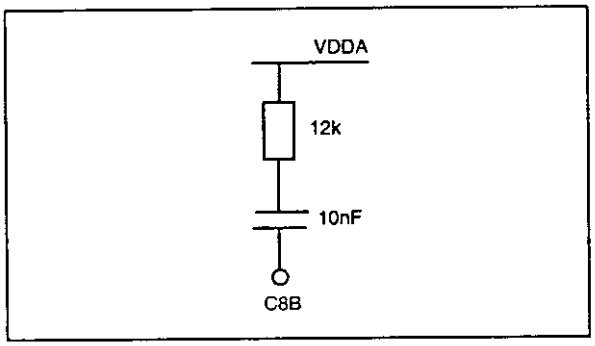


Fig. 17 Typical OSC8 Loop Filter

AFC Amplifier and Discriminator

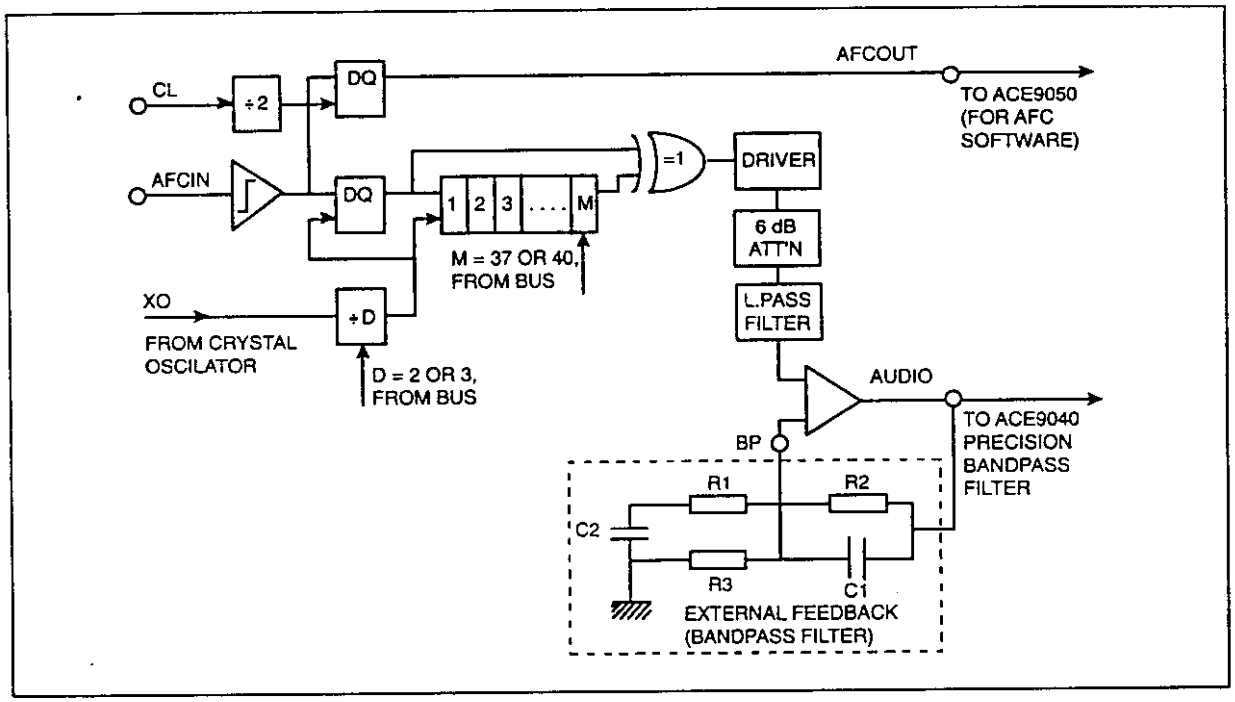


Fig. 18 Audio Discriminator And AFCOUT Circuit

The input signal to the pin AFCIN is approximately a squarewave from the second (final) I.F. amplifier-limiter at 450 or 455 kHz and is A.C. coupled to the pin through a capacitor of typically 1 nF to drive a Schmitt trigger and become a logic signal. This signal carries the received modulation - speech, SAT and signalling data. AFCIN is first amplified and limited and then processed in two separate paths as in figure 18.

One path samples the input signal at 504 kHz, with a clock generated by a divide-by-two from the CL clock. This sampling gives a mixed-down output AFCOUT at 54 kHz when the input is at exactly 450 kHz and otherwise tracks the offset to allow estimation of the local oscillator error and the crystal error so that an AFC loop can be built to adjust the crystal to exactly the correct frequency. Further details of this feature are given in the APPLICATIONS HINTS section. AFCOUT is also used by the modem in the ACE9050 to receive signalling DATA.

The other path is the audio discriminator which is a purely digital implementation of the quadrature technique where the exclusive-OR gate acts as a digital multiplier and compares two samples of the AFCIN signal separated by a programmable delay to extract the audio and drive the speech and SAT paths in the ACE9040. The delay length, M, and the crystal divider, D, are both programmable for the various crystal and intermediate frequency choices.

After demodulation the audio is low-pass filtered on-chip to remove the doubled sampling clock and then bandpass

filtered to nearer telephone bandwidth by an on-chip amplifier with off-chip feedback components.

The I.F. signal is digitised at a rate set by the crystal in use and by the divider D in figure 18 and so will be in the range 4·267 to 7·680 MHz. These rates are all greater than the maximum audio frequency of 3·4 kHz by a factor of at least 1254 (which is over 2^{10}) and so the quantisation allows better than 63 dB signal to noise ratio in the final audio, even though only single bit quantising is used. The I.F. is oversampled by a much smaller ratio and so will have a smaller signal to noise ratio if measured in its total bandwidth, but this bandwidth is reduced in the demodulation process to give a good audio signal to noise ratio in the system.

To power down the discriminator a Normal command can be used:

DATA1	DATA2	DATA3
xxxxxxxx	01 D_5 xxxxx	xxxxxxxx

where the discriminator is powered down if DATA2:D_5 is LOW or is set active if DATA2:D_5 is HIGH.

The values of the programmable constants D and M are set by a Set-up command, which can also use DATA1 bit D_5 for the lock logic filter period and DATA1 bits D_2, D_1, D_0 for the OSC8 mode programming:

DATA1	DATA2	DATA3
D_7 D_6 xxxxxx	10xxxxxx	xx1xxx00

The two control bits D_7, D_6 set the values for D and M as in table 2. From this table of frequencies and division ratios it is possible to calculate the length of the delay M in terms of cycles of the input I.F. to understand the discrimination process shown in table 3.

It can be seen that a 12·8 or 15·36 MHz crystal will give a delay of a few whole cycles plus or minus one quarter cycle to a very good accuracy and that a 14·85 MHz crystal similarly gives some whole cycles plus or minus an odd third of a cycle.

These non-integer delays are needed because the delays are not locked to the I.F. input on AFCIN, and to get a demodulated output the comparisons must include an edge time, at least for some samples. The odd quarter or third of a cycle ensures that the phase of the start of the delay time will rapidly increase relative to the I.F. signal and so avoid low frequency beats, when the system could sit in the state where a steady part of one cycle is compared with a steady part of another for a long period of time and so give no output.

The accuracy of the delay is not important as a small error will only give a D.C. offset in the output but the delay must be consistant to avoid adding modulation to the output so in the ACE9030 it is derived from the crystal frequency.

The sampling rate must not be a harmonic of the I.F., or very close to one, to prevent the sampling phase becoming synchronised to the signal and so missing all edges, leading to the modulation being lost for long periods of time at the beat frequency (a 14·85 MHz crystal cannot be used in D = 3 mode with an I.F. at 450 kHz as 14·85 MHz÷3 is 4·95 MHz which is 11 x 450 kHz). It cannot be assumed that a sampling rate greater than 4 MHz always meets the Nyquist criterion for the I.F. signal at nominally 450 or 455 kHz because the input signal is often a square wave from a limiting amplifier and if not is converted to a switching logic signal in the Schmitt trigger input buffer giving many significant harmonics. The modulation deviation is up to 14·5 kHz and is multiplied by the harmonic number to give increasingly wide deviation such that the spectrum eventually becomes continuous, but at a low level, for the very high (e.g.17th or above) harmonics. A sampling rate of a few MHz will then retain all required information and allow distortion free demodulation but is undersampling in Nyquist terms so aliasing effects must be avoided by choosing a frequency separated from the nearest harmonic of the I.F. by at least twice the modulation frequency. All combinations given in tables 2 and 3 can safely be used but care is needed if a different crystal or I.F. is required. For example, a 14·4 MHz crystal cannot be used in÷2 mode with a 450 kHz I.F. but÷3 can be used and with an M of 40 will give a delay of 3·75 I.F. cycles and alias-free demodulation.

Sampling the I.F. signal at a rate of only 9·3 to 16·9 times the I.F. will remove the fine detail of the modulation from each individual cycle of the I.F. but the modulation bandwidth is very low (both speech and tones) compared to this sampling rate so the information will be preserved as infrequent whole sample steps, which when averaged over many samples will show the correct modulation.

To explain the operation of the discriminator an example diagram of the sampling points and the comparison delay is given in figure 19, with the effect of modulation on the input shown by fine lines. The increasing separation of these dotted

DATA1 bit D_7	DATA1 bit D_6	Set D	Set M	Intended I.F.	Intended Crystal
0	0	2	39	450 kHz	12·8 or 14·85 MHz
1	0	3	40	455 kHz	12·8 or 14·85 MHz
0	1	3	37	450 kHz	15·36 MHz
1	1	2	38	455 kHz	15·36 MHz

Table 2

D_7, D_6	D	M	Crystal Freq.	Sampling Rate	I.F.	Delay as I.F. cycles
0, 0	2	39	12·80 MHz	6·400 MHz	450 kHz	2·742
0, 0	2	39	14·85 MHz	7·425 MHz	450 kHz	2·363
1, 0	3	40	12·80 MHz	4·267 MHz	455 kHz	4·266
1, 0	3	40	14·85 MHz	4·950 MHz	455 kHz	3·677
0, 1	3	37	15·36 MHz	5·120 MHz	450 kHz	3·252
1, 1	2	38	15·36 MHz	7·680 MHz	455 kHz	2·251

Table 3

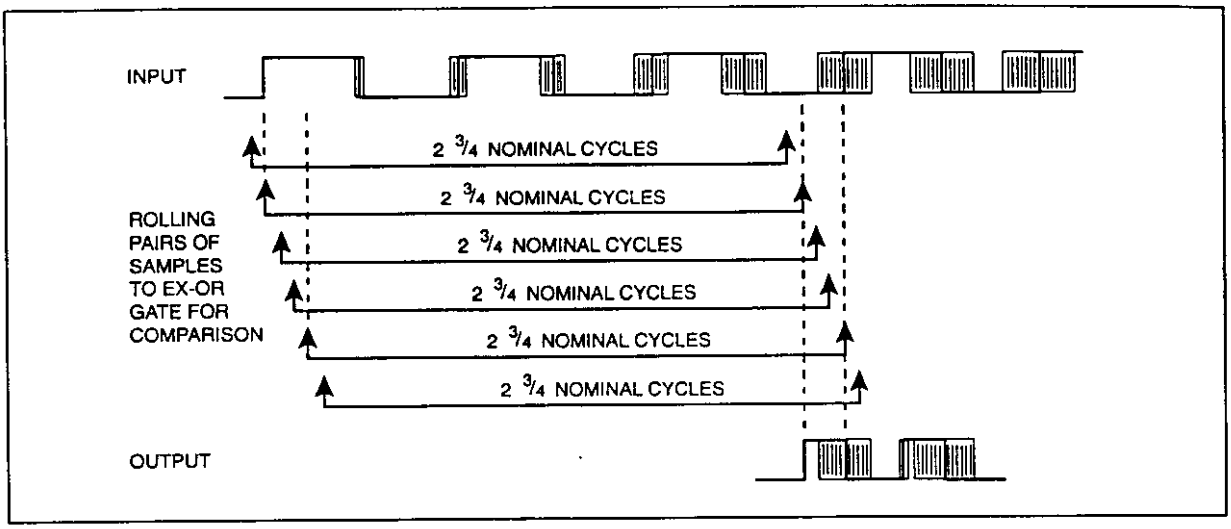


Fig. 19 F.M. Discriminator Example Timing Diagram

phase effect of f.m. increases as more cycles are examined. The modulation lines are drawn as the phase change on the real input waveform but the separation from the nominal edge position can also be interpreted as the probability of a whole cycle shift on the sampled version of the signal as in the ACE9030.

Only six delay comparisons are shown, stepping across at the sampling rate, but the effect of the pattern can easily be seen by continuing the sequence, and two conclusions can be drawn:

1) The output waveform is at twice the frequency of the input - this is true for all delay-and-multiply schemes.

2) The output high time is modulated by the phase modulation accumulated over the delay duration and the output period is only modulated slightly by the instantaneous input phase shifts so the effect is to modulate the duty cycle. Due to the sampling of the I.F. input the modulation will really be quantised so the width of the modulation box should be read as a probability of a whole cycle shift in edge position rather than as a phase shift but the effect is the same when averaged over many cycles.

By converting the modulation from a phase shift to a duty cycle all that is then needed to recover the original baseband signal is to smooth the discriminator output to remove the 900 kHz sampling, leaving an analog signal proportional to the original frequency deviation and to the delay length. The low-pass filter in ACE9030 is first order and has its – 3 dB point at approximately 70 to 80 kHz to significantly reduce the clock level; the audio bandpass filter then further reduces this level to give a cleaner audio output to drive the ACE9040 where it is again filtered.

The demodulation gain can be determined by considering the effects of a 1 kHz frequency offset on the input signal, and using I.F. = 450 kHz and Delay = 2·742 cycles and V_{DD} = 3·75 V in the example:

A 1 kHz frequency offset will give a phase change in the I.F. signal, during each cycle, of 2π x (1 kHz / I.F.) radians or as a fraction of a cycle, (1 kHz / I.F.) which in this example is 1/450 of a cycle.

If the discriminator delay is measured in I.F. cycles the change in output pulse width for each of the two output pulses is: (Delay in cycles) x (phase change per cycle) = Delay x (1 kHz / I.F.) in I.F. periods, which in this example is 2·742 x 1/450 periods of 450 kHz, or 13·5 ns.

Output pulses occur at a rate of 2 x I.F., so the change in output pulse width measured in output periods is 2 x (change measured in I.F. periods), giving 2 x Delay x 1 kHz / I.F. The duty cycle is defined as pulse width / period so the result is also the change in duty cycle. For this example the change is 0·012.

The output is a logic signal so its amplitude is V_{DD} for all settings and for all modulation, thus the final effect of a 1 kHz offset is an output change of 2 x Delay x 1 kHz x V_{DD} / I.F. and

D_7, D_6	D	M	Delay as I.F. cycles	I.F. kHz	Absolute Gain In µV/Hz, V_{DD} = 3·75 V.	Absolute Gain In µV/Hz, V_{DD} = 4·85 V.	Relative Gain
0, 0	2	39	2·742	450	45·7	59·1	1·8 dB
0, 0	2	39	2·363	450	39·4	50·9	0·5 dB
1, 0	3	40	4·266	455	70·3	90·9	5·6 dB
1, 0	3	40	3·677	455	60·6	78·4	4·3 dB
0, 1	3	37	3·252	450	54·2	70·1	3·3 dB
1, 1	2	38	2·251	455	37·1	48·0	0 dB

Table 5

the example gives 0·045 V.

Removing the arbitrary 1 kHz, the gain at the exclusive-OR gate is given by:

Gain = 2 x Delay in I.F. cycles x V_{DD} / I.F.
with the units of volts per Hertz of deviation.

To be strict, the pulse width is reduced for a positive deviation, so the gain is negative, but this may be ignored as the audio polarity is not of any relevance and also is inverted several times before driving the earpiece.

Using the delay lengths from table 3 the range of gains (at the exclusive-OR gate) can be listed and then compared with the lowest as shown in table 5.

This shows a gain range of 5·6 dB which must be allowed for in the later stages, but also gives absolute gains which show the discriminator could cause saturation in the following stage if a high deviation signal is received. For example speech can be set to 8 kHz deviation so the maximum voltage (with V_{DD} at 3·75 V) is 70·3 x 8000 µV = 562 mV peak. With ST and SAT the total deviation can become 14·5 kHz, potentially giving 1·019 V peak signal, or over 2 V peak-to-peak and leading to possible saturation. There is also the full V_{DD} switching waveform to handle. Other supply levels will simply scale the signals and not change the saturation problem. A 6 dB attenuator is included in the low pass filter that follows the discriminator output driver to avoid any possibility of saturation in the audio reconstruction filter. This attenuator is a simple 2:1 potential divider so will also halve the D.C. level of the signal.

A further effect to be considered is the D.C. offset that results from using delays that are not ideal multiples of cycles of the AFCIN frequency. It can be seen from the Timing Diagram, figure 19, that when the delay is exactly an odd number of quarter cycles each half cycle at one end of the delay will symmetrically straddle an edge the other end of the delay so an unmodulated input will give an output with a 1:1 mark:space ratio; this corresponds to a mid-supply level at the attenuator input, see figure 20. The attenuator output will then be centred at $V_{DD}/4$, so the nominal D.C. gain, 2 x, of the bandpass filter will give the AUDIO output centred at mid-supply.

When a mode is selected with an odd number of thirds of a cycle the output mark:space ratio is offset, and approximating 2·363 as $^7/_3$ or 3·677 as $^{11}/_3$ the effect can be seen in figure 21.

The signal will now be centred on a level at $^2/_3$ or $^1/_3$ of supply, at the attenuator input (giving $^1/_3$ or $^1/_6$ x V_{DD} at its output) and by adjusting the D.C. gain of the bandpass filter it is possible to set the AUDIO to a mid-supply centre if required.

The components used in the bandpass filter feedback circuit should be chosen to both set the pass band frequencies (for example 50 Hz to 30 kHz) and also to set the A.C. and D.C. gains to complement the discriminator's gain and D.C. offset. Typcal A.C. gain at mid-band is around 20 dB. This filter is not of high enough order to remove all out of band noise without distorting the speech channel so to get the final band limited signal precision high order filters such as in the ACE9040 are required.

The ACE9030 is specified with the following component values (see fig 18):

R1 = 47kΩ
R2 = 100kΩ
R3 = 33kΩ
C1 = 82pF
C2 = 100nF

These values are compatible with AMPS using a 14.85MHz reference crystal and 450kHz IF. Resistors R2 and R3 determine the dc gain and can be used to compensate for the dc offset of the demodulated output. Resistors R2 and R3, R1 determine the mid band ac gain of the band pass filter.

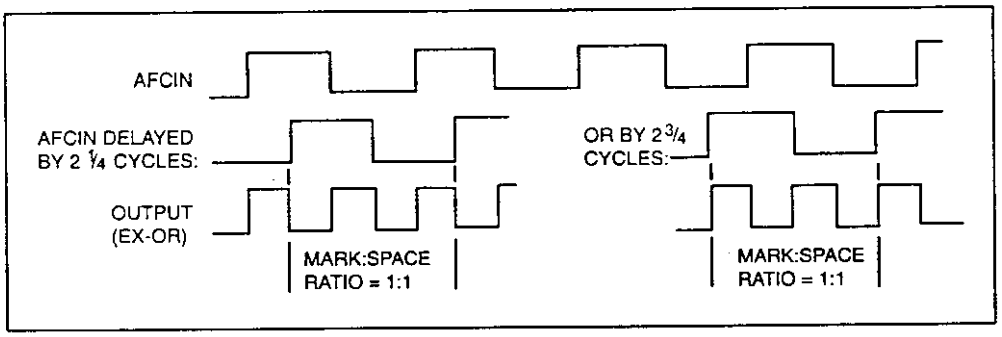


Fig. 20 Demodulation With Odd Number Of Quarter Cycles

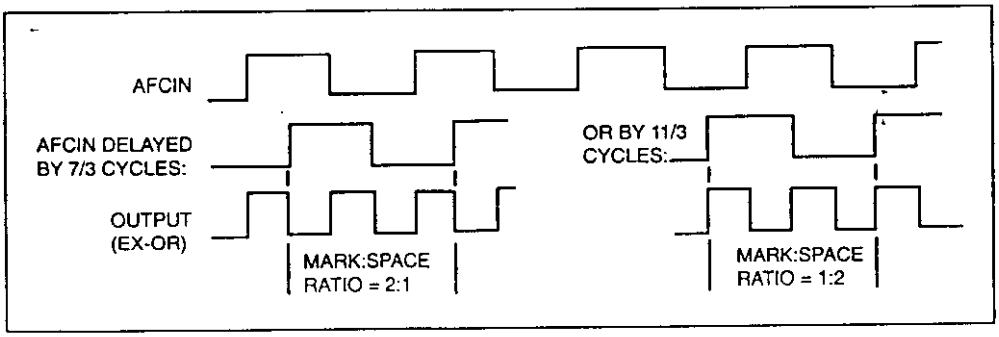


Fig. 21 Demodulation With Odd Thirds Of A Cycle

FUNCTIONAL DESCRIPTION - BLOCKS IN THE SYNTHESISERS

There are two synthesisers in the ACE9030 for use by the radio system, a Main loop to set the first local oscillator to the frequency needed for the channel to be received and an Auxiliary loop to generate an offset frequency to be mixed with the Main output to give the transmit frequency. The modulation is added to the Auxiliary loop by pulling the VCO tank circuit and is then mixed onto the final carrier frequency. In a typical cellular terminal the first Intermediate Frequency is 45 MHz so the Main synthesiser will be set 45 MHz above the receive channel frequency. Many cellular systems operating around 900 MHz use a 45 MHz transmit-receive offset, with the mobile transmit channel below the receive channel frequency so the Auxiliary synthesiser will be set to a fixed frequency of 90 MHz.

Loop dynamics needed for the Main synthesiser are set by the re-tuning time during hand-off and to help simplify the off-chip loop filter components there are Fractional-N and Speed-up modes available for this synthsiser, primarily for use in ETACS terminals. The Auxiliary loop does not change frequency so the only constraints are power-up time and microphonics, so a simple synthesiser is used.

The two loops share a common reference divider to save power and also to control the relative phase of the two sets of charge pumps.

As described in the section FUNCTIONAL DESCRIPTION - CONTROL BUS there is often benefit in holding LATCHC at a high level to minimise bus clock interference to the synthesiser loops. The dummy word in figure 11 is the preferred technique to set LATCHC to high for normal operation.

At power-on, the reset generator in the Radio Interface section is used to initialise both synthesisers to their power down state. In this state they can be programmed with required numbers to be ready for power-on when the whole terminal has fully initialised.

Reference Divider

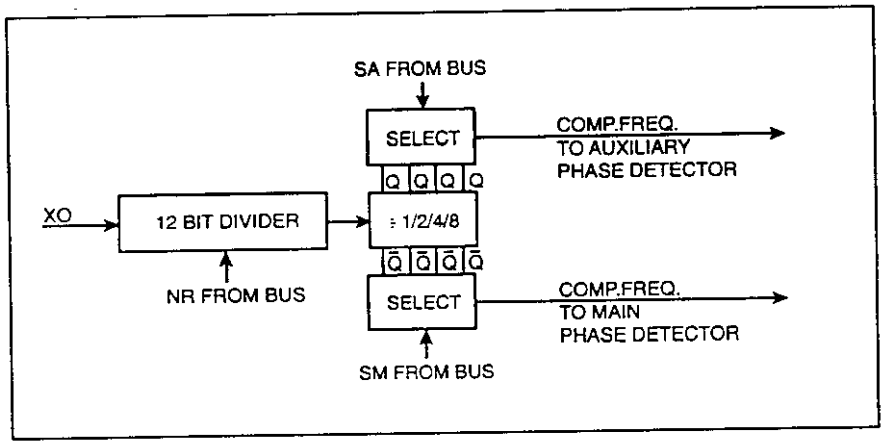


Fig. 22 Reference Divider

A common reference divider is used for the two synthesisers, but to allow some difference in comparison frequencies the final four stage output selectors are repeated for each synthesiser as shown in figure 22. To reduce interaction between the two synthesisers the divider outputs are arranged in antiphase so that loop correction charge pump pulses occur alternately in each loop. This phase separation also reduces the peak current in the charge pump power supply and can reduce interference to other sections of the mobile terminal.

The input clock to the reference divider is the internal signal XO from the crystal oscillator. The two outputs drive the Auxiliary and the Main phase detectors directly.

A standby mode is available for the reference divider and is enabled whenever both synthesisers are in standby.

The programming numbers are all loaded from the serial bus in Word D, NR directly sets the ratio of the 12 bit divider but SA and SM select the final divisions as in the following tables:

SA bit 1	SA bit 0	Auxiliary Tap
0	0	+1
0	1	+4
1	0	+2
1	1	+8

SM bit 1	SM bit 0	Main Tap
0	0	+1
0	1	+4
1	0	+2
1	1	+8

The minimum allowed value of NR is set by the need to generate some small time windows around the comparison edges for Lock Detect logic and for Fractional-N compensation so a value of at least 8 is required. The maximum NR is 4095 as normal for a 12 bit counter and this is then increased by a factor of 1, 2, 4, or 8 in the final divider. A typical required reference division is +512 so neither of these limits should constrain the system design.

Auxiliary Synthesiser

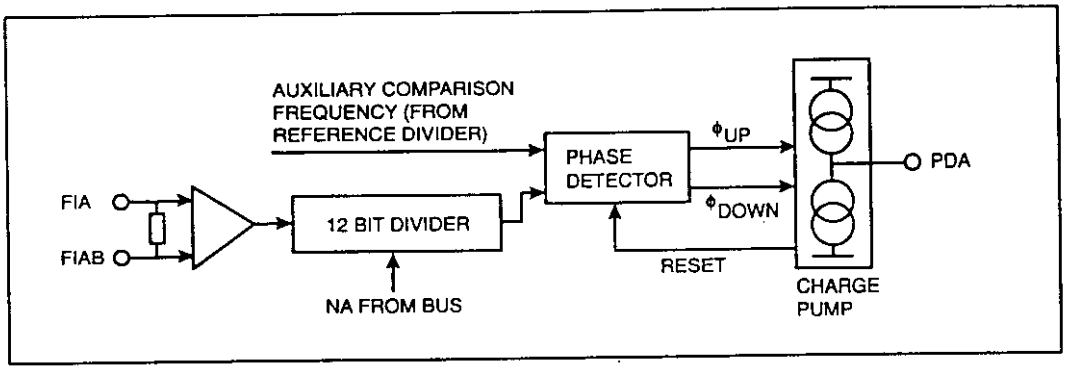


Fig. 23 Auxiliary Synthesiser

The Auxiliary Synthesiser operates with an input frequency up to 135 MHz. The input buffer will amplify and limit a small amplitude sinewave signal and so can be driven from the ACE9020 VCO directly. There are three main blocks in this synthesiser: a 12-bit programm-able divider, a digital phase detector, and output charge pumps to drive a passive loop filter.

To assist fast recovery from power-down the inputs FIA and FIAB are designed to be d.c. driven by the TXOSC+ and TXOSC– outputs from ACE9020.

FIA can also be used single-ended if it is driven by a signal with double amplitude, the correct d.c. level and if FIAB is decoupled to ground by a capacitor (see Electrical Characteristics for full details). Internal biasing will set the d.c. level on FIAB.

The 12 bit programmable divider is set by the NA bits in Word C and ratios from 3 to 4095 can be used. This drives the phase detector along with the comparison frequency signal from the common reference divider.

A digital phase detector is used and is designed to eliminate any deadband around the locked state, this is especially important when modulation is added.

The phase detector drives switched current sources to pump charge onto an external passive loop filter which is primarily an integrator, resulting in the minimum of external components. The charge pump output current level is set by the external resistor on pin RSMA and the ratio is fixed so that nominal $I_{AUX} = 8 \times I_{RSMA}$. This bias resistor also sets the main synthesiser output current but that current has a programmable ratio to enable different currents for each loop. The pin RSMA does not need any decoupling and to avoid all possibilities of oscillation the external capacitance should be less than 5 pF.

The polarity of the output is such that a more positive voltage on the loop filter (PDA pin) sets a higher VCO frequency.

A standby mode for the auxiliary synthesiser can be selected if bit DA in Word D is HIGH.

This synthesiser is used to add modulation to the transmitted signal. The most convenient approach, as shown in figure 31, is to drive the positive end of the varactor diode in the tank circuit with the loop filter to set the frequency and then to drive the negative end with the modulation from a summing circuit (speech plus SAT plus data or ST) from ACE9040.

Main Synthesiser

The main synthesiser in the ACE9030 is designed to operate with a two-modulus prescaler and will accept frequencies up to 30 MHz. To assist fast recovery from power-down the inputs FIM and FIMB are designed to be d.c. driven by the DIV_OUT+ and DIV_OUT– outputs from the ACE9020 or similar outputs from standard prescalers.

FIM can also be used single-ended if it is driven by a signal with double amplitude, the correct d.c. level and if FIMB is decoupled to ground by a capacitor (see Electrical Characteristics for full details). Internal biasing will set the d.c. level on FIMB.

The block diagram depends on which mode is selected but is basically the same as the Auxiliary synthesiser with added features for each mode. The common element is the phase detector, which is the same circuit used in the Auxiliary synthesiser and again drives switched current sources to pump charge into an external passive loop filter to minimise the external components. The charge pump output current level is set by the external resistor on pin RSMA and the multiplying ratio is programmable by the bus and the chosen mode as in table 6. This bias resistor also sets the Auxiliary synthesiser output current as described above.

A standby mode for the main synthesiser can be selected if bit DM in Word D is HIGH.

The Main synthesiser can be used in different modes depending on the requirements of the communication system it is operating in:

Normal mode

The most straightforward to use and adequate for most analogue cellular telephone systems.

Normal Mode with Speed-up

This adds a fast slew drive to the loop filter during channel changes so that the time from channel to channel is significantly reduced but once the change is expected to be complete the loop reverts to normal mode. A little care is needed in parameter choice and loop filter design to ensure the loop is stable in both modes and there is likely to be a higher level of comparison sidebands during speed-up mode. This combination offers a faster channel change or a lower level of comparison frequency sidebands once on channel, or with care some of each advantage.

Fractional-N mode

When selected this mode is permanently active and by interpolating channels between comparison frequency steps allows a higher comparison frequency to give both a faster channel change time and a lower comparison sideband level. The higher comparison frequency also allows a higher loop bandwidth which can reduce phase noise in the locked system. It is not difficult to get the Fractional-N loop compensation correct to minimise sidebands at the fractional frequency as the ACE9030 fractions are only $^1/_5$'s or $^1/_8$'s. For further details see the later section "Detailed Operation of Fractional-N Mode".

Fractional-N Mode with Speed-up

This gives the ultimate loop performance from the ACE9030 but care is needed when designing the loop filter and when choosing the values of the control parameters.

Main Synthesiser - Normal Mode

In Normal mode the Main synthesiser is similar to the Auxiliary synthesiser with the addition of control for an external prescaler, see figure 24.

The 12-bit counter first counts down for N1 cycles, with MODMP set HIGH, then counts up for N2 cycles, with MODMP set LOW, and finally gives an output pulse (every N1 + N2 cycles) to the phase comparator and repeats the whole sequence. The use of an up/down counter allows the control of a two modulus prescaler without needing a separate counter for that purpose. To give time for the function sequencing a minimum limit of 3 is put on N1 and a programmed value of 0 for N2 will be treated as 256 and so is not normally used. Choices of values for N1 and N2 are described in the later sections "Two Modulus Prescaler Control" and "Programming Example for Both Synthesisers".

The phase detector operates with the same arrangement of overlapping up and down pulses as the Auxiliary phase detector to again avoid any dead band, the charge pump current is also set by the same resistor on pin RSMA but for the Main charge pumps the current is also controlled by the bus. In the bias circuit the current I_{RSMA} through the external resistor on pin RSMA is divided by 32 to give a reference current Ibo ($Ibo = I_{RSMA} \times {}^1/_{32}$) and this current is then multiplied by the value CN from the control bus to give the normal charge pump current Iprop(0). The pin RSMA again does not need any decoupling and to avoid all possibilities of oscillation the external capacitance should be less than 5 pF.

CN can be changed for different channels, to track the division ratio set by N1 and N2, to maintain the same PLL loop gain over the operating band but in most cellular systems the total band is narrow compared to the frequencies and a fixed CN is adequate. Other synthesiser control parameters do not need changing and could be loaded at power-on and then left unaltered.

Main Synthesiser - Normal Mode withSpeed-up

During Speed-up the drive to the loop filter is increased to change channels faster. There will be a slight degradation of sideband performance during the change but this does not affect the final system performance. Speed-up lasts for the duration of the LATCHC pulse that loads an A or A2 word from the bus and as soon as the pulse ends the currents return to normal to give clean synthesis. The normal charge pump current is increased by a factor (2^{L+1}) to give 2, 4, 8, or 16 times Iprop(0), as defined in Normal Mode, and is then referred to as Iprop(1), as in figure 26. A second charge pump is enabled to drive the capacitor Ci in the loop filter directly, and as this is always larger than capacitor Cp this extra output is set to Iprop(1) x K. The factors L and K are used to control speed-up and are loaded at power-up and can be left at fixed values.

Speed-up is always enabled by LATCHC when an A or A2 word is loaded. When speed-up is not required the LATCHC pulse should be short and the parameters L and K set to their minimum to give an insignificant effect.

Main Synthesiser - Fractional-N Mode

Fractional-N mode is the same as Normal mode with the addition of the Fractional-N system, shown in figure 25.

In Fractional-N mode the modulus of the prescaler is changed in a cyclic manner to interpolate channels between the comparison frequency steps. Depending on the state of the FMOD bit loaded in Word D the pattern can be 5 (FMOD = 0) or 8 (FMOD = 1) cycles long, giving the choice of $^1/_5$'s or $^1/_8$'s of the comparison frequency and the fractional numerator is set by NF in Word A or A2. The accumulator repeatedly adds NF to its own value and generates an overflow whenever this value exceeds the count modulo number. This overflow output to the Modulus Control logic will force one cycle to change from MODMP HIGH to MODMP LOW to in turn set the prescaler to the higher ratio for one cycle

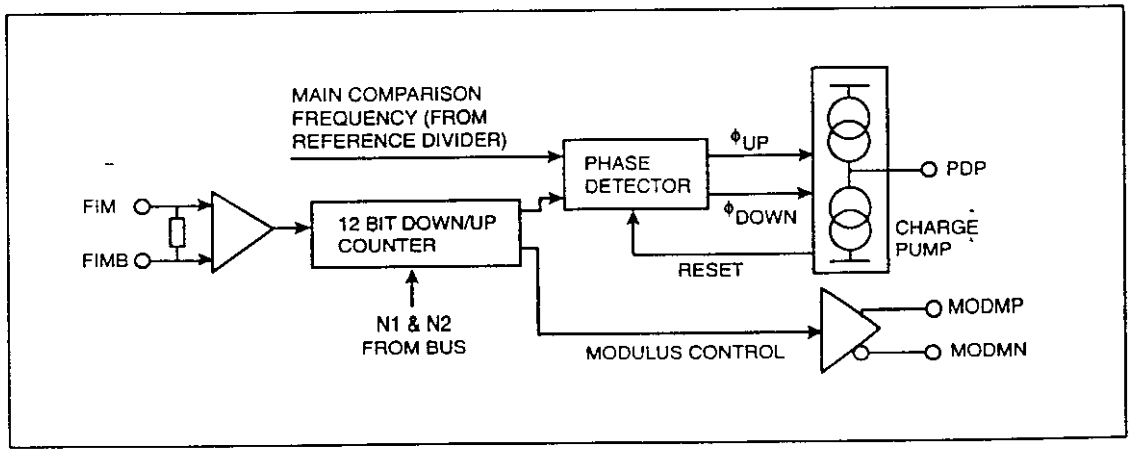


Fig. 24 Main Synthesiser - Normal Mode

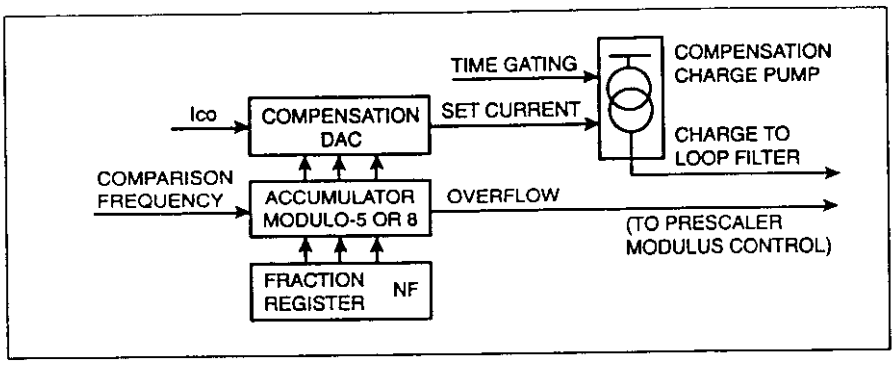


Fig. 25 Fractional-N Add-On To Main Synthesiser

and so increment the total division.

To avoid loop modulation due to the accumulating phase shift at the fractional frequency, a compensation charge must also be driven onto the loop filter to track the accumulated phase error so a current Icomp(0) is output on PDP for a fixed short duration. Icomp(0) is given by Icomp(0) = ACC x Ico, where ACC is the value of the phase accumulator and Ico is a current set by a resistor on pin RSC such that Ico = I_{RSC}/320. In a typical system the required value of Ico is between $^1/_{10}$ and $^1/_3$ of Ibo and thus the resistor on RSMA has a value between one and three times the value of the resistor on RSC. As with RSMA, the pin RSC does not need any decoupling and to avoid all possibilities of oscillation the external capacitance should be less than 5 pF. For a full description of this mode see the later section "Detailed Operation of Fractional-N Mode".

In fractional-N mode a zero fraction numerator, in both $^1/_5$'s and $^1/_8$'s mode, will force the accumulator to zero and not simply leave it at an arbitrary fixed value. This feature makes testing easier by setting the accumulator to a known state, but is also useful in operation by stopping all compensation pulses when none are needed. Similarly in $^1/_8$'s mode if $^1/_4$ (and $^3/_4$) or $^1/_2$ fractions are set then the LSB or two LSB's in the accumulator will be forced to zero to relax the tolerance on the compensation.

Main Synthesiser - Fractional-N Mode with Speed-up

In Fractional-N mode with Speed-up the normal compensation current is increased by the same factor (2^{+1}) as the main charge pump current to give Icomp(1), and at the same time the integrating capacitor is also driven with a compensating charge by a current Icomp(2) set to Icomp(1) x K. This extra compensation is included so that the loop will step to exactly the desired frequency during the Speed-up phase and then be on channel when normal Fractional-N begins.

Main Synthesiser Charge Pumps

The charge pumps for all modes are shown together in figure 26. The charge pumps on pin PDP are used normally to hold a channel and are also used in speed-up modes at a

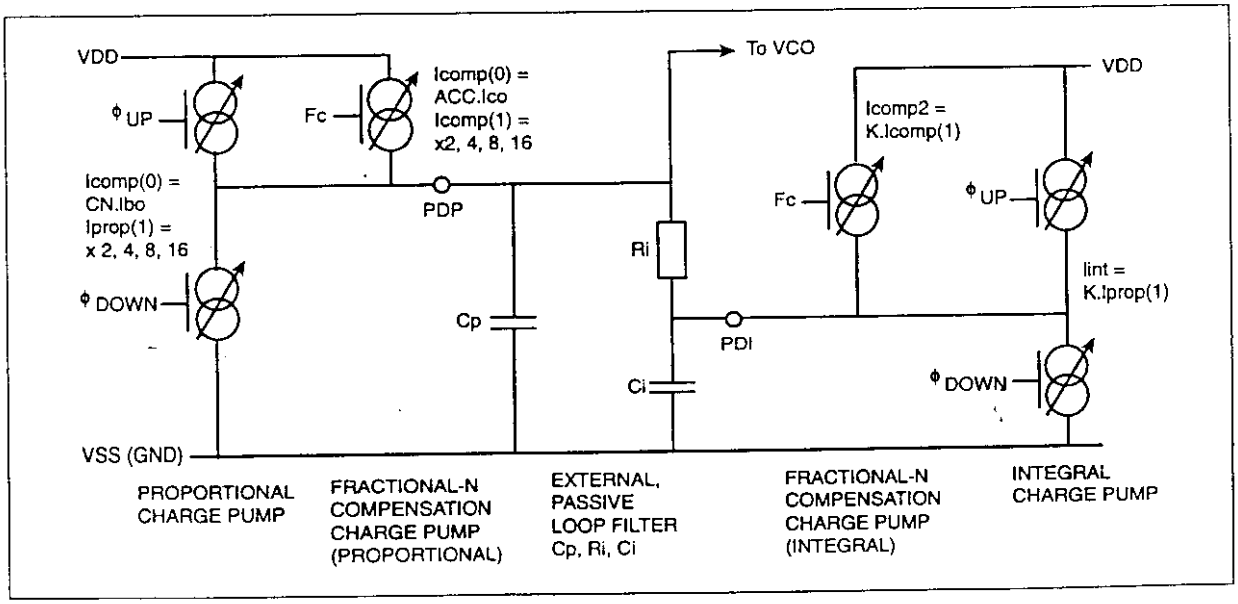


Fig. 26 Main Synthesiser Charge Pumps

larger current. The charge pumps on PDI are only used in speed-up and then drive the integrating capacitor Ci directly. The control signals $\emptyset_{UP}$ and $\emptyset_{DOWN}$ are the error signals from the phase detector and have a duration proportional to the phase error, the signal Fc is the Fractional-N compensation gating pulse and has a fixed duration set by the crystal oscillator.

Nominal Charge Pump Currents

Shown in table 5, charge pump currents are set by the resistors RSMA and RSC and by scaling coefficients loaded from the serial bus. CN is an 8 bit number, L is 2 bit and K is 4 bit. Fractional-N compensation also depends on the instantaneous value ACC in the fractional accumulator, a 3 bit number.

Pin	Charge pump	Normal	Speed-up	Maximum setting*
PDP	Main	$I_{prop}(0) = CN \times I_{RSMA}/32$	$I_{prop}(1) = 2^{L+1} \times I_{prop}(0)$	1·0 mA
PDI	Main	Off	$I_{int} = K \times I_{prop}(1)$	5 mA
PDP	Fractional-N	$I_{comp}(0) = ACC \times I_{RSC}/320$	$I_{comp}(1) = 2^{L+1} \times I_{comp}(0)$	12 µA
PDI	Fractional-N	Off	$I_{comp}(2) = K \times I_{comp}(1)$	180 µA
PDA	Auxiliary	$I_{auxil} = 8 \times I_{RSMA}$	no auxiliary speed-up	512 µA

* Larger values of current can be set by the programming numbers and the resistor values, but the circuit is not then guaranteed to give the calculated current.

Table 5

Two Modulus Prescaler Control

The Main ACE9030 synthesiser is designed to operate with the two-modulus prescaler section of the ACE9020. This allows channels to be spaced at the comparison frequency while keeping the clock rates within the range possible in CMOS. ACE9030 can also be used with standard two-modulus prescalers such as SP8715.

The prescaler will have two division ratios, R1 and R2, selected by a Modulus Control signal and designed to switch quickly from one ratio to the other so that a sequence of R1 and R2 can be used to give the required total division. It is usual to have R2 = R1 + 1 and to select R1 by setting Modulus Control to the HIGH state and R2 by a LOW state.

To reduce interference the Modulus Control output from ACE9030 is a pair of differential signals MODMP and MODMN each with a limited voltage swing but still able to drive selected standard prescalers from GEC-Plessey Semiconductors if MODMP is used alone. Even if a prescaler with non-differential control input is used there could still be some benefit in running a MODMN track on the circuit board beside the MODMP track to partly cancel capacitive coupling to sensitive nodes. Simplified waveforms are shown in figure 27.

Unlike many conventional synthesisers that use two separate counters, to give both the total count, M, and the portion for which the prescaler is at its higher ratio, A, there is only one counter in the ACE9030 for both these functions. This counter is loaded with the value N1, counts down to zero, changes direction, counts up to N2, is again loaded with the value N1 and changes direction to down, and so the cycle is repeated indefinitely.

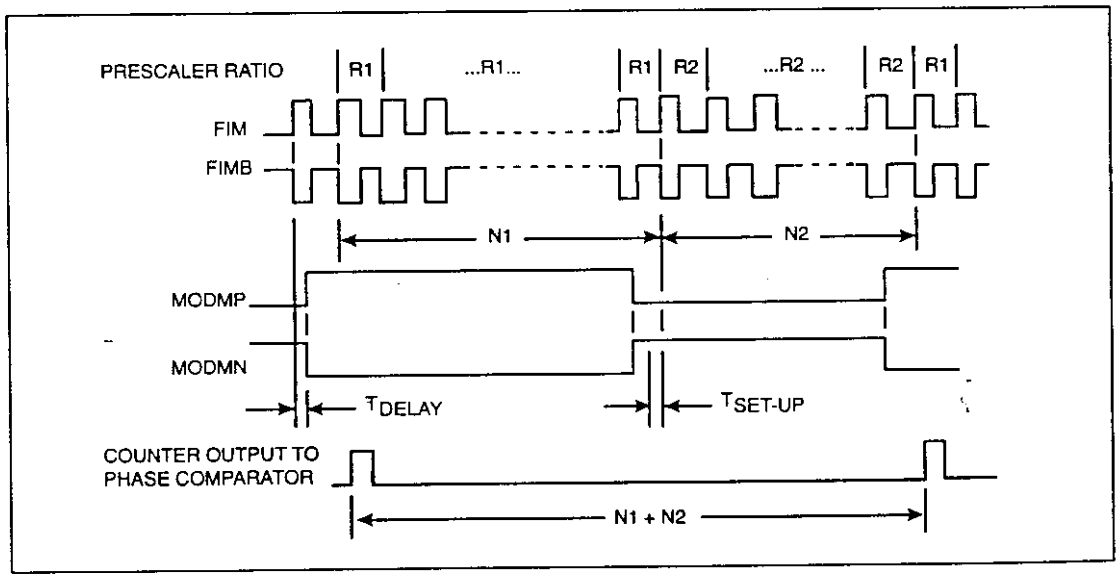


Fig. 27 Modulus Control Timing Diagram

An output to drive the phase comparator is generated from the N1 load signal at the start of each cycle, giving a pulse every (N1 + N2) counts and to help minimise phase noise in the complete synthesiser this pulse is re-timed to be closely synchronised to the FIM/FIMB input. During the N1 down count the modulus control MODMP is held HIGH to select prescaler ratio R1 and during the N2 up count it is LOW to select R2, so the total count from the VCO to comparison frequency is given by:

$$N_{TOT} = N1 \times R1 + N2 \times R2$$

but $R2 = R1 + 1$

so $N_{TOT} = (N1 + N2) \times R1 + N2$

It can be seen from this equation that to increase the total division by one (to give the next higher channel in many systems) the value of N2 must be increased by one but also that N1 must be decreased by one to keep the term (N1 + N2) constant. It is normal to keep the value of N2 in the range 1 to R1 by subtracting R1 whenever the channel incrementing allows this (i.e. if N2 > R1) and to then add one to N1. These calculations are different from those for many other synthesisers but are not difficult.

The 12-bit up/down counter has a maximum value for N1 of 4095 and to give time for the function sequencing a minimum limit of 3 is put on N1. There is no need for such large values for N2 so its range is limited by the programming logic to 8 bit numbers, 0 to 255 and to simplify the logic a set value of 0 will give a count of 256. If a value of 0 for N2 is wanted then N2 should be set instead to R1 and the value of N1 reduced by (R1 + 1), also equal to R2.

To ensure consistent operation some care is needed in the choice of prescaler so that the modulus control loop has adequate time for all of its propagation delays. In the synthesiser there is propogation delay T_{DELAY} from the FIM/FIMB input to the MODMP/MODMN output and in the prescaler there will be a minimum time T_{SET-UP} from the change in MODMP/MODMN to the next output edge on FIM/FIMB, as shown in figure 27. For predictable operation the sum $T_{DELAY} + T_{SET-UP}$ must be less than the period of FIM/FIMB or otherwise, if the rising and falling edges of MODMP/N are delayed differently, the prescaler might give the wrong balance of R1 and R2. This will often set a lower limit on the frequency of FIM than that set by the ability of the counter to clock at the FIM rate. For 900 MHz cellular telephones the use of a ÷ 64/65 prescaler normally ensures safe timing.

Fractional-N mode operates by forcing the MODMP/MODMN outputs to the R2 state for the last count of the N1 period whenever the Fractional-N accumulator overflows, effectively adding one to N2 and subtracting one from N1, and so increases the total division ratio by one for each overflow. The effect of this is to increase the average division ratio by the required fraction.

PROGRAMMING EXAMPLE FOR BOTH SYNTHESISERS

To illustrate the choice of programming numbers consider the ETACS system as now used in the UK.

This began as TACS with 600 channels (numbered 1 to 600) from 890 to 905 MHz (mobile transmit) with the provision to expand by 400 channels (601 to 1000) from 905 to 915 MHz. This additional spectrum was given over to GSM use before TACS needed expanding, so TACS was later extended by 720 extra channels from 872 to 890 MHz, to form ETACS and leaving a somewhat odd channel numbering system. The channel numbers are stored as 11-bit binary numbers and are listed here as both negative numbers to follow on downwards from channel 1 and also as large positive numbers as these are the preferred names. These two numbering schemes are really the same, as the MSB of a binary number can be interpreted as either a sign bit (2's complement giving the negative values) or as the bit with the highest weight (1024 for an 11 bit number, giving the large positive values).

Each channel is 25 kHz wide but as the channel edges are put onto the whole 25 kHz steps the centre frequencies all have an odd 12·5 kHz. This is not ideal for the synthesiser but does give the maximum number of channels in the allocated band.

The mobile receive channels are a fixed 45 MHz above the corresponding transmit frequency, as is the case with most cellular systems. In the ACE9030 the intention is to use the main synthesiser to generate the receiver local oscillator at the first I.F. above the mobile receive carrier, and to then mix the auxiliary synthesiser frequency with this to produce the transmit frequency. A typical I.F. is 45 MHz, leading to an auxiliary frequency of 90 MHz and a crystal of 14·85 MHz with a tripler for the second local oscillator, and a final I.F. of 450 kHz.

The channel numbers and corresponding frequencies are shown in table 6.

CHANNEL NUMBER	MOBILE TRANSMIT FREQUENCY (MHz)	MOBILE RECEIVE FREQUENCY (MHz)	MAIN VCO (MHz)
1329 or –719	872·0125	917·0125	962·0125
...	...	...	...
2047 or –1	889·9625	934·9625	979·9625
0	889·9875	934·9875	979·9875
1	890·0125	935·0125	980·0125
2	890·0375	935·0375	980·0375
3	890·0625	935·0625	980·0625
...	...	...	...
600	904·9875	949·9875	994·9875

Table 6

The reference divider needs to produce the main comparison frequency of 12·5 kHz from the crystal at 14·85 MHz, a ratio of 1188, which can be formed by a NR of 1188 followed by a SM select giving ÷1, or 594 followed by ÷2, or by 297 and ÷4. The auxiliary divider must divide 90 MHz down to the auxiliary comparison frequency, which is related to the main comparison frequency but can usefully be larger. Using 12·5 kHz needs a ratio of 7200 which is too large a value for NA, 25 kHz needs 3600 and could be used, but 50 kHz and a ratio of 1800 helps to minimise loop filter size. With this choice the values to be set are:

NR = 297, to give 50 kHz into SA, SM selector.
SA = 00, to give ÷1, and leave 50 kHz for auxiliary comparison frequency.
SM = 01, to give ÷4, and hence 12·5 kHz for main compari son frequency.
NA = 1800, to give 90 MHz.

In this example Fractional-N operation is not chosen, but if it is required then SM should be set to 00 to give 50 kHz comparison frequency in both synthesisers and then fractions of $^1/_4$ or $^3/_4$ used by setting NF = 2 or 6, with FMOD set to 1 to give $^1/_8$'s. The values of N1 and N2 can then be found by following a procedure similar to the following.

For the main synthesiser, starting at channel 1, to divide 980·0125 MHz down to 12·5 kHz is a total ratio of 78401 and this will be split between the prescaler and the ACE9030 programmable divider. A ÷64/65 prescaler is most common, and will be in ÷64 mode as its normal state, so the 78401 can be split into a ÷64 followed by ÷1225 with a remainder of 1. The remainder is achieved by setting the prescaler to ÷65 for 1 cycle, so using R1 = 64, and R2 = 65 the programmable values can be:

$$N2 = 1, \text{ and } (N1 + N2) = 1225, \text{ thus } N1 = 1224$$

These values are suitable for use but are not the only possible set - if desired N2 can be increased to 65 if N1 is reduced to 1160. The actual choice in practice is set by whichever gives the more convenient mathematics in the system controller, the only limits are the basic equation: $N_{TOT} = (N1 + N2) \times R1 + N2$, which must be met for all channels and the fact that a set value of 0 for N2 will actually give a count of 256 so for easy calculations N2 ≠ 0 (in practice for a TACS system not using Fractional-N all N2 values are odd numbers so 0 is never needed).

Other channels can easily be added, without forgetting that each channel is two comparison steps (2 x 12·5 kHz) above the next lower, so for channels 1 to 32,

$$N2 = 2 \times \text{Channel Number} - 1, \text{ and } N1 = 1225 - N2$$

and for channels 33 to 64,

$$N2 = 2 \times (\text{Channel Number} - 32) - 1, \text{ and } N1 = 1226 - N2$$

Rather than having several sets of separate equations for each group of channels it is possible to combine them all into one set by adding two variables to split the channel number into a modulo-32 and a remainder number. Let C32 = int((Channel Number − 1) ÷ 32), where "int(x)" means the integer part of (x), and let CN2 = Channel Number − (32 x C32), then:

$$N2 = (2 \times CN2) - 1, \text{ and } N1 = 1225 - N2 + C32$$

These are clearly valid for channels 1 to 600 (the original TACS channels) but to cover the extra channels for ETACS the negative numbers need more processing to avoid negative N2 values. The simplest answer is to add an offset to the channel number and then subtract an equivalent value from the N1 equation. As the channels are in blocks of 32 for the calculations it is helpful to choose a multiple of 32 for the offset, and the most negative channel is −719 so the lowest suitable offset value is 736 (that is 23 x 32). This gives the following steps for all TACS/ETACS channels:

CNOFF = Channel Number + 736
CB32 = int((CNOFF − 1) ÷ 32)
CN2 = CNOFF − (32 x CB32)
N2 = (2 x CN2) − 1
N1 = 1202 − N2 + CB32

These operations are given in easy to understand stages but in a real system it could be more efficient to combine or rearrange some steps. If a high level language is used then integer and remainder functions might be available and could save a little programming time, whereas if low level or assembler language is used an integer function will need to be built, in this case by a 5 bit right shift to both divide by 32 and to lose the fraction.

It might be noticed that avoiding N2 = 0 was very easy as all values of N2 in this system are odd numbers, due to the 12·5 kHz offset from band edges. Other systems do not have this offset so a little care is needed in choosing constants in the corresponding equations.

DETAILED OPERATION OF FRACTIONAL-N MODE

Without using the Fractional-N mode the loop will lock the VCO frequency, f_{VCO} to the comparison frequency, f_{COMP} at a multiple set by the total division ratio N_{TOT}, where:

$$N_{TOT} = (N1 + N2) \times R1 + N2$$

giving:

$$f_{VCO} = f_{COMP} \times N_{TOT}$$

From these equations it can be seen that if N_{TOT} is an integer the minimum frequency step is f_{COMP}. It is not possible to make a non-integer divider but by alternating the ratio between N_{TOT} and $N_{TOT} + 1$ in a suitable pattern the effect of a fractional increase in N_{TOT} can be achieved. This is called Fractional-N operation.

The control of the pattern of N_{TOT} and $N_{TOT} + 1$ cycles is by an accumulator set to count with a modulus equal to the fractional denominator and which adds the numerator of the fraction every comparison cycle. When the accumulator overflows by its value exceeding the value of the denominator the total division ratio is increased for one cycle. In ACE9030 the choice of denominator is 5 or 8 and is set by the FMOD bit in Word D, the numerator is set by the three NF bits in Word A or A2 and the increase in total division from N_{TOT} to $N_{TOT} + 1$ is done by changing the modulus control signal to the prescaler so that an R1 cycle becomes an R1 + 1 cycle.

As an example of the operation of the accumulator consider FMOD set HIGH to give modulo-8 counting and NF set to 011 to give a $^3/_8$ fraction and the accumulator starting at any arbitrary value as shown in table 7.

From this table it can be seen that the pattern repeats every 8 cycles and that the ratio is incremented for 3 of each 8, giving the desired $N_{TOT} + ^3/_8$. It can be shown that the pattern always repeats every 8 cycles, or whatever modulus is chosen for all fractions and that the number of $N_{TOT} + 1$ cycles is always the fractional numerator.

By spreading the ($N_{TOT} + 1$) counts throughout the pattern rather than having them as a continuous block the loop is less

Increment (= NF)	Accumulator value		Division Ratio
	...previous values		
3	5		N_{TOT}
3	0	& overflows	$N_{TOT} + 1$
3	3		N_{TOT}
3	6		N_{TOT}
3	1	& overflows	$N_{TOT} + 1$
3	4		N_{TOT}
3	7		N_{TOT}
3	2	& overflows	$N_{TOT} + 1$
3	5		N_{TOT}
3	0	& overflows	$N_{TOT} + 1$
	and so on...		

Table 7

disturbed by the variations in division ratio but there is still some frequency modulation given by the Fractional-N operation. The simplest way to remove this ripple on the synthesiser is to use a lower bandwidth loop filter but this also removes all of the advantage of fast channel change when using Fractional-N, so the method used in ACE9030 is to calculate the waveform of the ripple and then inject a compensation signal onto the loop filter.

Fractional-N Compensation

If the Fractional-N system is operating correctly the synthesiser sets the VCO frequency so that:

$$f_{VCO} = f_{COMP} \times (N_{TOT} + F) \quad .... (1)$$

where F is the fraction given by:

$$F = \frac{NF}{MOD}$$

NF is the fraction set in Word A or A2
MOD is the modulus, 5 or 8

The total division alternates between N_{TOT} and $N_{TOT} + 1$ so the frequency seen at the phase comparator will also alternate. This divided signal f_{FRACN} is compared with the uniform comparison frequency f_{COMP} and will give a phase error due to the different periods. There will also be some phase error due to leakage on the loop filter, leading to some correction pulses on the charge pumps to maintain lock, but these will be very small in a well designed synthesiser once the loop is locked, so can be ignored here. For each + (N_{TOT}) cycle:

$$f_{FRANC} = f_{COMP} \times \frac{N_{TOT} + F}{N_{TOT}} = f_{COMP} \times \left(1 + \frac{N_{TOT} + F}{N_{TOT}}\right)$$

and so the phase error increases each cycle by:

$$\frac{F}{N_{TOT}} \times (f_{COMP} \text{ Period}) \quad .... (2)$$

This phase error gives an unwanted correction pulse on the $\emptyset_{DOWN}$ output as the VCO frequency is too high for the division ratio in use. The phase error increases as + N_{TOT} cycles follow each other until eventually the accumulator overflows and causes a + (N_{TOT} + 1) cycle.
For each + (N_{TOT} + 1) cycle:

$$f_{FRANC} = f_{COMP} \times \frac{N_{TOT} + F}{N_{TOT} + 1}$$

and in this case the phase error increases in the opposite direction each cycle by:

$$\frac{(F - 1)}{(N_{TOT} + 1)} \times (f_{COMP} \text{ Period}) \quad .... (3)$$

This phase error gives an unwanted correction pulse on the $\emptyset_{UP}$ output, as the VCO frequency is too low for the division ratio in use.

Any phase can be considered to be the locked condition so to simplify later calculations the phase given by a + (NTOT + 1) cycle which leaves 000 in the accumulator will be chosen as the locked state and compensation will be added to achieve this. Only unwanted $\emptyset_{DOWN}$ outputs then need to be removed by cancellation and also that the total phase error in any cycle, based on formula (2), is given by replacing F, the fraction required, by the current sum of fractions, which is the value of the accumulator ACC divided by the modulus in use. This replacement is clearly valid if the state of the accumulator is considered when starting from a zero value and then adding the fractional count each cycle until an overflow is reached; when starting from a non-zero value there is some residual phase error from the overflow state so the accumulator still gives the correct phase error. Thus the phase error needing correction on the loop filter is:

$$\text{Phase error} = \frac{ACC}{N_{TOT} \times MOD} \times (f_{COMP} \text{ Period}) \quad .... (4)$$

This error could be cancelled by a phase shift on the comparison clock from the reference divider but this is very difficult in practice so the method used in ACE9030 is to add an extra charge pump to the loop filter to directly cancel the pulse given by the normal charge pump due to this phase error. The current given by the proportional charge pump is Iprop(0) in normal mode or Iprop(1) in speed-up mode so taking normal mode first the charge that must be cancelled is:

$$\frac{ACC}{N_{TOT} \times MOD} \times (f_{COMP} \text{ Period}) \times I_{prop}(0) \quad .... (5)$$

This formula could be used as it stands but the circuit can be simplified if it is recalled that Iprop(0) depends on the CN value so that loop dynamics are kept constant over a wide range of frequencies by changing CN in proportion to the total division ratio N_{TOT}. In those systems where CN is held constant the synthesiser is in effect considered to be operating over a narrow frequency band so N_{TOT} can also be considered constant and the following calculations still apply. The value of Iprop(0) is set by a DAC in ACE9030 from the reference current Ibo so that:

$$I_{prop}(0) = CN \times I_{bo} \quad .... (6)$$

and the value of CN tracks N_{TOT} with a scaling factor SF such that:

$$CN = SF \times N_{TOT}$$

putting both of these equations into formula (5) gives the charge to be cancelled as:

$$\text{Charge} = \frac{ACC \times SF}{MOD} \times (f_{COMP} \text{ Period}) \times I_{bo} \quad .... (7)$$

The value of SF can be found from any channel but to get a quick estimate the highest frequency can be considered as there is a fixed upper limit on CN of 256 so:

$$SF = \frac{CN(max)}{N_{TOT}(max)}$$

Putting suggested typical values into equation (7); $N_{TOT}(max) = 10000$, CN(max) = 250, and MOD = 8, and then assuming the current flows for the whole comparison period the current to be multiplied by ACC is Ibo / 320. The typical Ibo is only 1 µA so this is a very small current of around 3 nA and would be too small to control accurately and certainly too small for production testing.

The error signal to be cancelled is a narrow pulse at the comparison frequency so the best cancellation of the whole spectrum of the error is also a narrow pulse. It is not practical to generate a variable width pulse to match the error pulse but a fixed width variable amplitude pulse is possible and it can be timed to approximately coincide with the error pulse to give good cancellation.

The compensation current amplitude is also increased by gating it with a small time window and in ACE9030 the gate is set to two cycles of the reference clock which straddle the active edge of the comparison frequency signal to the phase comparator. The total reference division from reference clock to comparison frequency is the programmable divider set by NR in Word D multiplied by 1, 2, 4, or 8 as selected by the SM bits also in Word D and this total may be called R_{MAIN}, so for the compensation current the scaling is R_{MAIN} / 2.

The charge needed is still as in equation (7) but the current can be defined as:

$$Icomp\ (0) = ACC \times Ico \quad .....(8)$$

where, in ACE9030, the compensation reference current Ico is set by an external resistor RSC such that:

$$Ico = \frac{I_{RSC}}{320}$$

but this Ico must be chosen to cancel the error charge in equation (7), and the scaling effect of 2 reference cycles in R_{MAIN} has been derived above, giving:

$$Ico = \frac{SF}{MOD} \times \frac{R_{MAIN}}{2} \times Ibo$$

then removing SF to help evaluate the values needed:

$$Ico = \frac{CN\ (max)}{MOD \times N_{TOT}(max)} \times \frac{R_{MAIN}}{2} \times Ibo \quad ....(9)$$

this can then be further processed by replacing R_{MAIN} and $N_{TOT}(max)$ by the frequency ratios:

$$R_{MAIN} = \frac{f_{CRYSTAL}}{f_{COMP}} \text{ and } N_{TOT}\ (max) = \frac{f_{VCO}\ (max)}{f_{COMP}}$$

then when substituting these into equation (9) the f_{COMP} terms cancel leaving:

$$Ico = \frac{CN\ (max)}{MOD \times f_{VCO}\ (max)} \times \frac{f_{CRYSTAL}}{2} \times Ibo \quad ....(10)$$

For a typical AMPS cellphone the $f_{VCO}(max)$ for 45 MHz I.F. is 938·97 MHz, $f_{CRYSTAL}$ is 14·85 MHz, MOD is 8 and CN(max) can be assumed to be chosen around 200, giving Ico = 0·198 x Ibo.

Fractional-N Mode with Speed-Up

When Speed-up is active the main proportional charge pumps are run at an increased current and the integral charge pumps are switched on to move the loop filter voltage faster. The phase errors due to Fractional-N mode will be the same as normal once the loop is locked so the compensation pulses must be increased to match the proportional and integral charge pump currents in order to allow a smooth change over to normal mode at the end of Speed-up time. The same 2^{L+1} and K coefficients as used for the proportional and integral charge pump currents are used on the compensation currents so from equation (8):

Normal Mode:

Proportional Compensation Current:

$$Icomp(0) = ACC \times Ico$$

Integral Compensation Current:

$$Icomp = off$$

Speed-up Mode:

Proportional Compensation Current:

$$Icomp(1) = 2^{L+1} \times ACC \times Ico$$

Integral Compensation Current:

$$Icomp(2) = K \times 2^{L+1} \times ACC \times Ico$$

Required Accuracy of Compensation

With the compensation scheme used in ACE9030 it is not possible to get perfect cancellation of the loop disturbance by the Fractional-N system due to the mis-match of the pulse shapes leaving some high frequency terms, but if the areas are matched there will be complete removal of the low frequency components and the loop filter can be assumed able to remove higher frequencies.

Typical timing waveforms for the phase error and its compensation are shown in figure 28 for a loop operating in $^1/_8$'s mode (hence MOD = 8), with a VCO at 1 GHz, and a comparison frequency of 100 kHz (hence N_{TOT} = 10,000 and f_{COMP} period = 10 µs) so that each phase error can be found from equation (4) as:

(ACC x 10 µs) / (10,000 x 8) = ACC x 0·125 ns.

If the reference is a 12·8 MHz crystal, it gives a correction pulse duration, two reference cycles, of 2/(12·8 MHz) = 156 ns.

If the charge pump current of 250 µA is set by a CN value of 250 the reference current Ibo from equation (6) is 1 µA and the compensation step current Ico can be found from equation (10) as 0·2 x Ibo = 0·2 µA.

Areas of the error and the compensation pulses, equations (4) and (8) must match to get good low frequency cancellation. Although shown as a very narrow pulse on $\emptyset_{DOWN}$ the phase error will often appear as a change in size of the pulses on either $\emptyset_{DOWN}$ or $\emptyset_{UP}$ which occur to maintain lock. The following calculations would then apply to the changes and give the same final result.

If there was no compensation the $\emptyset_{DOWN}$ pulses would give sidebands at a level set by the loop filter capacitor values and the VCO gain.

In a typical system the filter proportional capacitor can be 6·8 nF and the VCO could cover 30 MHz in 3 V, giving 10 MHz/V. Assuming for the moment that all error pulses are the same at the level of a mid-range ACC value, say 4, and do

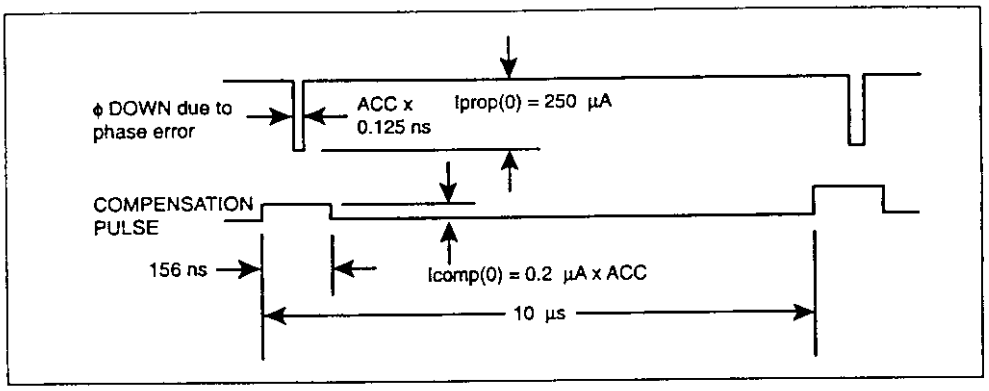


Fig. 28 Fractional-N Phase Error And Compensation Pulse

not ramp in size and that the loop somehow stays on the correct frequency:

Average phase error: = mid-range ACC x 0·125 ns
= 4 x 0·125 ns = 0·5 ns
Charge into filter: Q_{ERR} = 0·5 ns x 250 µA
= 125 fC per pulse
Voltage step: $V_{ERR} = Q_{ERR} \div C_{PROP}$
= 125 fC ÷ 6·8 nF = 18·4 µV
Frequency step: $F_{ERR} = V_{ERR}$ x VCO gain
= 18·4 µV x 10 MHz/V = 184 Hz

This gives a signal with a modulation frequency of 100 kHz with a step deviation of 184 Hz and if the loop is to stay on frequency the waveform must ramp back between steps, giving a sawtooth with an amplitude of ± 92 Hz. Fourier analysis gives the level of the fundamental as (2/π) x peak level, to give 58·6 Hz deviation and hence a modulation index β (peak deviation ÷ modulation frequency) of only 0·000586, putting it well into the narrow band f.m. category. At such small deviations the sideband amplitude is β/2 of the carrier, giving 0·000293 times or – 71 dBc. There will also be higher harmonics present but these will all be at lower levels.

This calculation assumed all phase error pulses are the same, but in reality the size varies in a pattern determined by the fractional numerator (0 to 7) with a period equal to the demoninator (8) times the comparison period. The fractions that give the highest level of output at $^1/_8 \times f_{COMP}$ are $^1/_8$ and $^7/_8$ and with these the phase error changes in seven steps of a staircase waveform until the eighth cycle, when the phase resets and the pattern starts again. The loop will settle to the correct average frequency by adding a d.c. offset for the mean level of the staircase, leading to an error waveform which is approximately a sawtooth wave with a step size of 7 in units of ACC value. The peak deviation is then $^7/_4$ times the previous calculation of ± 92 Hz and the level of the fundamental is again (2/π) x peak level, giving 102 Hz deviation at a frequency now of $^1/_8 \times f_{COMP}$ (12·5 kHz). β then becomes 102/12500 = 0·00816, giving sidebands at up to 0·00408 times or – 47 dBc.

Compensation pulses are used to cancel the effect of the unwanted phase corrections, and if these match to within 10 % they should give a reduction of 20 dB in the fundemental sideband levels, down to a worst figure of – 67 dBc. The low harmonics will also be adequately cancelled but higher harmonics will be left to the loop filter to remove, and as the bandwidth is set by the comparison frequency at only 8 times the Fractional-N fundamental these harmonics will always be well attenuated.

A typical system specification (AMPS) is – 60 dBc so the harmonic spectrum of the modulation needs to be considered to find the manufacturing margins but if the Fractional-N system is only used to help achieve correct lock times and spurious levels (rather than solve all loop problems on its own) then this example suggests that the compensation is not critical and can give a performance advantage at little cost.

More critical compensation is needed if N_{TOT} is less or if the comparison period is longer, but these cancel if the VCO stays at the same frequency, equation (4). Changing only the comparison frequency in the above example would then give the same 184 Hz deviation. In practice the loop filter capacitor value is likely to also change to match the new comparison frequency giving a peak deviation proportional to the comparison frequency. The modulation index is inversely proportional to the comparison frequency so the final sideband level is not, in practice, much affected by the comparison frequency choice, but the separation from the carrier is affected. This all suggests the above example is not just a spot typical result but will apply over a broad range of systems and allow Fractional-N to be used whenever desired.

APPLICATIONS HINTS

V_{DD} & V_{SS} Supply Pins

All V_{DD} pins must be well decoupled to ground. All V_{SS} pins must be connected through very low impedance lines to the ground point.

Serial Bus

Edge speeds on the serial bus should not be too fast in order to avoid ringing which then can cause significant modulation of the synthesisers, including CLK8.

Loop Filters

Both synthesisers use passive loop filters and typical circuits can be either of these two configurations; the need for the extra roll-off in the right hand circuit is only for the more critical applications.

The loop filter needed is partly set by the application specification and partly by the architectural design of the cellphone. The main synthesiser will need to hop channels at a rate set by the hand-off times of the network and so is well defined. The auxiliary synthesiser is always on the same frequency and so could be a very slow loop to lock but in many systems it will be powered down for as much time as possible to economise on battery use and will then need to power-up and lock quickly, leading to a more complex filter.

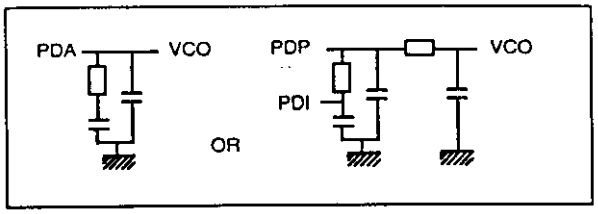


Fig. 29 Typical Synthesiser Loop Filters

The values of the components in these filters may be calculated with the help of appendix AB43 in the Personal Communications Handbook or for a more complete analysis the application note AN94, available from GEC Plessey Semiconductors' Marketing Department, may be used. This note was written specifically for the NJ88C33 synthesiser but the mathematics apply equally well to the ACE9030.

AFC Circuit

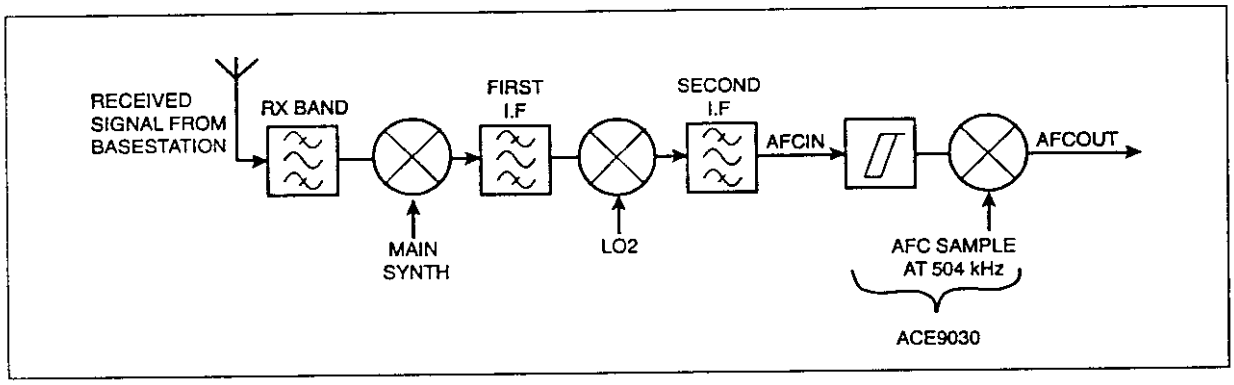


Fig. 30 Simplified Receiver Architecture

In order to fine trim the crystal oscillator frequency to the correct value the ACE9030 includes a sampling circuit to convert the final intermediate frequency signal (input on AFCIN) to a logic signal and then to mix it down to a low frequency output (on AFCOUT) for counting in the microcontroller. The operation of this system can be explained with the use of a simplified block diagram of the receiver architecture as in figure 30.

Most receivers run the first mixer with a high-side local oscillator controlled by the Main synthesiser, so a positive crystal frequency error will give an increased First I.F. This is then mixed down further by a low-side second oscillator, LO2 in the ACE9030, derived by multiplying the same crystal as used for the Main synthesiser. A positive crystal frequency error would now give a reduced second I.F. if the error in the first I.F. is ignored, but the overall effect is an increase by an amount slightly smaller than the increase in the first I.F.

The second I.F. signal AFCIN at around 450 kHz drives the F.M. Discriminator to recover the modulation and also feeds a third mixer where high-side injection is used to give a very low output frequency, around 54 kHz, and is output on AFCOUT for counting. This third mixer is driven by a clock derived from the crystal but at a much reduced frequency so the effect of the high-side mixing dominates to give an output which drops in frequency when the crystal has a positive frequency error. As a result of the chain of mixing stages the error in the first local oscillator due to the crystal frequency will give a similar frequency shift at the output of the third mixer which is then a large percentage change in the frequency of AFCOUT so it is possible to measure AFCOUT against the crystal to determine the trim needed.

To illustrate the sensitivity of the AFC loop a numerical example can be used, and in the calculations that follow the selection of parameters for the synthesisers are also included to show how some choices are made.

Assume the required receiver frequency is AMPS channel 1, that is 870·030 MHz and that the cellular terminal is built with a 45 MHz first I.F., a 450 kHz second I.F., and a 14·85 MHz crystal.

To receive 870·030 MHz with a 45 MHz first I.F. needs the first local oscillator, the Main synthesiser, to run at a frequency of 870·030 + 45·000 = 915·030 MHz when using high-side injection. For AMPS the most convenient comparison frequency is the channel spacing of 30 kHz so the total division from VCO to phase comparator (N_{TOT} as used elsewhere) will be 30501 for this channel and the reference

division will be 495 for a 14·85 MHz crystal; the term $f_{CRYSTAL}$ is used to refer to the exact crystal frequency in the following calculations.

Thus Main synthesiser (nominally 915·030 MHz) generates:

$$f_{CRYSTAL} \times 30501 + 495 = f_{CRYSTAL} \times 61{\cdot}61818182$$

This result is independant of the chosen comparison frequency which is given above as an illustration only.

With this drive to the first mixer the actual first I.F. (nominally 45 MHz) is:

$$f_{CRYSTAL} \times 61{\cdot}61818182 - 870{\cdot}030 \text{ MHz}$$

The second mixer is required to downconvert 45 MHz to 450 kHz so needs an LO2 at 44·550 MHz which is $3 \infty f_{CRYSTAL}$ and this integer multiplication is the reason for choosing a 14·85 MHz crystal. This mixer operates with low-side injection so the actual second I.F. on the AFCIN pin (nominally 450 kHz) is:

$$f_{CRYSTAL} \times 61{\cdot}61818182 - 870{\cdot}030 \text{ MHz} - 3 \infty f_{CRYSTAL}$$

$$= f_{CRYSTAL} \times 58{\cdot}61818182 - 870{\cdot}030 \text{ MHz}$$

This signal feeds the F.M. discriminator to extract the modulation and is also used to derive the AFC information.

The AFC mixer uses a 504 kHz clock derived from the crystal ($f_{CRYSTAL} \infty 504 \div 14850 = f_{CRYSTAL} \infty 0{\cdot}03393939$) to high-side downconvert AFCIN to a low frequency on AFCOUT, giving:

$$(f_{CRYSTAL} \times 0{\cdot}03393939) - (f_{CRYSTAL} \times 58{\cdot}61818182 - 870{\cdot}030 \text{ MHz}).$$

This is 870·030 MHz – $f_{CRYSTAL}$ x 58·58424243 and is the difference between two large but similar numbers, one fixed and the other a multiple of $f_{CRYSTAL}$ and will have an overall value strongly dependent on $f_{CRYSTAL}$.

To evaluate the sensitivity of the system consider a + 1 ppm change in crystal frequency, giving AFCOUT at 53·130 kHz instead of its nominal at 54 kHz, a shift of 870 Hz or 1·61 %. This frequency can be counted in the microcontroller using a timebase derived from $f_{CRYSTAL}$ or any other crystal reference as the error in the timebase due to the crystal is swamped by the changes in AFCOUT.

The counting of AFCOUT should be over a period long enough to resolve changes of around 1 % which means at least 2 ms but is normally a little longer to filter off some noise and modulation on the signal; around 10 ms is a good starting value for system development.

Once the crystal error has been estimated the DAC's controlling the crystal frequency can be adjusted to bring the whole cellular terminal into frequency alignment with the basestation which is normally assumed to be very accurately held at the correct frequency; effects like Doppler shift will be significantly less than 1 ppm for all intended users. Some damping in the control loop for the crystal will be needed to avoid overshoot and hunting, possibly implemented as always under-correcting the crystal or by limiting the slew rate of the corrections.

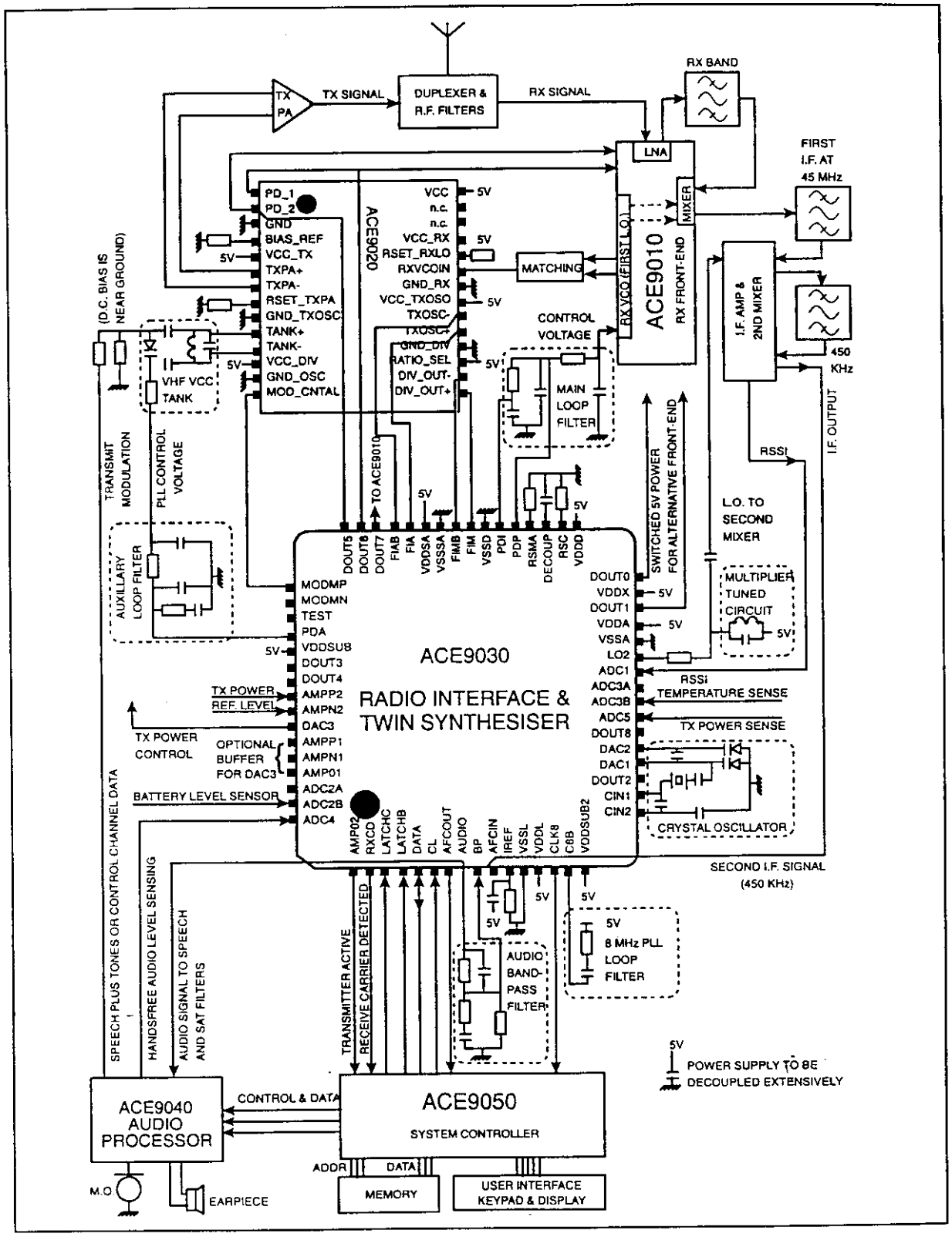
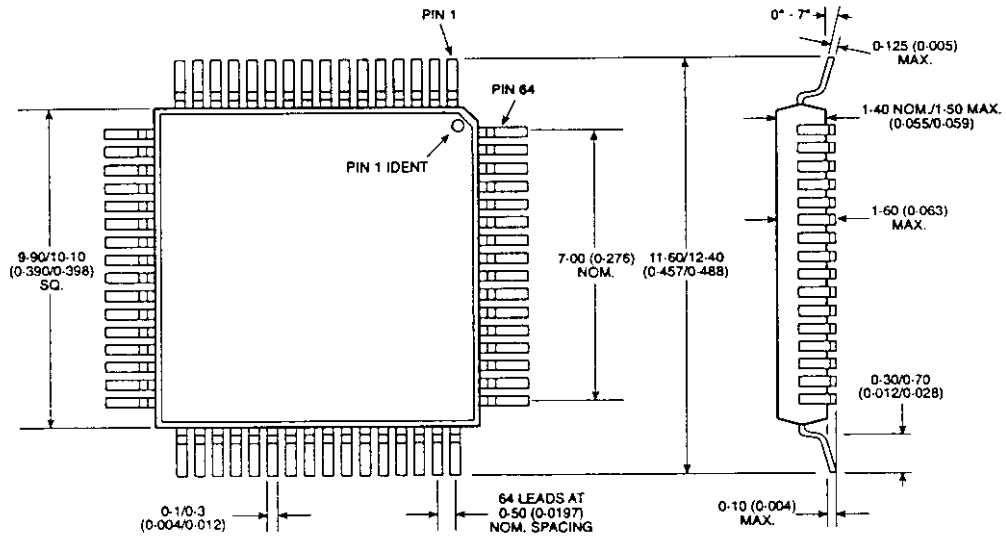


Fig. 31 Complete cellular terminal, showing details of ACE9030 typical application.

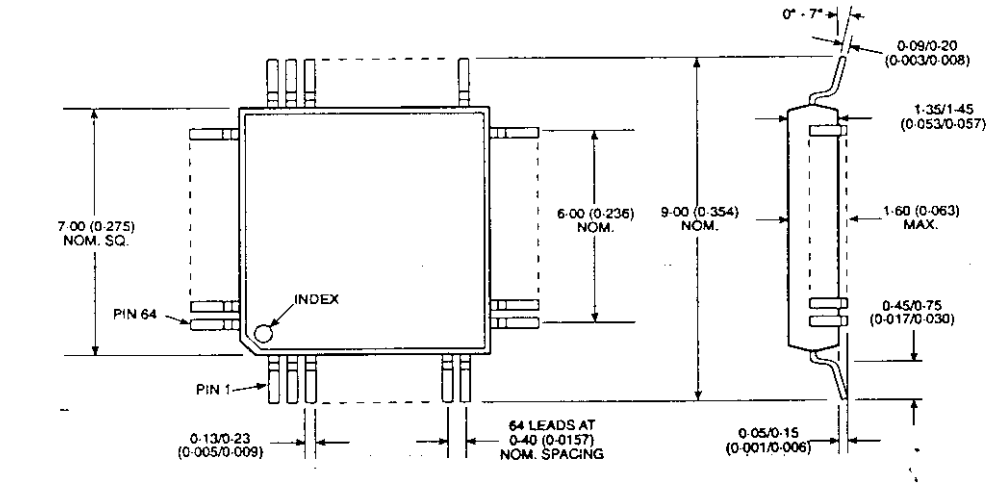
PACKAGE DETAILS

Dimensions are shown thus: mm (in). For further package information, please contact your local Customer Service Centre.



NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

64-LEAD FINE PITCH PLASTIC QUAD FLATPACK – FP64 (10 x 10 mm)



NOTES
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64-LEAD FINE PITCH PLASTIC QUAD FLATPACK – FP64 (7 x 7 mm)

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