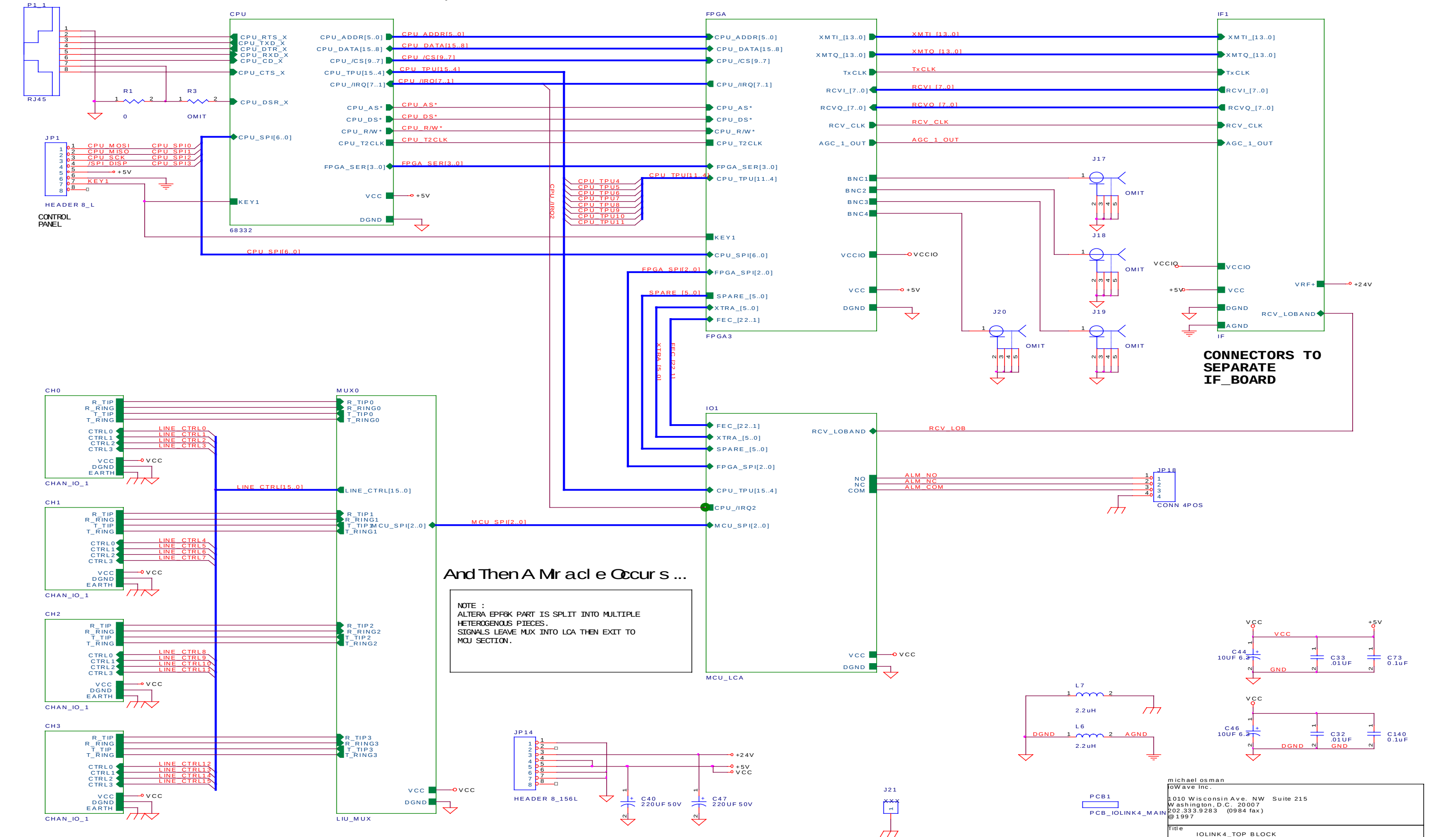


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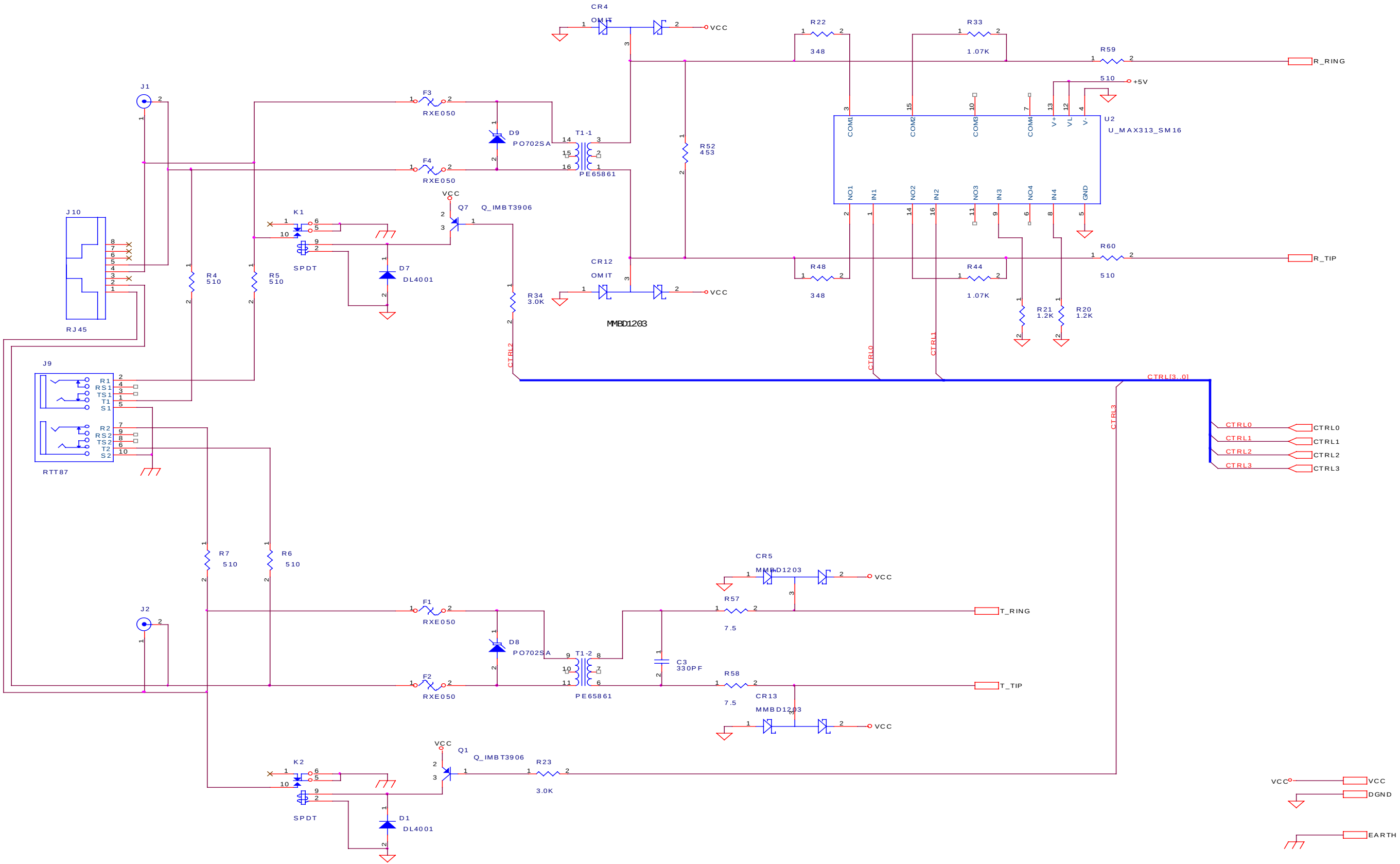
IoLink4

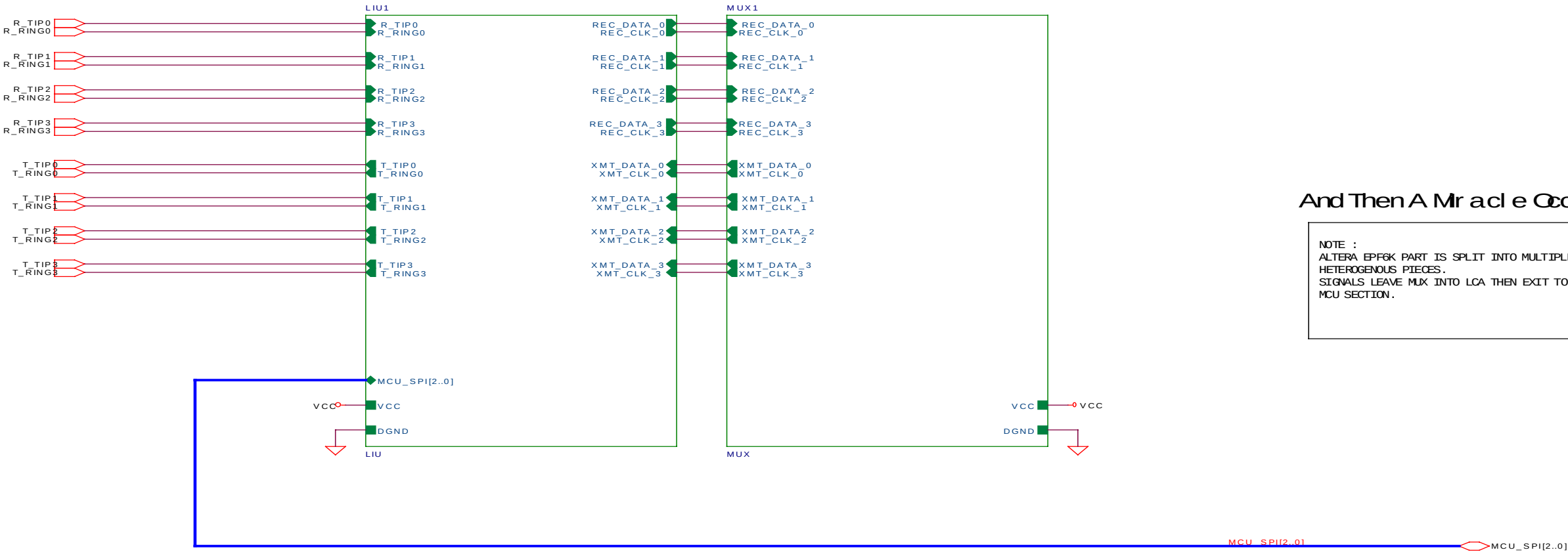
List of Figures :

PAGE 2	TOP BLOCK DIAGRAM
PAGE 3	CHANNEL IO (1 OF 4 SHOWN)
PAGE 4	LIU_MUX BLOCK DIAGRAM
PAGE 5	LIU (LINE INTERFACE UNIT)
PAGE 6	MUX (MULTIPLEXER)
PAGE 7	FEC (FORWARD ERROR CORRECTION)
PAGE 8	DTMF – ANALOG SIGNALING TO REMOTE UNIT
PAGE 9	FPGA (FIELD PROGRAMMABLE GATE ARRAY) NETWORK
PAGE 10	IF_CONNECTOR (TO IF_SECTION SCHEMATIC) – OFF-BOARD
PAGE 11	MCU_BLOCK DIAGRAM (MICROCONTROLLER BLOCK)
PAGE 12	MCU (68HC11 MICROCONTROLLER)
PAGE 13	LCA_LOAD (BASE FPGA LOAD CIRCUITRY)
PAGE 14	MPU (68332 MICROPROCESSOR)
PAGE 15	MEM1 (BOOT FLASH AND SRAM)
PAGE 16	MEM2 (EXPANSION FLASH AND EEPROM)



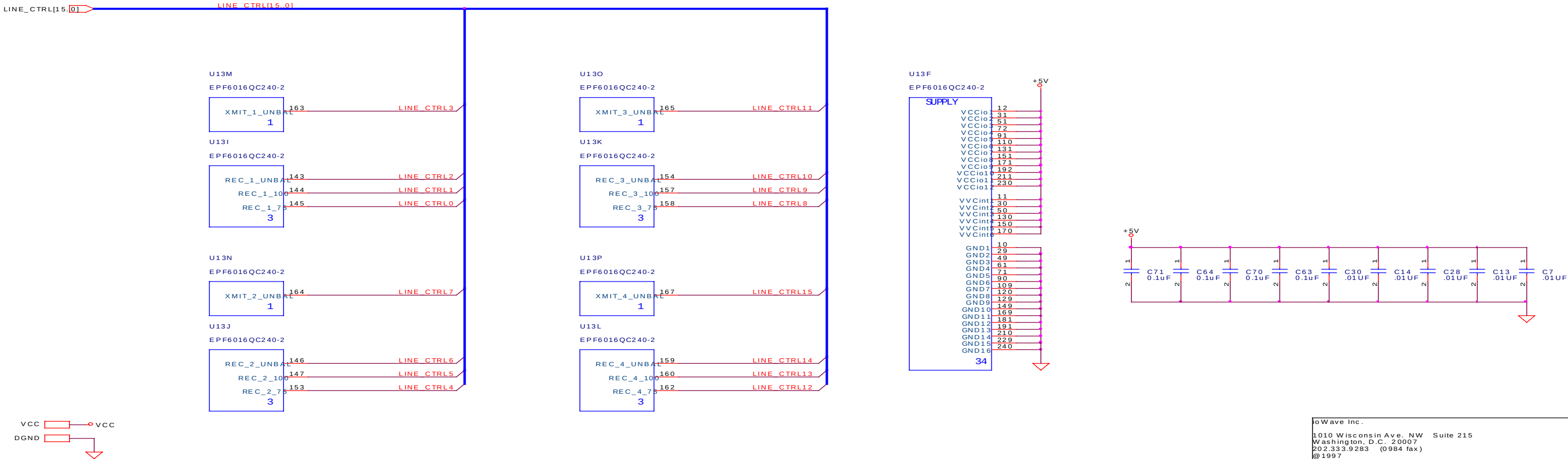
Title			IOLINK4_TOP BLOCK		
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Date:			Monday, February 22, 1999		
Sheet			1 of 19		
Rev			B		

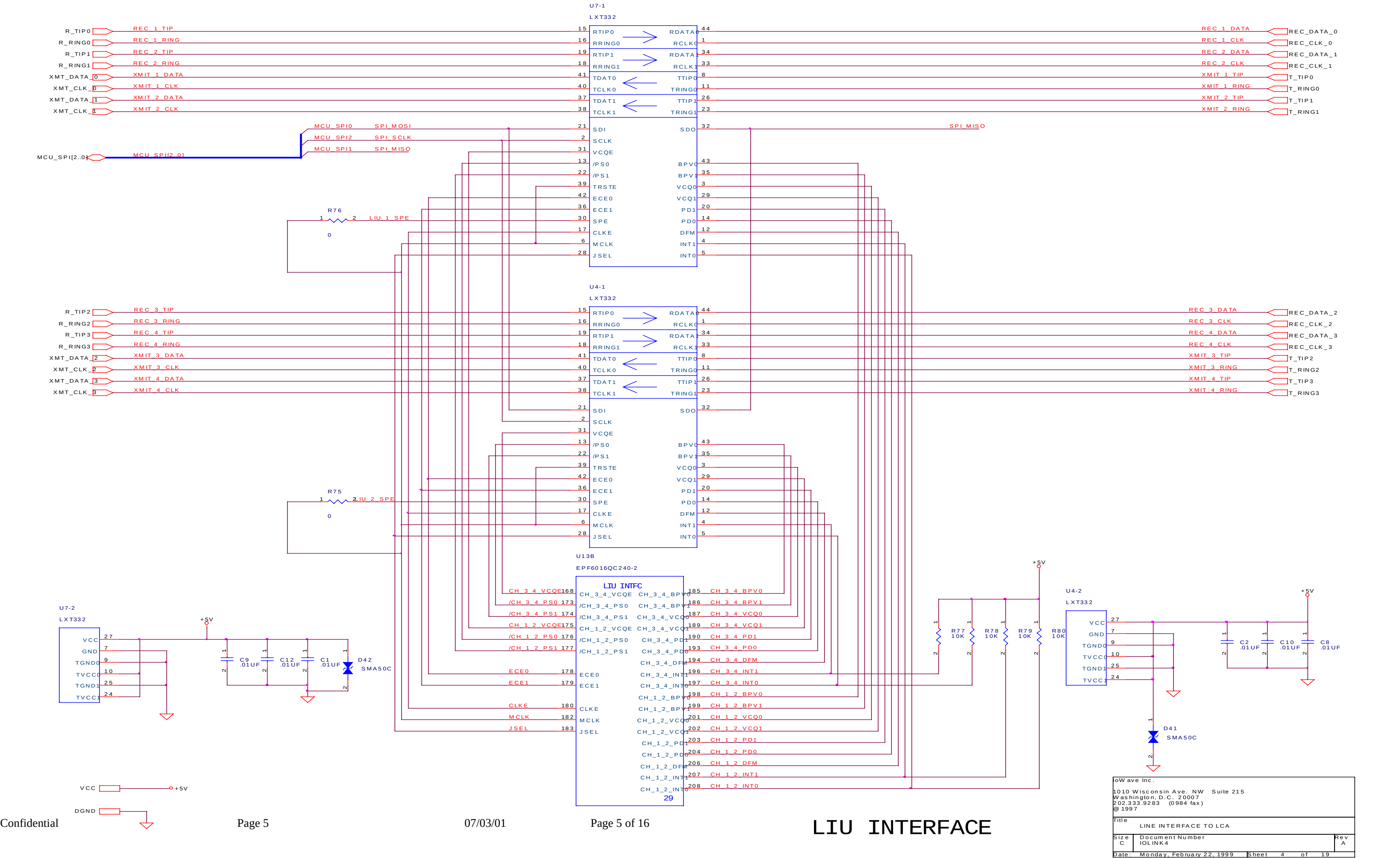


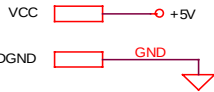
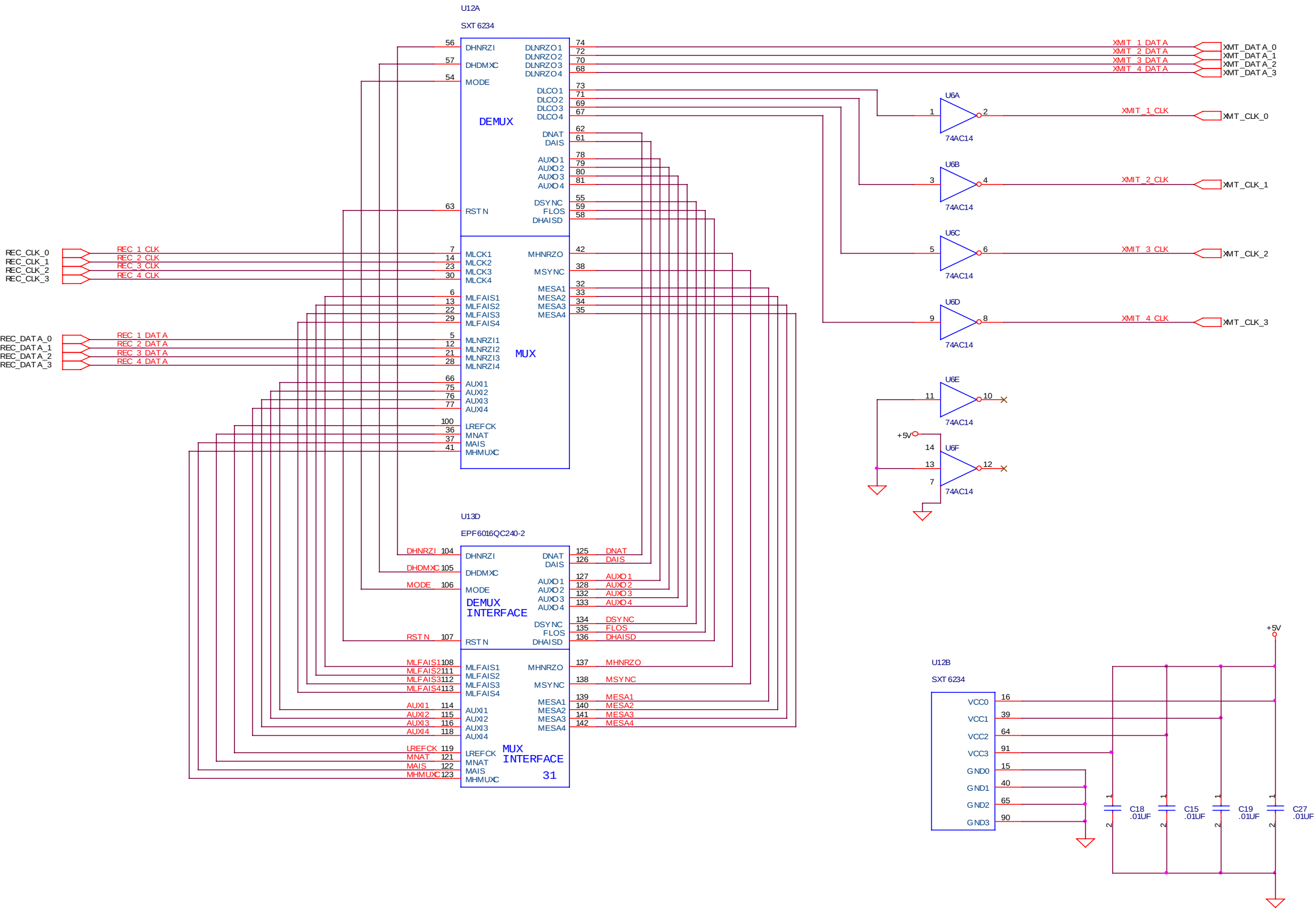


And Then A Miracle Occurs ...

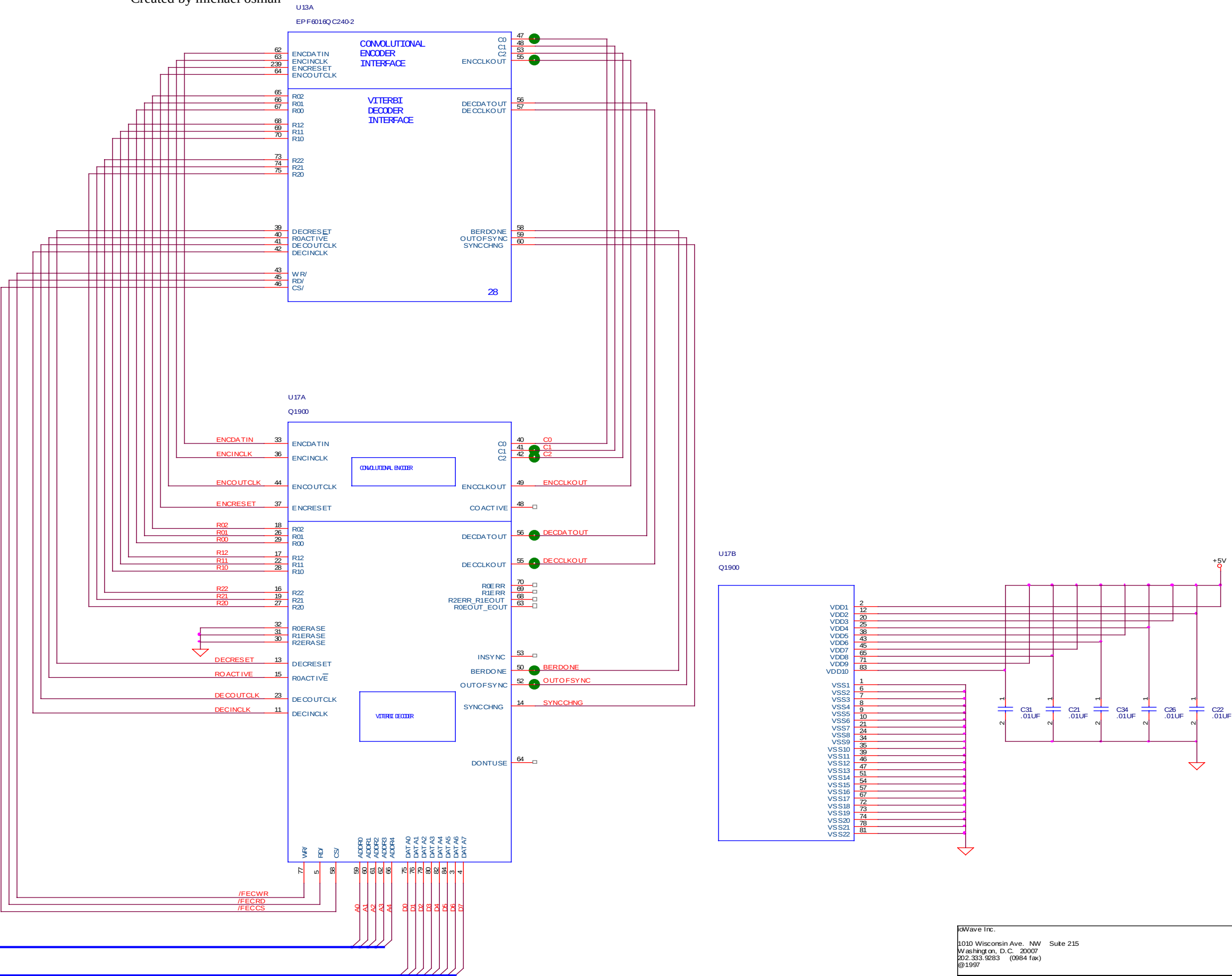
NOTE :
ALTERA EPF6K PART IS SPLIT INTO MULTIPLE
HETEROGENOUS PIECES.
SIGNALS LEAVE MUX INTO LCA THEN EXIT TO
MCU SECTION.





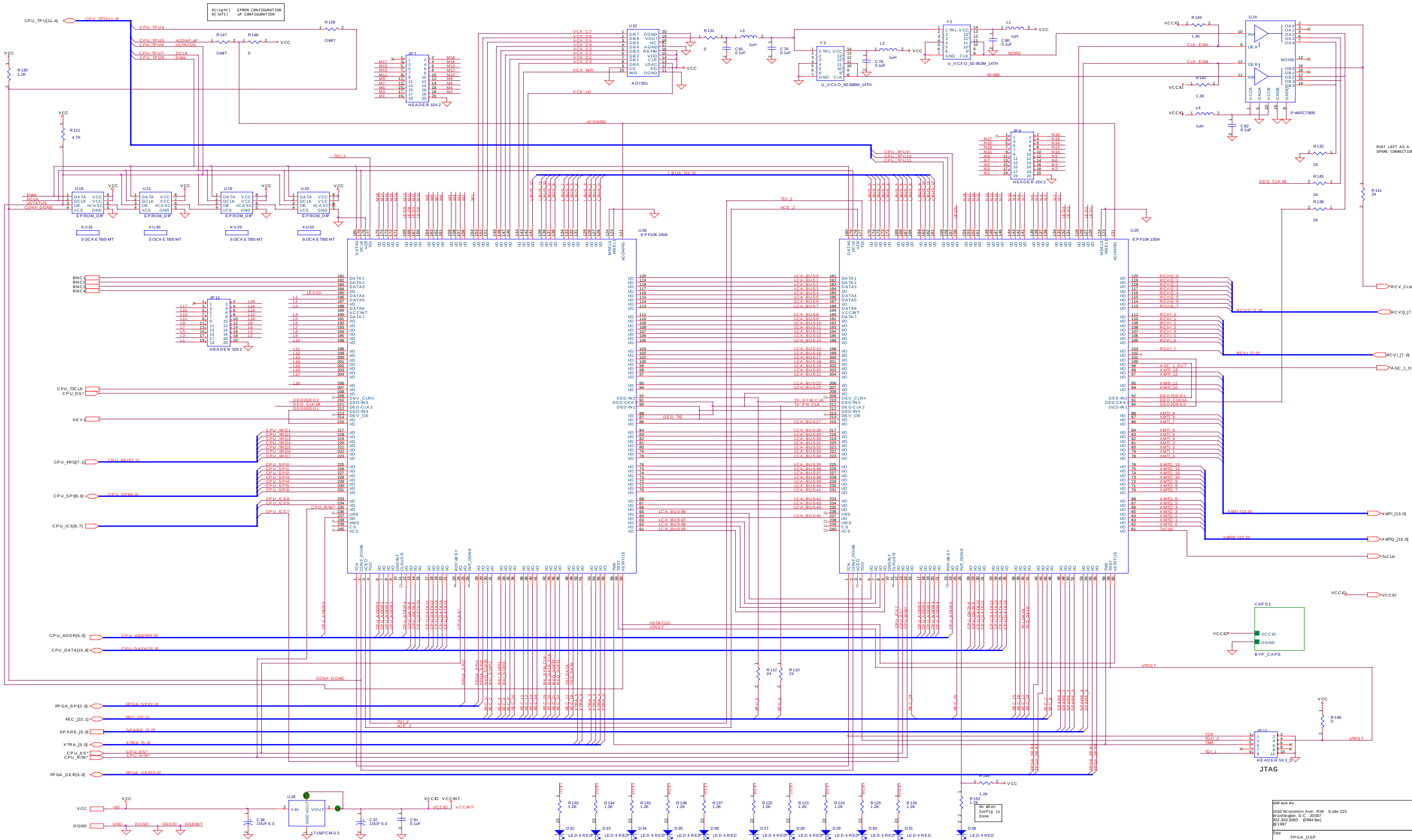


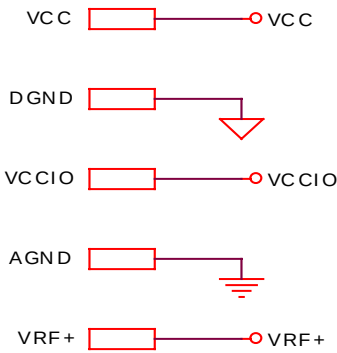
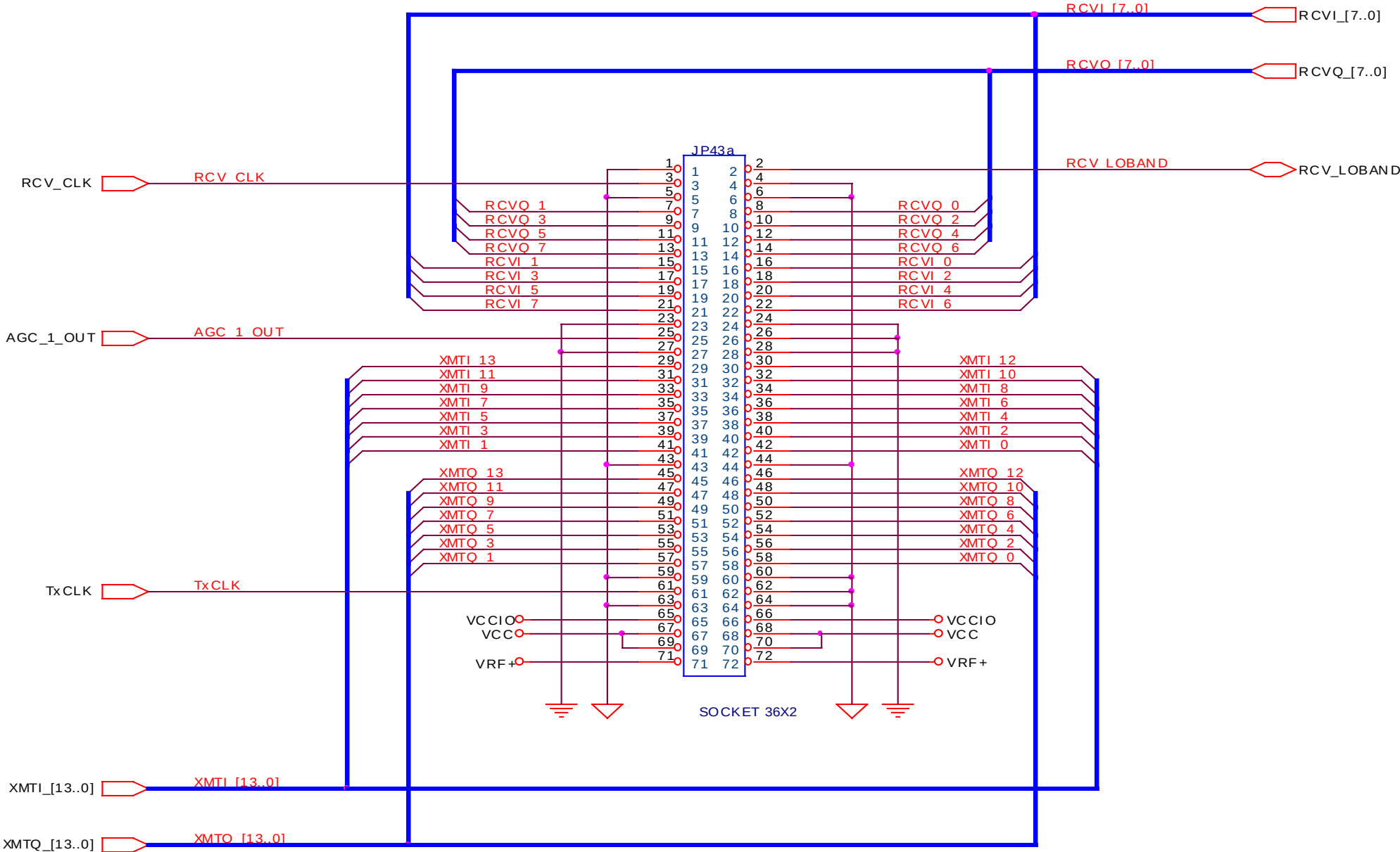
FEC INTERFACE



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Title FEC INTERFACE		
Size C	Document Number IOLINK4	Rev A
Date: Monday, February 22, 1999	Sheet 14	of 19







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Title IF_CONNECTOR		
Size B	Document Number IOLINK4	Rev A
Date:	Monday, February 22, 1999	Sheet 16 of 19

