

Automotive 5G-NR NAD Product Specification

UMC-STD35FFx

WNC Corporation

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1. INTRODUCTION

This chapter describes the general concept of the NAD and key specifications according to the modem mode applications

1.1 UMC-STD35FFX INTRODUCTION

This document describes and specifies technical features of UMC-STD35FF regional variant NAD(remarked as UMC-STD35FFx in the following section content). This NAD is an automotive-grade 5G NR Network Access Device of LGA type form-factor offering a full set of telematics features and functions including e-Call, GNSS, FOTA and so on. UMC-STD35FFx is fully approved, including regional, country, and carrier approvals. It supports automotive applications like Telematics Control Unit, Vehicle to Everything, Fleet Management, Automatic Metering Management, Tracking System, Emergency Call, Breakdown or Roadside Assistance

1.2 PRODUCT FEATURE

The NAD is employed with an MTK(MediaTek Inc.) MT2735 5G NR platform consisting of:

Function	Brand	Order P/N	Simplified P/N	Note
NR Modem	MTK	MT2735V/MZA	MT2735M	2-Core
Main Power Management IC	MTK	MT6330LW/A	MT6330LW	
Second Power Management IC	MTK	MT6319WW/A	MT6319WW	
RFIC	MTK	MT6190AV/A	MT6190AV	
GNSS RFIC	MTK	MT6635GW/B	MT6635GW	

1.3 NAD KEY SPECIFICATION

1.3.1 Electrical key specifications

Table 1.3-1

Electrical Key Specifications	Compliance	NAD Pad Name
Peripheral Interface		
PCIe 3.0 x2 Root Complex	Supported by Host Mode; Link Rate of 2.5GT/s, 5GT/s and 8GT/s per Lane	PCIE0_PERSTN; PCIE0_CLKREQN; PCIE0_PEWAKEN PCIE_A_CLKN; PCIE_A_CLKP PCIE_A_LN0_RXN; PCIE_A_LN0_RXP; PCIE_A_LN0_TXN; PCIE_A_LN0_TXP PCIE_A_LN1_RXN; PCIE_A_LN1_RXP; PCIE_A_LN1_TXN; PCIE_A_LN1_TXP
HS-USB 2.0	Supported for the debugging only	USB_DM; USB_DP
SS-USB 3.0	Reserved	SSUSB_RXN; SSUSB_RXP; SSUSB_TXN; SSUSB_TXP
4-bit SDIO	Reserved	MSDC1_CLK; MSDC1_CMD; MSDC1_DAT0; MSDC1_DAT1; MSDC1_DAT2; MSDC1_DAT3

Digital TDM(Out) (GPIO as the default)	Reserved	TDM_MCK; TDM_BCK; TDM_LRCK; TDM_DATA0; TDM_DATA1; TDM_DATA2; TDM_DATA3 (EINT201, EINT200, EINT199, EINT202, EINT203, EINT204, EINT205)
MIPI0 (GPIO as the default)	Reserved	MIPI0_D_SCLK, MIPI0_D_SDATA (EINT140, EINT141)
MIPI1 (GPIO as the default)	Reserved	MIPI1_D_SCLK, MIPI1_D_SDATA (EINT138, EINT139)
MIPI2 (GPIO as the default)	Reserved	MIPI2_D_SCLK, MIPI2_D_SDATA (EINT164, EINT165)
Digital Audio I2S0	Supported by Modem Mode as Slave	I2S0_MCK; I2S0_BCK; I2S0_LRCK; I2S0_DI; I2S0_DO
Digital Audio I2S2	Supported by Modem Mode as Slave	I2S2_MCK; I2S2_BCK; I2S2_LRCK; I2S2_DI; I2S1_DO
Digital Audio PCM0 (GPIO as the default)	Reserved	I2S4_MCK; PCM0_CLK; PCM0_SYNC; PCM0_DI; PCM0_DO (EINT96, EINT97, EINT98, EINT99, EINT100)
SGMII0	Reserved for Modem Mode ; supported by Host Mode w/ AVB only, no Data IPA; or Data IPA only, no AVB	GBE0_INT; GBE0_RST SGMII_0_RXN; SGMII_0_RXP; SGMII_0_TXN; SGMII_0_TXP
RGMII	Reserved for Modem Mode ; supported by Host Mode w/ AVB only, no Data IPA; or Half Data IPA only, no AVB	GBE_TXEN; GBE_TXER; GBE_RXER; GBE_RXDV; GBE_TXC; GBE_RXC; GBE_COL; GBE_INTR; GBE_MDC; GBE_MDIO GBE_TXD0; GBE_TXD1; GBE_TXD2; GBE_TXD3; GBE_RXD0; GBE_RXD1; GBE_RXD2; GBE_RXD3
SGMII1	Reserved for Modem Mode ; supported by Host Mode w/ Data IPA only, no AVB	GBE1_INT; GBE1_RST SGMII_1_RXN; SGMII_1_RXP; SGMII_1_TXN; SGMII_1_TXP
SIM1	Supported	INT_SIM1; SIM1_SCLK; SIM1_SIO; SIM1_SRST
SIM2	Supported	INT_SIM2; SIM2_SCLK; SIM2_SIO; SIM2_SRST
I2C0	Supported	SCL0; SDA0
I2C1	Supported	SCL1; SDA1
I2C2	Supported	SCL2; SDA2
I2C3 (GPIO as the default)	Reserved	SCL3; SDA3 (EINT198, EINT197)
I2C4 (GPIO as the default)	Reserved	SCL4; SDA4 (EINT80, EINT79)
I2C5 (GPIO as the default)	Reserved	SCL5; SDA5 (EINT82, EINT81)
UART0 (GPIO as the default)	Supported w/ 2-Wire	AP_UTXD0; AP_URXD0; AP_URTS0(EINT170); AP_UCTS0(EINT169)
UART1 (GPIO as the default)	Reserved; supported w/ 2- Wire	AP_UTXD1; AP_URXD1; AP_URTS1(EINT174); AP_UCTS1(EINT173)
UART2 (GPIO as the default)	Reserved; supported w/ 2- Wire	AP_UTXD2; AP_URXD2; AP_URTS2(EINT178); AP_UCTS2(EINT177)
UART3 (GPIO as the default)	Reserved; supported w/ 2- Wire	AP_UTXD3; AP_URXD3;(AP_UCTS3(EINT181); AP_URTS3(EINT182)

Analog-to-Digital Converter Input	Reserved	AUXIN0; AUXIN1; AUXIN2; AUXIN3
SPI0	Supported	SPI0_CSB, SPI0_CLK, SPI0_MI, SPI0_MO
SPI1	Reserved	SPI1_CSB, SPI1_CLK, SPI1_MI, SPI1_MO
SPI2	Reserved	SPI2_CSB, SPI2_CLK, SPI2_MI, SPI2_MO
SPI3	Reserved	SPI3_CSB, SPI3_CLK, SPI3_MI, SPI3_MO
General Purpose Input/Output	Supported	Refer to Section 2.2

1.3.2 RF key specifications

Table 1.3-2

RF Key Specification	Compliance
Envelope Tracking(ET) of Power Amplifier DC-feed Controlling	n/a
Average Power Tracking(APT) of Power Amplifier DC-feed Controlling	n/a
LTE Downlink Carrier Aggregation	See Section 3.4.1
NR Downlink Carrier Aggregation	See Section 3.4.2
LTE Uplink Carrier Aggregation	n/a
NR Uplink MIMO	n/a
NR/SA High Power UE(HPUE)	Power Class 2 supported by NA: n41 and n77 RW: n78
NR/NSA High Power UE(HPUE)	n/a
NR/SA Sounding Reference Signal(SRS)	1T2R supported by NA: n41 and n77 RW: n78
NR/NSA Sounding Reference Signal(SRS)	n/a
Dynamic Spectrum Sharing(DSS)	Supported
E-UTRAN New Radio - Dual Connectivity(EN-DC)	See Section 3.4.3
Dual SIM Dual Active	n/a
Dual SIM Dual Standby	Supported
Licensed Assisted Access(LAA)	n/a
Cellular Vehicle-to-Everything(C-V2X) over the legacy LTE Uu air interface	n/a

Cellular Vehicle-to-Everything(C-V2X) via PC5 interface	Supported with the limitation that NAD needs the external C-V2X
Dedicated Short Range Communication(DSRC) Vehicle-to-Everything(V2X)	Supported with the limitation that NAD needs the external DSRC
3rd Generation Partnership Project(3GPP) Circuit Switched(CS) emergency Call(eCall)	Supported w/ Embedded MTK/MT6635 GNSS RFIC
Europe(EU) CS eCall	Supported w/ Embedded MTK/MT6635 GNSS RFIC
EU Internet Multimedia System(IMS) eCall	Supported w/ Embedded MTK/MT6635 GNSS RFIC
3GPP IMS eCall included in Next Generation(NG)-eCall	Supported w/ Embedded MTK/MT6635 GNSS RFIC
ERA-Global Navigation Satellite System(GLONASS) eCall	Supported w/ Embedded MTK/MT6635 GNSS RFIC

1.3.3 NAD band plan and antenna configuration

UMC-STD35FFx NAD well-designed for countries and carriers in North America(UMC-STD35FFN) and Rest of World(UMC-STD35FFR)

NR NSA/SA low/middle/high band supports re-use of RF Front-End of LTE bands; GNSS antenna is not defined in the table and supported by NAD-Pad#AA1(RF_GNSS_L1_L5_ANT)

Table 1.3-3 UMC-STD35FFN

RAT/Variant	NA	RF-ANT1 (Transmitting and Primary Receiving)	RF-ANT2 (Diversity Receiving)	RF-ANT3 (MIMO1 Receiving)	RF-ANT4 (MIMO2 Receiving)
NSA/SA NR	n5 and n71 n2 and n66; n7 and n41 n77 and n78	n5 and n71 n2 and n66; n7 and n41 n77 and n78	n5 and n71 n2 and n66; n7 and n41 n77 and n78	n2 and n66; n7 and n41 n77 and n78	n2 and n66; n7 and n41 n77 and n78
LTE	B26(5), 12(17), 13, 14, 29 and 71 B25(2) and 66(4) B7, 30 and 41	B26(5), 12(17), 13, 14, 29 and 71 B25(2) and 66(4) B7, 30 and 41	B26(5), 12(17), 13, 14, 29 and 71 B25(2) and 66(4) B7, 30 and 41	B25(2) and 66(4) B7, 30 and 41	B25(2) and 66(4) B7, 30 and 41
WCDMA/TD-SCDMA	B1* ¹ , B2, B3* ¹ , B4 and 5	B1* ¹ , B2, B3* ¹ , B4 and 5	B1* ¹ , B2, B3* ¹ , B4 and 5	n/a	n/a
GSM/GPRS/EDGE	850* ² , 900* ² , 1800* ² , 1900* ²	850* ² , 900* ² , 1800* ² , 1900* ²	n/a	n/a	n/a

*1 WCDMA B1, B3 are only specified for Engineer testing purposes and will not be officially activated in NAD series production

*2 GSM 850/900/1800/1900 are only specified for Engineer testing purposes and will not be officially activated in NAD series production

Table 1.3-4 UMC-STD35FFR

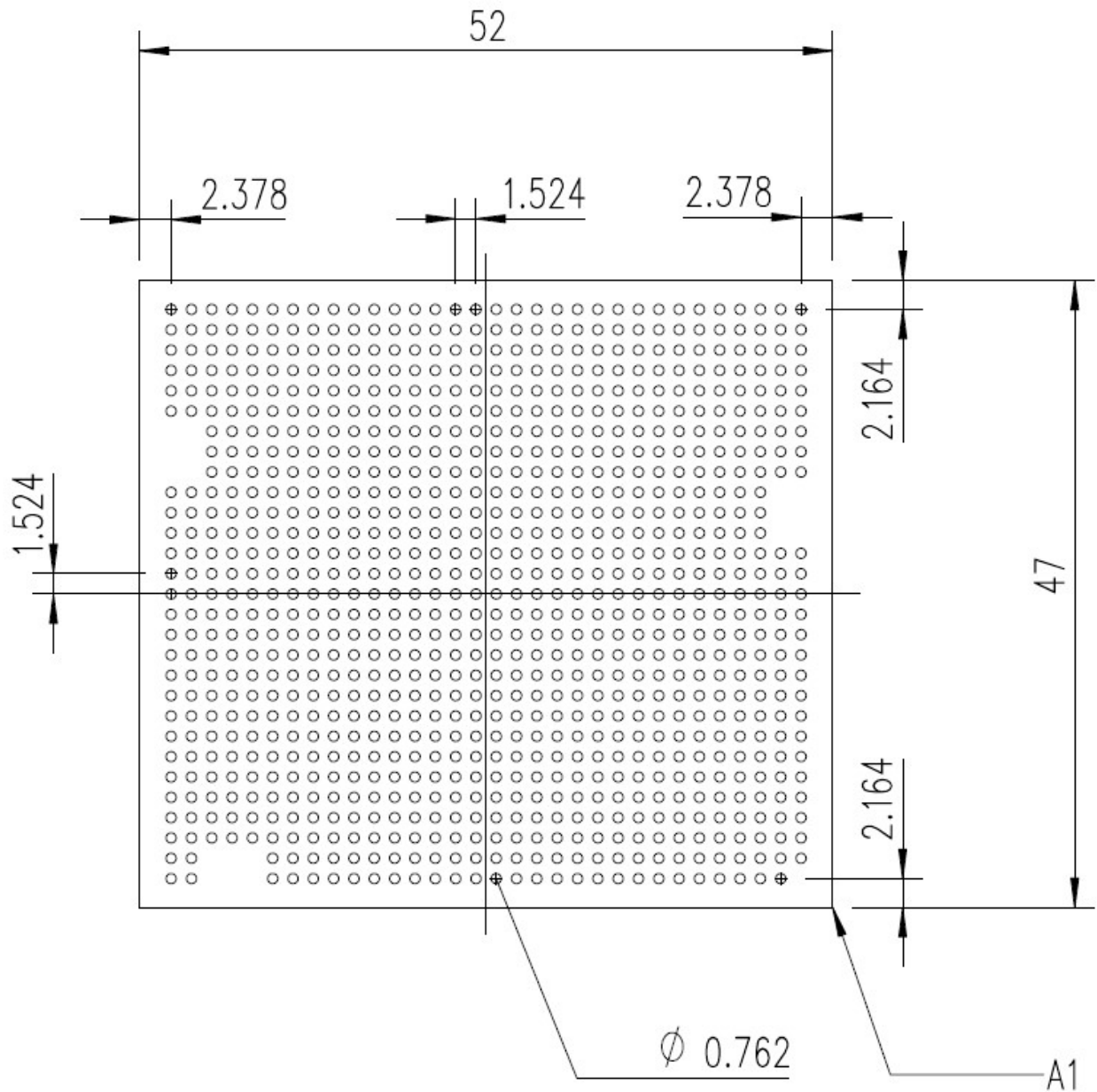
RAT/Variant	RW	RF-ANT1 (Transmitting and Primary Receiving)	RF-ANT2 (Diversity Receiving)	RF-ANT3 (MIMO1 Receiving)	RF-ANT4 (MIMO2 Receiving)
NSA/SA NR	n28 n1 and n3 n41 n77, n78 and n79	n28 n1 and n3 n41 n77, n78 and n79	n28 n1 and n3 n41 n77, n78 and n79	n1 and n3 n41 n77, n78 and n79	n1 and n3 n41 n77, n78 and n79
LTE	B26(5/18/19), 8, 20 and 28 B32 B1 and 3 B7, 40 and 41(38)	B26(5/18/19), 8, 20 and 28 B1 and 3 B7, 40 and 41(38)	B26(5/18/19), 8, 20 and 28 B1 and 3 B7, 40 and 41(38)	B32 B1 and 3 B7, 40 and 41(38)	B32 B1 and 3 B7, 40 and 41(38)
WCDMA/TD-SCDMA	B1, 3(9*1), 5(6*1/19) and 8	B1, 3(9*1), 5(6*1/19) and 8	B1, 3(9*1), 5(6*1/19) and 8	n/a	n/a
GSM/GPRS/EDGE	850, 900, 1800 and 1900	850, 900, 1800 and 1900	n/a	n/a	n/a

*1 WCDMA B6, B9 are only specified for Engineer testing purposes and will not be officially activated in NAD series production

2. PIN DEFINITIONS

NAD Land Pattern Diagram

- Bottom Side View
- 32 by 29 LGA-type Land Pattern
- #909 Contact Pins
- 0.762-mm Round Pad Size
- 1.524-mm Pad Pitch



Unit: mm

A7	Reserved(VIO18_1_PMU)	VIO18 1.8-V Output Power Rail		1.8V
A8	INT_SIM2	SIM2 Interrupt		1.8V
A9	SIM1_SCLK	SIM1 Clock	Pull-Down	1.8V/3V
A10	SIM2_SIO	SIM2 Data	Pull-Down	1.8V/3V
A11	SIM1_SIO	SIM1 Data	Pull-Down	1.8V/3V
A12	INT_SIM1	SIM1 Interrupt		1.8V
A13	D_GND			
A14	Reserved(SSUSB_RXP)	Super-speed RX Data		
A15	D_GND			
A16	Reserved(SSUSB_TXP)	Super-speed TX Data		
A17	D_GND			
A18	USB_DM	USB D- Differential Data Line		
A19	D_GND			
A20	PCIE_A_LN1_RXN	PCIe RX Data Lane1		
A21	D_GND			
A22	PCIE_A_LN0_RXN	PCIe RX Data Lane0		
A23	D_GND			
A24	PCIE_A_CLKN	PCIe Clock		
A25	D_GND			
A26	EINT41	External Interrupt Input	Pull-Down	1.8V
A27	EINT42	External Interrupt Input	Pull-Down	1.8V
A31	D_GND			
A32	D_GND			
B1	D_GND			
B2	Reserved(MDIO)	Management Data I/O of SGMII	Pull-Down	1.8V
B3	Reserved(GBE1_INT)	SGMII1 Interrupt	Pull-Down	1.8V
B4	Reserved(GBE1_RST)	SGMII1 RST	Pull-Down	1.8V
B5	VSYS	System 4.7-V Power Rail Feed-in		
B6	VSYS	System 4.7-V Power Rail Feed-in		
B7	VSIM2_PMU	Power for SIM2		
B8	FULL_ON	Input Key Powers-ON/OFF NAD/PMIC1		4V
B9	SIM1_SRST	SIM1 Reset	Pull-Down	1.8V/3V
B10	SIM2_SCLK	SIM2 Clock	Pull-Down	1.8V/3V
B11	SIM2_SRST	SIM2 Reset	Pull-Down	1.8V/3V
B12	D_GND			
B13	D_GND			
B14	Reserved(SSUSB_RXN)	Super-speed RX Data		
B15	D_GND			
B16	Reserved(SSUSB_TXN)	Super-speed RX Data		
B17	D_GND			
B18	USB_DP	USB D+ Differential Data Line		
B19	D_GND			
B20	PCIE_A_LN1_RXP	PCIe RX Data Lane1		
B21	D_GND			

B22	PCIE_A_LN0_RXP	PCIe Lane0 RX		
B23	D_GND			
B24	PCIE_A_CLKP	PCIe Clock		
B25	D_GND			
B26	D_GND			
B27	D_GND			
B31	D_GND			
B32	D_GND			
C1	D_GND			
C2	D_GND			
C3	Reserved(SGMII_0_TXP)	SGMII0 TX		
C4	Reserved(SGMII_0_TXN)	SGMII0 TX		
C5	VSYS	System 4.7-V Power Rail Feed-in		
C6	VSYS	System 4.7-V Power Rail Feed-in		
C7	VSIM1_PMU	Power for SIM1		
C8	VBUS	Detect of USB Power		
C9	Reserved(PWRKEY)	Power Key Trigger		1.8V
C10	KPCOLO	Forced Download Key	Pull-Up	
C11	PCIE0_CLKREQN	PCIe Clock Request	Pull-Up	1.8V
C12	SDA0	I2C0 Data	Pull-Up	1.8V
C13	D_GND			
C14	D_GND			
C15	D_GND			
C16	D_GND			
C17	D_GND			
C18	D_GND			
C19	D_GND			
C20	D_GND			
C21	PCIE_A_LN1_TXP	PCIe lane1 TX		
C22	D_GND			
C23	EINT40	External Interrupt Input	Pull-Down	1.8V
C24	Reserved(VCN18_PMU)	1V8 Power Output for External RF Components		1.8V
C25	D_GND			
C26	EINT211	External Interrupt Input	Pull-Down	1.8V
C27	EINT210	External Interrupt Input	Pull-Down	1.8V
C28	D_GND			
C29	D_GND			
C30	D_GND			
C31	D_GND			
C32	D_GND			
D1	Reserved(SGMII_0_RXP)	SGMII0 RX		
D2	Reserved(SGMII_0_RXN)	SGMII0 RX		
D3	D_GND			

D4	D_GND			
D5	D_GND			
D6	D_GND			
D7	D_GND			
D8	Reserved(SYSRSTB)	PMIC Reset Output		1.8V
D9	PMIC_RESET_B	Input to Reset NAD		1.8V
D10	PCIE0_PERSTN	PCIe reset	Pull-Up	1.8V
D11	PCIE0_PEWAKEN	PCIe Wake	Pull-Up	1.8V
D12	SCL0	I2C0 Clock	Pull-Up	1.8V
D13	D_GND			
D14	D_GND			
D15	D_GND			
D16	D_GND			
D17	D_GND			
D18	D_GND			
D19	PCIE_A_LN0_TXN	PCIe lane0 TX		
D20	PCIE_A_LN0_TXP	PCIe lane0 TX		
D21	PCIE_A_LN1_TXN	PCIe lane1 TX		
D22	D_GND			
D23	D_GND			
D24	D_GND			
D25	D_GND			
D26	EINT214	External Interrupt Input	Pull-Down	1.8V
D27	EINT209	External Interrupt Input	Pull-Down	1.8V
D28	D_GND			
D29	D_GND			
D30	D_GND			
D31	D_GND			
D32	D_GND			
E1	D_GND			
E2	D_GND			
E3	Reserved(SGMII_1_RXN)	SGMII1 RX		
E4	Reserved(SGMII_1_RXP)	SGMII1 RX		
E5	D_GND			
E6	D_GND			
E7	D_GND			
E8	D_GND			
E9	EINT78	External Interrupt Input	Pull-Down	1.8V
E10	EINT77	External Interrupt Input	Pull-Down	1.8V
E11	EINT75	External Interrupt Input	Pull-Down	1.8V
E12	EINT73	External Interrupt Input	Pull-Down	1.8V
E13	D_GND			
E14	D_GND			

E15	D_GND			
E16	D_GND			
E17	D_GND			
E18	D_GND			
E19	D_GND			
E20	D_GND			
E21	D_GND			
E22	D_GND			
E23	D_GND			
E24	D_GND			
E25	D_GND			
E26	EINT213	External Interrupt Input	Pull-Down	1.8V
E27	EINT212	External Interrupt Input	Pull-Down	1.8V
E28	EINT223	External Interrupt Input	Pull-Down	1.8V
E29	D_GND			
E30	D_GND			
E31	D_GND			
E32	D_GND			
F1	Reserved(SGMII_1_TXP)	SGMII1 TX		
F2	Reserved(SGMII_1_TXN)	SGMII1 TX		
F3	D_GND			
F4	SPI0_MO	SPI0 Data Out	Pull-Down	1.8V
F5	SPI0_CSB	SPI0 Chip Select	Pull-Down	1.8V
F6	D_GND			
F7	D_GND			
F8	EINT1	External Interrupt Input	Pull-Down	1.8V
F9	EINT74	External Interrupt Input	Pull-Down	1.8V
F10	EINT4	External Interrupt Input	Pull-Down	1.8V
F11	EINT0	External Interrupt Input	Pull-Down	1.8V
F12	EINT76	External Interrupt Input	Pull-Down	1.8V
F13	D_GND			
F14	D_GND			
F15	Reserved(EINT83)	Not Connected	Pull-Down	1.8V
F16	Reserved(EINT84)	Not Connected	Pull-Down	1.8V
F17	D_GND			
F18	D_GND			
F19	I2S2_LRCK	I2S2 Word Clock	Pull-Down	1.8V
F20	I2S2_MCK	I2S2 Master Clock	Pull-Down	1.8V
F21	I2S2_BCK	I2S2 Bit Clock	Pull-Down	1.8V
F22	I2S2_DI	I2S2 Data In	Pull-Down	1.8V
F23	I2S1_DO	I2S1 Data Out	Pull-Down	1.8V
F24	Reserved(EINT82)	External Interrupt Input	Pull-Down	1.8V
F25	Reserved(EINT81)	External Interrupt Input	Pull-Down	1.8V
F26	Reserved(EINT80)	External Interrupt Input	Pull-Down	1.8V

F27	Reserved(EINT79)	External Interrupt Input	Pull-Down	1.8V
F28	D_GND			
F29	D_GND			
F30	D_GND			
F31	D_GND			
F32	D_GND			
G1	D_GND			
G2	D_GND			
G3	D_GND			
G4	SPIO_MI	SPIO Data In	Pull-Down	1.8V
G5	SPIO_CLK	SPIO Clock	Pull-Down	1.8V
G6	D_GND			
G7	Reserved(SPI3_MO)	SPI3 Data Out	Pull-Down	1.8V
G8	D_GND			
G9	D_GND			
G10	EINT5	External Interrupt Input	Pull-Down	1.8V
G11	EINT7	External Interrupt Input	Pull-Down	1.8V
G12	D_GND			
G13	D_GND			
G14	D_GND			
G15	EINT177	External Interrupt Input	Pull-Down	1.8V
G16	EINT178	External Interrupt Input	Pull-Down	1.8V
G17	D_GND			
G18	D_GND			
G19	D_GND			
G20	D_GND			
G21	D_GND			
G22	EINT135	External Interrupt Input	Pull-Down	1.8V
G23	EINT134	External Interrupt Input	Pull-Down	1.8V
G24	EINT130	External Interrupt Input	Pull-Down	1.8V
G25	Reserved(EINT198)	External Interrupt Input	Pull-Down	1.8V
G26	Reserved(EINT197)	External Interrupt Input	Pull-Down	1.8V
G27	Reserved(EINT203)	External Interrupt Input	Pull-Down	1.8V
G28	D_GND			
G29	D_GND			
G30	I2S0_MCK	I2S0 Master Clock	Pull-Down	1.8V
G31	I2S0_LRCK	I2S0 Word Clock	Pull-Down	1.8V
G32	I2S0_DO	I2S0 Data Out	Pull-Down	1.8V
H1	D_GND			
H2	Reserved(VMC_PMU)	Power for MSDC1		
H3	EINT133	External Interrupt Input	Pull-Down	1.8V
H4	D_GND			
H5	D_GND			
H6	Reserved(SPI3_CSB)	SPI3 Chip Select	Pull-Down	1.8V

H7	Reserved(SPI3_MI)	SPI3 Data In	Pull-Down	1.8V
H8	D_GND			
H9	Reserved(BT_PRI_RXD)	Not Connected	Pull-Down	1.8V
H10	D_GND			
H11	Reserved(BT_ACT_TXD)	Not Connected	Pull-Down	1.8V
H12	D_GND			
H13	D_GND			
H14	D_GND			
H15	Reserved(AP_UTXD2)	UART TX	Pull-Down	1.8V
H16	Reserved(AP_URXD2)	UART RX	Pull-Down	1.8V
H17	EINT6	External Interrupt Input	Pull-Down	1.8V
H18	D_GND			
H19	D_GND			
H20	D_GND			
H21	D_GND			
H22	EINT144	External Interrupt Input	Pull-Down	1.8V
H23	EINT143	External Interrupt Input	Pull-Down	1.8V
H24	D_GND			
H25	Reserved(EINT199)	External Interrupt Input	Pull-Down	1.8V
H26	Reserved(EINT204)	External Interrupt Input	Pull-Down	1.8V
H27	Reserved(EINT200)	External Interrupt Input	Pull-Down	1.8V
H28	D_GND			
H29	D_GND			
H30	D_GND			
H31	I2S0_BCK	I2S0 Bit Clock	Pull-Down	1.8V
H32	I2S0_DI	I2S0 Data In	Pull-Down	1.8V
J1	D_GND			
J2	D_GND			
J3	Reserved(VMC_PMU)	Power for MSDC0		
J4	D_GND			
J5	D_GND			
J6	Reserved(SPI3_CLK)	SPI3 Clock	Pull-Down	1.8V
J7	EINT181	External Interrupt Input	Pull-Down	1.8V
J8	Reserved(AP_URXD3)	UART3 RX	Pull-Down	1.8V
J9	D_GND			
J10	Reserved(AP_UTXD3)	UART3 TX	Pull-Down	1.8V
J11	D_GND			
J12	D_GND			
J13	D_GND			
J14	D_GND			
J15	D_GND			
J16	D_GND			
J17	D_GND			
J18	D_GND			

J19	D_GND			
J20	D_GND			
J21	D_GND			
J22	D_GND			
J23	D_GND			
J24	D_GND			
J25	Reserved(EINT205)	External Interrupt Input	Pull-Down	1.8V
J26	Wake-up(EINT202)	External Interrupt Input; Be Activated High, External MCU wakes NAD Up	Pull-Down	1.8V
J27	Reserved(EINT201)	External Interrupt Input	Pull-Down	1.8V
J28	D_GND			
J29	D_GND			
J30	Wake-up(EINT165)	Output Interrupt Pin; SMS Wakes NAD Up, then NAD Wakes External MCU Up via Activating GPIO165 High	Pull-Down	1.8V
J31	Reserved(AP_URXD1)	UART RX	Pull-Down	1.8V
J32	Reserved(AP_UTXD1)	UART TX	Pull-Down	1.8V
K1	D_GND			
K2	SDA2	I2C2 Data	Pull-Up	1.8V
K3	SDA1	I2C1 Data	Pull-Up	1.8V
K4	D_GND			
K5	D_GND			
K6	D_GND			
K7	Reserved(EINT34)	Boot Strapping Signal. To be used as GPIO after boot up sequence completed	Pull-Down	1.8V
K8	D_GND			
K9	D_GND			
K10	D_GND			
K11	D_GND			
K12	D_GND			
K13	D_GND			
K14	D_GND			
K15	EINT170	External Interrupt Input	Pull-Up	1.8V
K16	EINT169	External Interrupt Input	Pull-Up	1.8V
K17	D_GND			
K18	D_GND			
K19	D_GND			
K20	D_GND			
K21	D_GND			
K22	D_GND			
K23	D_GND			
K24	D_GND			
K25	EINT31	External Interrupt Input	Pull-Down	1.8V
K26	EINT27	External Interrupt Input	Pull-Down	1.8V
K27	EINT30	External Interrupt Input	Pull-Down	1.8V
K28	D_GND			

K29	D_GND			
K30	Reserved(EINT164)	Not Connected	Pull-Down	1.8V
K31	EINT174	External Interrupt Input	Pull-Down	1.8V
K32	EINT173	External Interrupt Input	Pull-Down	1.8V
L1	D_GND			
L2	SCL2	I2C2 Clock	Pull-Up	1.8V
L3	SCL1	I2C1 Clock	Pull-Up	1.8V
L4	Reserved(EINT32)	Boot Strapping Signal. To be used as GPIO after boot up sequence completed	Pull-Down	1.8V
L5	D_GND			
L6	D_GND			
L7	EINT182	External Interrupt Input	Pull-Down	1.8V
L8	D_GND			
L9	D_GND			
L10	D_GND			
L11	D_GND			
L12	Reserved(SPI1_MO)	SPI1 Data Out	Pull-Down	1.8V
L13	Reserved(SPI1_CLK)	SPI1 Clock	Pull-Down	1.8V
L14	Reserved(SPI2_MO)	SPI2 Data Out	Pull-Down	1.8V
L15	D_GND			
L16	D_GND			
L17	D_GND			
L18	D_GND			
L19	EINT208	External Interrupt Input	Pull-Down	1.8V
L20	D_GND			
L21	D_GND			
L22	D_GND			
L23	D_GND			
L24	D_GND			
L25	EINT29	External Interrupt Input	Pull-Down	1.8V
L26	EINT26	External Interrupt Input	Pull-Down	1.8V
L27	EINT28	External Interrupt Input	Pull-Down	1.8V
L28	D_GND			
L29	D_GND			
L30	D_GND			
L31	D_GND			
L32	D_GND			
M1	D_GND			
M2	D_GND			
M3	Reserved(EINT99)	External Interrupt Input	Pull-Down	1.8V
M4	Reserved(EINT38)	Boot Strapping Signal. To be used as GPIO after boot up sequence completed	Pull-Down	1.8V
M5	Reserved(EINT33)	Boot Strapping Signal. To be used as GPIO after boot up sequence completed	Pull-Down	1.8V
M6	D_GND			
M7	D_GND			

M8	D_GND			
M9	D_GND			
M10	D_GND			
M11	D_GND			
M12	Reserved(SPI1_CSB)	SPI1 Chip Select	Pull-Down	1.8V
M13	Reserved(SPI1_MI)	SPI1 Data In	Pull-Down	1.8V
M14	Reserved(SPI2_MI)	SPI2 Data In	Pull-Down	1.8V
M15	D_GND			
M16	Reserved(SPI2_CLK)	SPI2 Clock	Pull-Down	1.8V
M17	Reserved(AUXIN3)	AUXADC CH3		
M18	D_GND			
M19	EINT207	External Interrupt Input	Pull-Down	1.8V
M20	D_GND			
M21	D_GND			
M22	D_GND			
M23	D_GND			
M24	D_GND			
M25	D_GND			
M26	D_GND			
M27	D_GND			
M28	D_GND			
M29	D_GND			
M30	D_GND			
M31	D_GND			
M32	D_GND			
N1	D_GND			
N2	D_GND			
N3	Reserved(EINT98)	External Interrupt Input	Pull-Down	1.8V
N4	Reserved(EINT35)	Boot Strapping Signal. To be used as GPIO after boot up sequence completed	Pull-Down	1.8V
N5	D_GND			
N6	GBE_RXD3	RGMII RX data3	Pull-Down	1.8V
N7	GBE_MDIO	Management Data I/O of RGMII	Pull-Down	1.8V
N8	GBE_TXD1	RGMII TX Data1	Pull-Down	1.8V
N9	D_GND			
N10	D_GND			
N11	D_GND			
N12	D_GND			
N13	Reserved(SPI2_CSB)	SPI2 Chip Select	Pull-Down	1.8V
N14	AP_URXD0	UART0 RX	Pull-Up	1.8V
N15	AP_UTXD0	UART0 TX	Pull-Up	1.8V
N16	Reserved(AUXIN1)	AUXADC CH1		
N17	Reserved(AUXIN2)	AUXADC CH2		
N18	Reserved(AUXIN0)	AUXADC CH0		

N19	EINT206	External Interrupt Input	Pull-Down	1.8V
N20	D_GND			
N21	D_GND			
N22	D_GND			
N23	D_GND			
N24	D_GND			
N25	Reserved(MSDC1_DAT0)	MSDC1 Data0	Pull-Down	1.8V
N26	Reserved(MSDC1_DAT1)	MSDC1 Data1	Pull-Down	1.8V
N27	Reserved(MSDC1_CMD)	MSDC1 Command	Pull-Down	1.8V
N28	D_GND			
N29	WATCHDOG		Pull-Down	1.8V
N30	D_GND			
N31	Reserved(EINT138)	External Interrupt Input	Pull-Down	1.8V
N32	EINT141	External Interrupt Input	Pull-Down	1.8V
P1	D_GND			
P2	D_GND			
P3	Reserved(EINT96)	External Interrupt Input	Pull-Down	1.8V
P4	Reserved(EINT36)	Boot Strapping Signal. To be used as GPIO after boot up sequence completed	Pull-Down	1.8V
P5	Reserved(EINT37)	Boot Strapping Signal. To be used as GPIO after boot up sequence completed	Pull-Down	1.8V
P6	GBE_RXD2	RGMII RX Data2	Pull-Down	1.8V
P7	GBE_RXD0	RGMII RX Data0	Pull-Down	1.8V
P8	GBE_RXDV	RGMII Receive Data Valid	Pull-Down	1.8V
P9	D_GND			
P10	D_GND			
P11	D_GND			
P12	D_GND			
P13	D_GND			
P14	D_GND			
P15	D_GND			
P16	D_GND			
P17	D_GND			
P18	D_GND			
P19	D_GND			
P20	D_GND			
P21	D_GND			
P22	D_GND			
P23	D_GND			
P24	D_GND			
P25	Reserved(MSDC1_DAT3)	MSDC1 Data3	Pull-Down	1.8V
P26	Reserved(MSDC1_CLK)	MSDC1 Clock	Pull-Down	1.8V
P27	Reserved(MSDC1_DAT2)	MSDC1 Data2	Pull-Down	1.8V
P28	D_GND			
P29	D_GND			

P30	D_GND			
P31	EINT140	External Interrupt Input	Pull-Down	1.8V
P32	Reserved(EINT139)	External Interrupt Input	Pull-Down	1.8V
R1	D_GND			
R2	D_GND			
R3	Reserved(EINT100)	External Interrupt Input	Pull-Down	1.8V
R4	D_GND			
R5	Reserved(EINT39)	Boot Strapping Signal. To be used as GPIO after boot up sequence completed	Pull-Down	1.8V
R6	GBE_MDC	Management Data Clock of RGMII	Pull-Down	1.8V
R7	GBE_COL	RGMII Collision	Pull-Down	1.8V
R8	GBE_TXC	RGMII TX Clock	Pull-Down	1.8V
R9	D_GND			
R10	D_GND			
R11	D_GND			
R12	D_GND			
R13	D_GND			
R14	D_GND			
R15	D_GND			
R16	D_GND			
R17	D_GND			
R18	D_GND			
R19	D_GND			
R20	D_GND			
R21	D_GND			
R22	D_GND			
R23	D_GND			
R24	D_GND			
R25	D_GND			
R26	D_GND			
R27	D_GND			
R28	D_GND			
R29	D_GND			
R30	D_GND			
R31	D_GND			
R32	D_GND			
S1	D_GND			
S2	D_GND			
S3	Reserved(EINT97)	External Interrupt Input	Pull-Down	1.8V
S4	D_GND			
S5	D_GND			
S6	GBE_TXEN	RGMII Transmit Enable	Pull-Down	1.8V
S7	GBE_TXD0	RGMII TX Data0	Pull-Down	1.8V
S8	GBE_INTR	RGMII Interrupt	Pull-Down	1.8V

S9	D_GND			
S10	D_GND			
S11	D_GND			
S12	D_GND			
S13	D_GND			
S14	D_GND			
S15	D_GND			
S16	D_GND			
S17	D_GND			
S18	D_GND			
S19	D_GND			
S20	D_GND			
S21	D_GND			
S22	D_GND			
S23	D_GND			
S24	D_GND			
S25	D_GND			
S26	D_GND			
S27	D_GND			
S28	D_GND			
S29	D_GND			
S30	D_GND			
S31	D_GND			
S32	D_GND			
T1	D_GND			
T2	D_GND			
T3	D_GND			
T4	D_GND			
T5	D_GND			
T6	GBE_RXD1	RGMII RX Data1	Pull-Down	1.8V
T7	GBE_RXER	RGMII RX Error	Pull-Down	1.8V
T8	GBE_TXD2	RGMII TX Data2	Pull-Down	1.8V
T9	D_GND			
T10	D_GND			
T11	D_GND			
T12	D_GND			
T13	D_GND			
T14	D_GND			
T15	D_GND			
T16	D_GND			
T17	D_GND			
T18	D_GND			
T19	D_GND			

T20	D_GND			
T21	D_GND			
T22	D_GND			
T23	D_GND			
T24	D_GND			
T25	D_GND			
T26	D_GND			
T27	D_GND			
T28	D_GND			
T29	VCC_VRF1	VRF1 4.2-V Power Rail Feed-in		
T30	VCC_VRF1	VRF1 4.2-V Power Rail Feed-in		
T31	VCC_VRF3	VRF3 4.7-V Power Rail Feed-in		
T32	VCC_VRF2	VRF2 4.7-V Power Rail Feed-in		
U3	D_GND			
U4	D_GND			
U5	D_GND			
U6	GBE_TXER	RGMII TX Error	Pull-Down	1.8V
U7	GBE_RXC	RGMII RX Clock	Pull-Down	1.8V
U8	GBE_TXD3	RGMII TX Data3	Pull-Down	1.8V
U9	D_GND			
U10	D_GND			
U11	D_GND			
U12	D_GND			
U13	D_GND			
U14	D_GND			
U15	D_GND			
U16	D_GND			
U17	D_GND			
U18	D_GND			
U19	D_GND			
U20	D_GND			
U21	D_GND			
U22	D_GND			
U23	D_GND			
U24	D_GND			
U25	D_GND			
U26	D_GND			
U27	D_GND			
U28	D_GND			
U29	VCC_VRF1	VRF1 4.2-V Power Rail Feed-in		
U30	VCC_VRF1	VRF1 4.2-V Power Rail Feed-in		
U31	VCC_VRF3	VRF3 4.7-V Power Rail Feed-in		
U32	VCC_VRF2	VRF2 4.7-V Power Rail Feed-in		

V3	D_GND			
V4	D_GND			
V5	D_GND			
V6	D_GND			
V7	D_GND			
V8	D_GND			
V9	D_GND			
V10	D_GND			
V11	D_GND			
V12	D_GND			
V13	D_GND			
V14	D_GND			
V15	D_GND			
V16	D_GND			
V17	D_GND			
V18	D_GND			
V19	D_GND			
V20	D_GND			
V21	D_GND			
V22	D_GND			
V23	D_GND			
V24	D_GND			
V25	D_GND			
V26	D_GND			
V27	D_GND			
V28	D_GND			
V29	D_GND			
V30	D_GND			
V31	D_GND			
V32	D_GND			
W3	D_GND			
W4	D_GND			
W5	D_GND			
W6	D_GND			
W7	D_GND			
W8	D_GND			
W9	D_GND			
W10	D_GND			
W11	D_GND			
W12	D_GND			
W13	D_GND			
W14	D_GND			
W15	D_GND			

W16	D_GND			
W17	D_GND			
W18	D_GND			
W19	D_GND			
W20	D_GND			
W21	D_GND			
W22	D_GND			
W23	D_GND			
W24	D_GND			
W25	D_GND			
W26	D_GND			
W27	D_GND			
W28	D_GND			
W29	D_GND			
W30	D_GND			
W31	D_GND			
W32	D_GND			
Y1	D_GND			
Y2	D_GND			
Y3	D_GND			
Y4	D_GND			
Y5	D_GND			
Y6	D_GND			
Y7	D_GND			
Y8	D_GND			
Y9	D_GND			
Y10	D_GND			
Y11	D_GND			
Y12	D_GND			
Y13	D_GND			
Y14	D_GND			
Y15	D_GND			
Y16	D_GND			
Y17	D_GND			
Y18	D_GND			
Y19	D_GND			
Y20	D_GND			
Y21	D_GND			
Y22	D_GND			
Y23	D_GND			
Y24	D_GND			
Y25	D_GND			
Y26	D_GND			

Y27	D_GND			
Y28	D_GND			
Y29	D_GND			
Y30	D_GND			
AA1	D_GND			
AA2	D_GND			
AA3	D_GND			
AA4	D_GND			
AA5	D_GND			
AA6	D_GND			
AA7	D_GND			
AA8	D_GND			
AA9	D_GND			
AA10	D_GND			
AA11	D_GND			
AA12	D_GND			
AA13	D_GND			
AA14	D_GND			
AA15	D_GND			
AA16	D_GND			
AA17	D_GND			
AA18	D_GND			
AA19	D_GND			
AA20	D_GND			
AA21	D_GND			
AA22	D_GND			
AA23	D_GND			
AA24	D_GND			
AA25	D_GND			
AA26	D_GND			
AA27	D_GND			
AA28	D_GND			
AA29	D_GND			
AA30	D_GND			
AB1	RF_GNSS_L1_ANT	RF GNSS Antenna		
AB2	D_GND			
AB3	D_GND			
AB4	D_GND			
AB5	D_GND			
AB6	D_GND			
AB7	D_GND			
AB8	D_GND			
AB9	D_GND			

AB10	D_GND			
AB11	D_GND			
AB12	D_GND			
AB13	D_GND			
AB14	D_GND			
AB15	D_GND			
AB16	D_GND			
AB17	D_GND			
AB18	D_GND			
AB19	D_GND			
AB20	D_GND			
AB21	D_GND			
AB22	D_GND			
AB23	D_GND			
AB24	D_GND			
AB25	D_GND			
AB26	D_GND			
AB27	D_GND			
AB28	D_GND			
AB29	D_GND			
AB30	D_GND			
AC1	D_GND			
AC2	D_GND			
AC3	D_GND			
AC4	D_GND			
AC5	D_GND			
AC6	D_GND			
AC7	D_GND			
AC8	D_GND			
AC9	D_GND			
AC10	D_GND			
AC11	D_GND			
AC12	D_GND			
AC13	D_GND			
AC14	D_GND			
AC15	D_GND			
AC16	D_GND			
AC17	D_GND			
AC18	D_GND			
AC19	D_GND			
AC20	D_GND			
AC21	D_GND			
AC22	D_GND			

AC23	D_GND			
AC24	D_GND			
AC25	D_GND			
AC26	D_GND			
AC27	D_GND			
AC28	D_GND			
AC29	D_GND			
AC30	D_GND			
AC31	D_GND			
AC32	D_GND			
AD1	D_GND			
AD2	D_GND			
AD3	D_GND			
AD4	D_GND			
AD5	D_GND			
AD6	D_GND			
AD7	D_GND			
AD8	D_GND			
AD9	D_GND			
AD10	D_GND			
AD11	D_GND			
AD12	D_GND			
AD13	D_GND			
AD14	D_GND			
AD15	D_GND			
AD16	D_GND			
AD17	D_GND			
AD18	D_GND			
AD19	D_GND			
AD20	D_GND			
AD21	D_GND			
AD22	D_GND			
AD23	D_GND			
AD24	D_GND			
AD25	D_GND			
AD26	D_GND			
AD27	D_GND			
AD28	D_GND			
AD29	D_GND			
AD30	D_GND			
AD31	D_GND			
AD32	D_GND			
AE1	D_GND			

AE2	D_GND			
AE3	D_GND			
AE4	D_GND			
AE5	D_GND			
AE6	D_GND			
AE7	D_GND			
AE8	D_GND			
AE9	D_GND			
AE10	D_GND			
AE11	D_GND			
AE12	D_GND			
AE13	D_GND			
AE14	D_GND			
AE15	D_GND			
AE16	D_GND			
AE17	D_GND			
AE18	D_GND			
AE19	D_GND			
AE20	D_GND			
AE21	D_GND			
AE22	D_GND			
AE23	D_GND			
AE24	D_GND			
AE25	D_GND			
AE26	D_GND			
AE27	D_GND			
AE28	D_GND			
AE29	D_GND			
AE30	D_GND			
AE31	D_GND			
AE32	D_GND			
AF1	D_GND			
AF2	D_GND			
AF3	D_GND			
AF4	D_GND			
AF5	D_GND			
AF6	D_GND			
AF7	D_GND			
AF8	D_GND			
AF9	D_GND			
AF10	D_GND			
AF11	D_GND			
AF12	D_GND			

AF13	D_GND			
AF14	D_GND			
AF15	D_GND			
AF16	D_GND			
AF17	D_GND			
AF18	D_GND			
AF19	D_GND			
AF20	D_GND			
AF21	D_GND			
AF22	D_GND			
AF23	D_GND			
AF24	D_GND			
AF25	D_GND			
AF26	D_GND			
AF27	D_GND			
AF28	D_GND			
AF29	D_GND			
AF30	D_GND			
AF31	D_GND			
AF32	D_GND			
AG1	D_GND			
AG2	D_GND			
AG3	D_GND			
AG4	D_GND			
AG5	D_GND			
AG6	D_GND			
AG7	D_GND			
AG8	D_GND			
AG9	D_GND			
AG10	D_GND			
AG11	D_GND			
AG12	D_GND			
AG13	D_GND			
AG14	D_GND			
AG15	D_GND			
AG16	D_GND			
AG17	D_GND			
AG18	D_GND			
AG19	D_GND			
AG20	D_GND			
AG21	D_GND			
AG22	D_GND			
AG23	D_GND			

AG24	D_GND			
AG25	D_GND			
AG26	D_GND			
AG27	D_GND			
AG28	D_GND			
AG29	D_GND			
AG30	D_GND			
AG31	D_GND			
AG32	D_GND			
AH1	D_GND			
AH2	D_GND			
AH3	D_GND			
AH4	RF-ANT3	RF Antenna; MIMO1 Receiving		
AH5	D_GND			
AH6	RF-ANT4	RF Antenna; MIMO2 Receiving		
AH7	D_GND			
AH8	D_GND			
AH9	D_GND			
AH10	D_GND			
AH11	D_GND			
AH12	D_GND			
AH13	RF-ANT2	RF Antenna; Diversity Receiving		
AH14	D_GND			
AH15	D_GND			
AH16	D_GND			
AH17	D_GND			
AH18	D_GND			
AH19	D_GND			
AH20	D_GND			
AH21	D_GND			
AH22	D_GND			
AH23	D_GND			
AH24	D_GND			
AH25	RF-ANT1	RF Antenna; Transmitting and Primary Receiving		
AH26	D_GND			
AH27	D_GND			
AH28	D_GND			
AH29	D_GND			
AH30	D_GND			
AH31	D_GND			
AH32	D_GND			

3. NAD SPECIFICATIONS

This chapter describes maximum ratings, operating condition, power on/off and reset timing

3.1 ABSOLUTE MAXIMUM RATINGS

Table 3.1-1

Parameter	Minimum	Maximum	Unit
Power-supply Voltages			
VSYS	-0.5	6	V
VRF1	-0.5	6	V
VRF2	-0.5	6	V
VRF3	-0.5	6	V
VSIM1_PMU	0	5	V
VSIM2_PMU	0	5	V
Signal Pins			
Digital power for I/O	-0.3	2.1	V
Thermal Conditions			
Ambient	-40	85	deg-C
Environmental			
Operating Humidity	-	85	%RH

3.2 OPERATING CONDITIONS

Table 3.2-1

Parameter		Minimum	Typical	Maximum	Unit
Power-supply Voltages					
VSYS	System 4.7-V Power Rail Feed-in	4.5	4.7	4.9	V
VBUS	Detect of USB Power	4.75	5	5.25	V
VRF1	RFFE Supply Voltage1	4.0	4.2	4.4	V
VRF2	RFFE Supply Voltage2	4.5	4.7	4.9	V
VRF3	RFFE Supply Voltage3	4.5	4.7	4.9	V
VSIM1_PMU	Output Voltage for UIM1	1.82	1.86	1.90	V
		2.94	3.00	3.06	V
VSIM2_PMU	Output Voltage for UIM2	1.82	1.86	1.90	V
		2.94	3.00	3.06	V
Power-supply Currents					
NAD OFF	OFF mode	n/a	120	n/a	uA

LPM(AIR1)	Airplane mode	n/a	5.8	n/a	mA
Standby(GS1)	GSM standby GSM900 DRX-3(0.706 sec)	n/a	4.69	n/a	mA
Standby(WS1)	WCDMA Band1 standby DRX-7(1.28 sec)	n/a	4.43	n/a	mA
Standby(WS2)	WCDMA Band1 standby DRX-9(5.12 sec)	n/a	4.34	n/a	mA
Standby(LS3)	LTE Band1 standby DRX-64(0.64 sec)	n/a	5.13	n/a	mA
Standby(5GSUB6-C01)	NR Sub6 TDD 1CC 100-MHz CDRX and LTE CDRX	n/a	12.57	n/a	mA
Talk(GT1)	GSM talk 5-dBm, no DTX, PGSM	n/a	121.2	310	mA
Talk(WT1)	WCDMA talk FET on 0% voice	n/a	200.8	400	mA
Talk(VoLTE1)	VoLTE FDD(40-ms DRX cycle, 0-dBm, MIMO, Band13)	n/a	326	624	mA
Talk(VoLTE6)	VoLTE TDD(40-ms DRX cycle, 0-dBm, MIMO, Band38)	n/a	311	561	mA
Talk(VoNR1)	VoNR FDD	n/a	398	643	mA
Talk(VoNR6)	VoNR TDD	n/a	323	577	mA
Link(HS61E)	DC HSDPA downlink 42-Mbps/0-dBm, IMT(No RxD)	n/a	232.1	448	mA
Thermal Conditions	*be extended to 95 for eCall				
	NAD operating temperature(ambient)	-40	25	85*	degree-C
	3GPP operating temperature(ambient)	-30	25	70	degree-C

3.3 POWER-SUPPLY SEQUENCES

3.3.1 Power on sequences

Refer to the latest document of AIC-FFN_NAD_Design-Guide

3.3.2 Power off sequences

Refer to the latest document of AIC-FFN_NAD_Design-Guide

3.3.3 Reset sequences

Refer to the latest document of AIC-FFN_NAD_Design-Guide

3.4 AIR INTERFACE NETWORKING

Listed here are all combinations defined in 3GPP Release 15(relative to LTE)/16(relative to NR), and then showing the compliance table of each section according the hardware capability of UMC-STD35FFx

3.4.1 LTE receiving CA supporting list

Table 3.4-1 UMC-STD35FFN

Band Combination Downlink
CA_12A_12A
CA_12A_25A
CA_12A_25A
CA_12A_30A
CA_12A_30A_66A
CA_12A_30A_66A
CA_12A_66A
CA_12A_66A
CA_12A_66A_66A
CA_12A_66A_66A
CA_12B
CA_13A_66A
CA_13A_66A
CA_13A_66A_66A
CA_13A_66A_66A
CA_14A_30A
CA_14A_66A
CA_14A_66A_66A
CA_14A_66A_66A
CA_25A_25A_26A
CA_25A_25A_26A
CA_25A_25A_41A
CA_25A_25A_41A
CA_25A_26A
CA_25A_26A
CA_25A_26A_41A
CA_25A_26A_41A
CA_25A_26A_41A
CA_25A_41A
CA_25A_41A
CA_26A_41A
CA_26A_41A
CA_29A_30A_66A
CA_29A_66A
CA_29A_66A_66A
CA_2A_2A_12A_66A_66A
CA_2A_2A_13A_66A_66A

CA_2A_2A_5A_66A_66A
CA_2A_12A
CA_2A_12A
CA_2A_12A_30A
CA_2A_12A_30A
CA_2A_12A_66A
CA_2A_12A_66A
CA_2A_12A_66A
CA_2A_12A_66A_66A
CA_2A_12A_66A_66A
CA_2A_12A_66A_66A
CA_2A_13A
CA_2A_13A
CA_2A_13A_66A
CA_2A_13A_66A
CA_2A_13A_66A
CA_2A_13A_66A_66A
CA_2A_13A_66A_66A
CA_2A_13A_66A_66A
CA_2A_14A
CA_2A_14A
CA_2A_14A_30A
CA_2A_14A_30A
CA_2A_14A_66A
CA_2A_14A_66A
CA_2A_14A_66A
CA_2A_17A
CA_2A_17A
CA_2A_29A
CA_2A_29A_30A
CA_2A_29A_66A
CA_2A_29A_66A
CA_2A_2A
CA_2A_2A_12A
CA_2A_2A_12A
CA_2A_2A_12A_66A_66A
CA_2A_2A_12A_66A_66A
CA_2A_2A_12A_66A
CA_2A_2A_12A_66A
CA_2A_2A_12A_66A
CA_2A_2A_13A

CA_2A_2A_13A
CA_2A_2A_13A_66A_66A
CA_2A_2A_13A_66A_66A
CA_2A_2A_13A_66A
CA_2A_2A_13A_66A
CA_2A_2A_13A_66A
CA_2A_2A_14A
CA_2A_2A_14A
CA_2A_2A_29A
CA_2A_2A_30A
CA_2A_2A_4A
CA_2A_2A_4A
CA_2A_2A_4A_12A
CA_2A_2A_4A_12A
CA_2A_2A_4A_12A
CA_2A_2A_4A_4A
CA_2A_2A_4A_4A
CA_2A_2A_4A_5A
CA_2A_2A_4A_5A
CA_2A_2A_4A_5A
CA_2A_2A_4A_71A
CA_2A_2A_4A_71A
CA_2A_2A_4A_71A
CA_2A_2A_5A
CA_2A_2A_5A
CA_2A_2A_5A_66A_66A
CA_2A_2A_5A_66A_66A
CA_2A_2A_5A_66A
CA_2A_2A_5A_66A
CA_2A_2A_5A_66A
CA_2A_2A_66A
CA_2A_2A_66A
CA_2A_2A_66A_66A
CA_2A_2A_66A_66A
CA_2A_2A_66A_71A
CA_2A_2A_66A_71A
CA_2A_2A_66A_71A
CA_2A_2A_71A
CA_2A_2A_71A
CA_2A_2A_7A_12A_66A
CA_2A_2A_7A

CA_2A_2A_7A
CA_2A_2A_7A_12A
CA_2A_2A_7A_12A
CA_2A_2A_7A_12A
CA_2A_2A_7A_12A_66A
CA_2A_2A_7A_12A_66A
CA_2A_2A_7A_12A_66A
CA_2A_2A_7A_66A
CA_2A_2A_7A_66A
CA_2A_2A_7A_66A
CA_2A_30A
CA_2A_30A_66A
CA_2A_30A_66A
CA_2A_4A
CA_2A_4A
CA_2A_4A_12A
CA_2A_4A_12A
CA_2A_4A_12A
CA_2A_4A_13A
CA_2A_4A_13A
CA_2A_4A_13A
CA_2A_4A_29A
CA_2A_4A_29A
CA_2A_4A_30A
CA_2A_4A_30A
CA_2A_4A_4A
CA_2A_4A_4A
CA_2A_4A_4A_12A
CA_2A_4A_4A_12A
CA_2A_4A_4A_12A
CA_2A_4A_4A_5A
CA_2A_4A_4A_5A
CA_2A_4A_4A_5A
CA_2A_4A_5A
CA_2A_4A_5A
CA_2A_4A_5A
CA_2A_4A_71A
CA_2A_4A_71A
CA_2A_4A_71A
CA_2A_4A_7A
CA_2A_4A_7A

CA_2A_4A_7A
CA_2A_4A_7A_12A
CA_2A_4A_7A_12A
CA_2A_4A_7A_12A
CA_2A_4A_7A_12A
CA_2A_4A_7A_7A
CA_2A_4A_7A_7A
CA_2A_4A_7A_7A
CA_2A_5A
CA_2A_5A
CA_2A_5A_30A
CA_2A_5A_30A
CA_2A_5A_66A
CA_2A_5A_66A
CA_2A_5A_66A
CA_2A_5A_66A_66A
CA_2A_5A_66A_66A
CA_2A_5A_66A_66A
CA_2A_5A_7A
CA_2A_5A_7A
CA_2A_5A_7A
CA_2A_66A
CA_2A_66A
CA_2A_66A_66A_71A
CA_2A_66A_66A_71A
CA_2A_66A_66A_71A
CA_2A_66A_71A
CA_2A_66A_71A
CA_2A_66A_71A
CA_2A_71A
CA_2A_71A
CA_2A_7A
CA_2A_7A
CA_2A_7A_12A
CA_2A_7A_12A
CA_2A_7A_12A
CA_2A_7A_12A_66A
CA_2A_7A_12A_66A
CA_2A_7A_12A_66A
CA_2A_7A_12A_66A
CA_2A_7A_66A

CA_2A_7A_66A
CA_2A_7A_66A
CA_2A_7A_66A_66A
CA_2A_7A_66A_66A
CA_2A_7A_66A_66A
CA_2A_7A_7A
CA_2A_7A_7A
CA_2A_7A_7A_66A
CA_2A_7A_7A_66A
CA_2A_7A_7A_66A
CA_2C
CA_30A_66A
CA_30A_66A_66A
CA_41A_41A
CA_41C
CA_4A_12A
CA_4A_12A
CA_4A_12A_30A
CA_4A_12A_30A
CA_4A_13A
CA_4A_13A
CA_4A_17A
CA_4A_17A
CA_4A_29A
CA_4A_29A_30A
CA_4A_30A
CA_4A_4A
CA_4A_4A_12A
CA_4A_4A_12A
CA_4A_4A_13A
CA_4A_4A_13A
CA_4A_4A_29A
CA_4A_4A_30A
CA_4A_4A_5A
CA_4A_4A_5A
CA_4A_4A_71A
CA_4A_4A_71A
CA_4A_4A_7A
CA_4A_4A_7A
CA_4A_5A
CA_4A_5A

CA_4A_5A_30A
CA_4A_5A_30A
CA_4A_71A
CA_4A_71A
CA_4A_7A
CA_4A_7A
CA_4A_7A_12A
CA_4A_7A_12A
CA_4A_7A_12A
CA_4A_7A_7A
CA_4A_7A_7A
CA_5A_25A
CA_5A_25A
CA_5A_30A
CA_5A_30A_66A
CA_5A_30A_66A
CA_5A_30A_66A_66A
CA_5A_41A
CA_5A_41A
CA_5A_5A_66A
CA_5A_5A_66A
CA_5A_5A_66A_66A
CA_5A_5A_66A_66A
CA_5A_66A
CA_5A_66A
CA_5A_66A_66A
CA_5A_66A_66A
CA_5A_7A
CA_5A_7A
CA_5A_7A_66A
CA_5A_7A_66A
CA_5A_7A_66A
CA_5A_7A_66A_66A
CA_5A_7A_66A_66A
CA_5A_7A_66A_66A
CA_5A_7A_7A
CA_5A_7A_7A
CA_5B
CA_66A_66A
CA_66A_66A_66A
CA_66A_66A_71A

CA_66A_66A_71A
CA_66A_71A
CA_66A_71A
CA_66B
CA_66C
CA_66D
CA_7A_12A
CA_7A_12A
CA_7A_12A_66A
CA_7A_12A_66A
CA_7A_12A_66A
CA_7A_26A
CA_7A_26A
CA_7A_66A
CA_7A_66A
CA_7A_66A_66A
CA_7A_66A_66A
CA_7A_7A
CA_7A_7A_26A
CA_7A_7A_26A
CA_7A_7A_66A
CA_7A_7A_66A
CA_7A_7A_66A_66A
CA_7A_7A_66A_66A
CA_7C
CA_12A_30A_66A_66A
CA_12A_30A_66A_66A
CA_29A_30A_66A_66A
CA_2A_12A_30A_66A_66A
CA_2A_12A_30A_66A_66A
CA_2A_12A_30A_66A_66A
CA_2A_12A_30A_66A
CA_2A_12A_30A_66A
CA_2A_12A_30A_66A
CA_2A_29A_30A_66A
CA_2A_29A_30A_66A
CA_2A_2A_12A_30A_66A
CA_2A_2A_12A_30A_66A
CA_2A_2A_12A_30A_66A
CA_2A_2A_12A_30A
CA_2A_2A_12A_30A

CA_2A_2A_29A_30A
CA_2A_2A_30A_66A
CA_2A_2A_30A_66A
CA_2A_2A_5A_30A_66A
CA_2A_2A_5A_30A_66A
CA_2A_2A_5A_30A_66A
CA_2A_2A_5A_30A
CA_2A_2A_5A_30A
CA_2A_30A_66A_66A
CA_2A_30A_66A_66A
CA_2A_5A_30A_66A
CA_2A_5A_30A_66A
CA_2A_5A_30A_66A

3.4.2 NR receiving CA supporting list

Table 3.4-2 UMC-STD35FFN

Band Combination Downlink
CA_n41A_n78A
CA_n41A_n78A
CA_n41C
CA_n77C
CA_n78C
CA_n41A_n78A
CA_n41A_n78A
CA_n2A_n2A
CA_n2A_n5A
CA_n2A_n5A
CA_n2A_n66A
CA_n2A_n66A
CA_n2A_n77A
CA_n2A_n77A
CA_n5A_n66A
CA_n5A_n66A
CA_n5A_n77A
CA_n5A_n77A
CA_n5B
CA_n66A_n66A
CA_n66A_n77A
CA_n66A_n77A

3.4.3 EN-DC supporting list

Table 3.4-3 UMC-STD35FFN

Band Combination Downlink	Uplink Band
DC_12A_66A_n78A	DC_12A_n78A
DC_12A_66A_n78A	DC_66A_n78A
DC_12A_n66A	DC_12A_n66A
DC_12A_n78A	DC_12A_n78A
DC_12A_n7A	DC_12A_n7A
DC_13A_66A_66A_n77A	DC_13A_n77A
DC_13A_66A_66A_n77A	DC_66A_n77A
DC_13A_66A_n2A	DC_13A_n2A
DC_13A_n2A	DC_13A_n2A
DC_13A_n66A	DC_13A_n66A
DC_13A_n77A	DC_13A_n77A
DC_26A_n41A	DC_26A_n41A
DC_2A_2A_66A_66A_n5A	DC_66A_n5A
DC_2A_2A_66A_66A_n71A	DC_66A_n71A
DC_2A_5A_7A_7A_n66A	DC_5A_n66A
DC_2A_7A_71A_n66A	DC_71A_n66A
DC_2A_12A_n78A	DC_12A_n78A
DC_2A_12A_n78A	DC_2A_n78A
DC_2A_13A_66A_n77A	DC_13A_n77A
DC_2A_13A_66A_n77A	DC_2A_n77A
DC_2A_13A_66A_n77A	DC_66A_n77A
DC_2A_13A_n66A	DC_13A_n66A
DC_2A_13A_n77A	DC_13A_n77A
DC_2A_13A_n77A	DC_2A_n77A
DC_2A_2A_12A_n66A	DC_12A_n66A
DC_2A_2A_5A_n66A	DC_5A_n66A
DC_2A_2A_66A_66A_n5A	DC_2A_n5A
DC_2A_2A_66A_66A_n71A	DC_2A_n71A
DC_2A_2A_66A_n71A	DC_2A_n71A
DC_2A_2A_66A_n71A	DC_66A_n71A
DC_2A_2A_66A_n77A	DC_2A_n77A
DC_2A_2A_66A_n77A	DC_66A_n77A
DC_2A_2A_7A_12A_n66A	DC_12A_n66A
DC_2A_2A_7A_66A_n71A	DC_66A_n71A
DC_2A_2A_7A_66A_n71A	DC_2A_n71A

DC_2A_2A_7A_66A_n71A	DC_7A_n71A
DC_2A_2A_7A_n71A	DC_2A_n71A
DC_2A_2A_7A_n71A	DC_7A_n71A
DC_2A_2A_n5A	DC_2A_n5A
DC_2A_2A_n71A	DC_2A_n71A
DC_2A_2A_n77A	DC_2A_n77A
DC_2A_2A_n78A	DC_2A_n78A
DC_2A_5A_n77A	DC_2A_n77A
DC_2A_5A_n77A	DC_5A_n77A
DC_2A_66A_66A_n71A	DC_2A_n71A
DC_2A_66A_66A_n71A	DC_66A_n71A
DC_2A_66A_66A_n77A	DC_2A_n77A
DC_2A_66A_66A_n77A	DC_66A_n77A
DC_2A_66A_n71B	DC_2A_n71A
DC_2A_66A_n71B	DC_66A_n71A
DC_2A_66A_n78A	DC_2A_n78A
DC_2A_66A_n78A	DC_66A_n78A
DC_2A_66C_n71A	DC_2A_n71A
DC_2A_66C_n71A	DC_66A_n71A
DC_2A_7A_66A_n71A	DC_2A_n71A
DC_2A_7A_66A_n71A	DC_66A_n71A
DC_2A_7A_66A_n71A	DC_7A_n71A
DC_2A_7A_71A_n66A	DC_71A_n66A
DC_2A_7A_n77A	DC_2A_n77A
DC_2A_7A_n78A	DC_2A_n78A
DC_2A_7A_n78A	DC_7A_n78A
DC_2A_n66A_n71A	DC_2A_n71A
DC_2A_n71B	DC_2A_n71A
DC_2A_n71B	DC_2A_n71B
DC_5A_30A_66A_66A_n2A	DC_5A_n2A
DC_5A_66A_n77A	DC_5A_n77A
DC_5A_66A_n77A	DC_66A_n77A
DC_5A_7A_66A_n2A	DC_5A_n2A
DC_5A_n2A	DC_5A_n2A
DC_5A_n41A	DC_5A_n41A
DC_5A_n66A	DC_5A_n66A
DC_5A_n77A	DC_5A_n77A
DC_5A_n7A	DC_5A_n7A
DC_66A_n71B	DC_66A_n71A
DC_66A_66A_n71A	DC_66A_n71A
DC_66A_66A_n77A	DC_66A_n77A

DC_66A_n71B	DC_66A_n71A
DC_66A_n71B	DC_66A_n71B
DC_66C_n71A	DC_66A_n71A
DC_71A_n2A	DC_71A_n2A
DC_71A_n41A	DC_71A_n41A
DC_71A_n78A	DC_71A_n78A
DC_7A_12A_66A_n2A	DC_12A_n2A
DC_7A_12A_n78A	DC_12A_n78A
DC_7A_12A_n78A	DC_7A_n78A
DC_7A_66A_71A_n2A	DC_71A_n2A
DC_7A_66A_n77A	DC_66A_n77A
DC_7A_66A_n77A	DC_7A_n77A
DC_7A_7A_n77A	DC_7A_n77A
DC_7A_7A_n78A	DC_7A_n78A
DC_7A_n71A	DC_7A_n71A
DC_7C_n78A	DC_7A_n78A
DC_13A_66A_n77C	DC_13A_n77A
DC_13A_66A_n77C	DC_66A_n77A
DC_13A_66B_n2A	DC_13A_n2A
DC_13A_66C_n2A	DC_13A_n2A
DC_13A_n77C	DC_13A_n77A
DC_2A_13A_n77C	DC_13A_n77A
DC_2A_13A_n77C	DC_2A_n77A
DC_2A_2A_n77C	DC_2A_n77A
DC_2A_5A_7A_n66A	DC_5A_n66A
DC_2A_5A_n77C	DC_2A_n77A
DC_2A_5A_n77C	DC_5A_n77A
DC_2A_66A_n77C	DC_2A_n77A
DC_2A_66A_n77C	DC_66A_n77A
DC_2A_66B_n5A	DC_2A_n5A
DC_2C_66A_n71A	DC_2A_n71A
DC_2C_66A_n71A	DC_66A_n71A
DC_2C_n71A	DC_2A_n71A
DC_5A_66A_66A_n2A	DC_5A_n2A
DC_5A_66A_66A_n77A	DC_5A_n77A
DC_5A_66A_66A_n77A	DC_66A_n77A
DC_5A_66A_n77C	DC_5A_n77A
DC_5A_66A_n77C	DC_66A_n77A
DC_5A_n77C	DC_5A_n77A
DC_66A_66A_n77C	DC_66A_n77A
DC_66C_n5A	DC_66A_n5A

3.4.4 RF transmitting output power

Table 3.4-4

Item	Bands	Minimum	Typical	Maximum	Unit
Maximum Output Power					
5G NR	FR1 Sub-6G bands	21	23	25	dBm
5G NR HPUE	n41 / n77 for NA variant n78 for RW variant	24	26	-	dBm
LTE	All bands	21	23	25	dBm
WCDMA	All bands	21	24	26	dBm
Minimum Output Power					
5G NR	FR1 Sub-6G bands(Bandwidth < 20-MHz)	-	-	-40	dBm
LTE	All bands	-	-	-40	dBm
WCDMA	All bands	-	-	-50	dBm

3.4.5 RF receiving sensitivity

Table 3.4-5 UMC-STD35FFN

RAT	Bands	Minimum	Typical	Maximum	Unit
NR Receiving Sensitivity(Two antenna port)					
5G NR	n2(BW: 20-MHz, SCS: 15-kHz)	-	-	-91.1	dBm
5G NR	n5(BW: 10-MHz, SCS: 15-kHz)	-	-	-94.1	dBm
5G NR	n7(BW: 20-MHz, SCS: 15-kHz)	-	-	-91.1	dBm
5G NR	n41(BW: 100-MHz, SCS: 30-kHz)	-	-	-84	dBm
5G NR	n66(BW: 20-MHz, SCS: 15-kHz)	-	-	-92.6	dBm
5G NR	n77(BW: 100-MHz, SCS: 30-kHz)	-	-	-84.4	dBm
5G NR	n78(BW: 100-MHz, SCS: 30-kHz)	-	-	-84.9	dBm
NR Receiving Sensitivity(Four antenna port)					
5G NR	n2(BW: 20-MHz, SCS: 15-kHz)	-	-	-93.8	dBm
5G NR	n7(BW: 20-MHz, SCS: 15-kHz)	-	-	-93.8	dBm
5G NR	n41(BW: 100-MHz, SCS: 30-kHz)	-	-	-86.7	dBm
5G NR	n66(BW: 20-MHz, SCS: 15-kHz)	-	-	-95.3	dBm
5G NR	n77(BW: 100-MHz, SCS: 30-kHz)	-	-	-86.6	dBm
5G NR	n78(BW: 100-MHz, SCS: 30-kHz)	-	-	-87.1	dBm
LTE Receiving Sensitivity					
LTE	Band2(BW: 10-MHz)	-	-	-94.3	dBm
LTE	Band4(BW: 10-MHz)	-	-	-96.3	dBm
LTE	Band5(BW: 10-MHz)	-	-	-94.3	dBm
LTE	Band7(BW: 10-MHz)	-	-	-94.3	dBm
LTE	Band12(BW: 10-MHz)	-	-	-93.3	dBm
LTE	Band13(BW: 10-MHz)	-	-	-93.3	dBm

LTE	Band14(BW: 10-MHz)	-	-	-93.3	dBm
LTE	Band17(BW: 10-MHz)	-	-	-93.3	dBm
LTE	Band25(BW: 10-MHz)	-	-	-92.8	dBm
LTE	Band29(BW: 10-MHz)	-	-	-93.3	dBm
LTE	Band30(BW: 10-MHz)	-	-	-95.3	dBm
LTE	Band41(BW: 10-MHz)	-	-	-94.3	dBm
LTE	Band66(BW: 10-MHz)	-	-	-95.8	dBm
LTE	Band71(BW: 10-MHz)	-	-	-93.5	dBm
WCDMA Receiving Sensitivity					
WCDMA	Band2	-	-	-104.7	dBm
WCDMA	Band4	-	-	-106.7	dBm
WCDMA	Band5	-	-	-104.7	dBm

3.4.6 GNSS receiving performance

GNSS performance is tested with the external LNA(Low Noise Amplifier)

Table 3.4-6

Item	Parameter	Minimum	Typical	Maximum	Unit
Sensitivity	Tracking	-	-163	-	dBm
	Cold start acquisition	-	-146	-	dBm
	Hot start acquisition	-	-155	-	dBm
TTFF	Cold start	-	33	-	s
	Warm tart	-	32	-	s
	Hot start	-	1	-	s
Accuracy	Horizontal(CEP-50)	-	4.5	-	m

3.4.7 SRS switching time

Item	Bands	Minimum	Typical	Maximum	Unit
1T2R NR SA	n41	-	-	2	ms
	n77	-	-	2	ms
	n78	-	-	2	ms

3.5 DC AND AC CHARACTERISTIC

3.5.1 I2S DC electrical characteristic

Table 3.5-1 I2S DC Electrical Characteristics(VIO18 = 1.8V)

Parameter	Description	Min.	Typ.	Max.	Unit
VIH	Input logic high voltage	0.65*VIO18	-	VIO18 + 0.3	V
VIL	Input logic low voltage	-0.3	-	0.35*VIO18	V
VOH	DC output logic high voltage	0.75*VIO18	-	1.84	V
VOL	DC output logic low voltage	0	-	0.25*VIO18	V

Table 3.5-2 I2S AC Electrical Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
Fs	Sampling frequency	8	-	192	KHz
fMCK	Master clock frequency	0.768	-	49.152	MHz
fBCK	Serial clock frequency	32*fs	-	64*fs	MHz
tBCK_H	BCK high-level time	-	0.5	-	1/fBCK
tBCK_L	BCK low-level time	-	0.5	-	1/fBCK
tV_WS	Output delay time BCLK low to LRCK valid	-	-	13	ns
tV_DO	Output delay time BCK low to SDOUT valid	-	-	13	ns
tS_DI	DI setup time	16	-	-	ns
tH_DI	DI hold time	16	-	-	ns

3.5.2 SPI electrical characteristics

Table 3.5-3 SPI DC Electrical Characteristics(VIO18 = 1.8V)

Parameter	Description	Min.	Typ.	Max.	Unit
VIH	Input logic high voltage	0.65*VIO18	-	VIO18 + 0.3	V
VIL	Input logic low voltage	-0.3	-	0.35*VIO18	V
VOH	DC output logic high voltage	0.75*VIO18	-	1.84	V
VOL	DC output logic low voltage	0	-	0.25*VIO18	V

Table 3.5-4 SPI AC Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
f _{sck}	SPI master SCK Clock frequency	-	-	52	MHz
t _{MOSI_SU}	MOSI to SCK rising setup time	7.1	-	-	ns
t _{MOSI_HD}	SCK rising to MOSI hold time	7.1	-	-	ns
t _{SCKL}	SCK low pulse	7.2	-	-	ns
t _{SCKH}	SCK high pulse	7.1	-	-	ns
t _{CSB_SU}	CSB falling to SCK rising setup time	7.1	-	-	ns
t _{CSB_HD}	CSB falling to SCK rising hold time	7.1	-	-	ns

3.5.3 I2C electrical characteristics

Table 3.5-5 I2C DC Electrical Characteristics(VIO18 = 1.8V)

Parameter	Description	Min.	Typ.	Max.	Unit
VIH	Input logic high voltage	0.65*VIO18	-	VIO18 + 0.3	V
VIL	Input logic low voltage	-0.3	-	0.35*VIO18	V
VOH	DC output logic high voltage	0.75*VIO18	-	1.84	V
VOL	DC output logic low voltage	0	-	0.2*VIO18	V

Table 3.5-6 I2C AC Timing Parameters

Symbol	Parameter	Standard-mode		Fast-mode		Fast-mode Plus		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f _{scl}	SCL clock frequency	0	100	0	400	0	1000	KHz
t _{HD,STA}	Hold time(repeater) START condition	4	-	0.6	-	0.26	-	us
t _{LOW}	LOW period of SCL clock	4.7	-	1.3	-	0.5	-	us
t _{HIGH}	HIGH period of SCL clock	4	-	0.6	-	0.26	-	us

$t_{SU,STA}$	Set-up time for repeated START condition	4.7	-	0.6	-	0.26	-	us
$t_{HD,DAT}$	Data hold time	0	-	0	-	0	-	us
$t_{SU,DAT}$	Data set-up time	250	-	100	-	50	-	ns
t_r	Rise time of both SDA and SCL signals	-	1000	20	300	-	120	ns
t_f	Fall time of both SDA and SCL signals	-	300	20*(VD D/5.5V)	300	20*(VD D/5.5V)	120	ns
$t_{SU,STD}$	Set-up time for STOP condition	4	-	0.6	-	0.26	-	us
$t_{VD,DAT}$	Data valid time	-	3.45	-	0.9	-	0.45	us
$t_{VD,ACK}$	Data valid acknowledge time	-	3.45	-	0.9	-	0.45	us

3.5.4 MSDC1 electrical characteristics

Table 3.5-7 MSDC1 DC Electrical Characteristics(VIO33 = 3.3V)

Parameter	Description	Min.	Typ.	Max.	Unit
V _{IH}	Input logic high voltage	0.625*VIO33	-	VIO33 + 0.3	V
V _{IL}	Input logic low voltage	-0.3	-	0.25*VIO33	V
V _{OH}	DC output logic high voltage	0.75*VIO33	-	VIO33 + 0.3	V
V _{OL}	DC output logic low voltage	-0.3	-	0.125*VIO33	V

Table 3.5-8 MSDC1 DC Electrical Characteristics(VIO18 = 1.8V)

Parameter	Description	Min.	Typ.	Max.	Unit
V _{IH}	Input logic high voltage	1.27	-	VIO18 + 0.3	V
V _{IL}	Input logic low voltage	-0.3	-	0.58	V
V _{OH}	DC output logic high voltage	1.4	-	1.84	V
V _{OL}	DC output logic low voltage	0	-	0.45	V

Table 3.5-9 MSDC1 AC Timing Diagram Parameters of High Speed

Parameter	Description	Min.	Max.	Unit
Clock CLK				
t_{pp}	Clock frequency data transfer mode	0	50	MHz
t_{WL}	Clock low time	7	-	ns
t_{WH}	Clock high time	7	-	ns
t_{TLH}	Clock rise time	-	3	ns
t_{THL}	Clock fall time	-	3	ns
Input CMD, DAT(referred to CLK)				
t_{ISU}	Input setup time	6	-	ns
t_{IH}	Input hold time	2	-	ns
Output CMD, DAT(referred to CLK)				
t_{QDLY}	Output delay time during data transfer mode	-	14	ns
t_{Qh}	Output hold time	2.5	-	ns

3.5.5 SIM electrical characteristics

Table 3.5-10 SIM DC Electrical Characteristics(VIO30 = 3.0V)

Parameter	Description	Min.	Typ.	Max.	Unit
V _{IH}	Input logic high voltage	2.6	-	3.3	V
V _{IL}	Input logic low voltage	-0.3	-	0.4	V
V _{OH}	DC output logic high voltage	2.6	-	3.1	V
V _{OL}	DC output logic low voltage	0	-	0.4	V

Table 3.5-11 SIM DC Electrical Characteristics(VIO18 = 1.8V)

Parameter	Description	Min.	Typ.	Max.	Unit
VIH	Input logic high voltage	1.4	-	2.1	V
VIL	Input logic low voltage	-0.3	-	0.27	V
VOH	DC output logic high voltage	1.4	-	1.9	V
VOL	DC output logic low voltage	0	-	0.22	V

Table 3.5-12 SIM AC Timing Parameters

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
SIM_SCLK						
Rise and fall time	DVDD28_SIM = 1.8V	T _{rise_fall}	-	50	50	ns
Clock duty		Duty	47	50	53	%
Rise and fall time	DVDD28_SIM = 3.0V	T _{rise_fall}	-	18	18	ns
Clock duty		Duty	47	50	53	%
SIM_SIO						
Rise and fall time	DVDD28_SIM = 1.8V	T _{rise_fall}	-	50	1000	ns
Rise and fall time	DVDD28_SIM = 3.0V	T _{rise_fall}	-	50	1000	ns
SIM_SRST						
Rise and fall time	DVDD28_SIM = 1.8V	T _{rise_fall}	-	18	1000	ns
Rise and fall time	DVDD28_SIM = 3.0V	T _{rise_fall}	-	18	1000	ns

3.5.6 UART DC electrical characteristics

Table 3.5-13 UART DC Electrical Characteristics(VIO18 = 1.8V)

Parameter	Description	Min.	Typ.	Max.	Unit
VIH	Input logic high voltage	0.65*VIO18	-	VIO18 + 0.3	V
VIL	Input logic low voltage	-0.3	-	0.35*VIO18	V
VOH	DC output logic high voltage	0.75*VIO18	-	1.84	V
VOL	DC output logic low voltage	0	-	0.25*VIO18	V

3.5.7 GPIO DC electrical characteristics

Table 3.5-14 GPIO DC Electrical Characteristics(VIO18 = 1.8V)

Parameter	Description	Min.	Typ.	Max.	Unit
VIH	Input logic high voltage	0.65*VIO18	-	VIO18 + 0.3	V
VIL	Input logic low voltage	-0.3	-	0.35*VIO18	V
VOH	DC output logic high voltage	0.75*VIO18	-	1.84	V
VOL	DC output logic low voltage	0	-	0.25*VIO18	V

3.5.8 RGMII electrical characteristics

Table 3.5-15 RGMII DC Electrical Characteristics(VIO18 = 1.8V)

Parameter	Description	Min.	Typ.	Max.	Unit
VIH	Input logic high voltage	0.65*VIO18	-	VIO18 + 0.3	V

VIL	Input logic low voltage	-0.3	-	0.35*VIO18	V
VOH	DC output logic high voltage	0.75*VIO18	-	1.84	V
VOL	DC output logic low voltage	0	-	0.25*VIO18	V

Table 3.5-16 RGMII AC Timing Parameters

Symbol	Description	Min.	Typ.	Max.	Unit
Tsetup D0	Data to clock output setup	1.2	2	2.8	V
Thold D0	Clock to Data output hold	1.2	2	2.8	V
Tsetup D0	Data to clock output setup	1.2	2	2.8	V
Thold D0	Clock to Data output hold	1.2	2	2.8	V
Tsetup D0	Data to clock output setup	1.2	2	2.8	V
Thold D0	Clock to Data output hold	1.2	2	2.8	V
Tsetup D0	Data to clock output setup	1.2	2	2.8	V
Thold D0	Clock to Data output hold	1.2	2	2.8	V
Tcyc_G	Clock cycle Duration for 1000Mbps	7.2	8	8.8	V
Duty_G	+Duty cycle for 1000Mbps	45	50	55	%
Tr	Rise time(20-80%)	-	-	0.75	ns
Tf	Fall time(20-80%)	-	-	0.75	ns

3.5.9 SGMII electrical characteristics

Table 3.5-17 SGMII TX/RX Gen1 Specification

Test Item	SGMII Spec
Vdiff(pp)	min. 300mV max. 950mV
Eye Height	-
Cycle to cycle clk jitter	max.100ps
Rise time	min. 100ps max. 200ps
Fall time	min. 100ps max. 200ps
Clk signal duty cycle(%)	min. 48% max. 52%

*1UI = 800ps(1/1.25-GHz)

Table 3.5-18 SGMII Gen2 Specification

Test Item	SGMII Spec
Vdiff(pp)	max. 1600mV
Dj	max. 0.37UI*
Rise time	-
Fall time	-
TJ(1E-12)	<= 0.55UI

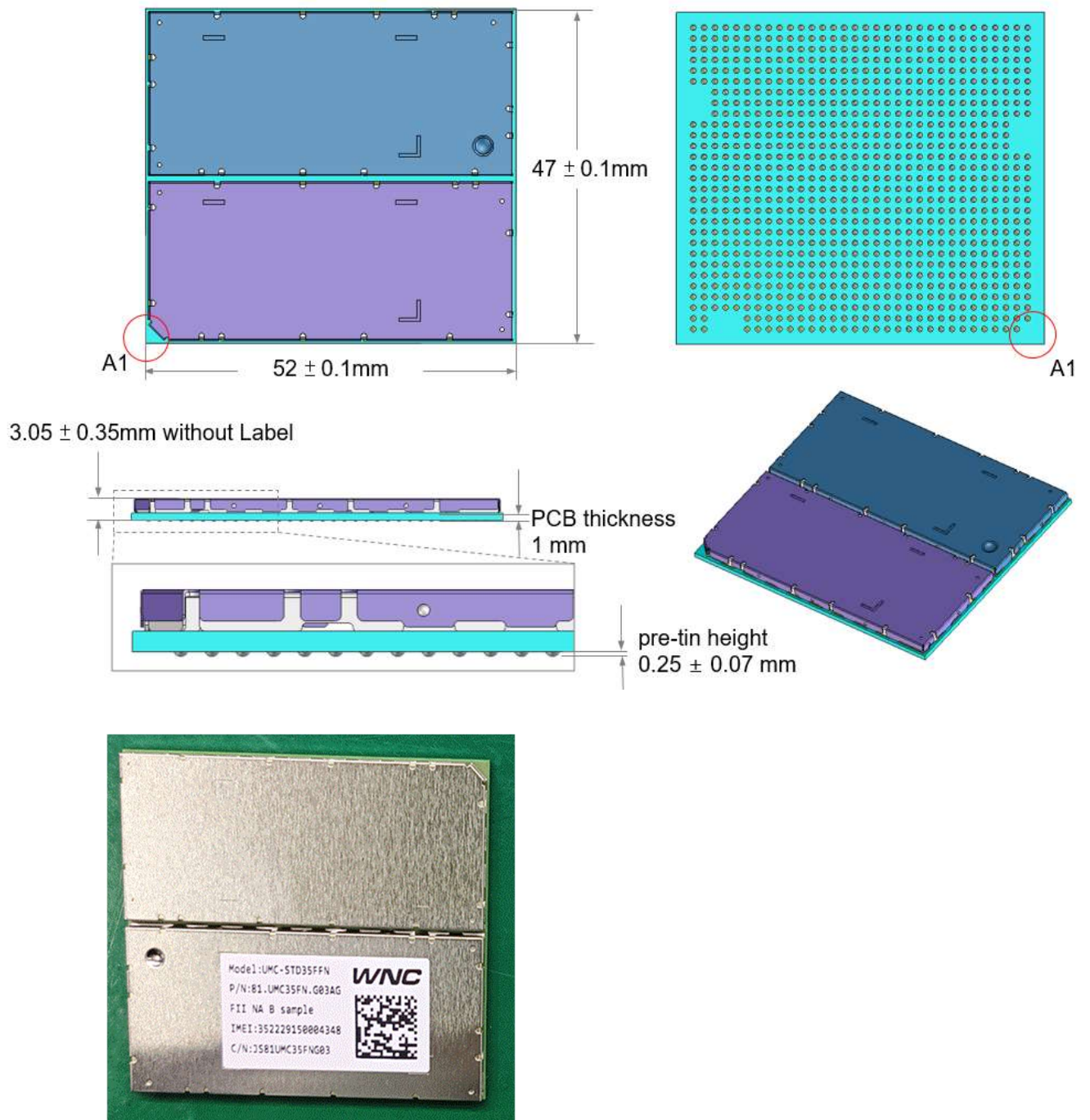
*1UI = 320ps(1/3.125-GHz)

4. MECHANICAL INFORMATION

NAD weight is under the total weight requirement of 15.6-g

4.1 NAD PHYSICAL DIMENSIONS

Product outline of finished-goods NAD is defined by dimensions with the fabrication tolerance in the drawing chart listed as below



4.2 NAD ORDERING INFORMATION

Label is applied to UMC-STD35FFx NAD shielding case top. It specifies the label with the content format as below and presents purchase ordering information of WNC part number for UMC-STD35FFx variant NAD.

UMC-STD35FFN

Ordering Part Number	Remark
81.UMC35FN.G01AG	n/a
81.UMC35FN.G02AG	NAD implemented with the optimized board-link and applied with Under-filling for 2 chips
81.UMC35FN.G03AG	NAD applied with Under-filling for 4 chips



UMC-STD35FFR

Ordering Part Number	Remark
81.UMC35FR.G01AG	NAD applied with Under-filling for 4 chips



4.3 NAD MOISTURE-SENSITIVITY LEVEL

UMC-STD35FFx NAD complies IPC/JEDEC J-STD-020 Standard MSL 3

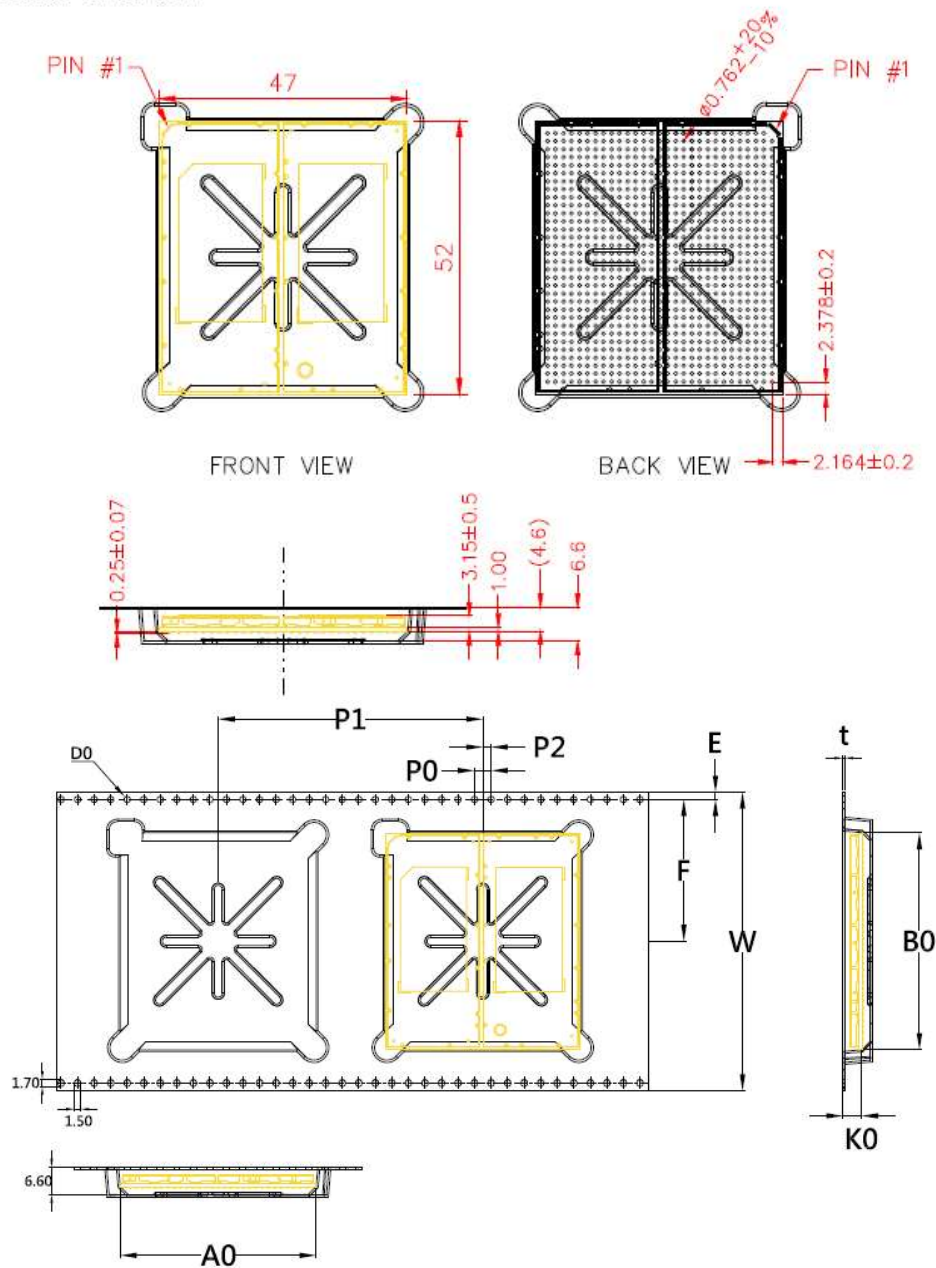
5. CARRIER, STORAGE AND HANDLING

This chapter describes NAD module packing information included in carrier, storage and handling.

5.1 CARRIER

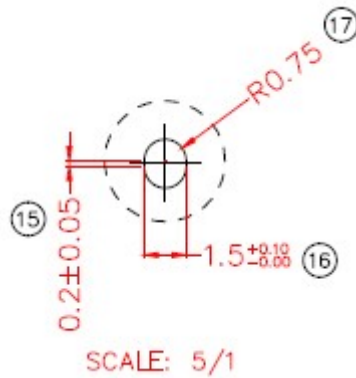
5.1.1 Tape and reel

MODULE DIRECTION



W	72.00±0.30	P2	2.00±0.20
S0	68.40±0.10	A0	47.4±0.15
E1	1.75±0.10	A1	—
F	34.20±0.30	B0	52.4±0.15
D0	1.50±0.05	B1	—
D1	—	K0	6.6±0.15
P1	64.00±0.10	K1	4.6±0.15
P0	4.00±0.10	T	0.50±0.05

1. CAMBER IN COMPLIANCE WITH EIA-481.
2. MATERIAL: PS BLACK, THICKNESS: 0.5±0.05MM
3. SURFACE RESISTIVITY: 10⁹~10¹⁰ OHMS/SQUARE
4. PACKING LENGTH PER ROLL : 8.5 METERS.
5. VENDOR SHIPPING LENGTH PER ROLL : 25.5 METERS.
6. COMPONENT POCKETS PER 13" REEL : 100 PCS
(TOTAL POCKETS PER 13" REEL & 7" HUB: 132 PCS
EMPTY POCKET IN FRONT OF REEL: 10 PCS
EMPTY POCKET IN BACK OF REEL: 15 PCS
BUFFER POCKET: 7 PCS)



5.2 STORAGE

5.2.1 Storage conditions

UMC-STD35FFx NAD delivered in tape and reel carriers must be stored in sealed, moisture-proof, anti-static bags between a temperature and humidity range of 15 to 35 deg-C, < 90% R.H.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a NAD can be on the factory floor before being installed onto a PCB. It is defined by the NAD MSL rating, as described in Section 4.3

5.3 HANDLING

This section describes NAD baking condition and ESD performance.

5.3.1 Baking

It is not necessary to bake the UMC-STD35FFx if the conditions specified in Section 5.2.1 and Section 5.2.2 have not been exceeded.

It is necessary to bake the UMC-STD35FFx NAD if the humidity card indicates NAD needs to undergo baking

Baking Conditions: 24-hours at 125 +/- 5 deg-C

5.3.2 Electrostatic discharge(ESD)

It is strongly recommended for the Developer to place ESD suppression components on the interconnection signal traces between NAD bottom pads and the application board to prevent NAD suffering ESD events with the voltage strength over the requirement defined in the table below:

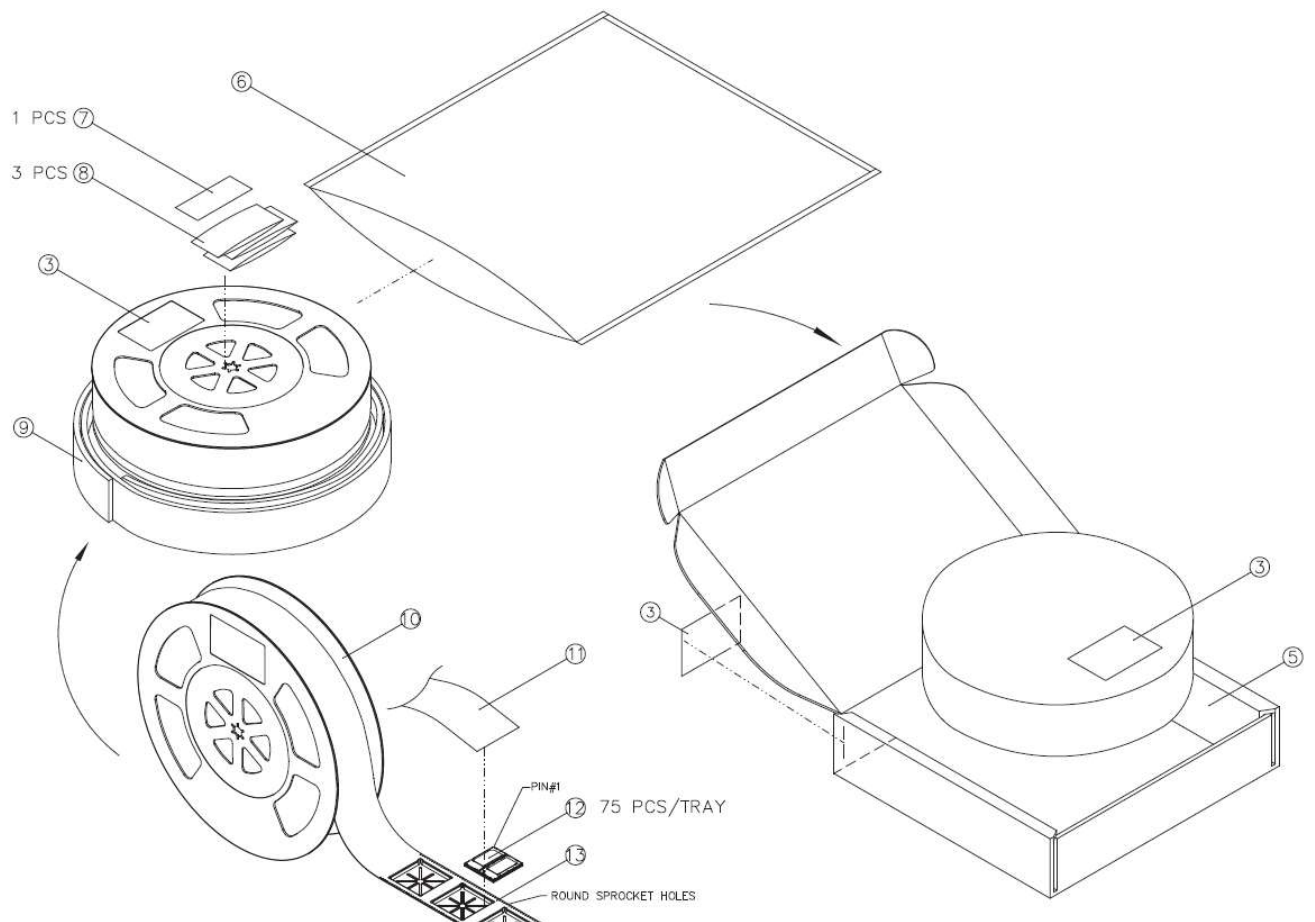
Table 5.3-1

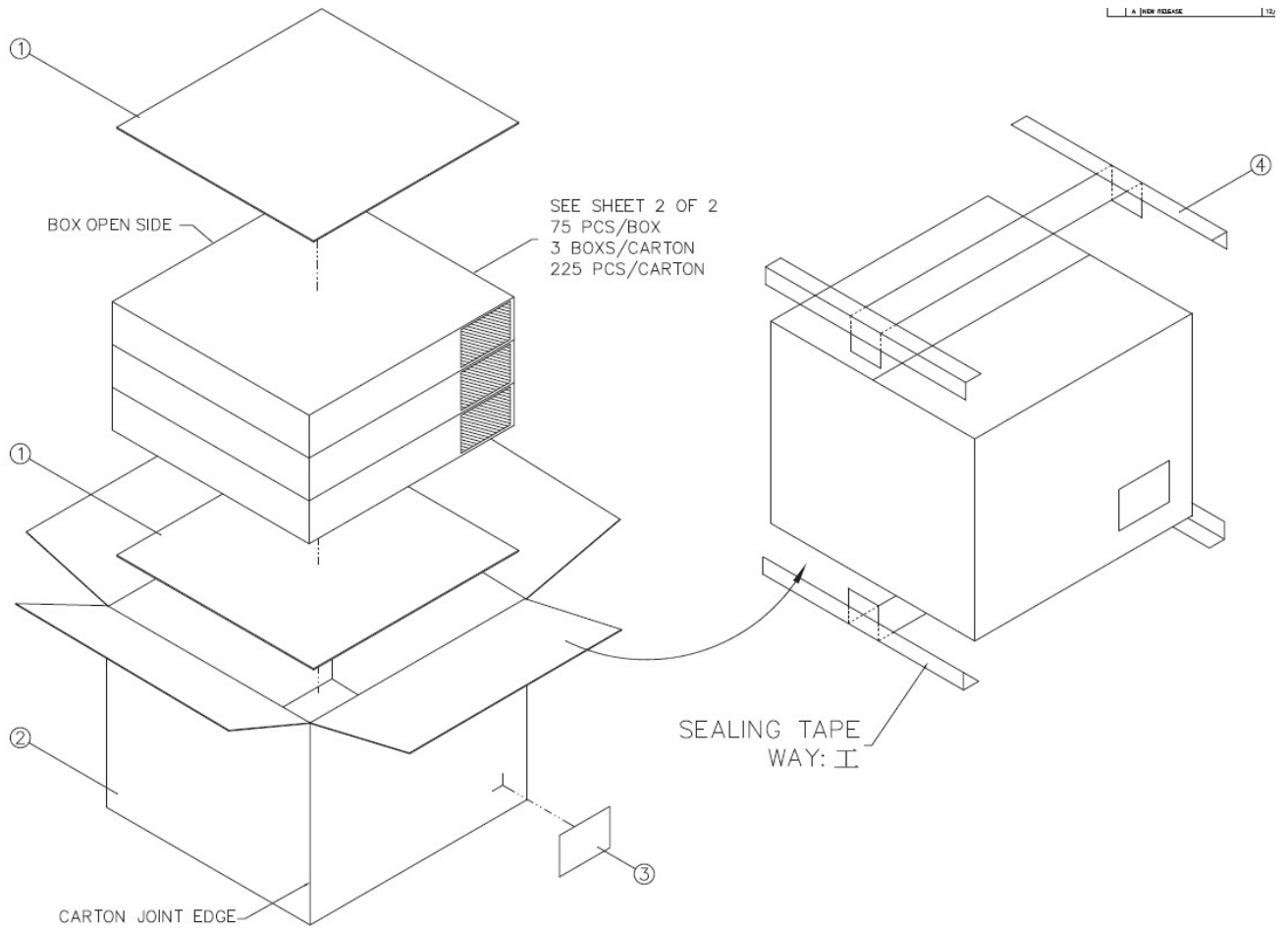
Specification/Requirements	Contact Discharge
Human Body Model(HBM)	1000 Voltages
Charge Device Model(CDM)	250 Voltages

5.4 BARCODE LABEL AND PACKING FOR SHIPMENT

This section describes label drawing and packing information

5.4.1 Packing and label location





5.4.2 Box label and tap reel for shipping

UMC-STD35FFN

(P)C P/N: 314.90006.005FT

 (Q)QTY: 75

 (M)Mfr P/N: 81.UMC35FN.G03AG

 (D)Date Code: 2401
 MSL: 3
 (L)Lot#: 240131

 (K)P.O: XXXXXXXXXX

 (S)PKG ID: VTW0011381YYMM000001

WNC
 RoHS

UMC-STD35FFR



5.4.3 Carton label for shipping

UMC-STD35FFN



UMC-STD35FFR

(P)C P/N: 314.90007.005FT



(Q)QTY: 225



(M)Mfr P/N: 81.UMC35FR.G01AG



(D)Date Code: 2501



MSL: 3

(L)Lot#: 250131



(K)P.O: 1234567890PO



(S)PKG ID: VTW0011381YYMM000001



WNC
RoHS

6. PCB MOUNTING GUIDELINES

6.1 ROHS COMPLIANCE

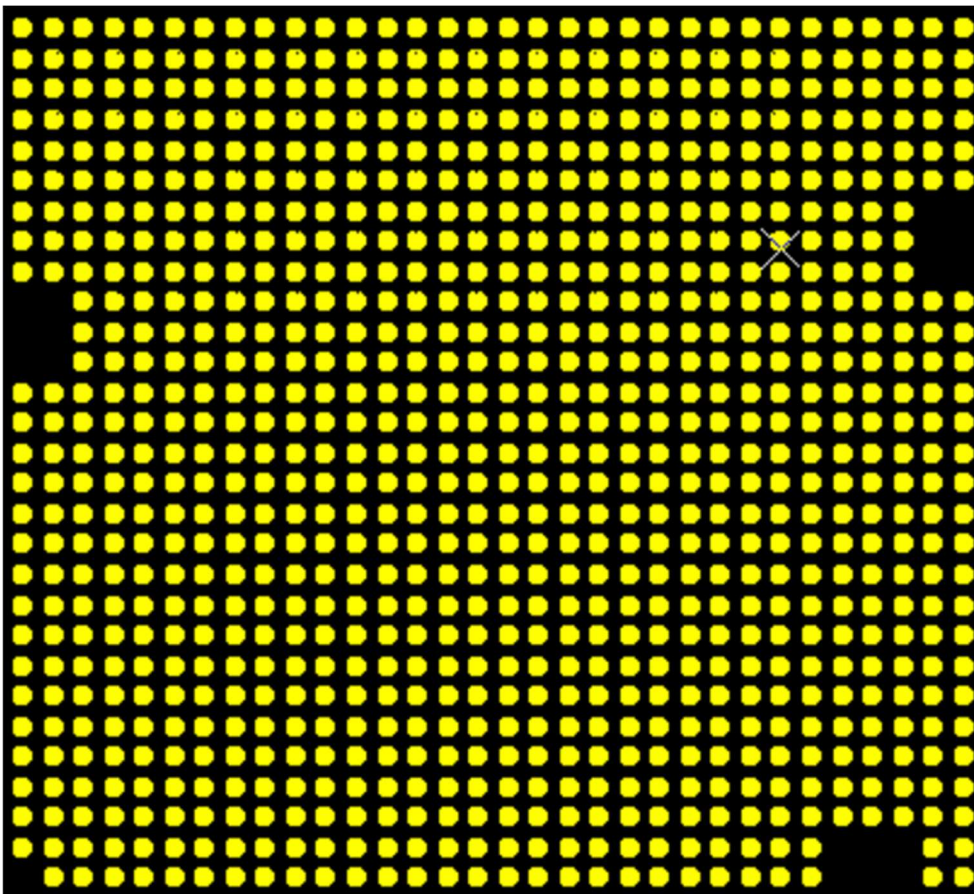
UMC-STD35FFx is lead-free and RoHS compliant. WNC defines it is lead-free(or Pb-free) product

6.2 SMT PARAMETER

This section describes WNC board-level characterization process parameters. It will help customers in their SMT process development; it is not intended to be a specification for their SMT process.

6.2.1 Land pad and stencil design

Top side view of NAD LGA pads



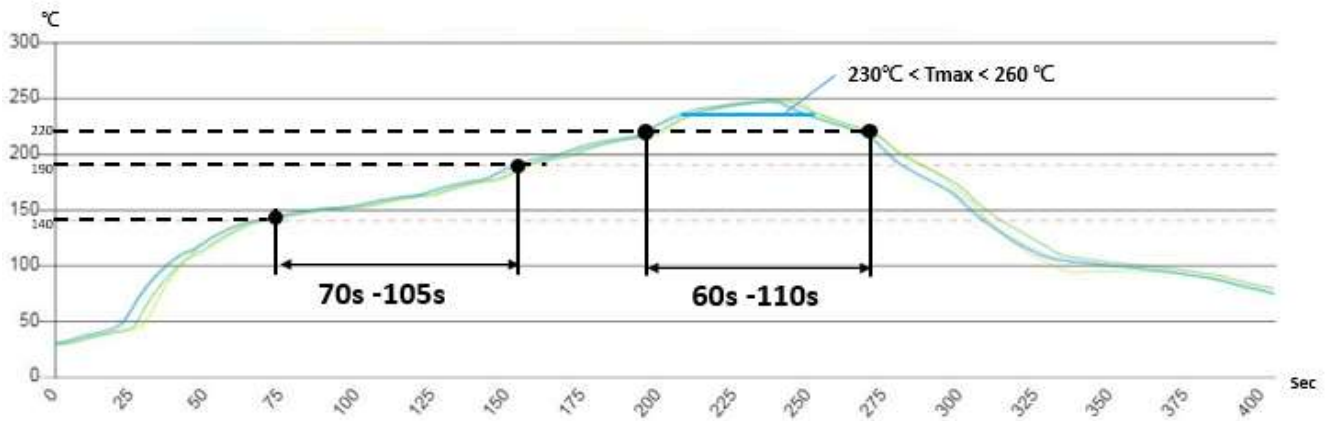
A1

Stencil Design Recommendation
Stencil Pad Size: 1(NAD Pad):1.2(Stencil Pad)
Stencil Thickness: 0.08-mm
Solder Paste Recommendation: SAC305 Alloy

6.2.2 Reflow profile

NAD maximum allowed SMT reflow times is twice based on the reflow temperature profile showed as below

Temperature Zone	Time	Key Parameter (Reflow Temperature)	Recommendation
Soak Zone	70 to 105 Seconds	140 to 190 deg-C	To well-control Soak Zone Time within 90 +/- 5 Seconds
Peak Zone	60 to 110 Seconds	230 to 250 deg-C	Peak Zone Reflow Temperature is better higher than 240 deg-C



6.2.3 SMT peak package body temperature

Tmax must be less than 260 deg-C

6.2.4 SMT process verification

WNC recommends verification of the SMT process prior to high volume board assembly, including

- In-line solder paste deposition monitoring
- Reflow temperature profile measurement and verification
- Visual and X-ray inspection after soldering to confirm adequate alignment, solder voids, solder pad shape, and solder bridging
- Cross-section inspection of solder joints for wetting, solder pad shape, and voiding

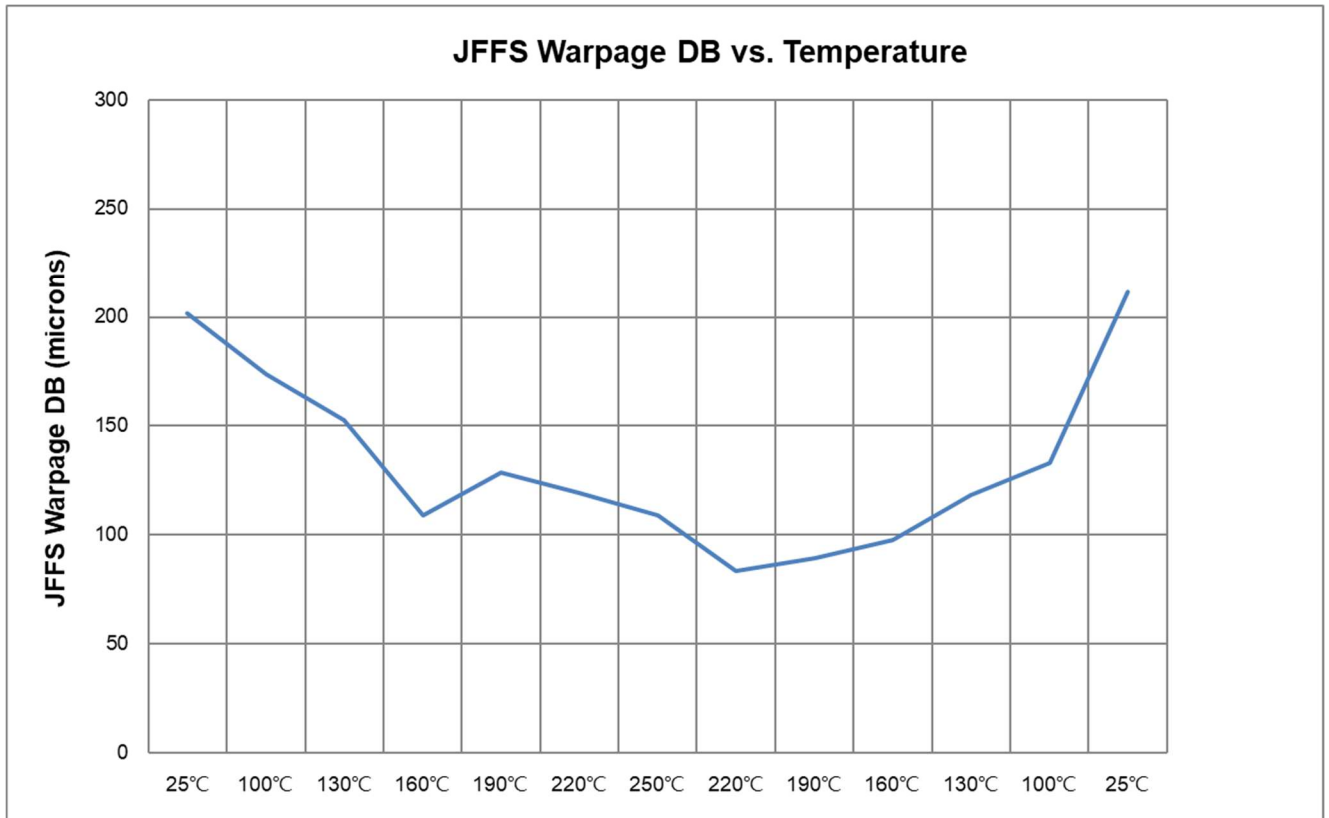
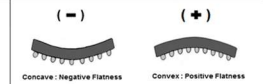
6.3 HIGH TEMPERATURE WARPAGE

This section describes the high temperature warpage performance of NAD by the shadow moire results.

unit: microns

Sample No. / Temperature	25°C	100°C	130°C	160°C	190°C	220°C	250°C	220°C	190°C	160°C	130°C	100°C	25°C
1	201.9	173.6	152.5	109.0	128.6	119.5	109.2	83.3	89.6	97.5	118.1	133.2	211.5

Remark1: Warpage sign is based on ball side face down.



7. RELIABILITY

Follow Test Group A, B, C, E and H listed in AECQ-104 standard

7.1 BOARD-LEVEL QUALIFICATIONS SUMMARY

Test Item	Test Sample Quantity	Pass Quantity	Fail Quantity	Result
A2 Temperature Humidity Bias (THB)	30pcs	30pcs	0pcs	Pass
A3 Temperature Humidity (TH)	30pcs	30pcs	0pcs	Pass
A4 Temperature Cycling (TC)	10pcs	10pcs	0pcs	Pass
A5 Power Temperature Cycling (PTC)	33pcs	33pcs	0pcs	Pass
A6 High Temperature Storage Life (HTSL)	30pcs	30pcs	0pcs	Pass
B1 High Temperature Operation Life (HTOL)	30pcs	30pcs	0pcs	Pass
C3 Solderability (SD)	15pcs	15pcs	0pcs	Pass
C4 Physical Dimensions (PD)	5pcs	5pcs	0pcs	Pass
C7 X-Ray (XRAY)	3pcs	3pcs	0pcs	Pass
E2 ESD (HBM)	12pcs	12pcs	0pcs	Pass
E3 ESD (CDM)	6pcs	6pcs	0pcs	Pass
E8 Radiated Emissions (RE)	2pcs	2pcs	0pcs	Pass
H2 Low Temperature Storage Life (LTSL)	30pcs	30pcs	0pcs	Pass
H3 Startup & Temperature Steps (STEP)	5pcs	5pcs	0pcs	Pass
H4 Drop test (DROP)	6pcs	6pcs	0pcs	Pass
K1 Damp Heat, Cyclic (K-08)	10pcs	10pcs	0pcs	Pass

This module is intended for OEM integrators only. Per FCC KDB 996369 D03 OEM Manual v01 guidance, the following conditions must be strictly followed when using this certified module:

KDB 996369 D03 OEM Manual v01 rule sections:

2.2 List of applicable FCC rules

This module has been tested for compliance to FCC Part 2, 22, 24, 27 and 90

2.3 Summarize the specific operational use conditions

The module is tested for standalone mobile RF exposure use condition. Any other usage conditions such as co-location with other transmitter(s) or being used in a portable condition will need a separate reassessment through a class II permissive change application or new certification.

2.4 Limited module procedures

Not applicable.

2.5 Trace antenna designs

Refer to "Operational Description Antenna trace"

Please contact the module supplier

Any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify the module grantee that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the grantee, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

2.6 RF exposure considerations

This equipment complies with FCC mobile radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 29 cm between the radiator & your body. If the module is installed in a portable host, a separate SAR evaluation is required to confirm compliance with relevant FCC portable RF exposure rules.

2.7 Antennas

The following antennas have been certified for use with this module; antennas of the same type with equal or lower gain may also be used with this module. The antenna must be installed such that 29 cm can be maintained between the antenna and users.

The final host product must comply with the requirements specified in §15.203, §15.204(b) and §15.204(c). As such, the host product must use a permanently attached antenna or an antenna that uses a unique coupling. The OEM integrator is responsible for using a unique external antenna connector in the host product, which must be selected from the types listed below.

Antenna Type	Dipole
Antenna connector	SMA

The host product is required to include an antenna which complies with the requirements specified within these integration instructions.

2.8 Label and compliance information

The final end product must be labeled in a visible area with the following:

“Contains FCC ID: NKR-UMCSTD35FFN”. The grantee's FCC ID can be used only when all FCC compliance requirements are met.

2.9 Information on test modes and additional testing requirements

This transmitter is tested in a standalone mobile RF exposure condition and any co-located or simultaneous transmission with other transmitter(s) or portable use will require a separate class II permissive change re-evaluation or new certification.

2.10 Additional testing, Part 15 Subpart B disclaimer

This transmitter module is tested as a subsystem and its certification does not cover the FCC Part 15 Subpart B (unintentional radiator) rule requirement applicable to the final host. The final host will still need to be reassessed for compliance to this portion of rule requirements if applicable.

As long as all conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

OEM/Host manufacturer responsibilities

OEM/Host manufacturers are ultimately responsible for the compliance of the Host and Module. The final product must be reassessed against all the essential requirements of the FCC rule such as FCC Part 15 Subpart B before it can be placed on the US market. This includes reassessing the transmitter module for compliance with the Radio and EMF essential requirements of the FCC rules. This module must not be incorporated into any other device or system without retesting for compliance as multi-radio and combined equipment

Industry Canada statement:

This device complies with ISSED's licence-exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Le présent appareil est conforme aux CNR d' ISSED applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) le dispositif ne doit pas produire de brouillage préjudiciable, et (2) ce dispositif doit accepter tout brouillage reçu, y compris un brouillage susceptible de provoquer un fonctionnement indésirable.

Radiation Exposure Statement

This equipment complies with ISSED radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with greater than 43 cm between the radiator & your body.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISSED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé à plus de 43 cm entre le radiateur et votre corps.

This device is intended only for OEM integrators under the following conditions

- 1) The antenna must be installed and operated with greater than 43 cm between the antenna and users
- 2) The transmitter module may not be co-located with any other transmitter or antenna.
- 3) Module approval valid only when the module is installed in the tested host or compatible series of host which have similar RF exposure characteristic with equal or larger antenna separation distance.

As long as 3 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes:

- 1) L'antenne doit être installée et exploitée avec plus de 43 cm entre l'antenne et les utilisateurs
- 2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.
- 3) Approbation du Module valable que lorsque le module est installé dans l'hôte testé ou de la série de l'hôte compatible qui ont même caractéristique de l'exposition aux RF avec la distance égale ou supérieure séparation antenne.

Tant que les 3 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE

In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the Canada authorization is no longer considered valid and the IC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considérée comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed and operated with greater than 43 cm between the antenna and users. The final end product must be labeled in a visible area with the following: "Contains IC: 4441A-UMCSTD35FFN".

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un appareil où l'antenne peut être installée et utilisée à plus de 43 cm entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: 4441A-UMCSTD35FFN".

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as shown in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.

Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel

DETACHABLE ANTENNA USAGE

This radio transmitter [IC: 4441A-UMCSTD35HN] has been approved by Innovation, Science and Economic Development Canada to operate with the antenna types listed below, with the maximum

permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.

Le présent émetteur radio [IC: 4441A-UMCSTD35FFN] a été approuvé par Innovation, Sciences et Développement économique Canada pour fonctionner avec les types d'antenne énumérés ci-dessous et ayant un gain admissible maximal. Les types d'antenne non inclus dans cette liste, et dont le gain est supérieur au gain maximal indiqué pour tout type figurant sur la liste, sont strictement interdits pour l'exploitation de l'émetteur.

Manufacturer	Antenna connector	Antenna Type	Frequency (MHz)	MaxGain (dBi)	Impedance (Ω)
WNC	SMA	Dipole	700	1.63	50
			960	2.63	
			1710	2.03	
			2690	2.26	
			3300	1.55	
			4200	2.62	