Automotive 5G-NR NAD Product Specification

UMC-STD35GX

Wistron NeWeb Corp.

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Revision	Revision Date	Revised By	Description
1.0	2024/7/11	Paul	1st Release

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1. INTRODUCTION

This chapter describes the general concept of the NAD and key specifications.

1.1 UMC-STD35GX INTRODUCTION

This document describes and specifies technical features of UMC-STD35GX. UMC-STD35GX is an automotive-grade 5G NR Network Access Device of LGA type form-factor offering a full set of telematics features and functions including e-Call, GNSS, FOTA and so on. UMC-STD35GX is fully approved, including regional, country, and carrier approvals. It supports automotive applications like Telematics Control Unit, Vehicle to Everything, Fleet Management, Automatic Metering Management, Tracking System, Emergency Call, Breakdown or Roadside Assistance.

1.2 PRODUCT FEATURES

The NAD is employed with an MTK (MediaTek Inc.) MT2735 5G NR platform consisting of:

(NR Modem) MTK/MT2735SM(2-Core)
(Main Power Management IC) MTK/MT6330LW
(Second Power Management IC) MTK/MT6319WW
(RF IC) MTK/MT6190AV
(GNSS RFIC) MTK/MT6635WW
LPDDR4X 2GB
eMMC 4GB

1.2.1 Electrical key specifications

Table 1-1

Electrical Key Specifications	Compliance	NAD Pad Name
Peripheral Interface		
PCIe 3.0 x2 Root Complex	Supported	PCIE0_PERSTN; PCIE0_CLKREQN; PCIE0_PEWAKEN PCIE_A_CLKN; PCIE_A_CLKP PCIE_A_LN0_RXN; PCIE_A_LN0_RXP; PCIE_A_LN0_TXN; PCIE_A_LN0_TXP PCIE_A_LN1_RXN; PCIE_A_LN1_RXP; PCIE_A_LN1_TXN; PCIE_A_LN1_TXP
HS-USB 2.0	Supported	USB_DM; USB_DP
SS-USB 3.0	Supported	SSUSB_RXN; SSUSB_RXP; SSUSB_TXN; SSUSB_TXP
4-bit SDIO	Supported	MSDC1_CLK; MSDC1_CMD; MSDC1_DAT0; MSDC1_DAT1; MSDC1_DAT2; MSDC1_DAT3
Digital TDM(Out) (GPIO as the default)	Supported per Customer Request	TDM_MCK; TDM_BCK; TDM_LRCK; TDM_DATA0; TDM_DATA1; TDM_DATA2; TDM_DATA3 (EINT201, EINT200, EINT199, EINT202, EINT203, EINT204, EINT205)
MIPI0 (GPIO as the default)	Supported per Customer Request	MIPI0_D_SCLK, MIPI0_D_SDATA (EINT140, EINT141)

MIPI1 (GPIO as the default)	Supported per Customer Request	MIPI1_D_SCLK, MIPI1_D_SDATA (EINT138, EINT139)
MIPI2 (GPIO as the default)	Supported per Customer Request	MIPI2_D_SCLK, MIPI2_D_SDATA (EINT164, EINT165)
Digital Audio I2S0	Supported	I2S0_MCK; I2S0_BCK; I2S0_LRCK; I2S0_DI; I2S0_DO
Digital Audio I2S2	Supported	I2S2_MCK; I2S2_BCK; I2S2_LRCK; I2S2_DI; I2S1_DO
Digital Audio PCM0 (GPIO as the default)	Supported per Customer Request	I2S4_MCK; PCM0_CLK; PCM0_SYNC; PCM0_DI; PCM0_DO (EINT96, EINT97, EINT98, EINT99, EINT100)
SGMII0	Supported w/ AVB only, no Data IPA; or Data IPA only, no AVB	GBE0_INT; GBE0_RST SGMII_0_RXN; SGMII_0_RXP; SGMII_0_TXN; SGMII_0_TXP
RGMII	Supported w/ AVB only, no Data IPA; or Half Data IPA only, no AVB	GBE_TXEN; GBE_TXER; GBE_RXER; GBE_RXDV; GBE_TXC; GBE_RXC; GBE_COL; GBE_INTR; GBE_MDC; GBE_MDIO GBE_TXD0; GBE_TXD1; GBE_TXD2; GBE_TXD3; GBE_RXD0; GBE_RXD1; GBE_RXD2; GBE_RXD3
SGMII1	Supported w/ Data IPA only, no AVB	GBE1_INT; GBE1_RST SGMII_1_RXN; SGMII_1_RXP; SGMII_1_TXN; SGMII_1_TXP
SIM1	Supported	INT_SIM1; SIM1_SCLK; SIM1_SIO; SIM1_SRST
SIM2	Supported	INT_SIM2; SIM2_SCLK; SIM2_SIO; SIM2_SRST
I2C0	Supported	SCL0; SDA0
I2C1	Supported	SCL1; SDA1
I2C2	Supported	SCL2; SDA2
I2C3 (GPIO as the default)	Supported per Customer Request	SCL3; SDA3 (EINT198, EINT197)
I2C4 (GPIO as the default)	Supported per Customer Request	SCL4; SDA4 (EINT80, EINT79)
I2C5 (GPIO as the default)	Supported per Customer Request	SCL5; SDA5 (EINT82, EINT81)
UART0 (GPIO as the default)	Supported w/ 2-Wire	AP_UTXD0; AP_URXD0; AP_URTS0(EINT170); AP_UCTS0(EINT169)
UART1 (GPIO as the default)	Supported w/ 2-Wire	AP_UTXD1; AP_URXD1; AP_URTS1(EINT174); AP_UCTS1(EINT173)
UART2 (GPIO as the default)	Supported w/ 2-Wire	AP_UTXD2; AP_URXD2; AP_URTS2(EINT178); AP_UCTS2(EINT177)
UART3 (GPIO as the default)	Supported w/ 2-Wire	AP_UTXD3; AP_URXD3; AP_URTS3(EINT182); AP_UCTS3(EINT181)
Analog-to-Digital Converter Input	Supported	AUXIN0; AUXIN1; AUXIN2; AUXIN3
SPI0	Supported	SPI0_CSB, SPI0_CLK, SPI0_MI, SPI0_MO
SPI1	Supported	SPI1_CSB, SPI1_CLK, SPI1_MI, SPI1_MO
SPI2	Supported	SPI2_CSB, SPI2_CLK, SPI2_MI, SPI2_MO

SPI3	Supported	SPI3_CSB, SPI3_CLK, SPI3_MI, SPI3_MO
General Purpose Input/Output	Supported	EINT0; EINT1; EINT4; EINT5; EINT6; EINT7; EINT26; EINT27; EINT28; EINT29; EINT30; EINT31; EINT32; EINT39

1.2.2 RF KEY SPECIFICATIONS

Table 1-2

RF Key Specification	Compliance
Envelope Tracking (ET) of Power Amplifier DC-feed Controlling	n/a
Average Power Tracking (APT) of Power Amplifier DC-feed Controlling	n/a
LTE Downlink Carrier Aggregation	Supported with CA combinations specified in this document
NR Downlink Carrier Aggregation	Supported with CA combinations specified in this document
LTE Uplink Carrier Aggregation	n/a
NR Uplink MIMO	n/a
High Power UE (HPUE)	Support please see section 1.3.5
Sounding Reference Signal (SRS)	Support please see section 1.3.4
Dynamic Spectrum Sharing (DSS)	Supported
E-UTRAN New Radio - Dual Connectivity (EN-DC)	Supported with EN-DC combinations specified in this document
Dual SIM Dual Active	n/a
Dual SIM Dual Standby	Supported
Licensed Assisted Access (LAA)	Supported
Cellular Vehicle-to-Everything (C-V2X) over the legacy LTE Uu air interface	n/a
Cellular Vehicle-to-Everything (C-V2X) via PC5 interface	Supported with the limitation that NAD needs the external C-V2X
Dedicated Short Range Communication (DSRC) Vehicle-to-Everything (V2X)	Supported with the limitation that NAD needs the external DSRC
3rd Generation Partnership Project (3GPP) Circuit Switched(CS) emergency Call (eCall)	Supported w/ Embedded MTK/MT6635 GNSS RFIC

Europe (EU) CS eCall	Supported w/ Embedded MTK/MT6635 GNSS RFIC
EU Internet Multimedia System (IMS) eCall	Supported w/ Embedded MTK/MT6635 GNSS RFIC
3GPP IMS eCall included in Next Generation (NG)-eCall	Supported w/ Embedded MTK/MT6635 GNSS RFIC
ERA-Global Navigation Satellite System (GLONASS) eCall	Supported w/ Embedded MTK/MT6635 GNSS RFIC

1.2.3 NAD BAND PLAN

There are four kinds of NAD variants well-designed for countries and carriers of different regions.

UMC-STD35GX /NA dedicated for carriers in North America
UMC-STD35GX /EU dedicated for Countries/Carriers in Europe
UMC-STD35GX /RW dedicated for Countries/Carriers in Rest of World

NR NSA/SA low/middle/high band supports re-use of RF Front-End of LTE bands and the table shows the planned design goal of UMC-STD35GX C-sample. Regarding supporting bands of both A- and B-sample, please contact WNC for details.

Table 1-3

RAT/Variant	NA	RW	EU
	UMC-STD35GN	UMC-STD35GW	UMC-STD35GE
NSA/SA NR	n5 and n71 n2 and n66; n7 and n41 n77 and n78	n28 n1 and n3; n41 n77, n78 and n79	n5 (*), n8 and n28 n1 and n3; n7 n77 and n78
LTE	B26(5), 12(17), 13, 14, 29 and 71 B1, 25(2), 3 and 66(4) B7, 30 and 41	B26(5/18/19), 8, 20 and 28 B1, 25(2), 3(9), 4, 34 and 39; B32 B7, 40 and 41(38)	B5(*), 8, 20 and 28 B1 and 3; B32 B7, 38 and 40
WCDMA/TD-SCDMA	B1, 2, 3, 4 and 5	B1, 3(9), 5(6/19) and 8	B1, 3, 5(*) and 8
GSM/GPRS/EDGE	850, 900, 1800 and 1900	850, 900, 1800 and 1900	900 and 1800

(*) NR band5, LTE band 5 and WCDMA Band 5 do not use in Europe

1.2.4 SRS SUPPORT BAND PLAN

Sounding Reference Signal	RAT/Variant		
	RW	EU	NA
1T1R(NR SA mode only)	n/a	n/a	n/a
1T2R(NR SA mode only)	NR SA n78	NR SA n78	NR SA n41 and n77
1T4R(NR SA mode only)	n/a	n/a	n/a
2T4R(NR SA mode only)	n/a	n/a	n/a

1.2.5 HIGH POWER UE SUPPORT BAND PLAN

Supported by the single antenna transmitting.

High Power UE(HPUE) power class	RAT/Variant		
	RW	EU	NA
Class 1	n/a	n/a	n/a
Class 1.5	n/a	n/a	n/a
Class 2	NR SA n78	NR SA n78	NR SA n41,n77

1.2.6 ANTENNA CONFIGURATION

(*) Uplink transmission is not allowed at this band for UE with external vehicle mounted antennas

(***)Band32 primary receiving signals is supported by MIMO1 antenna, as well as the diversity signals received by MIMO2 antenna; to-be-confirmed later, RoW/EU RFFE design is still under the optimization

Primary Transmitting/Receiving antenna is supported by NAD-Pad#AH25(RF-ANT1), as well as
Diversity Transmitting/Receiving antenna offered by NAD-Pad#AH13(RF-ANT2)
MIMO1 Receiving antenna offered by NAD-Pad#AH4(RF-ANT3)
MIMO2 Receiving antenna offered by NAD-Pad#AH6(RF-ANT4)

GNSS antenna is not defined in the table and supported by NAD-Pad#AA1(RF_GNSS_L1_L5_ANT)
Table 1-4
X: be supported

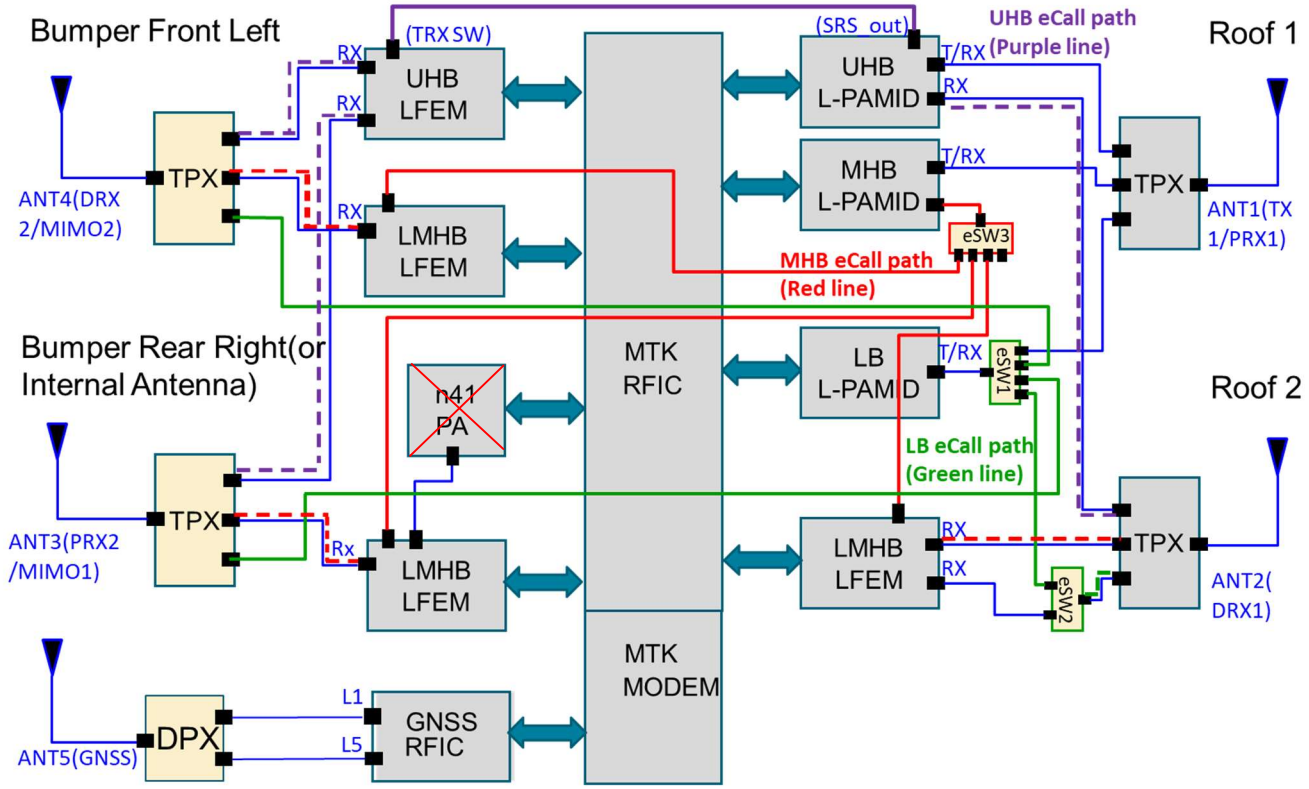
RAT / Band	Primary Transmitting	Primary Receiving	Diversity Transmitting	Diversity Receiving	MIMO1 Receiving	MIMO2 Receiving
GSM/EDGE 1900	X	X	n/a	n/a	n/a	n/a
GSM/EDGE 1800	X	X	n/a	n/a	n/a	n/a
GSM/EDGE 850	X	X	n/a	n/a	n/a	n/a
GSM/EDGE 900	X	X	n/a	n/a	n/a	n/a
WCDMA Band1	X	X	n/a	X	n/a	n/a
WCDMA Band2	X	X	n/a	X	n/a	n/a
WCDMA Band3	X	X	n/a	X	n/a	n/a
WCDMA Band4	X	X	n/a	X	n/a	n/a
WCDMA Band19	X	X	n/a	X	n/a	n/a
WCDMA Band5	X	X	n/a	X	n/a	n/a
WCDMA Band8	X	X	n/a	X	n/a	n/a
LTE/NR Band12/n12	X	X	n/a	X	n/a	n/a

LTE Band17	X	X	n/a	X	n/a	n/a
LTE Band13	X	X	n/a	X	n/a	n/a
LTE/NR Band14/n14	X	X	n/a	X	n/a	n/a
LTE/NR Band28/n28	X	X	n/a	X	n/a	n/a
LTE Band29	n/a	X	n/a	X	n/a	n/a
LTE/NR Band71/n71	X	X	n/a	X	n/a	n/a
LTE Band26	X	X	n/a	X	n/a	n/a
LTE/NR Band5/n5	X	X	n/a	X	n/a	n/a
LTE/NR Band18/n18	X	X	n/a	X	n/a	n/a
LTE Band19	X	X	n/a	X	n/a	n/a
LTE/NR Band8/n8	X	X	n/a	X	n/a	n/a
LTE/NR Band20/n20	X	X	n/a	X	n/a	n/a
LTE Band32(***)	n/a	n/a	n/a	n/a	X	X
LTE/NR Band1/n1	X	X	n/a	X	X	X
LTE Band25/n25	X	X	n/a	X	X	X
LTE Band2/n2	X	X	n/a	X	X	X
LTE Band3/n3	X	X	n/a	X	X	X
LTE Band9	X	X	n/a	X	X	X
LTE Band66/n66	X	X	n/a	X	X	X
LTE Band4	X	X	n/a	X	X	X
LTE Band10	X	X	n/a	X	X	X
LTE/NT Band34/n34	X	X	n/a	X	X	X
LTE/NR Band39/n39	X	X	n/a	X	X	X
LTE/NR Band7/n7	X	X	n/a	X	X	X
LTE/NR Band30/n30(*)	n/a	X	n/a	X	X	X
LTE/NR Band40/n40	X	X	n/a	X	X	X
LTE/NR Band41/n41	X	X	n/a	X	X	X
LTE/NR Band38/n38	X	X	n/a	X	X	X
LTE Band42	X	X	n/a	X	X	X
NR n77	X	X	n/a	X	X	X
NR n78	X	X	n/a	X	X	X
NR n79	X	X	n/a	X	X	X

1.2.7 ECALL-ASM BLOCK DIAGRAM AND SWITCH SCENARIO

The section describes the eCall-ASM block diagram and switch scenario of the NAD module which provide an over view for TCU eCall design

Block Diagram



Not1: The block diagram is displaying the normal mode operation of eCall Switch circuitry
Note2 : NAD ANT4 port signals is connected to the external RF SPDT switch(located on CM/B1.2) for CM/B1.2 Bumper Front Left or Internal Antenna connection

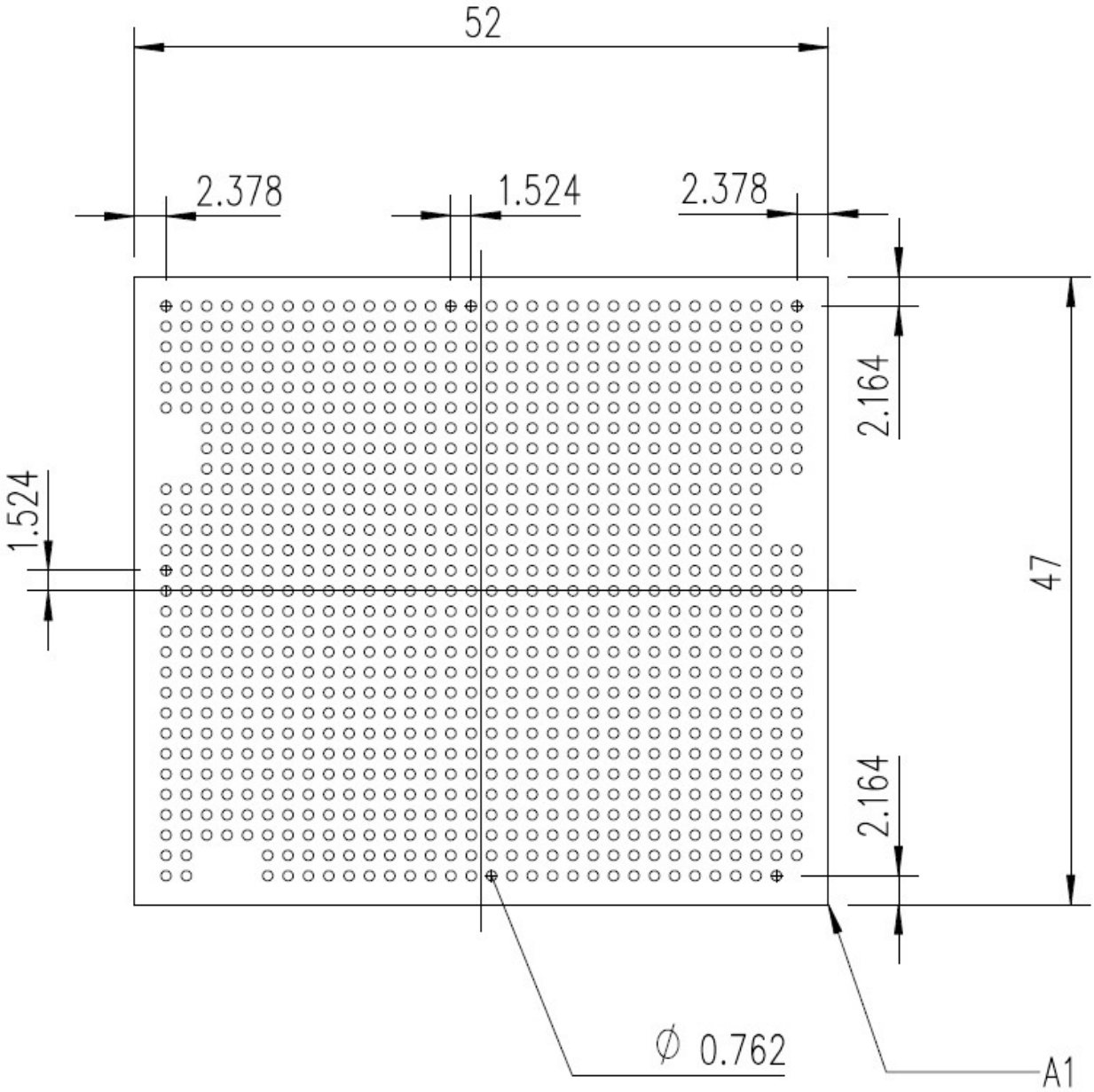
eCall switch scenario

eCall Switch Scenario(ConMod/B1.2)	Antenna Usage(ConMod/B1.2) NAD Port to Antenna			eCall Prio Antenna	ESO Antenna Sce	Setting Command	Connector(ConMod/B1.2)
Normal Operation	NAD/ANT1(TX1/PRX1)	to	CM/B1.2 Roof 1	All available antenna	ANTENNAS_SCEN	cmd1	LTE1@Con F Pin1
	NAD/ANT2(DRX1)	to	CM/B1.2 Roof 2				LTE2@Con F Pin2
	NAD/ANT3(PRX2)	to	CM/B1.2 Bumper Rear Right				LTE4@Con D Pin1
	NAD/ANT4(DRX2)	to	CM/B1.2 Bumper Front Left				LTE3@Con E Pin1
Backup 1	NAD/ANT3(TX1/PRX1)	to	CM/B1.2 Internal Antenna	eCall_Antenna_Prio	ANTENNAS_SCEN	cmd17	Internal Antenna
	NAD/ANT2(DRX1)	to	CM/B1.2 Roof 2	= "IVS_Antenna_1"			LTE2@Con F Pin2
	NAD/ANT4(DRX2)	to	CM/B1.2 Bumper Front Left				LTE3@Con E Pin1
Backup 3	NAD/ANT4(TX1/PRX1)	to	CM/B1.2 Bumper Front Left	eCall_Antenna_Prio	ANTENNAS_SCEN	cmd13	LTE3@Con E Pin1
	NAD/ANT2(DRX1)	to	CM/B1.2 Roof 2	= "IVS_Antenna_2"			LTE2@Con F Pin2
	NAD/ANT3(PRX2)	to	CM/B1.2 Bumper Rear Right				LTE4@Con D Pin1
Backup 4	NAD/ANT3(TX1/PRX1)	to	CM/B1.2 Bumper Rear Right	eCall_Antenna_Prio	ANTENNAS_SCEN	cmd9	LTE4@Con D Pin1
	NAD/ANT2(DRX1)	to	CM/B1.2 Roof 2	= "IVS_Antenna_3"			LTE2@Con F Pin2
	NAD/ANT4(DRX2)	to	CM/B1.2 Bumper Front Left				LTE3@Con E Pin1
Backup 2	NAD/ANT2(TX1/PRX1)	to	CM/B1.2 Roof 2	eCall_Antenna_Prio	ANTENNAS_SCEN	cmd5	LTE2@Con F Pin2
	NAD/ANT3(PRX2)	to	CM/B1.2 Bumper Rear Right	= "IVS_Antenna_4"			LTE4@Con D Pin1
	NAD/ANT4(DRX2)	to	CM/B1.2 Bumper Front Left				LTE3@Con E Pin1

2. PIN DEFINITIONS

NAD Land Pattern Diagram

- Bottom Side View
- 32 by 29 LGA-type Land Pattern
- #909 Contact Pins
- 0.762-mm Round Pad Size
- 1.524-mm Pad Pitch



Unit: mm

2.1 I/O PARAMETERS DEFINITIONS

NAD pin map is shown below and presented from top side view

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	
AH	D_GND	D_GND	D_GND	ANT_MIMO3	D_GND	ANT_MIMO4	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	ANT2_LGA	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	ANT1_LGA	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	AH
AG	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	AG
AF	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	AF
AE	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	AE
AD	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	AD
AC	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	AC
AB	RF_GNSS_L1_L5ANT	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND			AB
AA	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND			AA
Y	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND			Y
W			D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	W
V			D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	V
U			D_GND	D_GND	D_GND	GBE_TXER	GBE_RXC	GBE_TXD3	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	VCC_VRF1	VCC_VRF1	VCC_VRF3	VCC_VRF2	U
T	D_GND	D_GND	D_GND	D_GND	D_GND	GBE_RXD1	GBE_RXER	GBE_TXD2	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	VCC_VRF1	VCC_VRF1	VCC_VRF3	VCC_VRF2	T
S	D_GND	D_GND	EINT97	D_GND	D_GND	GBE_TXEN	GBE_TXD0	GBE_INTR	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	S
R	D_GND	D_GND	EINT100	D_GND	EINT39	GBE_MDC	GBE_COL	GBE_TXC	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	R
P	D_GND	D_GND	EINT96	EINT36	EINT37	GBE_RXD2	GBE_RXD0	GBE_RXDV	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	MSDC1_DAT3	MSDC1_CLK	MSDC1_DAT2	D_GND	D_GND	D_GND	EINT140	EINT139	P
N	D_GND	D_GND	EINT98	EINT35	D_GND	GBE_RXD3	GBE_MDIO	GBE_TXD1	D_GND	D_GND	D_GND	D_GND	SPI2_CSB	AP_URXD0	AP_UTXD0	AUXIN1	AUXIN2	AUXIN0	EINT206	D_GND	D_GND	D_GND	D_GND	D_GND	MSDC1_DAT0	MSDC1_DAT1	MSDC1_CMD	D_GND	WATCHDOG	D_GND	EINT138	EINT141	N
M	D_GND	D_GND	EINT99	EINT38	EINT33	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	SPI1_CSB	SPI1_MI	SPI2_MI	D_GND	SPI2_CLK	AUXIN3	D_GND	EINT207	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	M
L	D_GND	SCL2	SCL1	EINT32	D_GND	D_GND	EINT182	D_GND	D_GND	D_GND	D_GND	SPI1_MO	SPI1_CLK	SPI2_MO	D_GND	D_GND	D_GND	D_GND	EINT208	D_GND	D_GND	D_GND	D_GND	D_GND	EINT29	EINT26	EINT28	D_GND	D_GND	D_GND	D_GND	D_GND	L
K	D_GND	SDA2	SDA1	D_GND	D_GND	D_GND	EINT34	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	EINT170	EINT169	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	EINT31	EINT27	EINT30	D_GND	D_GND	EINT164	EINT174	EINT173	K
J	D_GND	D_GND	Reserve	D_GND	D_GND	SPI3_CLK	EINT181	AP_URXD3	D_GND	AP_UTXD3	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	EINT205	EINT202	EINT201	D_GND	D_GND	EINT165	AP_URXD1	AP_UTXD1	J
H	D_GND	VMC_PMU	EINT133	D_GND	D_GND	SPI3_CSB	SPI3_MI	D_GND	BT_PRI_RXD	D_GND	BT_ACT_TXD	D_GND	D_GND	D_GND	AP_UTXD2	AP_URXD2	EINT6	D_GND	D_GND	D_GND	D_GND	EINT144	EINT143	D_GND	EINT199	EINT204	EINT200	D_GND	D_GND	D_GND	I2S0_BCK	I2S0_DI	H
G	D_GND	D_GND	D_GND	SPI0_MI	SPI0_CLK	D_GND	SPI3_MO	D_GND	D_GND	EINT5	EINT7	D_GND	D_GND	D_GND	EINT177	EINT178	D_GND	D_GND	D_GND	D_GND	D_GND	EINT135	EINT134	EINT130	EINT198	EINT197	EINT203	D_GND	D_GND	I2S0_MCK	I2S0_LRCK	I2S0_DO	G
F	SGMII_1_TXP	SGMII_1_TXN	D_GND	SPI0_MO	SPI0_CSB	D_GND	D_GND	EINT1	EINT74	EINT4	EINT0	EINT76	D_GND	D_GND	EINT83	EINT84	D_GND	D_GND	I2S2_LRCK	I2S2_MCK	I2S2_BCK	I2S2_DI	I2S1_DO	EINT82	EINT81	EINT80	EINT79	D_GND	D_GND	D_GND	D_GND	D_GND	F
E	D_GND	D_GND	SGMII_1_RXN	SGMII_1_RXP	D_GND	D_GND	D_GND	D_GND	EINT78	EINT77	EINT75	EINT73	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	EINT213	EINT212	EINT223	D_GND	D_GND	D_GND	D_GND	E
D	SGMII_0_RXP	SGMII_0_RXN	D_GND	D_GND	D_GND	D_GND	D_GND	SYSRSTB	PMIC_RESET_B	PCIE0_PERSTN	PCIE0_PEWAKEN	SCL0	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	PCIE_A_LN0_TXN	PCIE_A_LN0_TXP	PCIE_A_LN1_TXN	D_GND	D_GND	D_GND	D_GND	EINT214	EINT209	D_GND	D_GND	D_GND	D_GND	D_GND	D
C	D_GND	D_GND	SGMII_0_TXP	SGMII_0_TXN	VSYS	VSYS	VSIM1_PMU	VBUS	PWRKEY	KPCOL0	PCIE0_CLKREQN	SDA0	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	PCIE_A_LN1_TXP	D_GND	EINT40	VCN18_PMU	D_GND	EINT211	EINT210	D_GND	D_GND	D_GND	D_GND	D_GND	C
B	D_GND	MDIO	GBE1_INT	GBE1_RST	VSYS	VSYS	VSIM2_PMU	FULL_ON	SIM1_SRST	SIM2_SCLK	SIM2_SRST	D_GND	D_GND	SSUSB_RXN	D_GND	SSUSB_TXN	D_GND	USB_DP	D_GND	PCIE_A_LN1_RXP	D_GND	PCIE_A_LN0_RXP	D_GND	PCIE_A_CLKP	D_GND	D_GND	D_GND				D_GND	D_GND	B
A		MDC	GBE0_RST	GBE0_INT	VSYS	VSYS	VIO18_1_PMU	INT_SIM2	SIM1_SCLK	SIM2_SIO	SIM1_SIO	INT_SIM1	D_GND	SSUSB_RXP	D_GND	SSUSB_TXP	D_GND	USB_DM	D_GND	PCIE_A_LN1_RXN	D_GND	PCIE_A_LN0_RXN	D_GND	PCIE_A_CLKN	D_GND	EINT41	EINT42				D_GND	D_GND	A
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	

2.2 PIN DESCRIPTION

Pin assignment of UMC-STD35GX is defined in Table 2-2.
EINT32~EINT39 are boot strapping signals and suggest leave them not connected. In case have to use these pins as GPIOs, please make sure to control these pins after boot up sequence completed.
Table 2-2 Pin Assignment

Pin number	NAD Pad name	Pin description	Internal PU/PD	Power domain
A2	MDC	Management data clock reference of SGMII	PD	1.8V
A3	GBE0_RST	SGMII0 Reset	PD	1.8V
A4	GBE0_INT	SGMII0 interrupt	PD	1.8V
A5	VSYS	System power input		
A6	VSYS	System power input		
A7	VIO18_1_PMU	1V8 power output		1.8V
A8	INT_SIM2	SIM2 interrupt		1.8V
A9	SIM1_SCLK	SIM1 Clock	PD	1.8V/3V
A10	SIM2_SIO	SIM2 data	PD	1.8V/3V
A11	SIM1_SIO	SIM1 data	PD	1.8V/3V
A12	INT_SIM1	SIM1 interrupt		1.8V
A13	D_GND			
A14	SSUSB_RXP	Super-speed RX data		
A15	D_GND			
A16	SSUSB_TXP	Super-speed TX data		
A17	D_GND			
A18	USB_DM	USB D- differential data line		
A19	D_GND			
A20	PCIE_A_LN1_RXN	PCIe RX data lane1		
A21	D_GND			
A22	PCIE_A_LN0_RXN	PCIe RX data lane0		
A23	D_GND			
A24	PCIE_A_CLKN	PCIe clock		
A25	D_GND			
A26	EINT41	External interrupt input	PD	1.8V
A27	EINT42	External interrupt input	PD	1.8V
A31	D_GND			
A32	D_GND			
B1	D_GND			
B2	MDIO	Management data I/O of SGMII	PD	1.8V
B3	GBE1_INT	SGMII1 interrupt	PD	1.8V
B4	GBE1_RST	SGMII1 RST	PD	1.8V
B5	VSYS	System power input		
B6	VSYS	System power input		
B7	VSIM2_PMU	Power for SIM2		
B8	FULL_ON	Enable of PMIC		4V
B9	SIM1_SRST	SIM1 Reset	PD	1.8V/3V
B10	SIM2_SCLK	SIM2 clock	PD	1.8V/3V
B11	SIM2_SRST	SIM2 Reset	PD	1.8V/3V

B12	D_GND			
B13	D_GND			
B14	SSUSB_RXN	Super-speed RX data		
B15	D_GND			
B16	SSUSB_TXN	Super-speed RX data		
B17	D_GND			
B18	USB_DP	USB D+ differential data line		
B19	D_GND			
B20	PCIE_A_LN1_RXP	PCIe RX data lane1		
B21	D_GND			
B22	PCIE_A_LN0_RXP	PCIe lane0 RX		
B23	D_GND			
B24	PCIE_A_CLKP	PCIe clock		
B25	D_GND			
B26	D_GND			
B27	D_GND			
B31	D_GND			
B32	D_GND			
C1	D_GND			
C2	D_GND			
C3	SGMII_0_TXP	SGMII0 TX		
C4	SGMII_0_TXN	SGMII0 TX		
C5	VSYS	System power input		
C6	VSYS	System power input		
C7	VSIM1_PMU	Power for SIM1		
C8	VBUS	Detect of USB power		
C9	PWRKEY	Power key trigger		1.8V
C10	KPCOL0	Forced download key	PU	
C11	PCIE0_CLKREQN	PCIe clock request	PU	1.8V
C12	SDA0	I2C0 Data	PU	1.8V
C13	D_GND			
C14	D_GND			
C15	D_GND			
C16	D_GND			
C17	D_GND			
C18	D_GND			
C19	D_GND			
C20	D_GND			
C21	PCIE_A_LN1_TXP	PCIe lane1 TX		
C22	D_GND			
C23	EINT40	External interrupt input	PD	1.8V
C24	VCN18_PMU	1V8 power output for RF component		1.8V
C25	D_GND			
C26	EINT211	External interrupt input	PD	1.8V
C27	EINT210	External interrupt input	PD	1.8V

C28	D_GND			
C29	D_GND			
C30	D_GND			
C31	D_GND			
C32	D_GND			
D1	SGMII_0_RXP	SGMII0 RX		
D2	SGMII_0_RXN	SGMII0 RX		
D3	D_GND			
D4	D_GND			
D5	D_GND			
D6	D_GND			
D7	D_GND			
D8	SYSRSTB	PMIC reset output		1.8V
D9	PMIC_RESET_B	PMIC reset input		1.8V
D10	PCIE0_PERSTN	PCIe reset	PU	1.8V
D11	PCIE0_PEWAKEN	PCIe Wake	PU	1.8V
D12	SCL0	I2C0 Clock	PU	1.8V
D13	D_GND			
D14	D_GND			
D15	D_GND			
D16	D_GND			
D17	D_GND			
D18	D_GND			
D19	PCIE_A_LN0_TXN	PCIe lane0 TX		
D20	PCIE_A_LN0_TXP	PCIe lane0 TX		
D21	PCIE_A_LN1_TXN	PCIe lane1 TX		
D22	D_GND			
D23	D_GND			
D24	D_GND			
D25	D_GND			
D26	EINT214	External interrupt input	PD	1.8V
D27	EINT209	External interrupt input	PD	1.8V
D28	D_GND			
D29	D_GND			
D30	D_GND			
D31	D_GND			
D32	D_GND			
E1	D_GND			
E2	D_GND			
E3	SGMII_1_RXN	SGMII1 RX		
E4	SGMII_1_RXP	SGMII1 RX		
E5	D_GND			
E6	D_GND			
E7	D_GND			
E8	D_GND			

E9	EINT78	External interrupt input	PD	1.8V
E10	EINT77	External interrupt input	PD	1.8V
E11	EINT75	External interrupt input	PD	1.8V
E12	EINT73	External interrupt input	PD	1.8V
E13	D_GND			
E14	D_GND			
E15	D_GND			
E16	D_GND			
E17	D_GND			
E18	D_GND			
E19	D_GND			
E20	D_GND			
E21	D_GND			
E22	D_GND			
E23	D_GND			
E24	D_GND			
E25	D_GND			
E26	EINT213	External interrupt input	PD	1.8V
E27	EINT212	External interrupt input	PD	1.8V
E28	EINT223	External interrupt input	PD	1.8V
E29	D_GND			
E30	D_GND			
E31	D_GND			
E32	D_GND			
F1	SGMII_1_TXP	SGMII1 TX		
F2	SGMII_1_TXN	SGMII1 TX		
F3	D_GND			
F4	SPI0_MO	SPI0 Data out	PD	1.8V
F5	SPI0_CSB	SPI0 Chip select	PD	1.8V
F6	D_GND			
F7	D_GND			
F8	EINT1	External interrupt input	PD	1.8V
F9	EINT74	External interrupt input	PD	1.8V
F10	EINT4	External interrupt input	PD	1.8V
F11	EINT0	External interrupt input	PD	1.8V
F12	EINT76	External interrupt input	PD	1.8V
F13	D_GND			
F14	D_GND			
F15	(NC)	External interrupt input	PD	1.8V
F16	(NC)	External interrupt input	PD	1.8V
F17	D_GND			
F18	D_GND			
F19	I2S2_LRCK	I2S2 Word clock	PD	1.8V
F20	I2S2_MCK	I2S2 Master clock	PD	1.8V
F21	I2S2_BCK	I2S2 Bit clock	PD	1.8V

F22	I2S2_DI	I2S2 data in	PD	1.8V
F23	I2S1_DO	I2S1 data out	PD	1.8V
F24	EINT82	External interrupt input	PD	1.8V
F25	EINT81	External interrupt input	PD	1.8V
F26	EINT80	External interrupt input	PD	1.8V
F27	EINT79	External interrupt input	PD	1.8V
F28	D_GND			
F29	D_GND			
F30	D_GND			
F31	D_GND			
F32	D_GND			
G1	D_GND			
G2	D_GND			
G3	D_GND			
G4	SPI0_MI	SPI0 data in	PD	1.8V
G5	SPI0_CLK	SPI0 clock	PD	1.8V
G6	D_GND			
G7	SPI3_MO	SPI3 data out	PD	1.8V
G8	D_GND			
G9	D_GND			
G10	EINT5	External interrupt input	PD	1.8V
G11	EINT7	External interrupt input	PD	1.8V
G12	D_GND			
G13	D_GND			
G14	D_GND			
G15	EINT177	External interrupt input	PD	1.8V
G16	EINT178	External interrupt input	PD	1.8V
G17	D_GND			
G18	D_GND			
G19	D_GND			
G20	D_GND			
G21	D_GND			
G22	EINT135	External interrupt input	PD	1.8V
G23	EINT134	External interrupt input	PD	1.8V
G24	EINT130	External interrupt input	PD	1.8V
G25	EINT198	External interrupt input	PD	1.8V
G26	EINT197	External interrupt input	PD	1.8V
G27	EINT203	External interrupt input	PD	1.8V
G28	D_GND			
G29	D_GND			
G30	I2S0_MCK	I2S0 Master clock	PD	1.8V
G31	I2S0_LRCK	I2S0 Word clock	PD	1.8V
G32	I2S0_DO	I2S0 Data out	PD	1.8V
H1	D_GND			
H2	VMC_PMU	Power for MSDC1		

H3	EINT133	External interrupt input	PD	1.8V
H4	D_GND			
H5	D_GND			
H6	SPI3_CSB	SPI3 Chip select	PD	1.8V
H7	SPI3_MI	SPI3 data in	PD	1.8V
H8	D_GND			
H9	BT_PRI_RXD	NC	PD	1.8V
H10	D_GND			
H11	BT_ACT_TXD	NC	PD	1.8V
H12	D_GND			
H13	D_GND			
H14	D_GND			
H15	AP_UTXD2	UART TX	PD	1.8V
H16	AP_URXD2	UART RX	PD	1.8V
H17	EINT6	External interrupt input	PD	1.8V
H18	D_GND			
H19	D_GND			
H20	D_GND			
H21	D_GND			
H22	EINT144	External interrupt input	PD	1.8V
H23	EINT143	External interrupt input	PD	1.8V
H24	D_GND			
H25	EINT199	External interrupt input	PD	1.8V
H26	EINT204	External interrupt input	PD	1.8V
H27	EINT200	External interrupt input	PD	1.8V
H28	D_GND			
H29	D_GND			
H30	D_GND			
H31	I2S0_BCK	I2S0 Bit clock	PD	1.8V
H32	I2S0_DI	I2S0 Data in	PD	1.8V
J1	D_GND			
J2	D_GND			
J3	VEMC_PMU	Power for MSDC0		
J4	D_GND			
J5	D_GND			
J6	SPI3_CLK	SPI3 Clock	PD	1.8V
J7	EINT181	External interrupt input	PD	1.8V
J8	AP_URXD3	UART3 RX	PD	1.8V
J9	D_GND			
J10	AP_UTXD3	UART3 TX	PD	1.8V
J11	D_GND			
J12	D_GND			
J13	D_GND			
J14	D_GND			
J15	D_GND			

J16	D_GND			
J17	D_GND			
J18	D_GND			
J19	D_GND			
J20	D_GND			
J21	D_GND			
J22	D_GND			
J23	D_GND			
J24	D_GND			
J25	EINT205	External interrupt input	PD	1.8V
J26	EINT202	External interrupt input	PD	1.8V
J27	EINT201	External interrupt input	PD	1.8V
J28	D_GND			
J29	D_GND			
J30	(NC)	External interrupt input	PD	1.8V
J31	AP_URXD1	UART RX	PD	1.8V
J32	AP_UTXD1	UART TX	PD	1.8V
K1	D_GND			
K2	SDA2	I2C2 data	PU	1.8V
K3	SDA1	I2C1 data	PU	1.8V
K4	D_GND			
K5	D_GND			
K6	D_GND			
K7	EINT34	External interrupt input	PD	1.8V
K8	D_GND			
K9	D_GND			
K10	D_GND			
K11	D_GND			
K12	D_GND			
K13	D_GND			
K14	D_GND			
K15	EINT170	External interrupt input	PU	1.8V
K16	EINT169	External interrupt input	PU	1.8V
K17	D_GND			
K18	D_GND			
K19	D_GND			
K20	D_GND			
K21	D_GND			
K22	D_GND			
K23	D_GND			
K24	D_GND			
K25	EINT31	External interrupt input	PD	1.8V
K26	EINT27	External interrupt input	PD	1.8V
K27	EINT30	External interrupt input	PD	1.8V
K28	D_GND			

K29	D_GND			
K30	(NC)	External interrupt input	PD	1.8V
K31	EINT174	External interrupt input	PD	1.8V
K32	EINT173	External interrupt input	PD	1.8V
L1	D_GND			
L2	SCL2	I2C2 Clock	PU	1.8V
L3	SCL1	I2C1 clock	PU	1.8V
L4	EINT32	External interrupt input	PD	1.8V
L5	D_GND			
L6	D_GND			
L7	EINT182	External interrupt input	PD	1.8V
L8	D_GND			
L9	D_GND			
L10	D_GND			
L11	D_GND			
L12	SPI1_MO	SPI1 data out	PD	1.8V
L13	SPI1_CLK	SPI1 clock	PD	1.8V
L14	SPI2_MO	SPI2 data out	PD	1.8V
L15	D_GND			
L16	D_GND			
L17	D_GND			
L18	D_GND			
L19	EINT208	External interrupt input	PD	1.8V
L20	D_GND			
L21	D_GND			
L22	D_GND			
L23	D_GND			
L24	D_GND			
L25	EINT29	External interrupt input	PD	1.8V
L26	EINT26	External interrupt input	PD	1.8V
L27	EINT28	External interrupt input	PD	1.8V
L28	D_GND			
L29	D_GND			
L30	D_GND			
L31	D_GND			
L32	D_GND			
M1	D_GND			
M2	D_GND			
M3	EINT99	External interrupt input	PD	1.8V
M4	EINT38	External interrupt input	PD	1.8V
M5	EINT33	External interrupt input	PD	1.8V
M6	D_GND			
M7	D_GND			
M8	D_GND			
M9	D_GND			

M10	D_GND			
M11	D_GND			
M12	SPI1_CSB	SPI1 chip select	PD	1.8V
M13	SPI1_MI	SPI1 data in	PD	1.8V
M14	SPI2_MI	SPI2 data in	PD	1.8V
M15	D_GND			
M16	SPI2_CLK	SPI2 clock	PD	1.8V
M17	AUXIN3	AUXADC ch3		
M18	D_GND			
M19	EINT207	External interrupt input	PD	1.8V
M20	D_GND			
M21	D_GND			
M22	D_GND			
M23	D_GND			
M24	D_GND			
M25	D_GND			
M26	D_GND			
M27	D_GND			
M28	D_GND			
M29	D_GND			
M30	D_GND			
M31	D_GND			
M32	D_GND			
N1	D_GND			
N2	D_GND			
N3	EINT98	External interrupt input	PD	1.8V
N4	EINT35	External interrupt input	PD	1.8V
N5	D_GND			
N6	GBE_RXD3	RGMII RX data3	PD	1.8V
N7	GBE_MDIO	Management data I/O of RGMII	PD	1.8V
N8	GBE_TXD1	RGMII TX data1	PD	1.8V
N9	D_GND			
N10	D_GND			
N11	D_GND			
N12	D_GND			
N13	SPI2_CSB	SPI2 chip select	PD	1.8V
N14	AP_URXD0	UART0 RX	PU	1.8V
N15	AP_UTXD0	UART0 TX	PU	1.8V
N16	AUXIN1	AUXADC ch1		
N17	AUXIN2	AUXADC ch2		
N18	AUXIN0	AUXADC ch0		
N19	EINT206	External interrupt input	PD	1.8V
N20	D_GND			
N21	D_GND			
N22	D_GND			

N23	D_GND			
N24	D_GND			
N25	MSDC1_DAT0	MSDC1 data0	PD	1.8V
N26	MSDC1_DAT1	MSDC1 data1	PD	1.8V
N27	MSDC1_CMD	MSDC1 command	PD	1.8V
N28	D_GND			
N29	WATCHDOG		PD	1.8V
N30	D_GND			
N31	EINT138	External interrupt input	PD	1.8V
N32	EINT141	External interrupt input	PD	1.8V
P1	D_GND			
P2	D_GND			
P3	EINT96	External interrupt input	PD	1.8V
P4	EINT36	External interrupt input	PD	1.8V
P5	EINT37	External interrupt input	PD	1.8V
P6	GBE_RXD2	RGMII RX data2	PD	1.8V
P7	GBE_RXD0	RGMII RX data0	PD	1.8V
P8	GBE_RXDV	RGMII receive data valid	PD	1.8V
P9	D_GND			
P10	D_GND			
P11	D_GND			
P12	D_GND			
P13	D_GND			
P14	D_GND			
P15	D_GND			
P16	D_GND			
P17	D_GND			
P18	D_GND			
P19	D_GND			
P20	D_GND			
P21	D_GND			
P22	D_GND			
P23	D_GND			
P24	D_GND			
P25	MSDC1_DAT3	MSDC1 data3	PD	1.8V
P26	MSDC1_CLK	MSDC1 clock	PD	1.8V
P27	MSDC1_DAT2	MSDC1 data2	PD	1.8V
P28	D_GND			
P29	D_GND			
P30	D_GND			
P31	EINT140	External interrupt input	PD	1.8V
P32	EINT139	External interrupt input	PD	1.8V
R1	D_GND			
R2	D_GND			
R3	EINT100	External interrupt input	PD	1.8V

R4	D_GND			
R5	EINT39	External interrupt input	PD	1.8V
R6	GBE_MDC	Management data clock of RGMII	PD	1.8V
R7	GBE_COL	RGMII Collision	PD	1.8V
R8	GBE_TXC	RGMII TX clock	PD	1.8V
R9	D_GND			
R10	D_GND			
R11	D_GND			
R12	D_GND			
R13	D_GND			
R14	D_GND			
R15	D_GND			
R16	D_GND			
R17	D_GND			
R18	D_GND			
R19	D_GND			
R20	D_GND			
R21	D_GND			
R22	D_GND			
R23	D_GND			
R24	D_GND			
R25	D_GND			
R26	D_GND			
R27	D_GND			
R28	D_GND			
R29	D_GND			
R30	D_GND			
R31	D_GND			
R32	D_GND			
S1	D_GND			
S2	D_GND			
S3	EINT97	External interrupt input	PD	1.8V
S4	D_GND			
S5	D_GND			
S6	GBE_TXEN	RGMII transmit enable	PD	1.8V
S7	GBE_TXD0	RGMII TX data0	PD	1.8V
S8	GBE_INTR	RGMII interrupt	PD	1.8V
S9	D_GND			
S10	D_GND			
S11	D_GND			
S12	D_GND			
S13	D_GND			
S14	D_GND			
S15	D_GND			
S16	D_GND			

S17	D_GND			
S18	D_GND			
S19	D_GND			
S20	D_GND			
S21	D_GND			
S22	D_GND			
S23	D_GND			
S24	D_GND			
S25	D_GND			
S26	D_GND			
S27	D_GND			
S28	D_GND			
S29	D_GND			
S30	D_GND			
S31	D_GND			
S32	D_GND			
T1	D_GND			
T2	D_GND			
T3	D_GND			
T4	D_GND			
T5	D_GND			
T6	GBE_RXD1	RGMII RX data1	PD	1.8V
T7	GBE_RXER	RGMII RX error	PD	1.8V
T8	GBE_TXD2	RGMII TX data2	PD	1.8V
T9	D_GND			
T10	D_GND			
T11	D_GND			
T12	D_GND			
T13	D_GND			
T14	D_GND			
T15	D_GND			
T16	D_GND			
T17	D_GND			
T18	D_GND			
T19	D_GND			
T20	D_GND			
T21	D_GND			
T22	D_GND			
T23	D_GND			
T24	D_GND			
T25	D_GND			
T26	D_GND			
T27	D_GND			
T28	D_GND			
T29	VCC_VRF1	RF power input		

T30	VCC_VRF1	RF power input		
T31	VCC_VRF3	RF power input		
T32	VCC_VRF2	RF power input		
U3	D_GND			
U4	D_GND			
U5	D_GND			
U6	GBE_TXER	RGMII TX error	PD	1.8V
U7	GBE_RXC	RGMII RX clock	PD	1.8V
U8	GBE_TXD3	RGMII TX data3	PD	1.8V
U9	D_GND			
U10	D_GND			
U11	D_GND			
U12	D_GND			
U13	D_GND			
U14	D_GND			
U15	D_GND			
U16	D_GND			
U17	D_GND			
U18	D_GND			
U19	D_GND			
U20	D_GND			
U21	D_GND			
U22	D_GND			
U23	D_GND			
U24	D_GND			
U25	D_GND			
U26	D_GND			
U27	D_GND			
U28	D_GND			
U29	VCC_VRF1	RF power input		
U30	VCC_VRF1	RF power input		
U31	VCC_VRF3	RF power input		
U32	VCC_VRF2	RF power input		
V3	D_GND			
V4	D_GND			
V5	D_GND			
V6	D_GND			
V7	D_GND			
V8	D_GND			
V9	D_GND			
V10	D_GND			
V11	D_GND			
V12	D_GND			
V13	D_GND			
V14	D_GND			

V15	D_GND			
V16	D_GND			
V17	D_GND			
V18	D_GND			
V19	D_GND			
V20	D_GND			
V21	D_GND			
V22	D_GND			
V23	D_GND			
V24	D_GND			
V25	D_GND			
V26	D_GND			
V27	D_GND			
V28	D_GND			
V29	D_GND			
V30	D_GND			
V31	D_GND			
V32	D_GND			
W3	D_GND			
W4	D_GND			
W5	D_GND			
W6	D_GND			
W7	D_GND			
W8	D_GND			
W9	D_GND			
W10	D_GND			
W11	D_GND			
W12	D_GND			
W13	D_GND			
W14	D_GND			
W15	D_GND			
W16	D_GND			
W17	D_GND			
W18	D_GND			
W19	D_GND			
W20	D_GND			
W21	D_GND			
W22	D_GND			
W23	D_GND			
W24	D_GND			
W25	D_GND			
W26	D_GND			
W27	D_GND			
W28	D_GND			
W29	D_GND			

W30	D_GND			
W31	D_GND			
W32	D_GND			
Y1	D_GND			
Y2	D_GND			
Y3	D_GND			
Y4	D_GND			
Y5	D_GND			
Y6	D_GND			
Y7	D_GND			
Y8	D_GND			
Y9	D_GND			
Y10	D_GND			
Y11	D_GND			
Y12	D_GND			
Y13	D_GND			
Y14	D_GND			
Y15	D_GND			
Y16	D_GND			
Y17	D_GND			
Y18	D_GND			
Y19	D_GND			
Y20	D_GND			
Y21	D_GND			
Y22	D_GND			
Y23	D_GND			
Y24	D_GND			
Y25	D_GND			
Y26	D_GND			
Y27	D_GND			
Y28	D_GND			
Y29	D_GND			
Y30	D_GND			
AA1	D_GND			
AA2	D_GND			
AA3	D_GND			
AA4	D_GND			
AA5	D_GND			
AA6	D_GND			
AA7	D_GND			
AA8	D_GND			
AA9	D_GND			
AA10	D_GND			
AA11	D_GND			
AA12	D_GND			

AA13	D_GND			
AA14	D_GND			
AA15	D_GND			
AA16	D_GND			
AA17	D_GND			
AA18	D_GND			
AA19	D_GND			
AA20	D_GND			
AA21	D_GND			
AA22	D_GND			
AA23	D_GND			
AA24	D_GND			
AA25	D_GND			
AA26	D_GND			
AA27	D_GND			
AA28	D_GND			
AA29	D_GND			
AA30	D_GND			
AB1	RF_GNSS_L1_L5_ANT	RF antenna		
AB2	D_GND			
AB3	D_GND			
AB4	D_GND			
AB5	D_GND			
AB6	D_GND			
AB7	D_GND			
AB8	D_GND			
AB9	D_GND			
AB10	D_GND			
AB11	D_GND			
AB12	D_GND			
AB13	D_GND			
AB14	D_GND			
AB15	D_GND			
AB16	D_GND			
AB17	D_GND			
AB18	D_GND			
AB19	D_GND			
AB20	D_GND			
AB21	D_GND			
AB22	D_GND			
AB23	D_GND			
AB24	D_GND			
AB25	D_GND			
AB26	D_GND			
AB27	D_GND			

AB28	D_GND			
AB29	D_GND			
AB30	D_GND			
AC1	D_GND			
AC2	D_GND			
AC3	D_GND			
AC4	D_GND			
AC5	D_GND			
AC6	D_GND			
AC7	D_GND			
AC8	D_GND			
AC9	D_GND			
AC10	D_GND			
AC11	D_GND			
AC12	D_GND			
AC13	D_GND			
AC14	D_GND			
AC15	D_GND			
AC16	D_GND			
AC17	D_GND			
AC18	D_GND			
AC19	D_GND			
AC20	D_GND			
AC21	D_GND			
AC22	D_GND			
AC23	D_GND			
AC24	D_GND			
AC25	D_GND			
AC26	D_GND			
AC27	D_GND			
AC28	D_GND			
AC29	D_GND			
AC30	D_GND			
AC31	D_GND			
AC32	D_GND			
AD1	D_GND			
AD2	D_GND			
AD3	D_GND			
AD4	D_GND			
AD5	D_GND			
AD6	D_GND			
AD7	D_GND			
AD8	D_GND			
AD9	D_GND			
AD10	D_GND			

AD11	D_GND			
AD12	D_GND			
AD13	D_GND			
AD14	D_GND			
AD15	D_GND			
AD16	D_GND			
AD17	D_GND			
AD18	D_GND			
AD19	D_GND			
AD20	D_GND			
AD21	D_GND			
AD22	D_GND			
AD23	D_GND			
AD24	D_GND			
AD25	D_GND			
AD26	D_GND			
AD27	D_GND			
AD28	D_GND			
AD29	D_GND			
AD30	D_GND			
AD31	D_GND			
AD32	D_GND			
AE1	D_GND			
AE2	D_GND			
AE3	D_GND			
AE4	D_GND			
AE5	D_GND			
AE6	D_GND			
AE7	D_GND			
AE8	D_GND			
AE9	D_GND			
AE10	D_GND			
AE11	D_GND			
AE12	D_GND			
AE13	D_GND			
AE14	D_GND			
AE15	D_GND			
AE16	D_GND			
AE17	D_GND			
AE18	D_GND			
AE19	D_GND			
AE20	D_GND			
AE21	D_GND			
AE22	D_GND			
AE23	D_GND			

AE24	D_GND			
AE25	D_GND			
AE26	D_GND			
AE27	D_GND			
AE28	D_GND			
AE29	D_GND			
AE30	D_GND			
AE31	D_GND			
AE32	D_GND			
AF1	D_GND			
AF2	D_GND			
AF3	D_GND			
AF4	D_GND			
AF5	D_GND			
AF6	D_GND			
AF7	D_GND			
AF8	D_GND			
AF9	D_GND			
AF10	D_GND			
AF11	D_GND			
AF12	D_GND			
AF13	D_GND			
AF14	D_GND			
AF15	D_GND			
AF16	D_GND			
AF17	D_GND			
AF18	D_GND			
AF19	D_GND			
AF20	D_GND			
AF21	D_GND			
AF22	D_GND			
AF23	D_GND			
AF24	D_GND			
AF25	D_GND			
AF26	D_GND			
AF27	D_GND			
AF28	D_GND			
AF29	D_GND			
AF30	D_GND			
AF31	D_GND			
AF32	D_GND			
AG1	D_GND			
AG2	D_GND			
AG3	D_GND			
AG4	D_GND			

AG5	D_GND			
AG6	D_GND			
AG7	D_GND			
AG8	D_GND			
AG9	D_GND			
AG10	D_GND			
AG11	D_GND			
AG12	D_GND			
AG13	D_GND			
AG14	D_GND			
AG15	D_GND			
AG16	D_GND			
AG17	D_GND			
AG18	D_GND			
AG19	D_GND			
AG20	D_GND			
AG21	D_GND			
AG22	D_GND			
AG23	D_GND			
AG24	D_GND			
AG25	D_GND			
AG26	D_GND			
AG27	D_GND			
AG28	D_GND			
AG29	D_GND			
AG30	D_GND			
AG31	D_GND			
AG32	D_GND			
AH1	D_GND			
AH2	D_GND			
AH3	D_GND			
AH4	ANT3_MIMO1	RF antenna		
AH5	D_GND			
AH6	ANT4_MIMO2	RF antenna		
AH7	D_GND			
AH8	D_GND			
AH9	D_GND			
AH10	D_GND			
AH11	D_GND			
AH12	D_GND			
AH13	ANT2	RF antenna		
AH14	D_GND			
AH15	D_GND			
AH16	D_GND			
AH17	D_GND			

AH18	D_GND			
AH19	D_GND			
AH20	D_GND			
AH21	D_GND			
AH22	D_GND			
AH23	D_GND			
AH24	D_GND			
AH25	ANT1	RF antenna		
AH26	D_GND			
AH27	D_GND			
AH28	D_GND			
AH29	D_GND			
AH30	D_GND			
AH31	D_GND			
AH32	D_GND			

3. NAD SPECIFICATIONS

This chapter describes maximum ratings, operating condition, power on/off and reset timing.

3.1 ABSOLUTE MAXIMUM RATINGS

Table 3-1

Parameter	Minimum	Maximum	Unit
Power-supply Voltages			
VSYS	-0.5	6	V
VRF1	-0.5	6	V
VRF2	-0.5	6	V
VRF3	-0.5	6	V
VSIM1_PMU	0	5	V
VSIM2_PMU	0	5	V
VIO18_1_PMU	0	1.98	V
VCN18_1_PMU	0	2.2	V
Signal Pins			
Digital power for I/O	-0.3	2.1	V
Thermal Conditions			
Ambient	-40	85	deg-C
Environmental			
Operating Humidity	--	85	%RH

3.2 OPERATING CONDITIONS

Table 3-2

tbc# data will be confirmed later after UMC-STD35GX software is completed

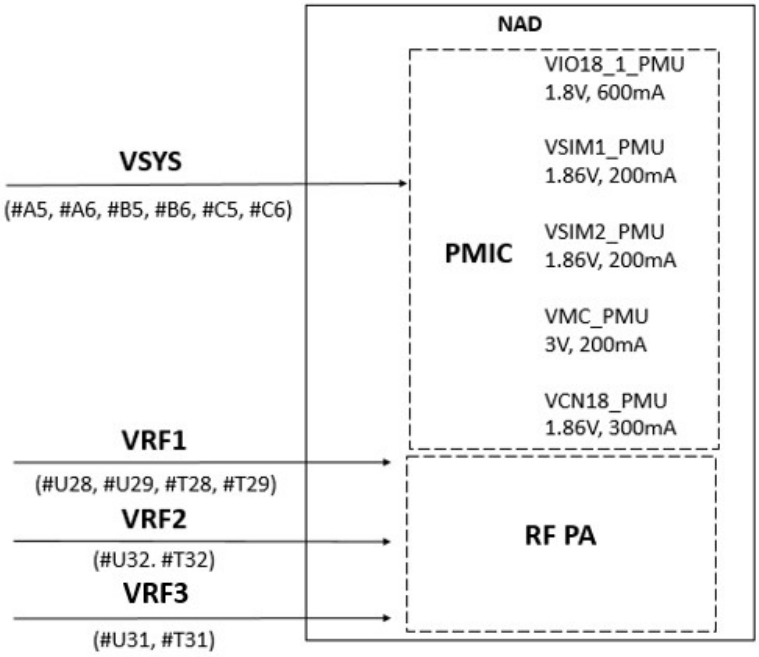
Parameter		Minimum	Typical	Maximum	Unit
Power-supply Voltages					
VSYS	NAD system voltage	4.5	4.7	4.9	V
VBUS	USB bus supply voltage	4.75	5	5.25	V
VRF1	RFFE supply voltage1	4.0	4.2	4.4	V
VRF2	RFFE supply voltage2	4.5	4.7	4.9	V
VRF3	RFFE supply voltage3	4.5	4.7	4.9	V
VSIM1_PMU	Output voltage for UIM1	1.82	1.86	1.90	V
		2.94	3.00	3.06	V
VSIM2_PMU	Output voltage for UIM2	1.82	1.86	1.90	V
		2.94	3.00	3.06	V
VIO18_1_PMU	Output voltage for external GNSS	1.76	1.8	1.84	V
VMC_PMU	Output voltage for external SDC	2.94	3.00	3.06	V

VCN18_PMU	Output voltage reserved for external Wireless Connectivity	1.82	1.84	1.88	V
Power-supply Currents					
LPM(AIR1)	Airplane mode	n/a	5.8	n/a	mA
Standby(GS1)	GSM standby 0.64 sec	n/a	10.2	n/a	mA
Standby(WS1)	WCDMA standby 2.56 sec	n/a	10.9	n/a	mA
Standby(LS1)	LTE standby 2.56 sec	n/a	10.2	n/a	mA
Standby(LS3)	LTE TDD standby 2.56 sec	n/a	10.5	n/a	mA
Standby(5GSUB6-C01)	NR Sub6 TDD 1CC 100-MHz CDRX and LTE CDRX	n/a	10.3	n/a	mA
Talk(GT1)	GSM talk 5-dBm, no DTX, PGSM	n/a	121.2	310	mA
Talk(WT1)	WCDMA talk FET on 0% voice	n/a	200.8	400	mA
Talk(VoLTE1)	VoLTE FDD(40-ms DRX cycle, 0-dBm, MIMO, B13)	n/a	326	624	mA
Talk(VoLTE6)	VoLTE TDD(40-ms DRX cycle, 0-dBm, MIMO, B38)	n/a	311	561	mA
Talk(VoNR1)	VoNR FDD	n/a	398	643	mA
Talk(VoNR6)	VoNR TDD	n/a	323	577	mA
Link(HS61E)	DC HSDPA downlink 42-Mbps/0-dBm, IMT(No RxD)	n/a	232.1	448	mA
Thermal Conditions	(*)be extended to 95 for eCall				
	NAD operating temperature(ambient)	-40	25	85*	degree-C
	3GPP operating temperature(ambient)	-30	25	70	degree-C

*Only for reference once complete DVT will update
* The value is reference to STD35 test data.

3.3 POWER-DISTRIBUTION NETWORK

Refer to the power delivery network diagram of UMC-STD35GX HDK (Hardware Development Kit)



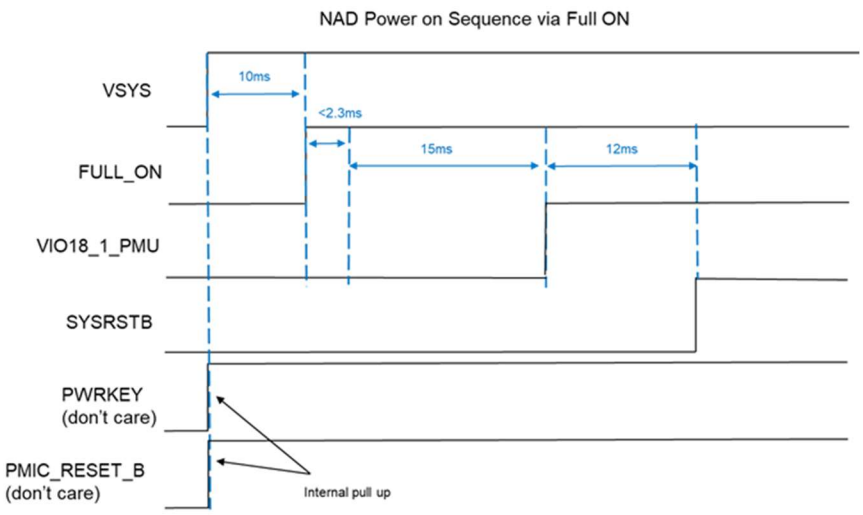
3.4 POWER-SUPPLY SEQUENCES

3.4.1 POWER ON SEQUENCES

FULL_ON(NAD/Pad#B8) is recommended to handle Power-on/-off of NAD, and to use PWRKEY(NAD/Pad#C9) to trigger the re-booting of NAD.

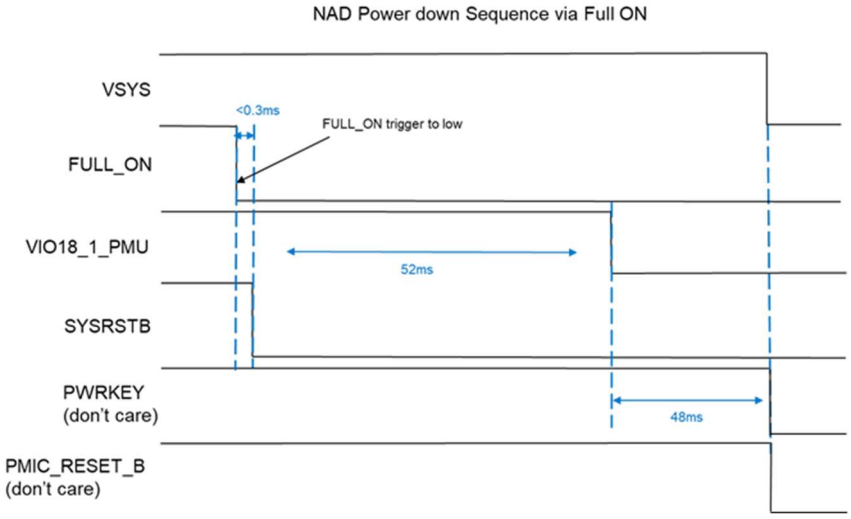
*VBUS(NAD/Pad#C8) will also trigger power-on NAD. Please make sure the VBUS is low (no power) before turn on NAD.
*Pull low PWRKEY(NAD/Pad#C9) for 9 second will re-booting NAD.

Power-on sequence according FULL_ON



3.4.2 POWER OFF SEQUENCES

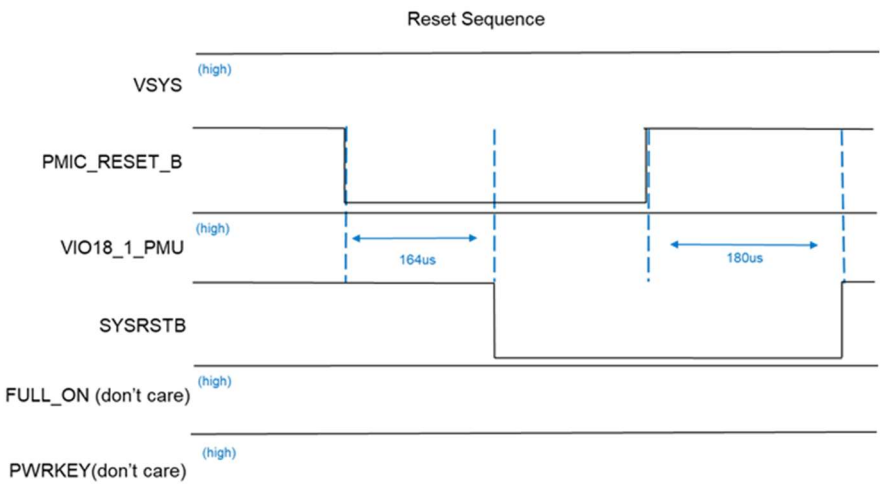
Power-off sequence according FULL_ON



3.4.3 RESET SEQUENCES

NAD RESET SEQUENCE BY PMIC_RESET_B (NAD/PAD#C12)

*Use PMIC_RESET_B (NAD/PAD#C12) will reset CPU without power off/on NAD.



3.5 AIR INTERFACE NETWORKING

Listed here are all combinations defined in 3GPP Release 15 (relative to LTE)/16 (relative to NR), and then showing the compliance table of each section according the hardware capability of UMC-STD35GX A-sample RF Front-end. Later on, these tables will be revised based on MTK coming software supported on their MT2735 platform.

3.5.1 LTE RECEIVING CA SUPPORTING LIST

Dedicated document of CA/ENDC supporting list will be released.

3.5.2 NR RECEIVING CA SUPPORTING LIST

Dedicated document of CA/ENDC supporting list will be released.

3.5.3 EN-DC SUPPORTING LIST

Dedicated document of CA/ENDC supporting list will be released.

3.5.4 RF OUTPUT POWER

Table 3-8

Item	Bands	Minimum	Typical	Maximum	Unit
Maximum Output Power					
5G NR	FR1 Sub-6G bands	21	23	25	dBm
5G NR HPUE	n78 for Row & EU Sku n41 /n77 for NA Sku	24	26	28	dBm
LTE	All bands	21	23	25	dBm
WCDMA	All bands	21	24	25	dBm
GSM	850、900	31	33	35	dBm
GSM	1800、1900	28	30	32	dBm

Minimum Output Power					
5G NR	FR1 Sub-6G bands (BW:<20MHz)	--	--	-40	dBm
LTE	All bands	--	--	-40	dBm
WCDMA	All bands	--	--	-50	dBm

3.5.5 RF RECEIVING SENSITIVITY

Table 3-9

Mode	Bands	Minimum	Typical	Maximum	Unit
NR Receiving Sensitivity (Two antenna port)					
5G NR	n1 (BW:20MHz, SCS: 15kHz)	--	--	-93.1	dBm
5G NR	n2 (BW:20MHz, SCS: 15kHz)	--	--	-91.1	dBm
5G NR	n3 (BW:20MHz, SCS: 15kHz)	--	--	-90.1	dBm
5G NR	n5 (BW:10MHz, SCS: 15kHz)	--	--	-94.1	dBm
5G NR	n7 (BW:20MHz, SCS: 15kHz)	--	--	-91.1	dBm
5G NR	n8 (BW:10MHz, SCS: 15kHz)	--	--	-93.1	dBm
5G NR	n28 (BW:10MHz, SCS: 15kHz)	--	--	-94.8	dBm
5G NR	n41 (BW:100MHz, SCS: 30kHz)	--	--	-84	dBm
5G NR	n66 (BW:20MHz, SCS: 15kHz)	--	--	-92.6	dBm
5G NR	n77 (BW:100MHz, SCS: 30kHz)	--	--	-84.4	dBm
5G NR	n78 (BW:100MHz, SCS: 30kHz)	--	--	-84.9	dBm
5G NR	n79 (BW:100MHz, SCS: 30kHz)	--	--	-84.9	dBm
NR Receiving Sensitivity (Four antenna port)					
5G NR	n1 (BW:20MHz, SCS: 15kHz)	--	--	-95.8	dBm
5G NR	n2 (BW:20MHz, SCS: 15kHz)	--	--	-93.8	dBm
5G NR	n3 (BW:20MHz, SCS: 15kHz)	--	--	-92.8	dBm
5G NR	n7 (BW:20MHz, SCS: 15kHz)	--	--	-93.8	dBm
5G NR	n41 (BW:100MHz, SCS: 30kHz)	--	--	-86.7	dBm
5G NR	n66 (BW:20MHz, SCS: 15kHz)	--	--	-95.3	dBm
5G NR	n77 (BW:100MHz, SCS: 30kHz)	--	--	-86.6	dBm
5G NR	n78 (BW:100MHz, SCS: 30kHz)	--	--	-87.1	dBm
5G NR	n79 (BW:100MHz, SCS: 30kHz)	--	--	-87.1	dBm
LTE Receiving Sensitivity					
LTE	B1 (BW:10MHz)	--	--	-96.3	dBm
LTE	B2 (BW:10MHz)	--	--	-94.3	dBm
LTE	B3 (BW:10MHz)	--	--	-93.3	dBm
LTE	B4 (BW:10MHz)	--	--	-96.3	dBm
LTE	B5 (BW:10MHz)	--	--	-94.3	dBm
LTE	B6 (BW:10MHz)	--	--	-96.3	dBm
LTE	B7 (BW:10MHz)	--	--	-94.3	dBm
LTE	B8 (BW:10MHz)	--	--	-93.3	dBm
LTE	B9 (BW:10MHz)	--	--	-95.3	dBm
LTE	B12 (BW:10MHz)	--	--	-93.3	dBm
LTE	B13 (BW:10MHz)	--	--	-93.3	dBm

LTE	B14 (BW:10MHz)	--	--	-93.3	dBm
LTE	B17 (BW:10MHz)	--	--	-93.3	dBm
LTE	B18 (BW:10MHz)	--	--	-96.3	dBm
LTE	B19 (BW:10MHz)	--	--	-96.3	dBm
LTE	B20 (BW:10MHz)	--	--	-93.3	dBm
LTE	B25 (BW:10MHz)	--	--	-92.8	dBm
LTE	B26 (BW:10MHz)	--	--	-93.8	dBm
LTE	B28 (BW:10MHz)	--	--	-94.8	dBm
LTE	B29 (BW:10MHz)	--	--	-93.3	dBm
LTE	B30 (BW:10MHz)	--	--	-95.3	dBm
LTE	B32 (BW:10MHz)	--	--	-96.5	dBm
LTE	B34 (BW:10MHz)	--	--	-96.3	dBm
LTE	B38 (BW:10MHz)	--	--	-96.3	dBm
LTE	B39 (BW:10MHz)	--	--	-96.3	dBm
LTE	B40 (BW:10MHz)	--	--	-96.3	dBm
LTE	B41 (BW:10MHz)	--	--	-94.3	dBm
LTE	B66 (BW:10MHz)	--	--	-95.8	dBm
LTE	B71 (BW:10MHz)	--	--	-93.5	dBm
WCDMA Receiving Sensitivity					
WCDMA	B1	--	--	-106.7	dBm
WCDMA	B2	--	--	-104.7	dBm
WCDMA	B3	--	--	-103.7	dBm
WCDMA	B4	--	--	-106.7	dBm
WCDMA	B5	--	--	-104.7	dBm
WCDMA	B6	--	--	-106.7	dBm
WCDMA	B8	--	--	-103.7	dBm
WCDMA	B9	--	--	-105.7	dBm
WCDMA	B19	--	--	-106.7	dBm
GSM Receiving Sensitivity					
GSM	850	--	--	-102	dBm
GSM	900	--	--	-102	dBm
GSM	1800	--	--	-102	dBm
GSM	1900	--	--	-102	dBm

3.5.6 GNSS PERFORMANCE

Table 3-10

Item	Parameter	Minimum	Typical	Maximum	Unit
Sensitivity	Tracking	--	-163	--	dBm
	Cold start acquisition	--	-146	--	dBm
	Hot start acquisition	--	-155	--	dBm
TTFF	Cold start	--	33	--	s
	Warm tart	--	32	--	s
	Hot start	--	1	--	s
Accuracy	Horizontal (CEP-50)	--	4.5	--	m

* The performance is tested with external GNSS LNAs.
* UMC-STD35GX NAD module support L1 only for C sample or later.

3.5.7 SRS SWITCHING TIME

Item	Bands	Minimum	Typical	Maximum	Unit
1T2R(NR SA mode only) 5G NR HPUE	N41	--	--	2ms	ms
	N77	--	--	2ms	ms
	N78	--	--	2ms	ms

*Only for reference once complete C sample DV test will update

4. Design guide

4.1 RF DESIGN GUIDE

4.1.1 GNSS performance

- Keep the nominal impedance for RF Antenna traces as 50 Ω with ground cleared above and below.
- As lots of ground via as possible to stitch around critical RF traces and sensitive analog signals to provide coplanar isolation and protection.
- Reserve the π-type matching elements for better RF characteristic.
- RF Antenna traces must be routed away from the noise sources such as USB interface, display connector, switching power supplies.

4.2 BASEBAND DESIGN GUIDE

4.2.1 MSDC interface

Schematic

- Use VMC for VCC of the SD

Layout

- Please keep SD card near NAD module. The Max. trace length should not be over 2 inch, and need to follow length matching.
- Length matching

A. |clock - Data/CMD|<= 150 mil

4.2.2 I2C interface

Schematic

- I2C0~I2C5 have internal pull up 1K ohm and external pull resistors are not required.
- Recommend to configure I/O type to open drain (internal pull up 1Kohm) for I2C standard mode, fast mode and fast mode plus.
- For I2C High speed mode, recommend using Push-pull type.
- I2C address must be unique for the devices in the same I2C bus.
- I2C0 support Slave mode, the slave address is 0x20.

Layout

N/A

4.2.3 SPI interface

Schematic

- Maximum data rate: 52Mbit/s

Layout

- SPI clock should be double side GND shielded and kept reference ground complete.

- SPI data should be grounded in both sides to reduce interference.
- The max length of SPI bus between SOC and PMIC should be less than 5 inches.

4.2.4 SIM interface

Schematic

- SIM Power, Reserve 1uF capacitor on the power rails of SIM with shunt connection and this capacitor should be placed close to SIM connector.
- SIO/SCLK/SRST don't need reserve Pull up resistor to VSIM.
- SIMDATA，SIMRST，SIMCLK, reserve capacitor or ESD component(Default no mount)，Cload<45pF
- Use INT_SIM1 for SIM1 hot plug, INT_SIM2 for SIM2 hot plug.

Layout

- ESD component should be placed closed to SIM connector.
- SIM CLK needs well ground shielding, SIMIO and SIMCLK must be not parallel with power trace that is closed layer or same layer
- SIM Socket needs well ground to PCB.

4.2.5 USB 2.0 interface

Schematic

- No resister/cap are needed on USB DP/DM trace.
- The maximum input capacitance of TVS on USB DP/DM must be less than 3pF for ESD protection.

Layout

- Differential 90-ohm characteristic impedance of USB DP/DM differential pair must be implemented.
- Differential pair shall be routed surround with ground plane and straight and symmetrically on the same layer.
- USB2.0: Maximum of 2 via-hole/layer change.
- The USB DP/DM length mismatch must not exceed 25 mil, and total length less than 7inch.
- TVS have to be placed as close to USB connector as possible and try to minimize stub on trace routing.

4.2.6 USB 3.0 interface

Schematic

- The maximum input capacitance of TVS on SSUSB TX/RX must be less than 0.5pF for ESD protection.
- Both SSUSB_TXP and SSUSB_TXN should be connected to 0.1uF AC coupling capacitor before USB 3.0 connector

Layout

- Differential 90-ohm characteristic impedance of SSUSB TX+/TX- and RX+/RX- differential pair must be implemented.
- Differential pair shall be routed surround with ground plane and straight and symmetrically on the same layer.
- USB3.0: Maximum of 2 via-hole/layer change.
- The SSUSB_TXN/P and SSUSB_RXN/P length mismatch must not exceed 2.5 mil, and total length less than 4 inch.
- TVS have to be placed as close to SSUSB connector as possible and try to minimize stub on trace routing.

4.2.7 PCI-E interface

Schematic

- The maximum input capacitance of TVS on PCIE TX/RX pair must be less than 0.5pF for ESD protection.
- The REFCLK pair must add resistor near the device (EP) side. The resister value recommend 50ohm +/- 1%.
- PCIE data pair PCIE_A_LN[0:1]_TXP/N should be connected to 0.22uF AC coupling capacitance
- PCIE PERST/CLKREQN/PEWAKEN is 1.8V power domain.

Layout

- The TX AC coupling capacitance should be place to NAD side and connector side if PCIE connector used.
- Differential 100-ohm characteristic impedance of REFCLK differential pair must be implemented.
- Differential 85-ohm characteristic impedance of PCIE_A_LN[0:1]_TXP/N and PCIE_A_LN[0:1]_RXP/N differential pair must be implemented.
- Differential pair shall be routed surround with ground plane and straight and symmetrically on the same layer.
- TVS have to be placed as close to PCIE connector as possible and try to minimize stub on trace routing.
- The Lane to Lane mismatch should be less than 100mil in PCIE group. (TX group<100 mil, RX group<100 mil)
- PCIE: Maximum of 2 via-hole/layer change.
- The PCIE_A_LN[0:1]_TXP/N and PCIE_A_LN[0:1]_RXP/N length mismatch must not exceed 2.5 mil, and total length less than 8 inch.

4.2.8 SGMII interface

Schematic

- Both SGMII[0:1]_TXP/N and SGMII[0:1]_RXP/N should be connected to 0.1uF AC coupling capacitance.

Layout

- The TX AC coupling capacitance should be place to receiver side.
- Differential 100-ohm characteristic impedance of SGMII differential pair must be implemented.
- Differential pair shall be routed surround with ground plane and straight and symmetrically on the same layer.
- SGMII: Maximum of 2 via-hole/layer change.
- The SGMII[0:1]_TXP/N and SGMII[0:1]_RXP/N length mismatch must not exceed 2.5 mil, and total length less than 5inch.

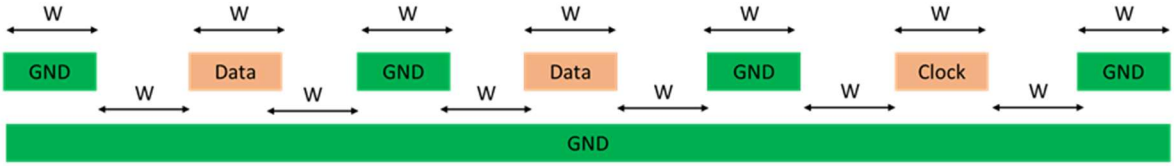
4.2.9 RGMII interface

Schematic

- MT2735 support MII/RMII/RGMII to external PHY
- 1.8V IO power domain
- External PHY IC must be supported delay mode (2ns needed).

Layout

- Trace length less than 5 inch.
- CLK: left and right side by ground shielding, and need GND reference plane
- DATA: one set of TX and RX signals, left and right side by ground shielding. The trace difference < 350 mil
- DATA: trace width/trace length is 1W/1W



4.2.10 AUDIO AND SPEECH

Table 4-1

	Function	SOC
PCM IF	PCM0	PCM Tx/Rx IFPCM Tx/Rx IF -Master & slave mode -1 data wires => Up to 2-CHs -24 bits, up to 48KHz
I2S IF	I2S0	I2S Tx/Rx IF -Master & slave mode -1 data wires => Up to 2-CHs -32 bits, up to 192KHz (Master)
	I2S2	I2S Rx IF -Master mode -1 data wires => Up to 2-CHs -32 bits, up to 192KHz

4.2.11 UNUSED PIN

Table 4-2

Interface	Pin	Unused state
USB_SS	SSUSB_TXP	NC
	SSUSB_TXN	NC
	SSUSB_RXP	1K ohm to GND
	SSUSB_RXN	1K ohm to GND
USB_HS	USB_DP	NC
	USB_DM	NC
PCIE (RC)	PCIE_A_CLKP/N	NC
	PCIE_A_LN0_RXP/N	1K ohm to GND
	PCIE_A_LN0_TXP/N	NC
	PCIE_A_LN1_RXP/N	1K ohm to GND
	PCIE_A_LN1_TXP/N	NC
SGMII	SGMII_0_TXP	NC
	SGMII_0_TXN	NC
	SGMII_0_RXP	1K ohm to GND
	SGMII_0_RXN	1K ohm to GND
	SGMII_1_TXP	NC
	SGMII_1_TXN	NC
	SGMII_1_RXP	1K ohm to GND
	SGMII_1_RXN	1K ohm to GND
MSDC1	MSDC1_CLK	NC
	MSDC0_CMD	NC
	MSDC0_DAT[0:3]	NC
AUXADC	AUXIN0	1K ohm to GND
	AUXIN1	1K ohm to GND
	AUXIN2	1K ohm to GND
	AUXIN3	1K ohm to GND
SIM1	SIM1_SCLK	NC
	SIM1_SIO	NC
	SIM1_SRST	NC
SIM2	SIM2_SCLK	NC
	SIM2_SIO	NC
	SIM2_SRST	NC
I2C SPI I2S TDM MIPI RGMII MDC MDIO PCM USB_DRVBUS USB_VBUSVALD	Interface when it's unused	NC

4.2.12 DC & AC CHARACTERISTIC

I2S DC Electrical Characteristics

Table I2S DC Electrical Characteristics (VIO18 =1.8V)

Parameter	Description	Min.	Typ.	Max.	Unit
VIH	Input logic high voltage	0.65* VIO18	--	VIO18+0.3	V

VIL	Input logic low voltage	-0.3	--	0.35* VIO18	V
VOH	DC output logic high voltage	0.75* VIO18	--	1.84	V
VOL	DC output logic low voltage	0	--	0.25* VIO18	V

Table I2S AC Electrical Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
Fs	Sampling frequency	8	--	192	kHz
fMCK	Master clock frequency	0.768	--	49.152	MHz
fBCK	Serial clock frequency	32*fs	--	64*fs	MHz
tBCK_H	BCK high-level time	--	0.5	--	1/fBCK
tBCK_L	BCK low-level time	--	0.5	--	1/fBCK
tV_WS	Output delay time BCLK low to LRCK valid	--	--	13	ns
tV_DO	Output delay time BCK low to SDOUT valid	--	--	13	ns
tS_DI	DI setup time	16	--	--	ns
tH_DI	DI hold time	16	--	--	ns

SPI DC Electrical Characteristics

Table SPI DC Electrical Characteristics (VIO18 =1.8V)

Parameter	Description	Min.	Typ.	Max.	Unit
VIH	Input logic high voltage	0.65* VIO18	--	VIO18+0.3	V
VIL	Input logic low voltage	-0.3	--	0.35* VIO18	V
VOH	DC output logic high voltage	0.75* VIO18	--	1.84	V
VOL	DC output logic low voltage	0	--	0.25* VIO18	V

SPI AC Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
SPI master SCK Clock frequency	f_{sck}	--	--	52	MHz
MOSI to SCK rising setup time	t_{MOSI_SU}	7.1	--	--	ns
SCK rising to MOSI hold time	t_{MOSI_HD}	7.1	--	--	ns
SCK low pulse	t_{SCKL}	7.2	--	--	ns
SCK high pulse	t_{SCKH}	7.1	--	--	ns
CSB falling to SCK rising setup time	t_{CSB_SU}	7.1	--	--	ns

CSB falling to SCK rising hold time	t_{CSB_HD}	7.1	--	--	ns

I2C DC Electrical Characteristics

Table I2C DC Electrical Characteristics (VIO18 =1.8V)

Parameter	Description	Min.	Typ.	Max.	Unit
VIH	Input logic high voltage	0.65* VIO18	--	VIO18+0.3	V
VIL	Input logic low voltage	-0.3	--	0.35* VIO18	V
VOH	DC output logic high voltage	0.75* VIO18	--	1.84	V
VOL	DC output logic low voltage	0	--	0.2* VIO18	V

I2C AC timing parameters

Symbol	Parameter	Standard-mode		Fast-mode		Fast-mode Plus		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{scl}	SCL clock frequency	0	100	0	400	0	1000	KHz
$t_{HD;STA}$	Hold time (repeater) START condition	4	--	0.6	--	0.26	--	us
t_{LOW}	LOW period of SCL clock	4.7	--	1.3	--	0.5	--	us
t_{HIGH}	HIGH period of SCL clock	4	--	0.6	--	0.26	--	us
$t_{SU;STA}$	Set-up time for repeated START condition	4.7	--	0.6	--	0.26	--	us
$t_{HD;DAT}$	Data hold time	0	--	0	--	0	--	us
$t_{SU;DAT}$	Data set-up time	250	--	100	--	50	--	ns
t_r	Rise time of both SDA and SCL signals	--	1000	20	300	--	120	ns
t_f	Fall time of both SDA and SCL signals	--	300	20x(VDD/ 5.5V)	300	20x(VDD/ 5.5V)	120	NS
$t_{SU;STD}$	Set-up time for STOP condition	4	--	0.6	--	0.26	--	us
$t_{VD;DAT}$	Data valid time	--	3.45	--	0.9	--	0.45	us
$t_{VD;ACK}$	Data valid acknowledge time	--	3.45	--	0.9	--	0.45	Us

MSDC1 DC Electrical Characteristics

Table MSDC1 DC Electrical Characteristics (VIO33 =3.3V)

Parameter	Description	Min.	Typ.	Max.	Unit
VIH	Input logic high voltage	0.625*VIO33	--	VIO33+0.3	V
VIL	Input logic low voltage	-0.3	--	0.25*VIO33	V

VOH	DC output logic high voltage	0.75*VIO33	--	VIO33+0.3	V
VOL	DC output logic low voltage	-0.3	--	0.125*VIO33	V

Table MSDC1 DC Electrical Characteristics (VIO18 =1.8V)

Parameter	Description	Min.	Typ.	Max.	Unit
VIH	Input logic high voltage	1.27	--	VIO18+0.3	V
VIL	Input logic low voltage	-0.3	--	0.58	V
VOH	DC output logic high voltage	1.4	--	1.84	V
VOL	DC output logic low voltage	0	--	0.45	V

MSDC1 AC timing diagram parameters of high speed

Parameter	Symbol	Min.	Max.	Unit
Clock CLK				
Clock frequency data transfer mode	t_{PP}	0	50	MHz
Clock low time	t_{WL}	7	--	ns
Clock high time	t_{Wh}	7	--	ns
Clock rise time	t_{TLH}	--	3	ns
Clock fall time	t_{THL}	--	3	ns
Input CMD,DAT (referenced to CLK)				
Input setup time	t_{ISU}	6	--	ns
Input hold time	t_{IH}	2	--	ns
Output CMD,DAT (referenced to CLK)				
Output delay time during data transfer mode	t_{QDLY}	--	14	ns
Output hold time	t_{Qh}	2.5	--	ns

SIM DC Electrical Characteristics

Table SIM DC Electrical Characteristics (VIO30 =3.0V)

Parameter	Description	Min.	Typ.	Max.	Unit
VIH	Input logic high voltage	2.6	--	3.3	V
VIL	Input logic low voltage	-0.3	--	0.4	V
VOH	DC output logic high voltage	2.6	--	3.1	V
VOL	DC output logic low voltage	0	--	0.4	V

Table SIM DC Electrical Characteristics (VIO18 =1.8V)

Parameter	Description	Min.	Typ.	Max.	Unit
VIH	Input logic high voltage	1.4	--	2.1	V
VIL	Input logic low voltage	-0.3	--	0.27	V
VOH	DC output logic high voltage	1.4	--	1.9	V
VOL	DC output logic low voltage	0	--	0.22	V

SIM AC timing parameters

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
SIM_SCLK						
Rise and fall time	DVDD28_SIM=1.8V	T_{rise_fall}	--	50	50	ns
Clock duty		Duty	47	50	53	%
Rise and fall time	DVDD28_SIM=3.0V	T_{rise_fall}	--	18	18	ns
Clock duty		Duty	47	50	53	%
SIM_SIO						
Rise and fall time	DVDD28_SIM=1.8V	T_{rise_fall}	--	50	1000	ns
Rise and fall time	DVDD28_SIM=3.0V	T_{rise_fall}	--	50	1000	ns
SIM_SRST						
Rise and fall time	DVDD28_SIM=1.8V	T_{rise_fall}	--	18	1000	ns
Rise and fall time	DVDD28_SIM=3.0V	T_{rise_fall}	--	18	1000	ns

RGMII DC Electrical Characteristics

Table RGMII DC Electrical Characteristics (VIO18 =1.8V)

Parameter	Description	Min.	Typ.	Max.	Unit
VIH	Input logic high voltage	0.65* VIO18	--	VIO18+0.3	V
VIL	Input logic low voltage	-0.3	--	0.35* VIO18	V
VOH	DC output logic high voltage	0.75* VIO18	--	1.84	V
VOL	DC output logic low voltage	0	--	0.25* VIO18	V

RGMII AC timing parameters

Symbol	Description	Min.	Typ.	Max.	Unit
Tsetup D0	Data to clock output setup	1.2	2	2.8	V
Thold D0	Clock to Data output hold	1.2	2	2.8	V
Tsetup D0	Data to clock output setup	1.2	2	2.8	V
Thold D0	Clock to Data output hold	1.2	2	2.8	V
Tsetup D0	Data to clock output setup	1.2	2	2.8	
Thold D0	Clock to Data output hold	1.2	2	2.8	V
Tsetup D0	Data to clock output setup	1.2	2	2.8	V
Thold D0	Clock to Data output hold	1.2	2	2.8	V
Tcyc_G	Clock cycle Duration for 1000Mbps	7.2	8	8.8	V
Duty_G	+Duty cycle for 1000Mbps	45	50	55	%
Tr	Rise time (20-80%)	--	--	0.75	ns
Tf	Fall time (20-80%)	--	--	0.75	ns

SGMII GEN1 SPEC

Test Item	SGMII spec
Vdiff (pp)	min. 300mV max. 950mV
Eye Height	--
Cycle to cycle clk jitter	max.100ps
Rise time	min. 100ps max. 200ps
Fall time	min. 100ps max. 200ps

Clk signal duty cycle(%)	min. 48% max. 52%

*1UI=800ps (1/1.25GHz)

SGMII GEN2 SPEC

Test Item	SGMII spec
Vdiff (pp)	max. 1600mV
Dj	max.0.37UI
Rise time	--
Fall time	--
TJ(1E-12)	<=0.55UI

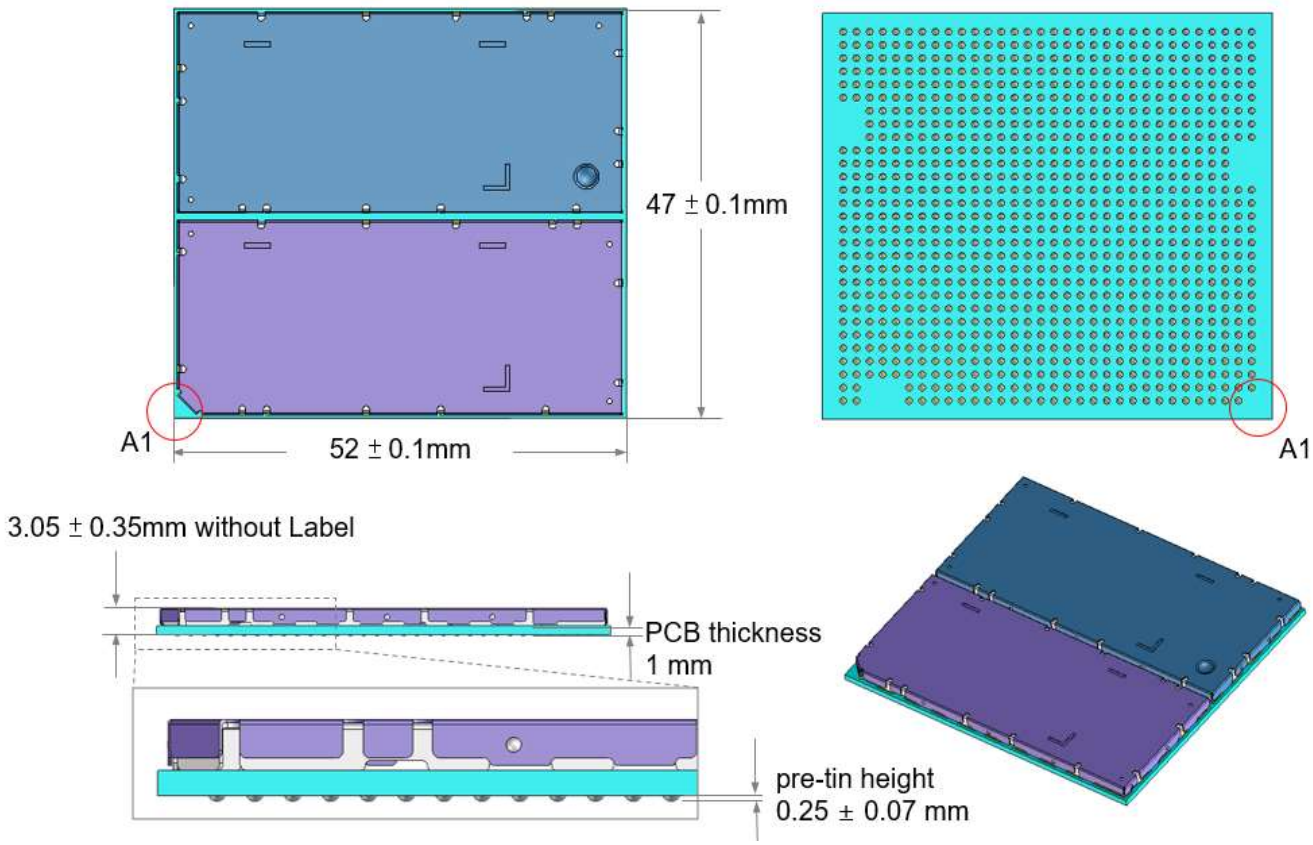
*1UI=320ps (1/3.125GHz)

5. MECHANICAL INFORMATION

NAD weight must be under the total weight requirement of 15.6-g

5.1 NAD PHYSICAL DIMENSIONS

Product outline of finished-goods NAD is defined by dimensions with the fabrication tolerance in the drawing chart listed as below



5.2 NAD ORDERING INFORMATION

Label is applied to UMC-STD35GX NAD shielding case top. It specifies the label with the content format as below and presents purchase ordering information of WNC part number for UMC-STD35GX variant NAD.

Note: Label of other NAD variants will be provided after B-Sample, hardware design is ready.

UMC-STD35GN NA

UMC-STD35GW RoW

UMC-STD35GE EU

5.3 NAD MOISTURE-SENSITIVITY LEVEL

UMC-STD35GX series complies IPC/JEDEC J-STD-020 Standard MSL 3

5.4 THERMAL INFORMATION

5.4.1 DEVICE THERMAL CHARACTERISTICS

TABLE 5-1

IC (Model)	Location	Tj Limit	ΘJC (°C/W)	ΘJB (°C/W)
Modem (MT2735)	U1001	105 (115 for UC4*note)	3.9	2.4
RFIC (MT6190AV)	IC4	125	3.9	5.7
PMIC1 (MT6630LW)	U2000	125	6.7	4
PMIC2 (MT6319WW)	U2501	125	15.5	10
GNSS (MT6635GW)	IC6635	125	9.18	5.3
(LPDDR4)MT53D512M32D2DS-046 AAT	U4405	110	2.8	13.2
(eMMC) MTFC4GLWDM-4M AAT	U4403	110	14.47	45.82
LTE MHB PAMiD (SKY5A3035/ SKY5A3047)	IC12	150	43	49
LTE LB PAMiD (SKY5A3043/ SKY5A3049)	IC11	150	33	44
NR UHB PAMiD (SKY5A3037/ SKY5A3048)	IC521	150	36	46

*note: Thermal use case definition of UC4 and UC6.

Conmod MEB/MQBevo – Redefined Thermal Use Cases

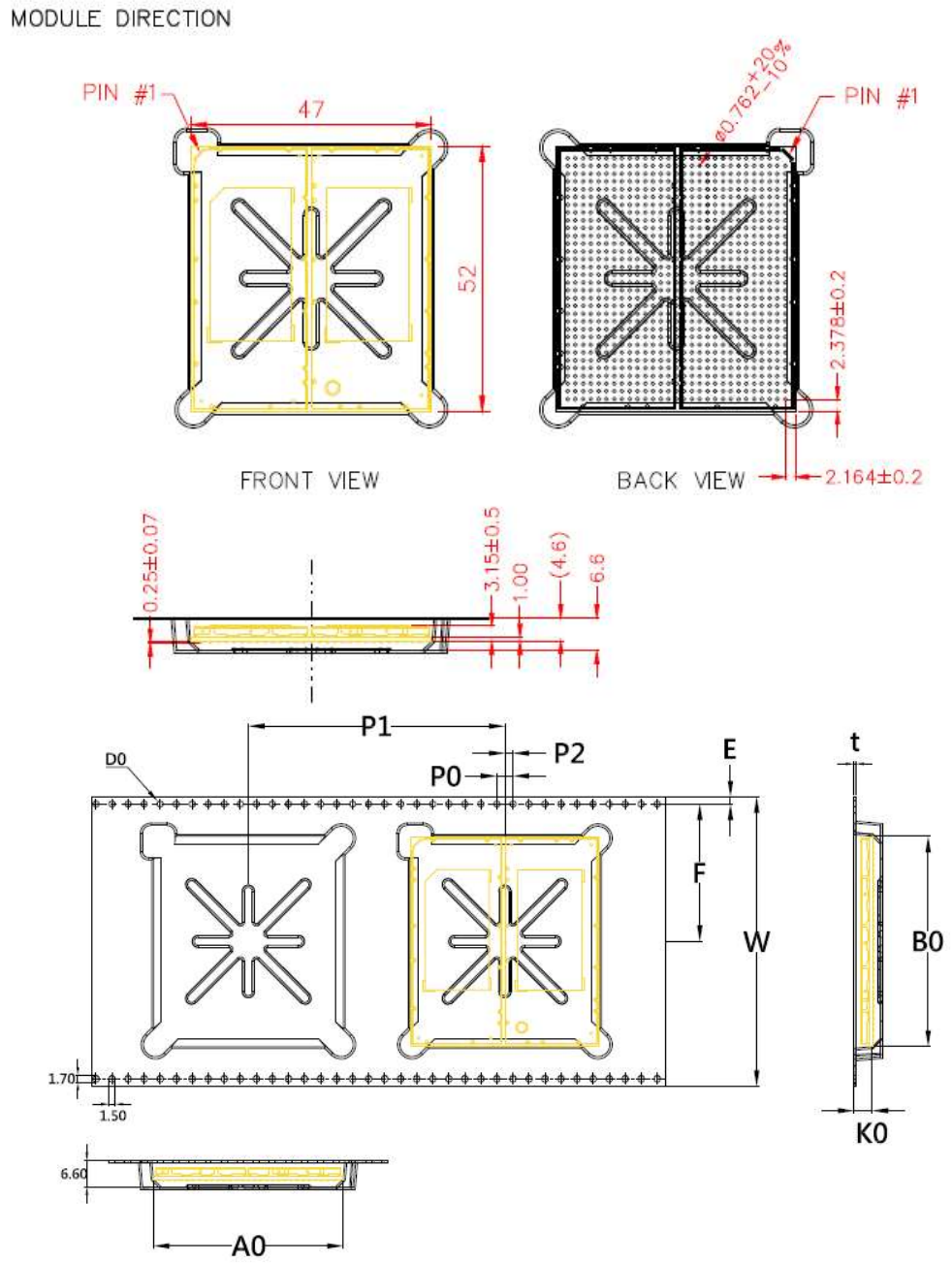
Use Case	RAT	Band	Scenario	TP DL/UL [Mbps]	Tx Power [dBm]	Audio PA [W]	WiFi [Mbps]	V2X	FAN	Duration [min]	Harman Test Result Tambiant [°C]	VW/Cariad/Harmen Notes
UC4	4G	B1	LTE general Data	50/5	15	Low	Low	Low	80% for 5 min then 30%	60		to be tested at Tambiant 95°C/85°C/ 95°C with -10°C per hour
UC6	5G SA	n1	5G SA general Data	50/5	15	Low	Low	Low	80% for 5 min then 30%	60		to be tested at Tambiant 95°C/85°C/ 95°C with -10°C per hour

6. CARRIER, STORAGE AND HANDLING

This chapter describes NAD module packing information include carrier, storage and handling.

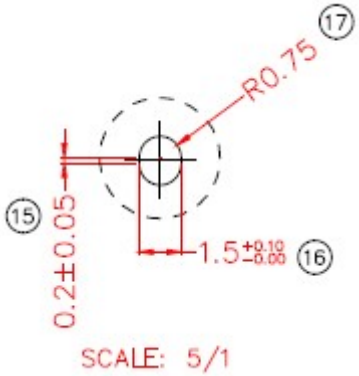
6.1 CARRIER

6.1.1 TAPE AND REEL



W	72.00±0.30	P2	2.00±0.20
S0	68.40±0.10	A0	47.4±0.15
E1	1.75±0.10	A1	——
F	34.20±0.30	B0	52.4±0.15
D0	$1.50^{+0.10}_{-0.00}$	B1	——
D1	——	K0	6.6±0.15
P1	64.00±0.10	K1	4.6±0.15
P0	4.00±0.10	T	0.50±0.05

1. CAMBER IN COMPLIANCE WITH EIA-481.
2. MATERIAL: PS BLACK, THICKNESS: 0.5±0.05MM
3. SURFACE RESISTIVITY: 10^5~10^9 OHMS/SQUARE
4. PACKING LENGTH PER ROLL : 8.5 METERS.
5. VENDOR SHIPPING LENGTH PER ROLL : 25.5 METERS.
6. COMPONENT POCKETS PER 13" REEL : 100 PCS
   (TOTAL POCKETS PER 13" REEL & 7" HUB: 132 PCS
   EMPTY POCKET IN FRONT OF REEL: 10 PCS
   EMPTY POCKET IN BACK OF REEL: 15 PCS
   BUFFER POCKET: 7 PCS)



6.2 STORAGE

6.2.1 STORAGE CONDITIONS

STD35GX devices delivered in tape and reel carriers must be stored in sealed, moisture-proof, anti-static bags between a temperature and humidity range of 15°C to 35°C, < 90% R.H.

6.2.2 OUT-OF-BAG DURATION

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in section 5.3

6.3 HANDLING

This section describes NAD baking condition and ESD performance.

6.3.1 BAKING

It is not necessary to bake the UMC-STD35GX if the conditions specified in Section 6.2.1 and Section 6.2.2 have not been exceeded.
It is necessary to bake the UMC-STD35GX if the humidity card indicates module needs to undergo baking.
Baking conditions: 24hrs at + 125C +/- 5 C

6.3.2 ELECTROSTATIC DISCHARGE (ESD)

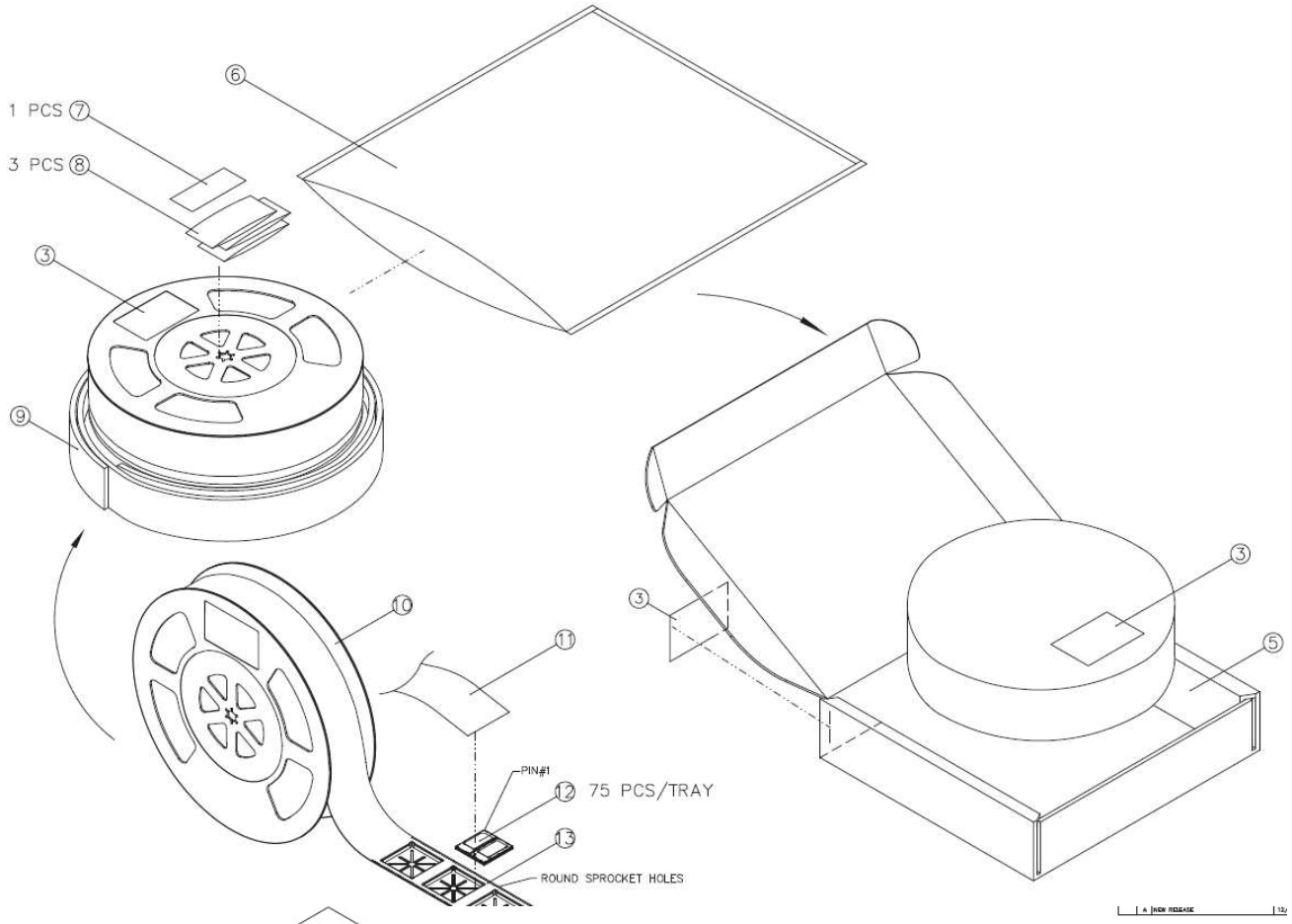
It is strongly recommended for the Developer to place ESD suppression components on the interconnection signal traces between NAD bottom pads and the application board to prevent NAD suffering ESD events with the voltage strength over the requirement defined in the table below:
Table 6-1

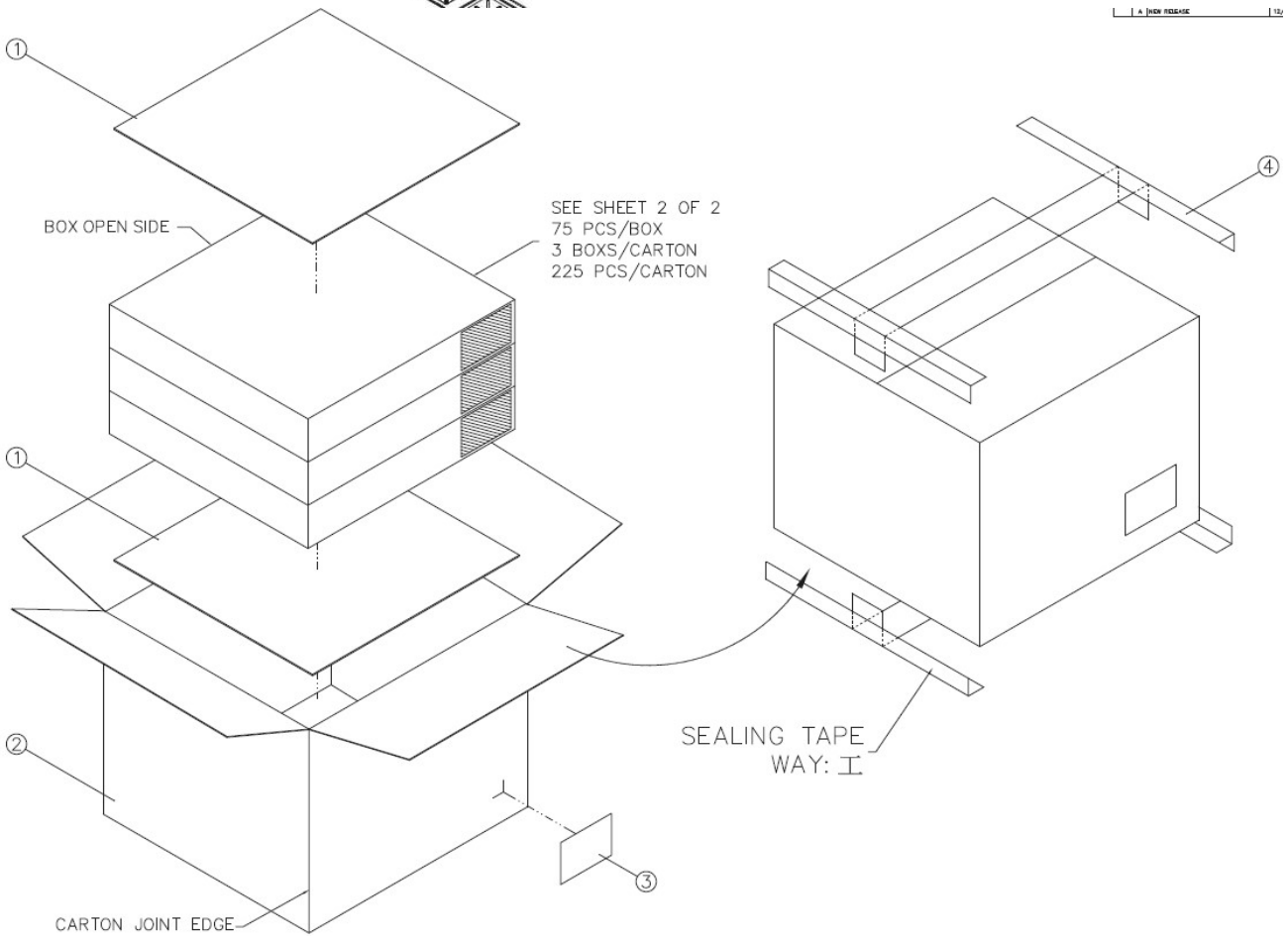
Specification/Requirements	Contact Discharge
Human Body Model(HBM)	1000 Volts
Charge Device Model(CDM)	250 Volts

6.4 BARCODE LABEL AND PACKING FOR SHIPMENT

This section describes label drawing and packing information

6.4.1 PACKING AND LABEL LOCATION


1 PCS ⑦
3 PCS ⑧
⑥
③
⑨
⑩
⑪
PIN#1
⑫ 75 PCS/TRAY
⑬
ROUND SPROCKET HOLES
③
③
⑤


①
BOX OPEN SIDE
SEE SHEET 2 OF 2
75 PCS/BOX
3 BOXS/CARTON
225 PCS/CARTON
④
①
②
③
SEALING TAPE
WAY:
CARTON JOINT EDGE

7. PCB MOUNTING GUIDELINES

7.1 ROHS COMPLIANCE

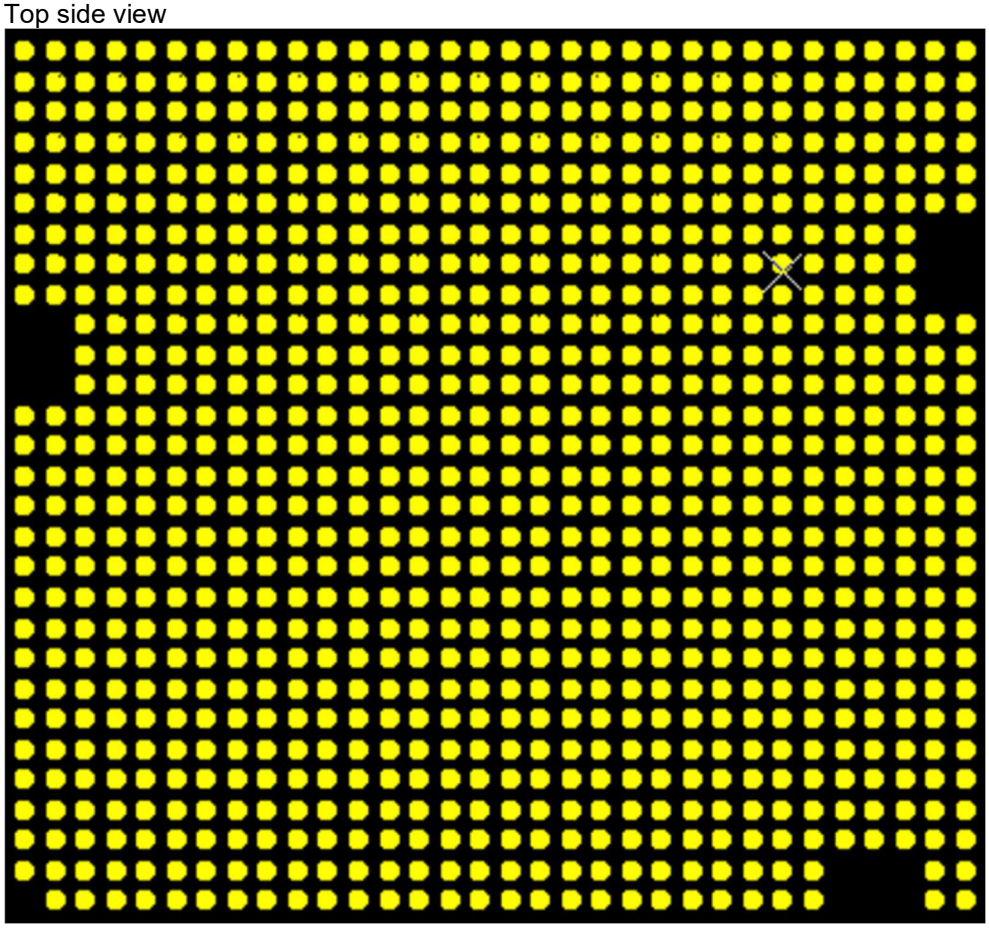
UMC-STD35GX is lead-free and RoHS compliant. WNC defines it is lead-free (or Pb-free) product

7.2 SMT PARAMETER

This section describes WNC board-level characterization process parameters. It will help customers in their SMT process development; it is not intended to be a specification for their SMT process.

7.2.1 LAND PAD AND STENCIL DESIGN

Top side view



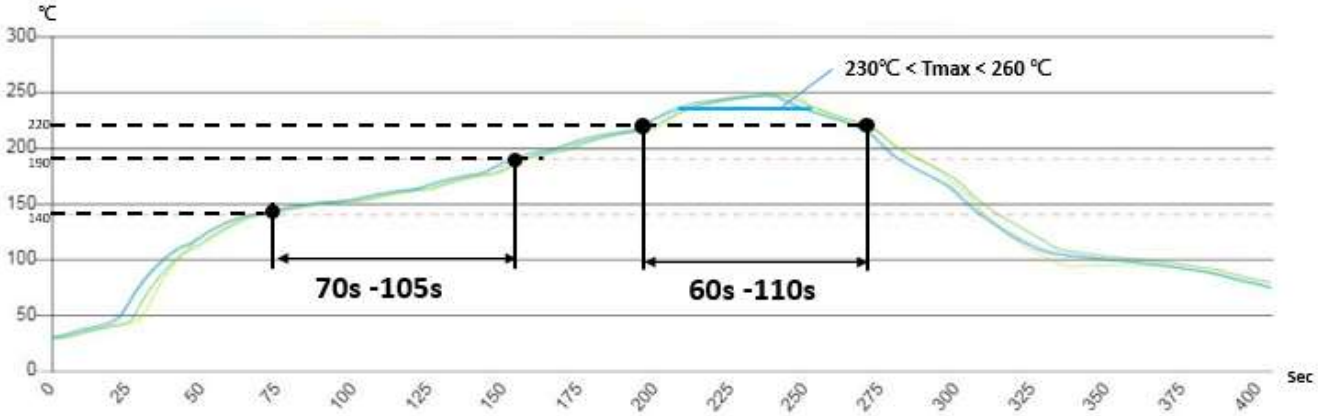
A1

Stencil Design:

I. Ball Pad : 1:1.2 (Suggestion only, will update after verified)
II. Thickness of stencil : 0.08mm
III. Solder Paste Recommendation : SAC305 Alloy

7.2.2 REFLOW PROFILE

Temperature Zone	Time	Key Parameter	Suggest
Soak Zone	70sec～105sec	Temperature : 140℃～190℃	It is recommended to control the number of seconds to 90 sec ± 5 sec
Peak Zone	60sec～110sec	Temperature : 230℃～250℃	It is recommended to control it above 240℃



Note: The module only allow <= 2 times reflow.

7.2.3 SMT PEAK PACKAGE BODY TEMPERATURE

Tmax < 260℃

7.2.4 SMT PROCESS VERIFICATION

WNC recommends verification of the SMT process prior to high volume board assembly, including

- In-line solder paste deposition monitoring
- Reflow temperature profile measurement and verification
- Visual and X-ray inspection after soldering to confirm adequate alignment, solder voids, solder pad shape, and solder bridging
- Cross-section inspection of solder joints for wetting, solder pad shape, and voiding

7.3 HIGH-TEMPERATURE WARPAGE

tbc, this information will be included in future revision of this document.

8. RELIABILITY

Follow AECQ-104 standard

For NADs AEC-Q104 Validation Plan

Group A - Acceleration Environment Stress Tests

Group A2	Group A3	Group A4	Group A5	Group A6

Visual Inspection / Performance Characteristics

Preconditioning(PC) (JESD22-A113 & JEDEC J-STD-020)

Solder NAD to Test Board

1. Temperature Cycling at - 40C to + 85C for 5 Cycles. Dwell time for 30 mins.
2. Bake the device for 24hrs at + 125C +/- 5 C and move to moisture soak within 2 hrs.
3. Moisture soak at + 30 C / 60%Rh for (MSL3 = 192 hrs)/(MSL4 = 96 hrs) and completed reflow stage within 15 mins to 4 hrs.
4. Reflow 2 times, solder NAD to test board during 2nd reflow.

Visual Inspection / Tri-temp Performance Characteristics

	B2 - Early Life Failure Rate(ELFR)	B2 - Early Life Failure Rate(ELFR)	B2 - Early Life Failure Rate(ELFR)	B2 - Early Life Failure Rate(ELFR)	B2 - Early Life Failure Rate(ELFR)
# reference	AEC-Q104/JESD22-A108	AEC-Q104/JESD22-A108	AEC-Q104/JESD22-A108	AEC-Q104/JESD22-A108	AEC-Q104/JESD22-A108
# samples	30 pcs	30 pcs	30 pcs	30 pcs	30 pcs
condition	+ 85 C@ Vmax	+ 85 C@ Vmax	+ 85 C@ Vmax	+ 85 C@ Vmax	+ 85 C@ Vmax
duration	48 hrs	48 hrs	48 hrs	48 hrs	48 hrs
op. mode	3.2	3.2	3.2	3.2	3.2
monitoring	continuous	continuous	continuous	continuous	continuous
checks	0/end	0/end	0/end	0/end	0/end

	A2 - Temperature Humidity Bias(THB)	A3 - Temperature Humidity w/o Bias(TH)	A4 - Temperature Cycling(TC)	A5 - Power Temperature Cycling(PTC)	A6 - High Temperature Storage Life(HTSL)
# reference	AEC-Q104/JESD22-A101	AEC-Q104/JESD22-A101	AEC-Q104/JESD22-A104	AEC-Q104/JESD22-A105	AEC-Q104/JESD22-A103
# samples	30 pcs	30 pcs	30 pcs	10 pcs	30 pcs
condition	+ 85 C / 85 % Rh@ Vnom	+ 85 C / 85 % Rh	- 40 C / + 85 C	- 40 C / + 85 C	+ 85 C
duration	1,000 hours	1,000 hours	500 cycles ext. 1000 cyc	709 cyc	1,000 hours
op. mode	3.2	1.1	1.1	3.1/3.2	1.1
monitoring	continuous	no	no	continuous	no
checks	0/end	0/end	0/500/700/900/end	0/500/700/900/end	0/end

Visual Inspection / Tri-temp Performance Characteristics

General op.mode:
Operating mode 1:
No voltage is applied to the DUT.
— Operating mode 1.1: not connected to wiring harness.
— Operating mode 1.2: connected to wiring harness simulating vehicle installation.
Operating mode 2:
The DUT is electrically operated with test voltage UB as in a vehicle with shut-off engine and with all electrical connections made.
— Operating mode 2.1: system/component functions are not activated (e.g. sleep mode).
— Operating mode 2.2: systems/components with electric operation and control in typical operating mode.
— Operating mode 2.3: systems/components with electric operation and control in minimum load.
— Operating mode 2.4: systems/components with electric operation and control in maximum load.
Operating mode 3:
The DUT is electrically operated with test voltage UA with all electrical connections made.
— Operating mode 3.1: system/component functions are not activated.
— Operating mode 3.2: systems/components with electric operation and control in typical operating mode.
— Operating mode 3.3: systems/components with electric operation and control in minimum load.
— Operating mode 3.4: systems/components with electric operation and control in maximum load.

For NADs AEC-Q104 Validation Plan

Group B - Acceleration Lifetime Simulation Tests

Group B1

Solder NAD to Test Board

Visual Inspection / Tri-temp Performance Characteristics

B2 - Early Life Failure Rate(ELFR)

# reference	AEC-Q104/JESD22-A108
# samples	30 pcs
condition	+ 85 C@ Vmax
duration	48 hrs
op. mode	3.2
monitoring	continuous
checks	0/end

B1 - High Temperature Operation Life(HTOL)

# reference	AEC-Q104/JESD22-A108
# samples	30 pcs
condition	+ 85 C@ Vnom
duration	1000 hours
op. mode	3.2
monitoring	continuous
checks	0/end

Visual Inspection / Tri-temp Performance Characteristics

Group B2

K1 - Damp Heat,Cyclic(K-08)

# reference	VW80000 Chapter 11.8
# samples	10 pcs
condition	Variant 1,+55C,6cycles
duration	144 hrs
op. mode	airplan mode
monitoring	continuous
checks	0/end

For NADs AEC-Q104 Validation Plan

Group C - Package Assembly Integrity Tests

Group C3

Visual Inspection / Performance Characteristics

C3 - Solderability(SD)

# reference	J-STD-002
# samples	15 pcs
condition	+ 150 C
duration	16 hours
op. mode	1.1
monitoring	no
checks	0/end

Group C4

C4 - Physical Dimensions(PD)

# reference	JESD22- B100/B108
# samples	10 pcs
condition	no
duration	no
op. mode	1.1
monitoring	no
checks	no

Group C7

C7 - X-Ray(XRAY)

# reference	no
# samples	5 pcs
condition	no
duration	no
op. mode	1.1
monitoring	no
checks	no

For NADs AEC-Q104 Validation Plan

Group E - Electrical Varication Tests

Group E2

Group E3

Group E8

Visual Inspection / Performance Characteristics

Solder NAD to Test Board

Visual Inspection / Performance Characteristics

Visual Inspection / Tri-temp Performance Characteristics

E2 - ESD(HBM)

# reference	AEC-Q104/JS-001
# samples	12 pcs
condition	1000V
duration	5 pulses/ ±Voltage
op. mode	1.1
monitoring	no
checks	0/end

E3 - ESD(CDM)

# reference	JEDEC JS-002
# samples	6 pcs
condition	500V
duration	1 Zaps/±Voltage
op. mode	1.1
monitoring	no
checks	0/end

E8 - Radiated Emissions(RE)

# reference	Test Plan
# samples	2/2 pcs
condition	See Test Plan
duration	as need
op. mode	3.2
monitoring	continuous
checks	0/end

Visual Inspection / Performance Characteristics

Group H2

Solder NAD to Test Board

Visual Inspection / Tri-temp Performance Characteristics

B2 - Early Life Failure Rate(ELFR)

# reference	AEC-Q104/JESD22-A108
# samples	30 pcs
condition	+ 85 C@ Vmax
duration	48 hrs
op. mode	3.2
monitoring	continuous
checks	0/end

H2 - Low Temperature Storage Life(LTSL)

# reference	AEC-Q104/JESD22-A119
# samples	30 pcs
condition	- 40 C
duration	1,000 hours
op. mode	1.1
monitoring	no
checks	0/end

Visual Inspection / Tri-temp Performance Characteristics

Group H3

Solder NAD to Test Board

Visual Inspection / Tri-temp Performance Characteristics

H3 - Startup & Temperature Steps(STEPs)

# reference	ISO16750-4
# samples	5 pcs
condition	- 40 C / + 85 C
duration	follow ISO16750-4
op. mode	3.1/3.2
monitoring	continuous
checks	0/end

Group H4

Visual Inspection / Performance Characteristics

H4 - Drop test(DROP)

# reference	JESD22-B110
# samples	6 pcs
condition	1500G, 0.5ms
duration	1 shock for +/- X,Y,Z
op. mode	1.1
monitoring	no
checks	0/end

Visual Inspection / Performance Characteristics

9. BOARD-LEVEL CERTIFICATION

tbc, this information will be included in future revision of this document.

10. WARNING STATEMENT

Federal Communication Commission Interference Statement:

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 29cm between the radiator & your body.

This module is intended for OEM integrators only. Per FCC KDB 996369 D03 OEM Manual v01 guidance, the following conditions must be strictly followed when using this certified module:

KDB 996369 D03 OEM Manual v01 rule sections:

2.2 List of applicable FCC rules

This module has been tested for compliance to FCC Part 2, 22, 24, 27 and 90

2.3 Summarize the specific operational use conditions

The module is tested for standalone mobile RF exposure use condition. Any other usage conditions such as co-location with other transmitter(s) or being used in a portable condition will need a separate reassessment through a class II permissive change application or new certification.

2.4 Limited module procedures

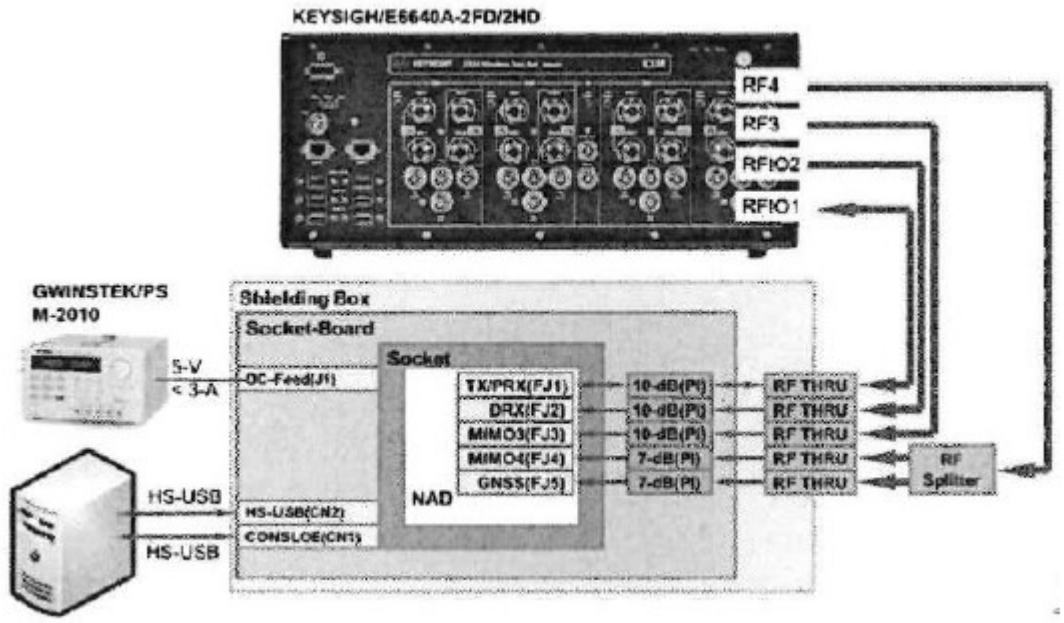
Not applicable.

2.5 Trace antenna designs

Refer to "Antenna trace" provided as a separate document to this integration manual.
Please contact the module supplier

Any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify the module grantee that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the grantee, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

The Module will 100% perform test with standard equipment to ensure all design and antenna trance tolerances meet product specifications and compliance 3GPP standards.



2.6 RF exposure considerations

This equipment complies with FCC mobile radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 29 cm between the radiator & your body. If the module is installed in a portable host, a separate SAR evaluation is required to confirm compliance with relevant FCC portable RF exposure rules.

2.7 Antennas

The following antennas have been certified for use with this module; antennas of the same type with equal or lower gain may also be used with this module. The antenna must be installed such that 29 cm can be maintained between the antenna and users.

Antenna Type	Frequency (MHz)	MaxGain (dBi)	Impedance(Ω)
Dipole	700	1.63	50
	960	2.63	
	1710	2.03	
	2690	2.26	
	3300	1.55	
	4200	2.62	

The final host product must comply with the requirements specified in §15.203, §15.204(b) and §15.204(c). As such, the host product must use a permanently attached antenna or an antenna that uses a unique coupling. The OEM integrator is responsible for using a unique external antenna connector in the host product, which must be selected from the types listed below.

Acceptable Unique Connector: R-SMA

The host product is required to include an antenna which complies with the requirements specified within these integration instructions.

2.8 Label and compliance information

The final end product must be labeled in a visible area with the following:
“Contains FCC ID: NKR-UMCSTD35GN”. The grantee's FCC ID can be used only when all FCC compliance requirements are met.

2.9 Information on test modes and additional testing requirements

This transmitter is tested in a standalone mobile RF exposure condition and any co-located or simultaneous transmission with other transmitter(s) or portable use will require a separate class II permissive change re-evaluation or new certification.

2.10 Additional testing, Part 15 Subpart B disclaimer

This transmitter module is tested as a subsystem and its certification does not cover the FCC Part 15 Subpart B (unintentional radiator) rule requirement applicable to the final host. The final host will still need to be reassessed for compliance to this portion of rule requirements if applicable.

2.11 Note EMI Considerations

Note that a host manufacture is recommended to use D04 Module Integration Guide recommending as "best practice" RF design engineering testing and evaluation in case non-linear interactions generate additional non-compliant limits due to module placement to host components or properties For standalone mode, reference the guidance in D04 Module Integration Guide and for simultaneous mode7; see D02 Module Q&A Question 12, which permits the host manufacturer to confirm compliance.

2.12 How to make changes

Since only Grantees are permitted to make permissive changes, host integrators who expect to use this module outside of the certification conditions should contact Wistron NeWeb Corp. at wnc.info@wnc.com.tw.

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As long as all conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

OEM/Host manufacturer responsibilities

OEM/Host manufacturers are ultimately responsible for the compliance of the Host and Module. The final product must be reassessed against all the essential requirements of the FCC rule such as FCC Part 15 Subpart B before it can be placed on the US market. This includes reassessing the transmitter module for compliance with the Radio and EMF essential requirements of the FCC rules. This module must not be incorporated into any other device or system without retesting for compliance as multi-radio and combined equipment

Industry Canada statement:

This device complies with ISED's licence-exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Le présent appareil est conforme aux CNR d' ISED applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) le dispositif ne doit pas produire de brouillage préjudiciable, et (2) ce dispositif doit accepter tout brouillage reçu, y compris un brouillage susceptible de provoquer un fonctionnement indésirable.

Radiation Exposure Statement

This equipment complies with ISED radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with greater than 43 cm between the radiator & your body.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé à plus de 43 cm entre le radiateur et votre corps.

This device is intended only for OEM integrators under the following conditions

1) The antenna must be installed and operated with greater than 43 cm between the antenna and users
2) The transmitter module may not be co-located with any other transmitter or antenna.
3) Module approval valid only when the module is installed in the tested host or compatible series of host which have similar RF exposure characteristic with equal or larger antenna separation distance.

As long as 3 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes:

1) L'antenne doit être installé et exploité avec plus de 43 cm entre l'antenne et les utilisateurs
2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.
3) Approbation du Module valable que lorsque le module est installé dans l'hôte testé ou de la série de l'hôte compatible qui ont même caractéristique de l'exposition aux RF avec la distance égale ou supérieure séparation antenne.

Tant que les 3 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE

In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the Canada authorization is no longer considered valid and the IC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed and operated with greater than 43 cm between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC: 4441A-UMCSTD35GN”.

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un appareil où l’antenne peut être installée et utilisée à plus de 43 cm entre l’antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: 4441A-UMCSTD35GN ".

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module.
The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.
Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel

DETACHABLE ANTENNA USAGE

This radio transmitter [IC: 4441A-UMCSTD35GN] has been approved by Innovation, Science and Economic Development Canada to operate with the antenna types listed below, with the maximum permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.

Le présent émetteur radio [IC: 4441A-UMCSTD35GN] a été approuvé par Innovation, Sciences et Développement économique Canada pour fonctionner avec les types d'antenne énumérés ci-dessous et ayant un gain admissible maximal. Les types d'antenne non inclus dans cette liste, et dont le gain est supérieur au gain maximal indiqué pour tout type figurant sur la liste, sont strictement interdits pour l'exploitation de l'émetteur.

Manufacturer	Antenna connector	Antenna Type	Frequency (MHz)	MaxGain (dBi)	Impedance (Ω)
WNC	SMA	Dipole	700	1.63	50
			960	2.63	
			1710	2.03	
			2690	2.26	
			3300	1.55	
			4200	2.62	