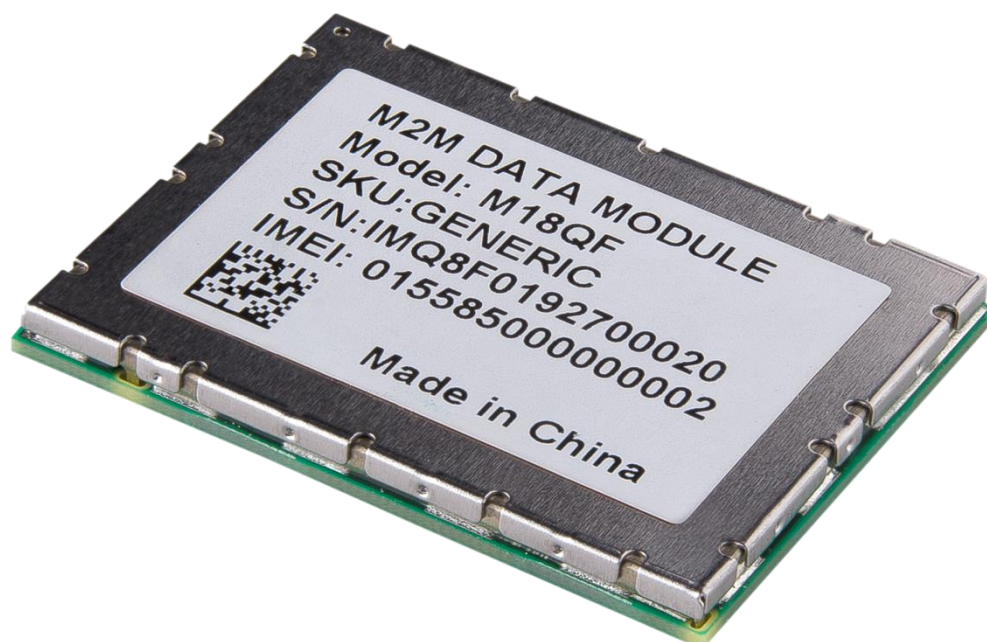




## Product user manual

**Project Name:** M18QF&M18QA series

**Author:** Wistron NeWeb Corporation

**Revision:** 1.1

**Revision Date:** 2019/10/28

## Contact Information

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## Revision History

| Rev. # | Author | Summary of Changes          | Date       |
|--------|--------|-----------------------------|------------|
| 1.0    | WNC    | First release               | 2019/8/12  |
| 1.1    | WNC    | Correct the band definition | 2019/10/28 |
|        |        |                             |            |
|        |        |                             |            |
|        |        |                             |            |
|        |        |                             |            |
|        |        |                             |            |
|        |        |                             |            |

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# Contents

|                                          |           |
|------------------------------------------|-----------|
| <b>Contact Information.....</b>          | <b>2</b>  |
| <b>Revision History.....</b>             | <b>2</b>  |
| <b>Contents.....</b>                     | <b>4</b>  |
| <b>1. Introduction.....</b>              | <b>7</b>  |
| 1.1. Abbreviation.....                   | 7         |
| 1.2. Features.....                       | 8         |
| <b>2. Electrical Specifications.....</b> | <b>10</b> |
| 2.1. Host interface pin assignments..... | 10        |
| 2.1.1. LGA Pad Diagram.....              | 10        |
| 2.1.2. Pin Assignments.....              | 11        |
| 2.2. Power supply.....                   | 20        |
| 2.3. USB interface.....                  | 21        |
| 2.4. SGMII interface.....                | 23        |
| 2.5. UIM interface.....                  | 24        |
| 2.6. Control interface.....              | 28        |
| 2.6.1. Power-on Signal.....              | 28        |
| 2.6.2. Wake-up interface.....            | 29        |
| 2.6.3. Reset Signal.....                 | 30        |
| 2.6.4. WWAN state Signal.....            | 31        |
| 2.7. Digital interface.....              | 31        |
| 2.7.1. JTAG Interface.....               | 31        |
| 2.7.2. SPI Master Interface.....         | 31        |
| 2.7.3. PCM Interface.....                | 32        |
| 2.7.4. I2S Interface.....                | 34        |

|                                                            |           |
|------------------------------------------------------------|-----------|
| 2.7.5. I2C Interface.....                                  | 35        |
| 2.7.6. UART Interface.....                                 | 36        |
| 2.7.7. ADC Interface.....                                  | 36        |
| <b>3. RF Specifications.....</b>                           | <b>37</b> |
| 3.1. RF connections.....                                   | 37        |
| 3.2. Interference and sensitivity.....                     | 38        |
| 3.3. GNSS external circuit design.....                     | 39        |
| 3.4. RF Specification.....                                 | 41        |
| 3.5.1 Band support.....                                    | 41        |
| 3.5.2 Bandwidth support.....                               | 42        |
| 3.5.3 RF Transmit Specification.....                       | 42        |
| 3.5.4 RF Receiver Specification.....                       | 42        |
| 3.5.5 GNSS Receiver Specification.....                     | 44        |
| <b>4. Power.....</b>                                       | <b>46</b> |
| 4.1. Power consumption.....                                | 46        |
| <b>5. Software Interface.....</b>                          | <b>48</b> |
| 5.1. Support tools.....                                    | 48        |
| 5.2. USB interface.....                                    | 48        |
| <b>6. Mechanical and Environmental Certifications.....</b> | <b>49</b> |
| 6.1. PCBA Form Factor.....                                 | 49        |
| 6.2. Reflow.....                                           | 52        |
| 6.3. PCB pad design.....                                   | 53        |
| 6.4. Labeling.....                                         | 54        |
| 6.5. SMT Voids control.....                                | 55        |
| 6.5.1. Mother board PCB thickness.....                     | 55        |
| 6.5.2. Stencil design.....                                 | 55        |

6.6. Thermal considerations..... 56

**7. Regulatory Compliance and Certification..... 58**

7.1. Certification testing..... 58

**8. Packaging..... 59**

8.1. Tape-and-Reel Package..... 59

8.2. Single Packaging for Samples..... 61

8.3. MSL level..... 61

**9. Safety Recommendation..... 62**

# 1. Introduction

The M18QF/M18QA Series modules are LTE modems which incorporate an application CPU subsystem and peripheral interfaces and functions uniquely designed to address the power/performance/cost requirements of IoT and M2M applications. The CPU is based on Qualcomm's MDM architecture which offers OFDMA-related software based signal processing capabilities that significantly exceed traditional communications ARM cores. M18QF/M18QA Series modules provide a variety of interfaces including USB 2.0, SGMII, SPI, UART, PCM, I2C, UIM & SDIO.

## 1.1. Abbreviation

Table 1. Abbreviation

| Abbreviation | Definition                                                                                 |
|--------------|--------------------------------------------------------------------------------------------|
| AC           | Alternating Current                                                                        |
| DC           | Direct Current                                                                             |
| ETSI         | European Telecommunications Standards Institute                                            |
| GND          | Ground                                                                                     |
| GPS          | Global Positioning System                                                                  |
| GNSS         | Any single or combined satellite navigation system (GPS, GLONASS and combined GPS/GLONASS) |
| GPIO         | General Purpose Input Output                                                               |
| I/O          | Input/Output                                                                               |
| IoT          | Internet of Things                                                                         |
| I2C          | Inter-Integrated Circuit                                                                   |
| LGA          | Land Grid Array                                                                            |
| LTE          | Long Term Evolution                                                                        |
| Mbps         | Megabits per second                                                                        |
| MIPS         | Millions of Instructions Per Second                                                        |
| N/A          | Not/Applicable                                                                             |
| OS           | Operating System                                                                           |
| PC           | Personal Computer                                                                          |
| PCM          | Pulse Code Modulation                                                                      |

|              |                                             |
|--------------|---------------------------------------------|
| <b>PIN</b>   | Personal Identification Number              |
| <b>SIM</b>   | Subscriber Identity Module                  |
| <b>SMA</b>   | Surface Mount Antenna                       |
| <b>SPI</b>   | Serial Peripheral Interface                 |
| <b>UART</b>  | Universal Asynchronous Receiver-Transmitter |
| <b>UIM</b>   | User Identity Module                        |
| <b>USB</b>   | Universal Serial Bus                        |
| <b>Vref</b>  | Voltage reference                           |
| <b>WCDMA</b> | Wideband Code Division Multiple Access      |
| <b>WNC</b>   | Wistron NeWeb Corporation                   |

## 1.2. Features

This section lists main features of M18QF/M18QA Series module support. For wireless technology and band support information among different modules, please refer to table2 for detail information.

Table 2. M18QF/M18QA Series module overview

| Module | Category | LTE<br>B2/5/4/12/13 | LTE<br>B2/5/4/12/14 | WCDMA<br>B2/5 | GNSS          | Temperature Grade |
|--------|----------|---------------------|---------------------|---------------|---------------|-------------------|
| M18QF  | 4        | √                   | ×                   | √             | √<br>Optional | Industrial        |
| M14QF  | 1        | √                   | ×                   | √             | √<br>Optional | Industrial        |
| M18QA  | 4        | ×                   | √                   | √             | ×             | Industrial        |
| M14QA  | 1        | ×                   | √                   | √             | ×             | Industrial        |

Note: 1.Refer to section6.6 for more information about industrial grade.

2.“√” indicates supporting. “×” indicates not supporting.

3. The 2nd harmonic of LTE B14 is not isolated completely from embedded GNSS receiver, the interference would make GNSS de-sense seriously when LTE B14 and GNSS are working simultaneously, the external GNSS receiver is recommended to use instead of embedded GNSS in M18QA/M14QA.

**Feature list:**

- LTE 3GPP release 10 without Carrier Aggregation
- M18QF/M18QA: 3GPP, LTE Cat. 4 with 150/50 Mbps for DL/UL
- M14QF/M14QA: 3GPP, LTE Cat. 1 with 10/5 Mbps for DL/UL
- Supports LTE B2/4/5/12/13/14
- Supports WCDMA B2/5, 3GPP release 8
- Ultra-high-performance Cortex A7 microprocessor
- Modem subsystem (MSS)
- Resource and power management (RPM) subsystem
- Optimized for M2M and IoT markets
- Interfaces
  - HS USB 2.0 with integrated PHY
  - SGMII interface
  - Dual UART interfaces (4 bit and 2 bit) for data transfer and diagnostic tools
  - SDC1/First SPI interface
  - I2C/Second SPI interface
  - USIM interface
  - GPIOs
  - ADC
  - PCM/I2S
  - JTAG interface

## 2. Electrical Specifications

### 2.1. Host interface pin assignments

#### 2.1.1. LGA Pad Diagram

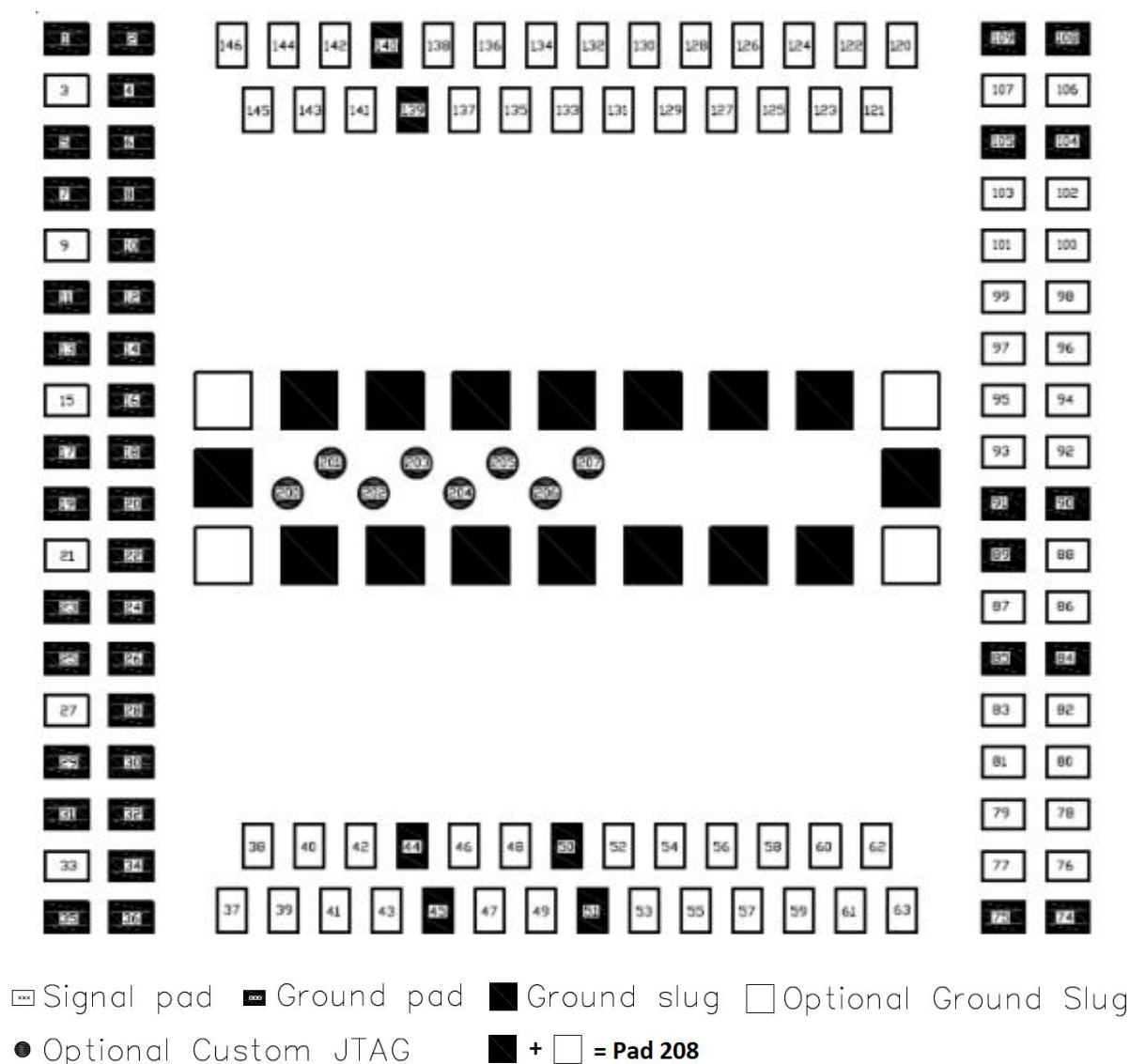


Figure 1. LGA pad diagram (top view)

### 2.1.2. Pin Assignments

I/O type description:

- AO : Analog Output
- AI : Analog Input
- DO : Digital Output
- DI : Digital Input

Table 3. Pin interface family

| Interface Family                | Signal      | Description                 | I/O   |
|---------------------------------|-------------|-----------------------------|-------|
| <b>RF Interfaces</b>            |             |                             |       |
|                                 | RF_2        | Diversity antenna           | AI    |
|                                 | RF_GNSS     | Reserved for GNSS receiver  | AI    |
|                                 | RF_1        | Main Antenna                | AI/AO |
| <b>User Identity Module</b>     |             |                             |       |
|                                 | UIM_VCC     | Power source for UIM        | AO    |
|                                 | UIM_DATA    | Data in/out                 | DI/DO |
|                                 | UIM_CLK     | Clock signal                | DO    |
|                                 | UIM_RESET   | Reset signal                | DO    |
|                                 | UIM_DETECT  | UIM Detect signal           | DI/DO |
| <b>Data Interfaces- USB 2.0</b> |             |                             |       |
|                                 | USB_HS_DP   | USB Data Positive           | DI/DO |
|                                 | USB Detect  | USB Detect                  | DI    |
|                                 | USB_HS_DM   | USB Data Negative           | DI/DO |
|                                 |             |                             |       |
|                                 |             |                             |       |
| <b>Data Interfaces- SGMII</b>   |             |                             |       |
|                                 | SGMII_RX_P  | SGMII receive - plus        | DI    |
|                                 | SGMII_RX_M  | SGMII receive - minus       | DI    |
|                                 | SGMII_TX_P  | SGMII transmit - plus       | DO    |
|                                 | SGMII_TX_M  | SGMII transmit - minus      | DO    |
|                                 | SGMII_MDIO  | SGMII Management data       | DI/DO |
|                                 | SGMII_MDC   | SGMII Management data clock | DI/DO |
| <b>Data Interfaces- UART1</b>   |             |                             |       |
|                                 | UART1_CTS_N | Clear To Send for UART 1    | DI    |
|                                 | UART1_RFR_N | Ready for receive for UART1 | DO    |

|                                            |                             |       |
|--------------------------------------------|-----------------------------|-------|
| UART1_RX                                   | Receive for UART 1          | DI    |
| UART1_TX                                   | Transmit for UART 1         | DO    |
| <b>Data Interfaces- UART2</b>              |                             |       |
| UART2_RX                                   | Receive for UART 2          | DI    |
| UART2_TX                                   | Transmit for UART 2         | DO    |
| <b>Data Interfaces- I2C/2nd_SPI</b>        |                             |       |
| I2C_SDA                                    | Data in/out                 | DI/DO |
| 2nd_SPI_EN_1                               | 2nd_SPI chip select         | DO    |
| I2C_SCL                                    | Clock signal                | DO    |
| 2nd_SPI_CLK                                | 2nd_SPI serial clock        | DO    |
| SPI_MOSI                                   | 2nd_SPI master out slave in | DO    |
| NC                                         | NC                          | -     |
| SPI_MISO                                   | 2nd_SPI master in slave out | DI    |
| <b>Data Interfaces- SDC1/1st_SPI</b>       |                             |       |
| SDC1_DATA_3                                | SDC1_DATA_3                 | DI/DO |
| 1st_SPIM_MOSI                              | 1st_SPI master out slave in | DO    |
| SDC1_DATA_2                                | SDC1_DATA_2                 | DI/DO |
| 1st_SPIM_MISO                              | 1st_SPI master in slave out | DI    |
| SDC1_DATA_1                                | SDC1_DATA_1                 | DI/DO |
| 1st_SPIM_EN_1                              | 1st_SPI chip select         | DO    |
| SDC1_DATA_0                                | SDC1_DATA_0                 | DI/DO |
| 1st_SPIM_CLK                               | 1st_SPI serial clock        | DO    |
| SDC1_CMD                                   | SDC1_CMD                    | DI/DO |
| SDC1_CLK                                   | SDC1_CLK                    | DO    |
| <b>Module Control and State Interfaces</b> |                             |       |
| WWAN_STATE                                 | Wireless WAN Radio State    | DO    |
| POWER_ON                                   | Power On the module         | DI    |
| WAKEUP_OUT                                 | Module wakes up host        | DO    |
| WAKEUP_IN                                  | Host wakes up module        | DI    |
| RESET                                      | Reset the module            | DI    |
| <b>Power and Ground</b>                    |                             |       |
| VREF                                       | Voltage Reference Output    | AO    |
| VCC                                        | Main Power                  | AI    |
| GND                                        | GND                         | AI    |
| <b>General Purpose</b>                     |                             |       |
| GPIO                                       | Digital I/O                 | DI/DO |

|                              |                       |                         |       |
|------------------------------|-----------------------|-------------------------|-------|
|                              | ADC_CONVENTOR         | ADC_CONVENTOR           | AI    |
| <b>AUDIO- PCM/I2S</b>        |                       |                         |       |
|                              | PCM_DIN               | PCM_DIN                 | DI    |
|                              | I2S_DATA0             | I2S_DATA0               | DI/DO |
|                              | PCM_DOUT              | PCM_DOUT                | DO    |
|                              | I2S_DATA1             | I2S_DATA1               | DI/DO |
|                              | PCM_CLK               | PCM_CLK                 | DO    |
|                              | I2S_SCK               | I2S_SCK                 | DO    |
|                              | PCM_SYNC              | PCM_SYNC                | DO    |
|                              | I2S_WS                | I2S_WS                  | DO    |
| <b>RFU- RFU</b>              |                       |                         |       |
|                              | RFU                   | Reserved For Future Use | -     |
| <b>Debug- JTAG</b>           |                       |                         |       |
|                              | JTAG_SRST_N           | JTAG reset for debug    | DI    |
|                              | JTAG_TCK              | JTAG clock input        | DI    |
|                              | JTAG_TDI              | JTAG data input         | DI    |
|                              | JTAG_TDO              | JTAG data output        | DO    |
|                              | JTAG_TMS              | JTAG mode select input  | DI    |
|                              | JTAG_TRST_N           | JTAG reset              | DO    |
|                              | PS_HOLD               | PS_HOLD                 | DI    |
| <b>Debug- Force_USB_BOOT</b> |                       |                         |       |
|                              | Force_USB_BOOT_CONFIG | Force USB BOOT CONFIG   | DI    |

Table 4. Pin Assignments

| Pin No. | Modem mode | Host Mode | Voltage Level (V) |      |      |
|---------|------------|-----------|-------------------|------|------|
|         |            |           | Min.              | Typ. | Max. |
| 1       | GND        | GND       | -                 | 0    | -    |
| 2       | GND        | GND       | -                 | 0    | -    |
| 3       | NC         | NC        | -                 | -    | -    |
| 4       | GND        | GND       | -                 | 0    | -    |
| 5       | GND        | GND       | -                 | 0    | -    |
| 6       | GND        | GND       | -                 | 0    | -    |
| 7       | GND        | GND       | -                 | 0    | -    |
| 8       | GND        | GND       | -                 | 0    | -    |
| 9       | RF_GNSS    | RF_GNSS   | -                 | -    | -    |
| 10      | GND        | GND       | -                 | 0    | -    |

|    |                 |                 |     |     |     |
|----|-----------------|-----------------|-----|-----|-----|
| 11 | GND             | GND             | -   | 0   | -   |
| 12 | GND             | GND             | -   | 0   | -   |
| 13 | GND             | GND             | -   | 0   | -   |
| 14 | GND             | GND             | -   | 0   | -   |
| 15 | RF_1            | RF_1            | -   | -   | -   |
| 16 | GND             | GND             | -   | 0   | -   |
| 17 | GND             | GND             | -   | 0   | -   |
| 18 | GND             | GND             | -   | 0   | -   |
| 19 | GND             | GND             | -   | 0   | -   |
| 20 | GND             | GND             | -   | 0   | -   |
| 21 | RF_2            | RF_2            | -   | -   | -   |
| 22 | GND             | GND             | -   | 0   | -   |
| 23 | GND             | GND             | -   | 0   | -   |
| 24 | GND             | GND             | -   | 0   | -   |
| 25 | GND             | GND             | -   | 0   | -   |
| 26 | GND             | GND             | -   | 0   | -   |
| 27 | NC              | NC              | -   | -   | -   |
| 28 | GND             | GND             | -   | 0   | -   |
| 29 | GND             | GND             | -   | 0   | -   |
| 30 | GND             | GND             | -   | 0   | -   |
| 31 | GND             | GND             | -   | 0   | -   |
| 32 | GND             | GND             | -   | 0   | -   |
| 33 | NC              | NC              | -   | -   | -   |
| 34 | GND             | GND             | -   | 0   | -   |
| 35 | GND             | GND             | -   | 0   | -   |
| 36 | GND             | GND             | -   | 0   | -   |
| 37 | VCC1            | VCC1            | 3.3 | 3.8 | 4.2 |
| 38 | VCC2            | VCC2            | 3.3 | 3.8 | 4.2 |
| 39 | VCC3            | VCC3            | 3.3 | 3.8 | 4.2 |
| 40 | VCC4            | VCC4            | 3.3 | 3.8 | 4.2 |
| 41 | VCC5            | VCC5            | 3.3 | 3.8 | 4.2 |
| 42 | VCC6            | VCC6            | 3.3 | 3.8 | 4.2 |
| 43 | NC              | NC              | -   | -   | -   |
| 44 | GND             | GND             | -   | 0   | -   |
| 45 | GND             | GND             | -   | 0   | -   |
| 46 | PCM_SYNC/GPIO46 | PCM_SYNC/GPIO46 | 1.7 | 1.8 | 1.9 |

|    |                                               |                                               |     |       |     |
|----|-----------------------------------------------|-----------------------------------------------|-----|-------|-----|
| 47 | PCM_DIN/GPIO47                                | PCM_DIN/GPIO47                                | 1.7 | 1.8   | 1.9 |
| 48 | PCM_DOUT/GPIO48                               | PCM_DOUT/GPIO48                               | 1.7 | 1.8   | 1.9 |
| 49 | PCM_CLK/GPIO49                                | PCM_CLK/GPIO49                                | 1.7 | 1.8   | 1.9 |
| 50 | GND                                           | GND                                           | -   | 0     | -   |
| 51 | GND                                           | GND                                           | -   | 0     | -   |
| 52 | GPIO01/Force USB<br>BOOT Config* <sup>8</sup> | GPIO01/Force USB<br>BOOT Config* <sup>8</sup> | 1.7 | 1.8   | 1.9 |
| 53 | GPIO02                                        | GPIO02                                        | 1.7 | 1.8   | 1.9 |
| 54 | GPIO03                                        | GPIO03                                        | 1.7 | 1.8   | 1.9 |
| 55 | GPIO04                                        | GPIO04                                        | 1.7 | 1.8   | 1.9 |
| 56 | NC                                            | SGMII_TX_P                                    | -   | Note5 | -   |
| 57 | NC                                            | SGMII_TX_M                                    | -   | Note5 | -   |
| 58 | NC                                            | SGMII_RX_P                                    | -   | Note5 | -   |
| 59 | NC                                            | SGMII_RX_M                                    | -   | Note5 | -   |
| 60 | I2C_SDA                                       | I2C_SDA/<br>2nd_SPI_EN_1                      | 1.7 | 1.8   | 1.9 |
| 61 | I2C_SCL                                       | I2C_SCL/<br>2nd_SPI_CLK                       | 1.7 | 1.8   | 1.9 |
| 62 | NC                                            | 2nd_SPI_MOSI                                  | 1.7 | 1.8   | 1.9 |
| 63 | NC                                            | 2nd_SPI_MISO                                  | 1.7 | 1.8   | 1.9 |
| 74 | GND                                           | GND                                           | -   | 0     | -   |
| 75 | GND                                           | GND                                           | -   | 0     | -   |
| 76 | RFFE1_DATA                                    | RFFE1_DATA                                    | -   | -     | -   |
| 77 | RFFE1_CLK                                     | RFFE1_CLK                                     | -   | -     | -   |
| 78 | NC                                            | NC                                            | -   | -     | -   |
| 79 | NC                                            | NC                                            | -   | -     | -   |
| 80 | UART1_CTS (UART 1)                            | UART1_CTS (UART 1)                            | 1.7 | 1.8   | 1.9 |
| 81 | UART1_RTS (UART 1)                            | UART1_RTS (UART 1)                            | 1.7 | 1.8   | 1.9 |
| 82 | UART1_RX (UART 1)                             | UART1_RX (UART 1)                             | 1.7 | 1.8   | 1.9 |
| 83 | UART1_TX (UART 1)                             | UART1_TX (UART 1)                             | 1.7 | 1.8   | 1.9 |
| 84 | GND                                           | GND                                           | -   | 0     | -   |
| 85 | GND                                           | GND                                           | -   | 0     | -   |
| 86 | USB_Dp                                        | USB_Dp                                        | -   | Note6 | -   |
| 87 | USB Detect* <sup>7</sup>                      | USB Detect* <sup>7</sup>                      | 1.7 | 1.8   | 1.9 |
| 88 | USB_Dn                                        | USB_Dn                                        | -   | Note6 | -   |
| 89 | GND                                           | GND                                           | -   | 0     | -   |

|     |                   |                               |     |       |     |
|-----|-------------------|-------------------------------|-----|-------|-----|
| 90  | GND               | GND                           | -   | 0     | -   |
| 91  | GND               | GND                           | -   | 0     | -   |
| 92  | NC                | GPIO92                        | 1.7 | 1.8   | 1.9 |
| 93  | GPIO93            | GPIO93                        | 1.7 | 1.8   | 1.9 |
| 94  | GPIO94            | GPIO94                        | 1.7 | 1.8   | 1.9 |
| 95  | GPIO95            | GPIO95                        | 1.7 | 1.8   | 1.9 |
| 96  | GPIO96            | GPIO96                        | 1.7 | 1.8   | 1.9 |
| 97  | GPIO97            | GPIO97                        | 1.7 | 1.8   | 1.9 |
| 98  | NC                | GPIO98                        | 1.7 | 1.8   | 1.9 |
| 99  | NC                | NC                            | -   | -     | -   |
| 100 | NC                | NC                            | -   | -     | -   |
| 101 | NC                | GPIO101                       | 1.7 | 1.8   | 1.9 |
| 102 | NC                | GPIO102                       | 1.7 | 1.8   | 1.9 |
| 103 | NC                | EPHY_RST_N                    | 1.7 | 1.8   | 1.9 |
| 104 | GND               | GND                           | -   | 0     | -   |
| 105 | GND               | GND                           | -   | 0     | -   |
| 106 | UART2_RX (UART 2) | UART2_RX (UART 2)             | 1.7 | 1.8   | 1.9 |
| 107 | UART2_TX (UART 2) | UART2_TX (UART 2)             | 1.7 | 1.8   | 1.9 |
| 108 | GND               | GND                           | -   | 0     | -   |
| 109 | GND               | GND                           | -   | 0     | -   |
| 120 | NC                | SGMII_MDC                     | -   | Note5 | -   |
| 121 | NC                | SGMII_MDIO                    | -   | Note5 | -   |
| 122 | AD Converter      | AD Converter                  | 0.1 | -     | 1.7 |
| 123 | NC                | SDC1_CMD                      | 1.7 | 1.8   | 1.9 |
| 124 | NC                | SDC1_CLK                      | 1.7 | 1.8   | 1.9 |
| 125 | 1st_SPI_MOSI      | SDC1_DATA_3/<br>1st_SPIM_MOSI | 1.7 | 1.8   | 1.9 |
| 126 | 1st_SPI_MISO      | SDC1_DATA_2/<br>1st_SPIM_MISO | 1.7 | 1.8   | 1.9 |
| 127 | 1st_SPI_EN_1      | SDC1_DATA_1/<br>1st_SPIM_EN_1 | 1.7 | 1.8   | 1.9 |
| 128 | 1st_SPI_CLK       | SDC1_DATA_0/<br>1st_SPIM_CLK  | 1.7 | 1.8   | 1.9 |
| 129 | GPIO05            | GPIO05                        | 1.7 | 1.8   | 1.9 |
| 130 | GPIO06            | GPIO06                        | 1.7 | 1.8   | 1.9 |
| 131 | GPIO07            | GPIO07                        | 1.7 | 1.8   | 1.9 |

|     |                          |                          |         |         |         |
|-----|--------------------------|--------------------------|---------|---------|---------|
| 132 | GPIO08                   | EPHY_INT_N/GPIO08        | 1.7     | 1.8     | 1.9     |
| 133 | UIM_VCC                  | UIM_VCC                  | 1.7/2.7 | 1.8/3.0 | 1.9/3.3 |
| 134 | UIM_DATA                 | UIM_DATA                 | 1.7/2.7 | 1.8/3.0 | 1.9/3.3 |
| 135 | UIM_CLK                  | UIM_CLK                  | 1.7/2.7 | 1.8/3.0 | 1.9/3.3 |
| 136 | UIM_RESET                | UIM_RESET                | 1.7/2.7 | 1.8/3.0 | 1.9/3.3 |
| 137 | UIM_DETECT               | UIM_DETECT               | 1.7     | 1.8     | 1.9     |
| 138 | NC                       | NC                       | -       | -       | -       |
| 139 | GND                      | GND                      | -       | 0       | -       |
| 140 | GND                      | GND                      | -       | 0       | -       |
| 141 | WWAN_STATE               | WWAN_STATE               | 1.7     | 1.8     | 1.9     |
| 142 | POWER_ON <sup>*4</sup>   | POWER_ON <sup>*4</sup>   | 1.7     | 1.8     | 1.9     |
| 143 | WAKEUP_OUT <sup>*2</sup> | WAKEUP_OUT <sup>*2</sup> | 1.7     | 1.8     | 1.9     |
| 144 | WAKEUP_IN <sup>*3</sup>  | WAKEUP_IN <sup>*3</sup>  | 1.7     | 1.8     | 1.9     |
| 145 | RESET                    | RESET                    | 1.7     | 1.8     | 1.9     |
| 146 | VREF                     | VREF                     | 1.7     | 1.8     | 1.9     |
| 200 | JTAG_SRST_N              | JTAG_SRST_N              | 1.7     | 1.8     | 1.9     |
| 201 | JTAG TCK                 | JTAG TCK                 | 1.7     | 1.8     | 1.9     |
| 202 | JTAG TDI                 | JTAG TDI                 | 1.7     | 1.8     | 1.9     |
| 203 | JTAG TDO                 | JTAG TDO                 | 1.7     | 1.8     | 1.9     |
| 204 | JTAG_TMS                 | JTAG_TMS                 | 1.7     | 1.8     | 1.9     |
| 205 | JTAG TRST_N              | JTAG TRST_N              | 1.7     | 1.8     | 1.9     |
| 206 | PS_HOLD                  | PS_HOLD                  | 1.7     | 1.8     | 1.9     |
| 207 | NC                       | NC                       | -       | -       | -       |

Notes: \*2. Do not pull pin143 WAKEUP\_OUT to high; otherwise boot will fail.

\*3. Pull Pin144 WAKEUP\_IN to VREF with a 100k resistor and keep it high before system boot process is complete.

\*4. Pull pin142 POWER\_ON to VREF with a 100k resistor for stability considerations.

\*5. Refer to SGMII standard for more electronic characteristics.

\*6. Refer to section 2.3, for more information please check USB2.0 standard

\*7. Pull pin87 USB detect to VREF with a 100k resistor to enable module USB, pull pin87 low to disable module USB, CPU USB PHY consumes some current when USB is enabled.

\*8. Do not pull pin52 to high before the system boot process is complete.

\*9. Leave unused pins floating

- \*10. Reserve test points on pin52/86/88/106/107 for debug purpose if possible.
- \*11. If voltage level of digital I/O from the other side is not compatible with module, level shifter is recommended to transfer the voltage level to 1.8V.



Note2,3,4,8,9,10 must be followed otherwise module may fail or malfunction.

Table 5. Digital I/O characteristics

| Parameter         |                                        | Comments                      | Min                       | Max                       | Unit |
|-------------------|----------------------------------------|-------------------------------|---------------------------|---------------------------|------|
| V <sub>IH</sub>   | High-level input voltage               | CMOS/Schmitt                  | 0.65 * V <sub>DD_Px</sub> | –                         | V    |
| V <sub>IL</sub>   | Low-level input voltage                | CMOS/Schmitt                  | –                         | 0.35 * V <sub>DD_Px</sub> | V    |
| V <sub>OH</sub>   | High-level output voltage              | CMOS, at rated drive strength | V <sub>DD_Px</sub> - 0.45 |                           | V    |
| V <sub>OL</sub>   | Low-level output voltage               | CMOS, at rated drive strength | –                         | 0.45                      | V    |
| R <sub>P</sub>    | Pull resistance                        | Pullup and pulldown           | 55                        | 390                       | kΩ   |
| R <sub>K</sub>    | Keeper resistance                      |                               | 30                        | 150                       | kΩ   |
| I <sub>IH</sub>   | Input high leakage current             | No pulldown                   | –                         | 1                         | μA   |
| I <sub>IL</sub>   | Input low leakage current <sup>4</sup> | No pullup                     | -1                        | –                         | μA   |
| V <sub>SHYS</sub> | Schmitt hysteresis voltage             |                               | 100                       | –                         | mV   |
| C <sub>I/O</sub>  | I/O capacitance                        |                               | –                         | 5                         | pF   |

Below is the I/O default setting table to describe the level. It's recommended to follow the pulling High or Low to choose a suitable GPIO for application.

PU: Pull Up.

PD: Pull Down

NP: Non-Pull

Table 6. I/O default setting table

| Pin No. | Signal Name     | Type   | Default setting in Normal mode |
|---------|-----------------|--------|--------------------------------|
| 46      | PCM_SYNC/GPIO46 | DI /DO | PD                             |
| 47      | PCM_IN/GPIO47   | DI /DO | PD                             |
| 48      | PCM_OUT/GPIO48  | DI /DO | PD                             |
| 49      | PCM_CLK/GPIO49  | DI /DO | PD                             |
| 52      | GPIO01          | DI/DO  | PD                             |
| 53      | GPIO02          | DI/DO  | PD                             |
| 54      | GPIO03          | DI/DO  | PD                             |
| 55      | GPIO04          | DI/DO  | PD                             |
| 60      | I2C_SCL/        | DI/DO  | PD                             |

|            |                          |       |    |
|------------|--------------------------|-------|----|
|            | 2nd_SPI_CLK              |       |    |
| <b>61</b>  | I2C_SDA/<br>2nd_SPI_EN_1 | DI/DO | PD |
| <b>62</b>  | 2nd_SPI_MOSI             | DI/DO | PD |
| <b>63</b>  | 2nd_SPI_MISO             | DI/DO | PD |
| <b>80</b>  | UART1_CTS (UART1)        | DI/DO | PD |
| <b>81</b>  | UART1_RTS (UART1)        | DI/DO | PD |
| <b>82</b>  | UART1_RX (UART1)         | DI/DO | PD |
| <b>83</b>  | UART1_TX (UART1)         | DI/DO | PD |
| <b>92</b>  | GPIO92                   | DI/DO | PD |
| <b>93</b>  | GPIO93                   | DO    | NP |
| <b>94</b>  | GPIO94                   | DI/DO | PD |
| <b>95</b>  | GPIO95                   | DI/DO | PD |
| <b>96</b>  | GPIO96                   | DI/DO | PD |
| <b>97</b>  | GPIO97                   | DI/DO | PD |
| <b>98</b>  | GPIO98                   | DI/DO | PU |
| <b>101</b> | GPIO101                  | DI/DO | PD |
| <b>102</b> | GPIO102                  | DI/DO | PD |
| <b>103</b> | GPIO103                  | DI/DO | PD |
| <b>106</b> | UART2_RX (UART2)         | DI/DO | PD |
| <b>107</b> | UART2_TX (UART2)         | DI/DO | PD |
| <b>120</b> | GPIO120                  | DI/DO | PD |
| <b>123</b> | GPIO123                  | DI/DO | PD |
| <b>124</b> | GPIO124                  | DI/DO | NP |
| <b>125</b> | SPIM_MOSI                | DI/DO | PD |
| <b>126</b> | SPIM_MISO                | DI/DO | PD |
| <b>127</b> | SPIM_EN                  | DI/DO | PD |
| <b>128</b> | SPIM_CLK                 | DI/DO | PD |
| <b>129</b> | GPIO05                   | DI/DO | PD |
| <b>130</b> | GPIO06                   | DI/DO | PD |
| <b>131</b> | GPIO07                   | DI/DO | PU |
| <b>132</b> | GPIO08                   | DI/DO | PD |
| <b>141</b> | WWAN_STATE               | DI/DO | PD |

|     |            |       |    |
|-----|------------|-------|----|
| 143 | WAKEUP_OUT | DI/DO | PD |
|-----|------------|-------|----|

2.2. Power supply

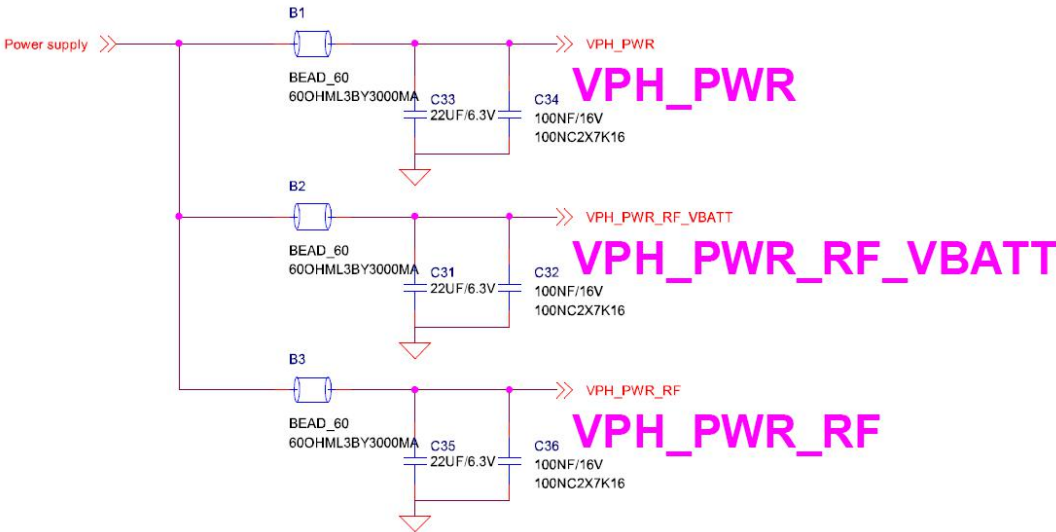
LTE module power input is VCC. The internal power chipset will transfer VCC to other power level.

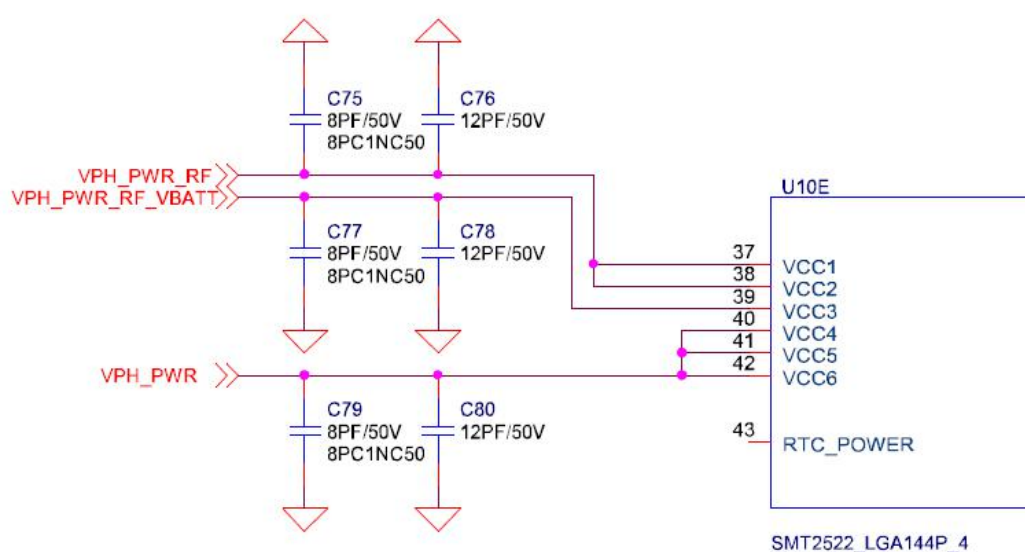
Table 7. Power supply voltage level

| Power | Pin Name     | Pads          | Description       | Voltage Level (V) |      |      |
|-------|--------------|---------------|-------------------|-------------------|------|------|
|       |              |               |                   | Min.              | Typ. | Max. |
| VCC   | VCC1 to VCC6 | Nos. 37 to 42 | Main Power Supply | 3.3               | 3.8  | 4.2  |

The M18QF/M18QA Series include an integrated power manager enabling single and direct voltage supply from the battery, reducing the overall bill of materials. The typical voltage 3.8V is recommended.

**Schematic suggestion:** Must to separate module power supply to three paths to keep power clean as below for TX spurious performance. The VPH\_PWR is for Baseband and RF transceiver, the VPH\_PWR\_RF is for RF PA, the VPH\_PWR\_RF\_VBATT is for RF PA control circuit.





**Layout Suggestion:** The 22 $\mu$ F, 0.1 $\mu$ F, 12pF and 8pF capacitors are required to place near VCC pins as close as possible. Each power trace should possess sufficient line width to withstand its respective current listed in the table below:

| Net Name       | Current Value |
|----------------|---------------|
| VCC(1–2) total | 2A            |
| VCC(3) total   | 100mA         |
| VCC(4–6) total | 1A            |
| UIM_VCC        | 150 mA        |
| VREF           | 300 mA        |

## 2.3. USB interface

The M18QF/M18QA Series modules comply with USB 2.0 high-speed protocol. The USB input/output lines follow USB 2.0 specifications.

Table 8. Signals of the USB interface

| Name | Description                         | Input/Output<br>(Direction to module) | Voltage Level (V) |      |      |
|------|-------------------------------------|---------------------------------------|-------------------|------|------|
|      |                                     |                                       | Min.              | Typ. | Max. |
| D+   | USB data positive (low-/full-speed) | Input High                            | 2                 | 3.3  | 3.6  |

|                                     |             |      |      |      |
|-------------------------------------|-------------|------|------|------|
|                                     | Input Low   | 0    |      | 0.8  |
|                                     | Output High | 2.8  | 3.3  | 3.6  |
|                                     | Output Low  |      |      | 0.3  |
| USB data positive (high-speed)      |             |      |      |      |
|                                     | Input High  | 0.3  |      | 0.44 |
|                                     | Input Low   | 0    |      | 0.01 |
|                                     | Output High | 0.36 | 0.38 | 0.44 |
|                                     | Output Low  | 0    |      | 0.01 |
| D-                                  |             |      |      |      |
| USB data negative (low-/full-speed) |             |      |      |      |
|                                     | Input High  | 2    | 3.3  | 3.6  |
|                                     | Input Low   | 0    |      | 0.8  |
|                                     | Output High | 2.8  | 3.3  | 3.6  |
|                                     | Output Low  |      |      | 0.3  |
| USB data negative (high-speed)      |             |      |      |      |
|                                     | Input High  | 0.3  |      | 0.44 |
|                                     | Input Low   | 0    |      | 0.01 |
|                                     | Output High | 0.36 | 0.38 | 0.44 |
|                                     | Output Low  | 0    |      | 0.01 |

The layout design of this circuit on the carrier board should comply with the USB 2.0 high-speed protocol.

**Layout suggestion:**

- Differential impedance: 90  $\Omega$
- Space to other signals should be at least 20 mils
- Intra-lane length difference should be less than 150 mils
- Maximum length for each trace: 150 mm

Signals lengths on modules are tuned as below:

| Function | Net    | Length (mil) |
|----------|--------|--------------|
| USB      |        |              |
|          | USB_Dp | 545.54       |
|          | USB_Dn | 503.04       |

## 2.4. SGMII interface

The M18QF/M18QA Series modules integrate Ethernet MAC with SGMII interfaces with the following key features:

- IEEE 802.3 compliance
- Full duplex at 1 Gbps
- Half/full duplex for 10/100 Mbps
- Supports VLAN tagging
- Supports IEEE 1588, Precision Time Protocol (PTP)
- Can be used to connect to external Ethernet PHYs such as AR8033 or to an external switch

The following figure illustrates an example of the additional logic connection between the modules and the Ethernet chip. Refer to ENG-46158, Rev 1.8 for electrical and timing specifications.

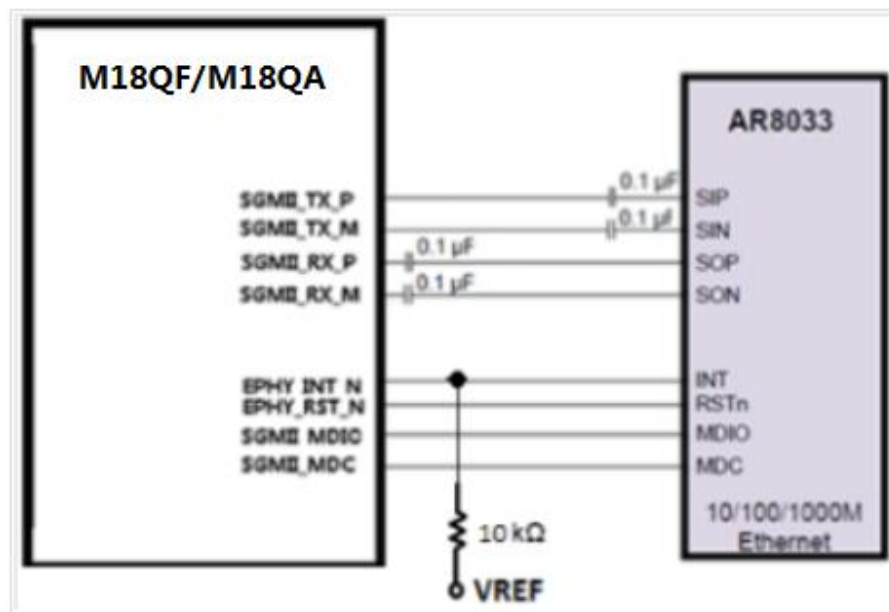


Figure 2. SGMII circuit example

### Layout suggestion:

- Differential impedance: 100 Ω
- Space to other signals: > 3x line width
- Lane-to-lane space: > 3x line width
- Intra-lane mismatch: < 0.7 mm

Signal lengths on the modules are tuned as below:

| Function     | Net                     | Length (mil) |
|--------------|-------------------------|--------------|
| <b>SGMII</b> |                         |              |
|              | SGMII_TX_P              | 617.11       |
|              | SGMII_TX_M              | 642.13       |
|              | SGMII_RX_P_C+SGMII_RX_P | 661.40       |
|              | SGMII_RX_M_C+SGMII_RX_M | 675.06       |

## 2.5. UIM interface

M18QF/M18QA Series modules provide an UIM\_DETECT input pin for UIM connector to detect UIM card. When UIM card is present, UIM\_DETECT should be high (1.8V). If UIM card is absent, UIM\_DETECT should be low. It's required to pull UIM\_DETECT to VREF with a 470k resistor.

A 0.1μF and a 33pF capacitor are recommended to place between UIM\_VCC and Ground in parallel. A 33pF capacitor is recommended to place between UIM\_RESET, UIM\_CLK and UIM\_DATA and Ground in parallel, see Figure5 for reference.

Electrostatic discharge (ESD) protection circuit is also recommended to place near the UIM socket as close as possible, and the Ground pin of the ESD protection component must be well connected to the Ground plane.

The following figure shows an example of UIM card circuit.



## 5.2.2 Reset (RST) (contact C2)

The terminal shall operate the UICC within the following limits.

**Table 5.6: Electrical characteristics of RESET (RST) under normal operating conditions**

| Symbol                                                                                                                       | Conditions                 | Minimum             | Maximum             | Unit    |
|------------------------------------------------------------------------------------------------------------------------------|----------------------------|---------------------|---------------------|---------|
| $V_{OH}$                                                                                                                     | $I_{OHmax} = +20 \mu A$    | $0,8 \times V_{CC}$ | $V_{CC}$ (see note) | V       |
| $V_{OL}$                                                                                                                     | $I_{OLmax} = -200 \mu A$   | 0 (see note)        | $0,2 \times V_{CC}$ | V       |
| $t_R t_F$                                                                                                                    | $C_{in} = C_{out} = 30 pF$ |                     | 400                 | $\mu s$ |
| NOTE: To allow for overshoot the voltage on RST should remain between -0,3 V and $V_{CC} + 0,3 V$ during dynamic operations. |                            |                     |                     |         |

## 5.2.3 Clock CLK (contact C3)

The terminal shall support 1 MHz to 5 MHz. The terminal shall supply the clock. When only the interface specified in the present document is activated, no "internal clock" shall be used in the UICC.

The duty cycle shall be between 40 % and 60 % of the period during stable operation.

The terminal shall operate the UICC within the following limits.

**Table 5.7: Electrical characteristics of Clock (CLK) under normal operating conditions**

| Symbol                                                                                                                       | Conditions                 | Minimum             | Maximum             | Unit |
|------------------------------------------------------------------------------------------------------------------------------|----------------------------|---------------------|---------------------|------|
| $V_{OH}$                                                                                                                     | $I_{OHmax} = +20 \mu A$    | $0,7 \times V_{CC}$ | $V_{CC}$ (see note) | V    |
| $V_{OL}$                                                                                                                     | $I_{OLmax} = -20 \mu A$    | 0 (see note)        | $0,2 \times V_{CC}$ | V    |
| $t_R t_F$                                                                                                                    | $C_{in} = C_{out} = 30 pF$ |                     | 50                  | ns   |
| NOTE: To allow for overshoot the voltage on CLK should remain between -0,3 V and $V_{CC} + 0,3 V$ during dynamic operations. |                            |                     |                     |      |

## 5.2.4 I/O (contact C7)

Table 5.8 defines the electrical characteristics of the I/O (contact C7). The values given in the table allow the derivation of the values of the pull-up resistor in the terminal and the impedance of the drivers and receivers in the terminal and UICC.

**Table 5.8: Electrical characteristics of I/O under normal operating conditions**

| Symbol                                                                                                                                                                                                      | Conditions                              | Minimum             | Maximum                  | Unit          |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------|---------------------|--------------------------|---------------|
| $V_{IH}$                                                                                                                                                                                                    | $I_{IHmax} = \pm 20 \mu A$ (see note 2) | $0,7 \times V_{CC}$ | $V_{CC} + 0,3$           | V             |
| $V_{IL}$                                                                                                                                                                                                    | $I_{ILmax} = +1 mA$                     | -0,3                | $0,2 \times V_{CC}$      | V             |
| $V_{OH}$<br>(see note 1)                                                                                                                                                                                    | $I_{OHmax} = +20 \mu A$                 | $0,7 \times V_{CC}$ | $V_{CC}$ (see note 3)    | V             |
| $V_{OL}$                                                                                                                                                                                                    | $I_{OLmax} = -1mA$                      | 0 (see note 3)      | 0,4                      | V             |
| $t_R t_F$                                                                                                                                                                                                   | $C_{in} = C_{out} = 30 pF$              |                     | 1<br>100<br>(see note 4) | $\mu s$<br>ns |
| NOTE 1: It is assumed that a pull-up resistor is used on the interface device (recommended value: 20 k $\Omega$ ).                                                                                          |                                         |                     |                          |               |
| NOTE 2: During static conditions (idle state) only the positive value can apply. Under dynamic operating conditions (transmissions) short-term voltage spikes on the I/O line may cause a current reversal. |                                         |                     |                          |               |
| NOTE 3: To allow for overshoot the voltage on I/O shall remain between -0,3 V and $V_{CC} + 0,3 V$ during dynamic operation.                                                                                |                                         |                     |                          |               |
| NOTE 4: This value applies when the low impedance buffer is selected.                                                                                                                                       |                                         |                     |                          |               |

### 5.3 Class C operating conditions

#### 5.3.1 Supply voltage Vcc (contact C1)

The terminal shall operate the UICC within the following limits.

**Table 5.9: Electrical characteristics of Vcc under normal operating conditions**

| Symbol | Minimum | Maximum | Unit |
|--------|---------|---------|------|
| Vcc    | 1,62    | 1,98    | V    |

#### 5.3.2 Reset (RST) (contact C2)

The terminal shall operate the UICC within the following limits.

**Table 5.10: Electrical characteristics of RESET (RST) under normal operating conditions**

| Symbol                                                                                                                  | Conditions                                 | Minimum      | Maximum        | Unit    |
|-------------------------------------------------------------------------------------------------------------------------|--------------------------------------------|--------------|----------------|---------|
| V <sub>OH</sub>                                                                                                         | I <sub>OHmax</sub> = +20 $\mu$ A           | 0,8 x Vcc    | Vcc (see note) | V       |
| V <sub>OL</sub>                                                                                                         | I <sub>OLmax</sub> = -200 $\mu$ A          | 0 (see note) | 0,2 x Vcc      | V       |
| t <sub>R</sub> t <sub>F</sub>                                                                                           | C <sub>in</sub> = C <sub>out</sub> = 30 pF |              | 400            | $\mu$ s |
| NOTE: To allow for overshoot the voltage on RST should remain between -0,3 V and Vcc + 0,3 V during dynamic operations. |                                            |              |                |         |

#### 5.3.3 Clock CLK (contact C3)

**Table 5.11: Electrical characteristics of Clock (CLK) under normal operating conditions**

| Symbol                                                                                                                  | Conditions                                 | Minimum      | Maximum        | Unit |
|-------------------------------------------------------------------------------------------------------------------------|--------------------------------------------|--------------|----------------|------|
| V <sub>OH</sub>                                                                                                         | I <sub>OHmax</sub> = +20 $\mu$ A           | 0,7 x Vcc    | Vcc (see note) | V    |
| V <sub>OL</sub>                                                                                                         | I <sub>OLmax</sub> = -20 $\mu$ A           | 0 (see note) | 0,2 x Vcc      | V    |
| t <sub>R</sub> t <sub>F</sub>                                                                                           | C <sub>in</sub> = C <sub>out</sub> = 30 pF |              | 50             | ns   |
| NOTE: To allow for overshoot the voltage on CLK should remain between -0,3 V and Vcc + 0,3 V during dynamic operations. |                                            |              |                |      |

### 5.3.4 I/O (contact C7)

Table 5.12 defines the electrical characteristics of the I/O (contact C7). The values given in the table allow the derivation of the values of the pull-up resistor in the terminal and the impedance of the drivers and receivers in the terminal and UICC.

**Table 5.12: Electrical characteristics of I/O under normal operating conditions**

| Symbol                                                                                                                                                                                                      | Conditions                              | Minimum             | Maximum                  | Unit          |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------|---------------------|--------------------------|---------------|
| $V_{IH}$                                                                                                                                                                                                    | $I_{IHmax} = \pm 20 \mu A$ (see note 2) | $0,7 \times V_{CC}$ | $V_{CC} + 0,3$           | V             |
| $V_{IL}$                                                                                                                                                                                                    | $I_{ILmax} = +1 \text{ mA}$             | -0,3                | $0,2 \times V_{CC}$      | V             |
| $V_{OH}$<br>(see note 1)                                                                                                                                                                                    | $I_{OHmax} = +20 \mu A$                 | $0,7 \times V_{CC}$ | $V_{CC}$ (see note 3)    | V             |
| $V_{OL}$                                                                                                                                                                                                    | $I_{OLmax} = -1 \text{ mA}$             | 0 (see note 3)      | 0,3                      | V             |
| $t_R$ $t_F$                                                                                                                                                                                                 | $C_{in} = C_{out} = 30 \text{ pF}$      |                     | 1<br>100<br>(see note 4) | $\mu s$<br>ns |
| NOTE 1: It is assumed that a pull-up resistor is used on the interface device (recommended value: 20 k $\Omega$ ).                                                                                          |                                         |                     |                          |               |
| NOTE 2: During static conditions (idle state) only the positive value can apply. Under dynamic operating conditions (transmissions) short-term voltage spikes on the I/O line may cause a current reversal. |                                         |                     |                          |               |
| NOTE 3: To allow for overshoot the voltage on I/O shall remain between -0,3 V and $V_{CC} + 0,3 \text{ V}$ during dynamic operation.                                                                        |                                         |                     |                          |               |
| NOTE 4: This value applies when the low impedance buffer is selected.                                                                                                                                       |                                         |                     |                          |               |

## 2.6. Control interface

This section describes the power-on/off, wake-up and reset interface on how to control the module.

### 2.6.1. Power-on Signal

The POWER\_ON is an active Low input signal used to enable or disable the module. Do not toggle the PERST# pin during power-on. This signal has the highest priority over the wakeup, the alarms signals, and the digital control pins.

There are three possible states of the module:

- Module Off - VCC is not present.
- Module Enabled - VCC is supplied, and the module is enabled.
- Module Disabled - VCC is supplied, and the module is disabled.

The state transitions are defined as follows:

- When voltage is applied to VCC, the module shall enter the Module Disabled state.

- An input to the POWER\_ON pin shall trigger the transition from the Module Disabled to the Module Enabled state. See figure6, a low pulse( $t_{low} > 0s$ ) on POWER\_ON pad will enable the module after VCC is applied.
- An input to the POWER\_ON pin shall trigger the transition from the Module Enabled to the Module Disabled state. See figure6, after power on, a low pulse ( $t_{low} > 2s$ ) on POWER\_ON pin will disable (power-off) the module.

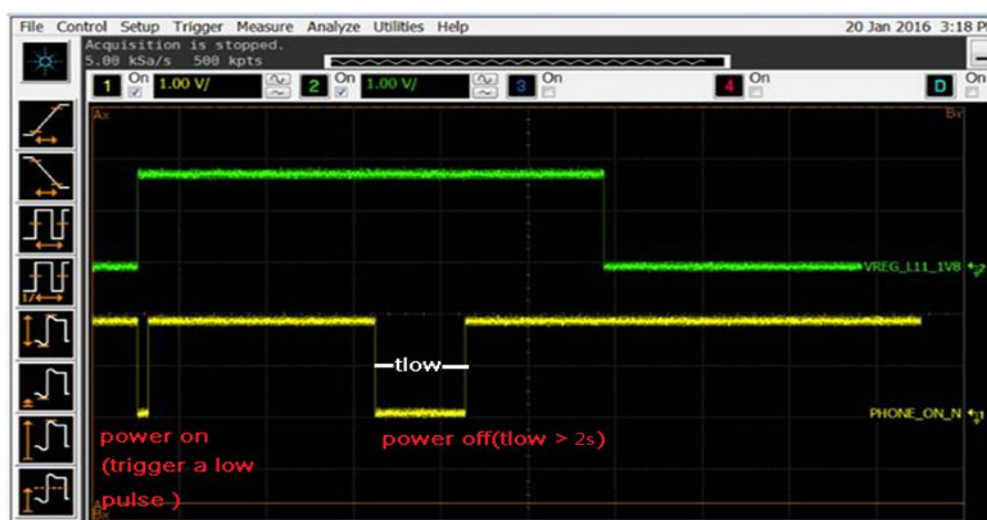


Figure 4. Power ON/OFF timing

### 2.6.2. Wake-up interface

In applications where power consumption is a major factor in performance metrics (such as battery-operated sensors that are based on IOT/M2M modem solution and also include a third party host), it is necessary to define a simple interface that will allow both the modem and the host to be able to enter low power states whenever possible and the other side to wake it up once required.

For example, if the host has no data to transmit or any other tasks, it may enter some low power state according to its own capabilities and configurations. If during that period the host is in a low power state and the modem suddenly receives data, it must wake-up the host.

A similar requirement exists from the other side. For example, if the modem is in a low power state and suddenly the host must transmit data, it must be able to wake-up the modem.

The interface consists of two signals: One is driven by the host and received by the modem; the other is driven by the modem and received by the host.

Each side can wake the other side by toggling wakeup signal high and allowing the other side to go to sleep when not needed by toggling it low.

■ “WAKEUP\_IN” (Host: Output, Modem: Input):

- LOW: SoC does not require the MODEM (allowing it to sleep).
- HIGH: SoC requires the MODEM or acknowledges it is ready following a wakeup request from the MODEM.

■ “WAKEUP\_OUT” (Host: Input, Modem: Output):

- LOW: The MODEM does not require the Host (allowing it to sleep)
- HIGH: The MODEM requires the Host or acknowledges it is ready following a wakeup request from the SoC.

When M18QF/M18QA Series modules act as modem, keep WAKEUP\_IN high before system boot process is complete, after system boot, keep WAKEUP\_IN low. WAKEUP\_IN and WAKEUP\_OUT behavior of host mode will be discussed according to product specification.

### 2.6.3. Reset Signal

The Reset Signal is a hardware reset signal to control the system reset directly. You can connect it to a key or a control signal. A low pulse ( $3s < t_{low} < 8s$ ) after power on will reset the module, see figure7.

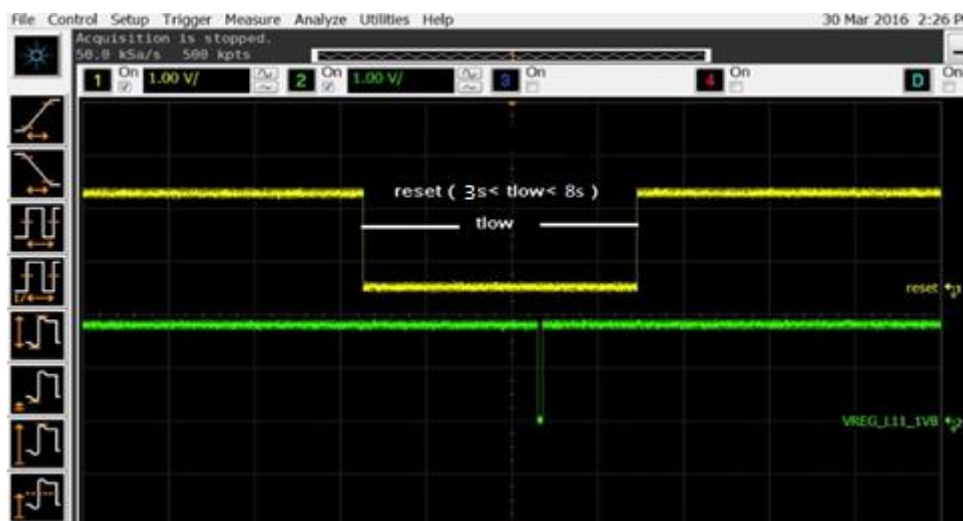


Figure 5. Reset Signals circuit

### 2.6.4. WWAN state Signal

The WWAN state pin definition as below.

- WWAN state pin output “high”  
When device register to network, the WWAN state pin output “high”.
- WWAN state pin output “low”  
When device not to register to network, the WWAN state pin output “low”.

## 2.7. Digital interface

This section provides required AC timing information related to module digital interfaces.

### 2.7.1. JTAG Interface

M18QF/M18QA Series provide one JTAG interface, leave JTAG pins floating if not used.

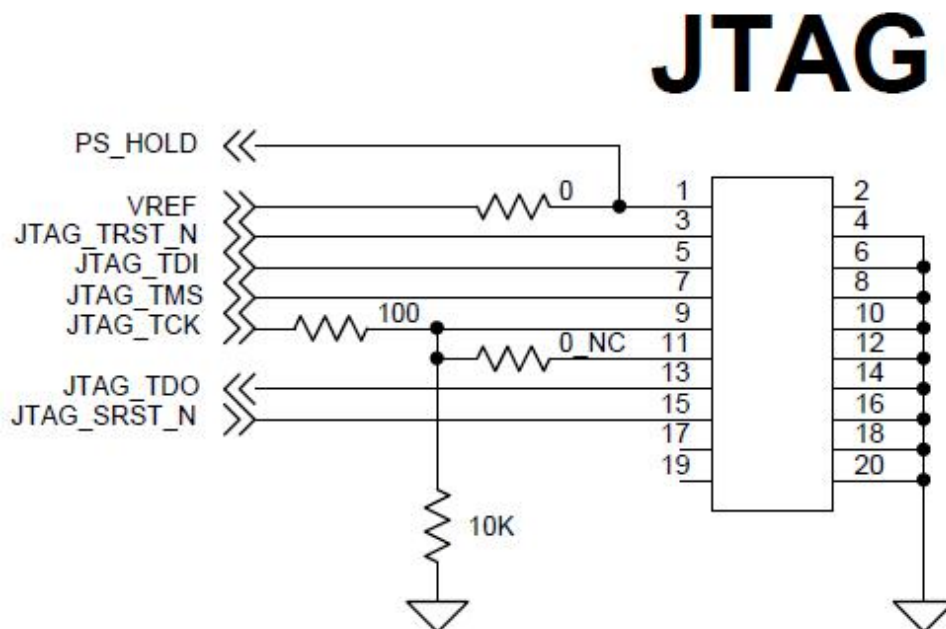


Figure 6. JTAG schematic (example)

### 2.7.2. SPI Master Interface

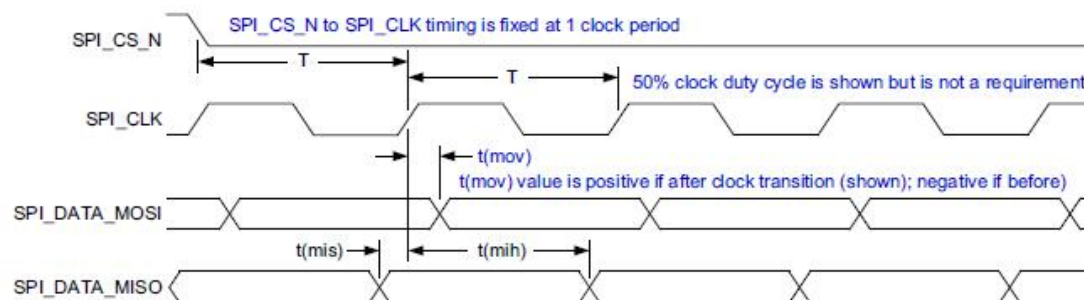
SPIM\_CLK – Output clock

SPIM\_CS – Output, chip-select

SPIM\_MOSI – Output, data to slave

SPIM\_MISO – Input, data from slave

## Timing



| Parameter      | Comments                     | Min  | Typ | Max | Unit |
|----------------|------------------------------|------|-----|-----|------|
| T <sup>1</sup> | SPI clock period: 50 MHz max | 20.0 | –   | –   | ns   |
| t(ch)          | Clock high                   | 9.0  | –   | –   | ns   |
| t(cl)          | Clock low                    | 9.0  | –   | –   | ns   |
| t(mov)         | Master output valid          | -5.0 | –   | 5.0 | ns   |
| t(mis)         | Master input setup           | 5.0  | –   | –   | ns   |
| t(mih)         | Master input hold            | 1.0  | –   | –   | ns   |

1. The minimum clock period includes 1% jitter of the maximum frequency.

Figure 7. SPI timing parameters

## 2.7.3. PCM Interface

M18QF/M18QA Series modules provide one PCM master digital audio interface. Keep PCM signal traces far away from noise and radiating signal on PCB

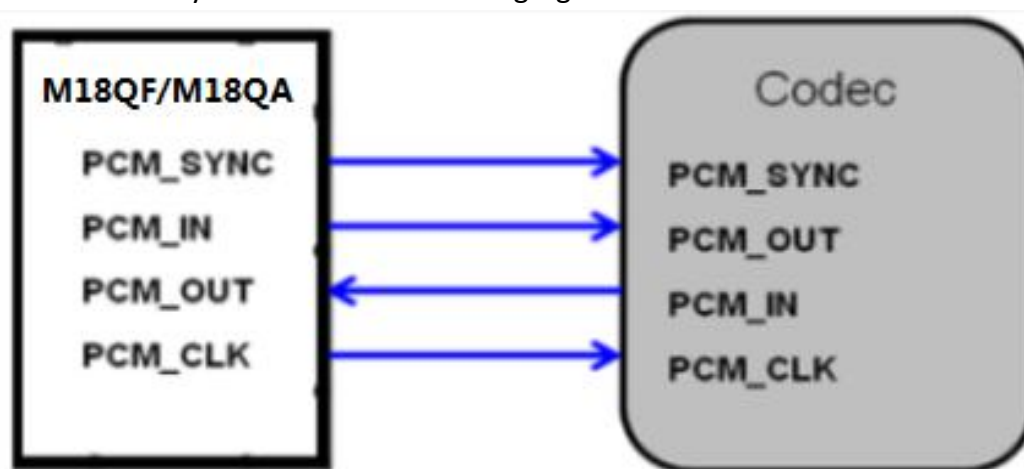


Figure 8. PCM connection (example)

## Timing

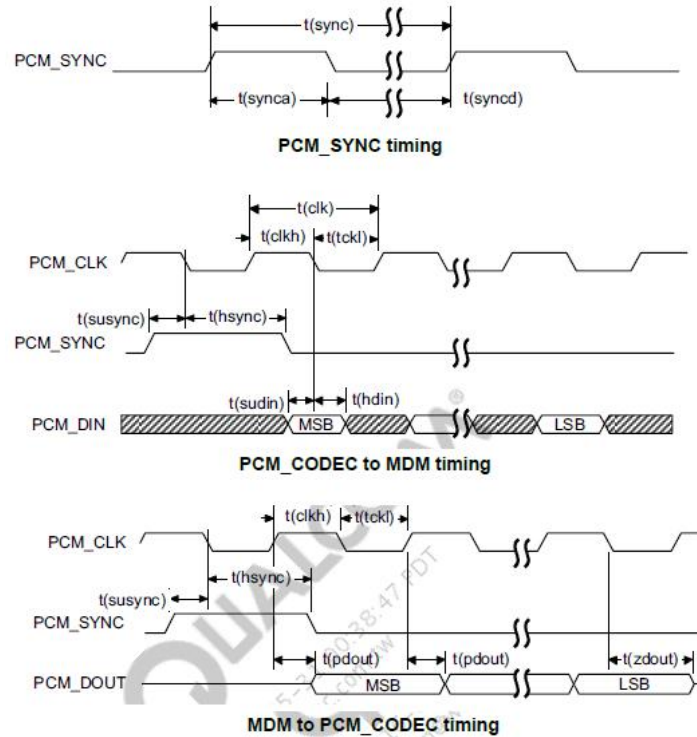


Figure 9. PCM timing diagram

| Parameter          | Comments                                      | Min | Typ   | Max | Unit          |
|--------------------|-----------------------------------------------|-----|-------|-----|---------------|
| $t(\text{sync})$   | PCM_SYNC cycle time                           | –   | 125   | –   | $\mu\text{s}$ |
| $t(\text{synca})$  | PCM_SYNC asserted time                        | –   | 488   | –   | ns            |
| $t(\text{syncd})$  | PCM_SYNC de-asserted time                     | –   | 124.5 | –   | $\mu\text{s}$ |
| $t(\text{clk})$    | PCM_CLK cycle time                            | –   | 488   | –   | ns            |
| $t(\text{clkh})$   | PCM_CLK high time                             | –   | 244   | –   | ns            |
| $t(\text{ckl})$    | PCM_CLK low time                              | –   | 244   | –   | ns            |
| $t(\text{susync})$ | PCM_SYNC offset time to PCM_CLK falling       | –   | 122   | –   | ns            |
| $t(\text{sudin})$  | PCM_DIN setup time to PCM_CLK falling         | 60  | –     | –   | ns            |
| $t(\text{hdin})$   | PCM_DIN hold time after PCM_CLK falling       | 10  | –     | –   | ns            |
| $t(\text{pdout})$  | Delay from PCM_CLK rising to PCM_DOUT valid   | –   | –     | 60  | ns            |
| $t(\text{zdout})$  | Delay from PCM_CLK falling to PCM_DOUT HIGH-Z | –   | 160   | –   | ns            |

Figure 10. PCM timing parameters

## 2.7.4. I2S Interface

PCM and I2S share the same pins on the modules, I2C only support master mode, keep I2S signal trace far away from noise and radiating signal on PCB

| Config1  | Config2   |
|----------|-----------|
| PCM_SYNC | I2S_WS    |
| PCM_DIN  | I2S_DATA0 |
| PCM_DOUT | I2S_DATA1 |
| PCM_CLK  | I2S_SCK   |

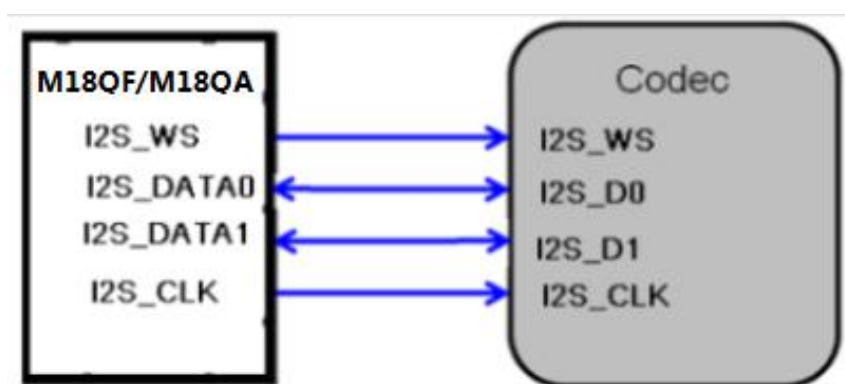


Figure 11. I2S connection (example)

## Timing

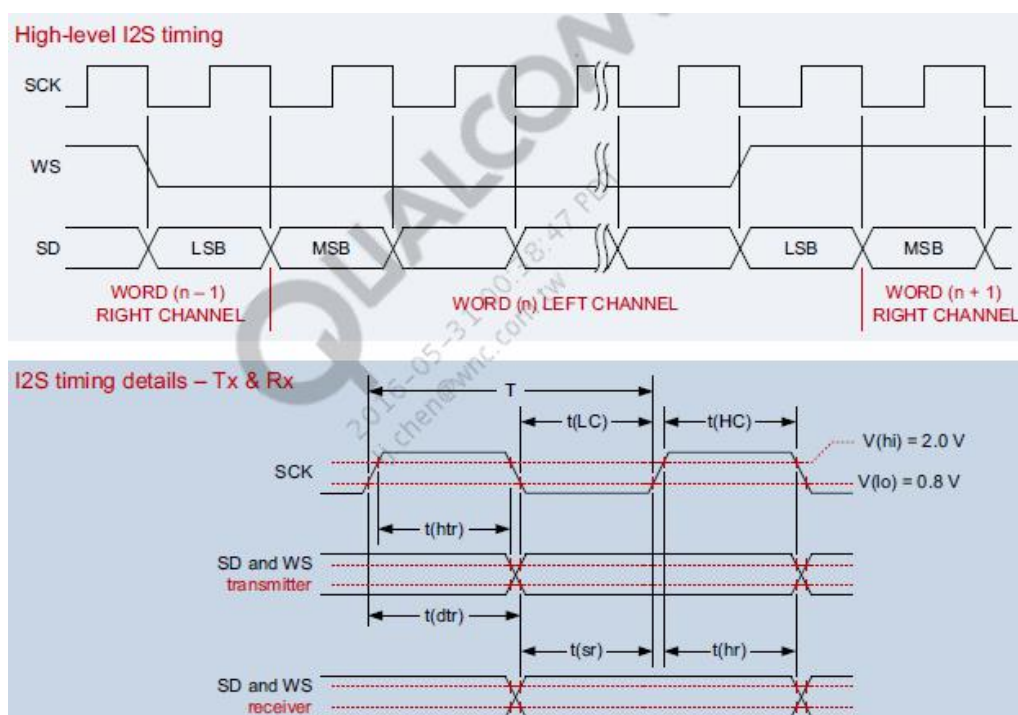


Figure 12. I2S timing diagram

| Parameter                 |                            | Comments <sup>1</sup> | Min            | Typ | Max            | Unit |
|---------------------------|----------------------------|-----------------------|----------------|-----|----------------|------|
| <i>Using internal SCK</i> |                            |                       |                |     |                |      |
|                           | Frequency                  |                       | –              | –   | 12.288         | MHz  |
| T                         | Clock period               |                       | 81.380         | –   | –              | ns   |
| t(HC)                     | Clock high                 |                       | $0.45 \cdot T$ | –   | $0.55 \cdot T$ | ns   |
| Parameter                 |                            | Comments <sup>1</sup> | Min            | Typ | Max            | Unit |
| t(LC)                     | Clock low                  |                       | $0.45 \cdot T$ | –   | $0.55 \cdot T$ | ns   |
| t(sr)                     | SD and WS input setup time |                       | 16.276         | –   | –              | ns   |
| t(hr)                     | SD and WS input hold time  |                       | 0              | –   | –              | ns   |
| t(dtr)                    | SD and WS output delay     |                       | –              | –   | 65.100         | ns   |
| t(htr)                    | SD and WS output hold time |                       | 0              | –   | –              | ns   |
| <i>Using external SCK</i> |                            |                       |                |     |                |      |
|                           | Frequency                  |                       | –              | –   | 12.288         | MHz  |
| T                         | Clock period               |                       | 81.380         | –   | –              | ns   |
| t(HC)                     | Clock high                 |                       | $0.45 \cdot T$ | –   | $0.55 \cdot T$ | ns   |
| t(LC)                     | Clock low                  |                       | $0.45 \cdot T$ | –   | $0.55 \cdot T$ | ns   |
| t(sr)                     | SD and WS input setup time |                       | 16.276         | –   | –              | ns   |
| t(hr)                     | SD and WS input hold time  |                       | 0              | –   | –              | ns   |
| t(dtr)                    | SD and WS output delay     |                       | –              | –   | 65.100         | ns   |
| t(htr)                    | SD and WS output hold time |                       | 0              | –   | –              | ns   |

1. Load capacitance is between 10 and 40 pF.

Figure 13. I2S timing parameters

### 2.7.5. I2C Interface

M18QF/M18QA Series modules provide one I2C interface, I2C only support master mode.

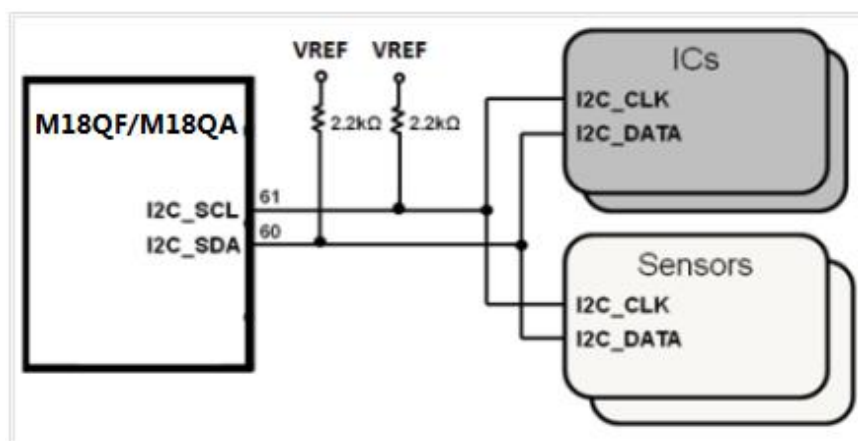


Figure 14. I2C connection (example)

### 2.7.6. UART Interface

There are two UART interfaces on M18QF/M18QA Series: One is a 4 bit UART(UART1) for high-speed data transfer, max baud rate can be up to 4Mbps. Another is a 2 bit UART(UART2) for diagnostic tools and debugging, the default baud rate 115200bps is recommended.

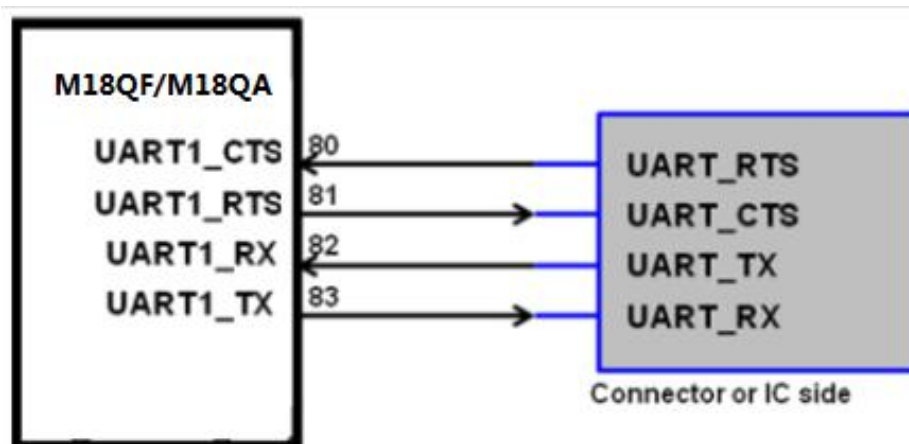


Figure 15. UART connection (example)

### 2.7.7. ADC Interface

An Analog to Digital Converter (ADC) input is provided by the M18QF/M18QA Series. The converter is 16 bit resolution, ranging from 0.1 V to 1.7 V, with a sampling rate of 2.4 MHz.

| Parameter              | Comments                        | Minimum | Typ | Maximum | Units |
|------------------------|---------------------------------|---------|-----|---------|-------|
| Supply voltage         | Connected internally to VREG_L3 | –       | 1.8 | –       | V     |
| Resolution             | Decimated data                  | –       | –   | 15      | bits  |
| Analog-input bandwidth |                                 | –       | 100 | –       | kHz   |
| Sample rate            | XO/8                            | –       | 2.4 | –       | MHz   |
| Offset error           | Relative to full-scale          | –1      | –   | +1      | %     |
| Gain error             | Relative to full-scale          | –1      | –   | +1      | %     |
| INL                    | 15-bit output                   | –8      | –   | +8      | LSB   |
| DNL                    | 15-bit output                   | –4      | –   | +4      | LSB   |

#### Layout suggestion:

- ADC signal trace should be well protected by GND plane
- ADC signal trace should be protected from noise and other radiating signals

## 3. RF Specifications

### 3.1. RF connections

The M18QF/M18QA Series modules have three RF pads; developers must connect them via 50  $\Omega$  traces to the main board.

ANT0\_TRX pad (Pin15) – Primary RX/TX path

ANT1\_DRX pad (Pin21) – Diversity path

ANT\_GNSS pad (Pin9) – GNSS path (For M18QF/M14QF\*)

Notes: \* Due to the 2nd harmonic of B14 impacts GNSS reception performance seriously, embedded GNSS is not recommended to use for M18QA/M14QA.

It is recommended that grounds not be present under the surface of the RF pads in the layout. Details are included below. Layer2 has the same keep out size as Layer1

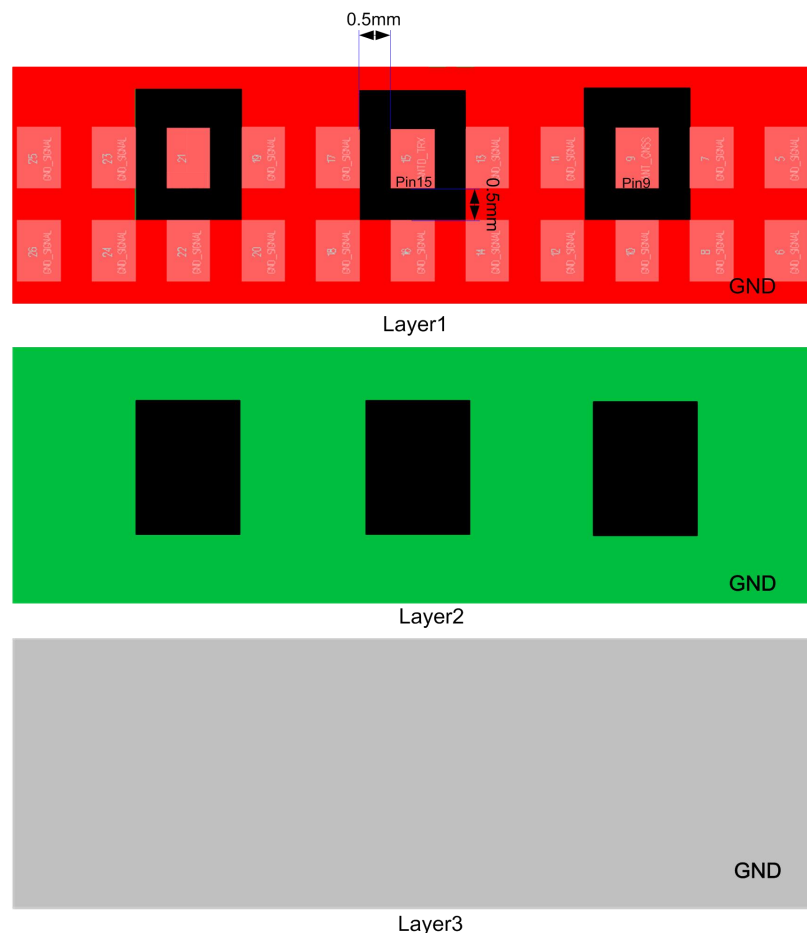


Figure 16. RF pad layout suggestion

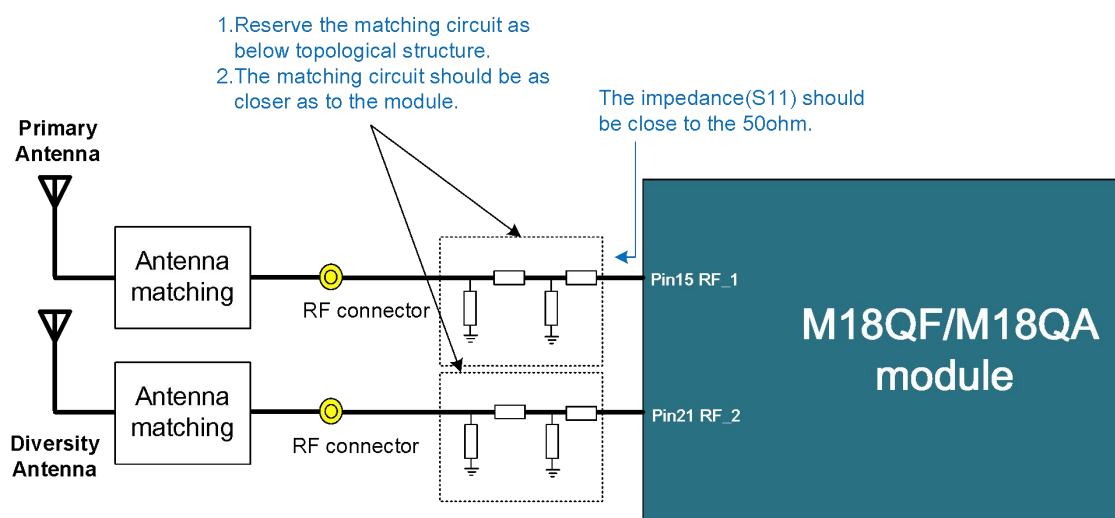


Figure 17. RF matching guide

## 3.2. Interference and sensitivity

This section includes tips to assist developers in identifying the interference that may affect M18QF/M18QA Series modules when used in systems.

### ■ Interference from other wireless devices

- Harmonics, inter-modulated signal generated from wireless devices that fall in RX ranges of the modules, may result in degraded RX performance.
- It is highly recommended to check RX performance of entire systems within the shielding environment.

### ■ Interference from host interface

- High-speed signal-switching elements in systems can easily couple noise into the module (Ex.: DDR memory, LCD modules, DC-DC converter, PCM signal).

### ■ Methods to avoid sources of interference

- Antenna location is important; we recommend directing the antenna

away from high-speed switching signals. Furthermore, the trace from the module to the antenna should be as short as possible and must be shielded by complete grounding.

- The M18QF/M18QA Series modules are well shielded; the high-speed elements (Ex.: DDR memory, LCD modules, DC-DC converter, PCM signal) on a system should have shielding reserved during the early stages of development.
- trace impedance for connection external shall be 50 ohms.
- trace should be kept as short as possible and avoid possible nearby unwanted signal pick up and transmitted by the antenna.
- System integrator should verify if unwanted radiated signal still complies with the relevant rule(s) requirements.



**Caution:** DDR bus, LCD bus, DC-DC switching and PCM signals are easily to influence the WWAN and GNSS receiver performance, these signals must to be routed in the inner layer of the PCB and far away from the WWAN and GNSS receiver path.

### 3.3. GNSS external circuit design

One Notch filter, GNSS SAW filter, LNA, and another GNSS SAW filter need to be used between the module and antenna. Detail design guide as below.

- 1.Minimize GNSS trace length from antenna to Module.
- 2.Maximize overall efficiency in antenna design and maximize isolation Between GNSS and other transmit antennas to limit transmitter Leakage into the GNSS Rx path. The isolation between GNSS and LTE B14 recommend over 20dB.
- 3.Isolate GNSS antenna from jammer sources, digital traces, and power traces, especially SMPS outputs.
- 4.Noisy digital circuits such as the SIM card, USB interface, Camera Module, Display connector, speaker and other audio circuits, and SD/ MMC card should be away from the GNSS antenna.

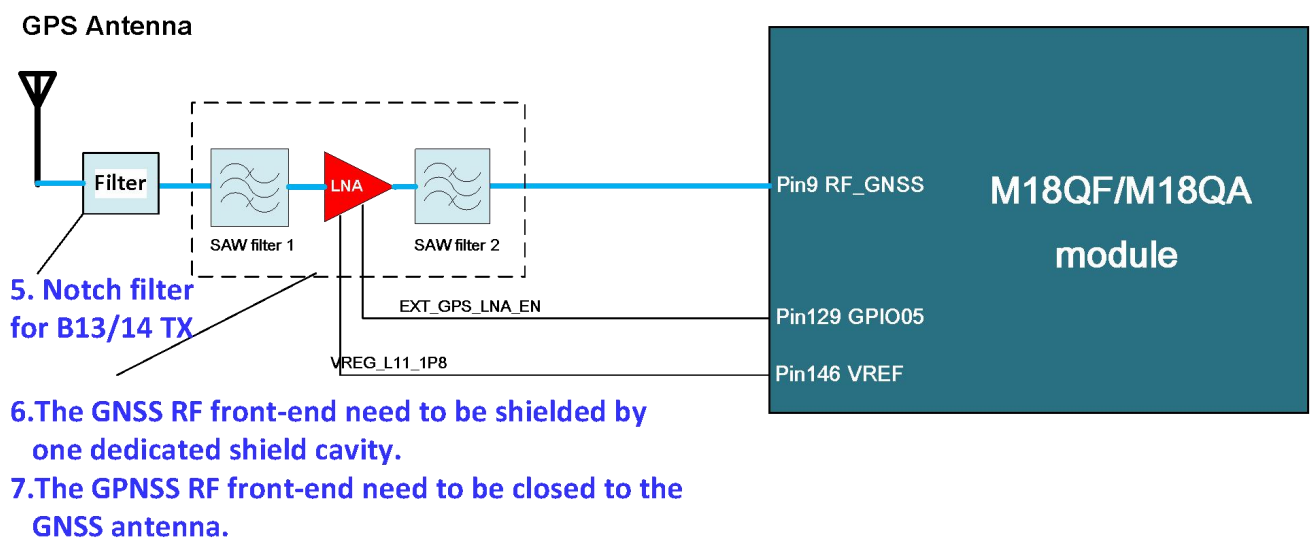


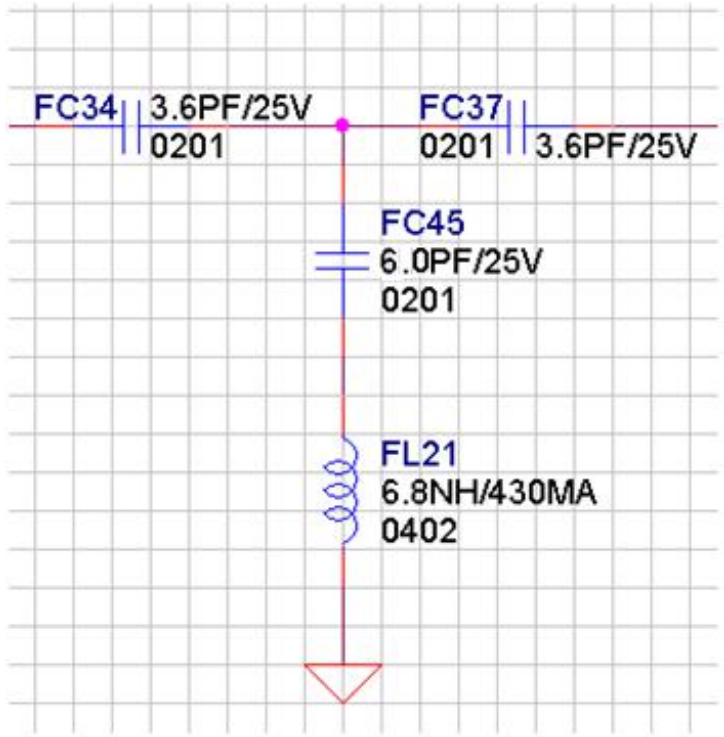
Figure 18. GNSS design suggestion

The following SAW filter and LNA components have been implemented by WNC development board.

- SAW filter1: Murata SAFFB1G56KB0F0AR15
- LNA: INFINEON BGA824N6
- SAW filter2: Murata SAFFB1G56KB0F0AR15

If use module embedded GNSS, please follow above reference design. Pin146 (VREF, 1.8V) of module connects to the external LNA power supply pin. Pin129 (GPIO05) of module connects to external LNA enable control pin.

The Notch filter reference design as below:



3.4. RF Specification

3.5.1 Band support

Table 9. Band support

| Band         | Uplink (MHz) | Downlink (MHz) |
|--------------|--------------|----------------|
| LTE Band 2   | 1,850–1,910  | 1,930–1,990    |
| LTE Band 4   | 1,710–1,755  | 2,110–2,155    |
| LTE Band 5   | 824–849      | 869–894        |
| LTE Band 12  | 699–716      | 729–746        |
| LTE Band 13  | 777–787      | 746–756        |
| LTE Band 14  | 788–798      | 758–768        |
| Band         | Uplink (MHz) | Downlink (MHz) |
| WCDMA Band 2 | 1,850–1910   | 1,930–1,990    |
| WCDMA Band 5 | 824–849      | 869–894        |

### 3.5.2 Bandwidth support

Table 10. Bandwidth support

| Band        | Bandwidth |       |       |        |        |        |
|-------------|-----------|-------|-------|--------|--------|--------|
|             | 1.4 MHz   | 3 MHz | 5 MHz | 10 MHz | 15 MHz | 20 MHz |
| LTE Band 2  | ✓         | ✓     | ✓     | ✓      | ✓      | ✓      |
| LTE Band 4  | ✓         | ✓     | ✓     | ✓      | ✓      | ✓      |
| LTE Band 5  | ✓         | ✓     | ✓     | ✓      | -      | -      |
| LTE Band 12 | ✓         | ✓     | ✓     | ✓      | -      | -      |
| LTE Band 13 | -         | -     | ✓     | ✓      | -      | -      |
| LTE Band 14 | -         | -     | ✓     | ✓      | -      | -      |

### 3.5.3 RF Transmit Specification

Table 11. Conductive Tx output power

| Band         | Items         | Parameter          | Unit | Min. | Typ. | Max. |
|--------------|---------------|--------------------|------|------|------|------|
| LTE Band 2   | Max. TX Power | 10 MHz 12 RBs/QPSK | dBm  | 20.3 | 23   | 25.7 |
| LTE Band 4   | Max. TX Power | 10 MHz 12 RBs/QPSK | dBm  | 20.3 | 23   | 25.7 |
| LTE Band 5   | Max. TX Power | 10 MHz 12 RBs/QPSK | dBm  | 20.3 | 23   | 25.7 |
| LTE Band 12  | Max. TX Power | 10 MHz 12 RBs/QPSK | dBm  | 20.3 | 23   | 25.7 |
| LTE Band 13  | Max. TX Power | 10 MHz 12 RBs/QPSK | dBm  | 20.3 | 23   | 25.7 |
| LTE Band 14  | Max. TX Power | 10 MHz 12 RBs/QPSK | dBm  | 20.3 | 23   | 25.7 |
| Band         | Items         | Parameter          | Unit | Min. | Typ. | Max. |
| WCDMA Band 2 | Max. TX power | -                  | dBm  | 20.3 | 24   | 25.7 |
| WCDMA Band 5 | Max. TX power | -                  | dBm  | 20.3 | 24   | 25.7 |

Note: 1.The RF Transmit Specification is defined at the LGA pad.

2. M18QF/M18QA Series meet 3GPP TS 36.521-1/TS 34.121-1 test standard.

### 3.5.4 RF Receiver Specification

Table 12. Conductive Rx sensitivity-3GPP

| Band       | Items          | Parameter          | Unit | Typ. | 3GPP standard limit |
|------------|----------------|--------------------|------|------|---------------------|
| LTE Band 2 | RX Sensitivity | 10 MHz with 50 RBs | dBm  | -100 | -94.3               |

| <b>LTE Band 4</b>   | RX Sensitivity | 10 MHz with 50 RBs | dBm  | -102 | -96.3  |
|---------------------|----------------|--------------------|------|------|--------|
| <b>LTE Band 5</b>   | RX Sensitivity | 10 MHz with 50 RBs | dBm  | -102 | -94.3  |
| <b>LTE Band 12</b>  | RX Sensitivity | 10 MHz with 50 RBs | dBm  | -103 | -93.3  |
| <b>LTE Band 13</b>  | RX Sensitivity | 10 MHz with 50 RBs | dBm  | -102 | -93.3  |
| <b>LTE Band 14</b>  | RX Sensitivity | 10 MHz with 50 RBs | dBm  | -102 | -93.3  |
| Band                | Items          | Parameter          | Unit | Typ. | Max.   |
| <b>WCDMA Band 2</b> | RX Sensitivity | -                  | dBm  | -110 | -104.7 |
| <b>WCDMA Band 5</b> | RX Sensitivity | -                  | dBm  | -110 | -104.7 |

Note: 1. The RF Receiver Specification is defined at the LGA pad.

2. Meet 3GPP TS 36.521-1/TS 34.121-1 test standard.

Table 13. Conductive Rx sensitivity-CITA

The below table show the sensitivity data of primary only and second only which is defined in the **CITA Test Plan for Wireless Device Over-the-Air Performance V 3.5.2 Table 6-6**. This data could be the reference in the OTA performance evaluation.

| Band | Channel Bandwidth (MHz) | Channel | RX Frequency (MHz) [center of DL RB allocation] | UL RB Allocation      | DL RB Allocation     | Primary only -Typical (dBm) | Second only -Typical (dBm) |
|------|-------------------------|---------|-------------------------------------------------|-----------------------|----------------------|-----------------------------|----------------------------|
| 2    | 10                      | 650     | 1935                                            | 50 RB with RBstart=0  | 50 RB with RBstart=0 | -98.5                       | -98                        |
|      |                         | 900     | 1960                                            | 50 RB with RBstart=0  | 50 RB with RBstart=0 | -99                         | -99                        |
|      |                         | 1150    | 1985                                            | 50 RB with RBstart=0  | 50 RB with RBstart=0 | -98.5                       | -99                        |
| 4    | 10                      | 2000    | 2115                                            | 50 RB with RBstart=0  | 50 RB with RBstart=0 | -98.0                       | -99                        |
|      |                         | 2175    | 2132.5                                          | 50 RB with RBstart=0  | 50 RB with RBstart=0 | -99.0                       | -99                        |
|      |                         | 2350    | 2150                                            | 50 RB with RBstart=0  | 50 RB with RBstart=0 | -98.5                       | -99                        |
| 5    | 10                      | 2450    | 874                                             | 25 RB with RBstart=25 | 50 RB with RBstart=0 | -99                         | -99.5                      |
|      |                         | 2525    | 881.5                                           | 25 RB with RBstart=25 | 50 RB with RBstart=0 | -99.5                       | -100.0                     |

|    |   |      |       |                          |                         |        |        |
|----|---|------|-------|--------------------------|-------------------------|--------|--------|
|    |   | 2600 | 889   | 25 RB with<br>RBstart=25 | 50 RB with<br>RBstart=0 | -99    | -100.5 |
|    |   | 5035 | 731.5 | 20 RB with<br>RBstart=5  | 25 RB with<br>RBstart=0 | -102   | -103   |
| 12 | 5 | 5095 | 737.5 | 20 RB with<br>RBstart=5  | 25 RB with<br>RBstart=0 | -102   | -103   |
|    |   | 5155 | 743.5 | 20 RB with<br>RBstart=5  | 25 RB with<br>RBstart=0 | -102   | -103   |
|    |   | 5205 | 748.5 | 20 RB with<br>RBstart=5  | 25 RB with<br>RBstart=0 | -101   | -102   |
| 13 | 5 | 5230 | 751   | 20 RB with<br>RBstart=5  | 25 RB with<br>RBstart=0 | -100.5 | -102   |
|    |   | 5255 | 753.5 | 20 RB with<br>RBstart=5  | 25 RB with<br>RBstart=0 | -101   | -102   |
|    |   | 5305 | 760.5 | 20 RB with<br>RBstart=5  | 25 RB with<br>RBstart=0 | -101   | -102   |
| 14 | 5 | 5330 | 763   | 20 RB with<br>RBstart=5  | 25 RB with<br>RBstart=0 | -100.5 | -102   |
|    |   | 5355 | 765.5 | 20 RB with<br>RBstart=5  | 25 RB with<br>RBstart=0 | -101   | -102   |

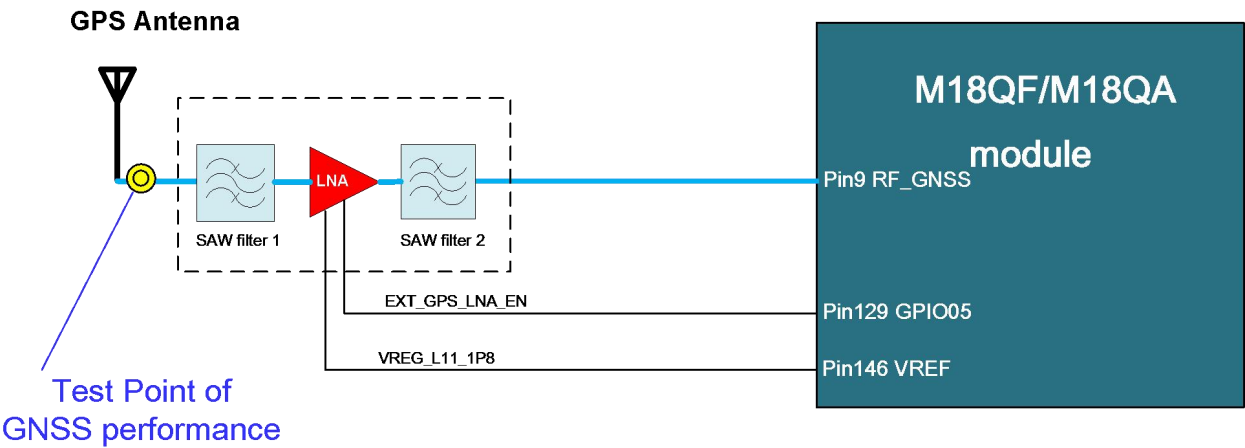
Note: 1. The RF typical data is defined at the LGA pad.

### 3.5.5 GNSS Receiver Specification

Table 14. GNSS receiver performance

| Test items                            | Parameter                                       | Min. | Typ.    | Max. |
|---------------------------------------|-------------------------------------------------|------|---------|------|
| <b>Cold start TTFF</b>                | (@-130dBm)                                      | -    | 38S     | -    |
| <b>Hot start TTFF</b>                 | (@-130dBm)                                      | -    | 2S      | -    |
| <b>CEP-50 Accuracy</b>                | Open sky with -130 dBm<br>input                 | -    | <3m     | -    |
| <b>Cold start sensitivity</b>         | Acquire First with Signal level                 | -    | -146dBm | -    |
| <b>Tracking sensitivity(GPS)</b>      | Detect an in-view satellite<br>50% of the time. | -    | -162dBm | -    |
| <b>Tracking sensitivity (Glonass)</b> | Detect an in-view satellite<br>50% of the time. | -    | -162dBm | -    |

Note1: The test point shows as below.



## 4. Power

### 4.1. Power consumption

This section describes typical power consumption of M18QF/M18QA Series for reference. The current data is measured at 3.8V VCC.

Table 15. LTE power consumption

| Working Mode                     | Conditions                                                                                                                            | Result |
|----------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|--------|
| <b>Airplane mode</b>             |                                                                                                                                       |        |
|                                  | Only Module, no other device                                                                                                          | 1.50mA |
| <b>LTE standby(DRX=1.28 sec)</b> |                                                                                                                                       |        |
|                                  | Band2 –LTE Standby mode, DRX = 1.28 sec, BW=10MHz                                                                                     | 2.24mA |
|                                  | Band4 –LTE Standby mode, DRX = 1.28 sec, BW=10MHz                                                                                     | 2.17mA |
|                                  | Band5 –LTE Standby mode, DRX = 1.28 sec, BW=10MHz                                                                                     | 2.20mA |
|                                  | Band12 –LTE Standby mode, DRX = 1.28 sec, BW=10MHz                                                                                    | 2.14mA |
|                                  | Band13 –LTE Standby mode, DRX = 1.28 sec, BW=10MHz                                                                                    | 2.17mA |
|                                  | Band14 –LTE Standby mode, DRX = 1.28 sec, BW=10MHz                                                                                    | 2.13mA |
| <b>LTE Band2 Working mode</b>    |                                                                                                                                       |        |
|                                  | Bandwidth 20MHz,TM3–DLRB 100–ULRB 100– IPV4-UDP ,<br>TX Power=23dbm,Downlink throughput is 145Mbps via<br>USB interface by Iperf tool | 714mA  |
| <b>LTE Band4 Working mode</b>    |                                                                                                                                       |        |
|                                  | Bandwidth 20MHz,TM3–DLRB 100–ULRB 100–IPV4-UDP ,<br>TX Power=23dbm,Downlink throughput is 145Mbps via<br>USB interface by Iperf tool  | 749mA  |
| <b>LTE Band5 Working mode</b>    |                                                                                                                                       |        |
|                                  | Bandwidth 10MHz,TM3–DLRB 50–ULRB 50– IPV4-UDP,<br>TX Power=23dbm,Downlink throughput is 72Mbps via USB<br>interface by Iperf tool     | 595mA  |
| <b>LTE Band12 Working mode</b>   |                                                                                                                                       |        |
|                                  | Bandwidth 10MHz,TM3–DLRB 50–ULRB 50–IPV4-UDP ,<br>TX Power=23dbm,Downlink throughput is 72Mbps via USB                                | 633mA  |

|                                    |                                                                                                                                   |               |
|------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------|---------------|
| interface by Iperf tool            |                                                                                                                                   |               |
| <b>LTE Band13 Working mode</b>     |                                                                                                                                   |               |
|                                    | Bandwidth 10MHz,TM3–DLRB 50–ULRB 50–IPV4-UDP ,<br>TX Power=23dbm,Downlink throughput is 72Mbps via USB<br>interface by Iperf tool | 593mA         |
| <b>LTE Band14 Working mode</b>     |                                                                                                                                   |               |
|                                    | Bandwidth 10MHz,TM3–DLRB 50–ULRB 50–IPV4-UDP ,<br>TX Power=23dbm,Downlink throughput is 72Mbps via USB<br>interface by Iperf tool | 583mA         |
| <b>WCDMA standby(DRX=1.28 sec)</b> |                                                                                                                                   |               |
|                                    | Band2 –WCDMA Standby mode, DRX = 1.28 sec                                                                                         | 1.94mA        |
|                                    | Band5 –WCDMA Standby mode, DRX = 1.28 sec                                                                                         | 1.95mA        |
| <b>WCDMA Band2 Working mode</b>    |                                                                                                                                   |               |
|                                    | HSPA+ downlink 21 Mbps ,TX Power=23dbm                                                                                            | 438mA         |
| <b>WCDMA Band5 Working mode</b>    |                                                                                                                                   |               |
|                                    | HSPA+ downlink 21 Mbps ,TX Power=23dbm                                                                                            | 386mA         |
| <b>Powering on</b>                 | <b>Conditions</b>                                                                                                                 | <b>Result</b> |
| <b>Peak power consumption</b>      |                                                                                                                                   |               |
|                                    | Power consumption peak when the module is powering up                                                                             | 550mA         |
| <b>Power off</b>                   | <b>Conditions</b>                                                                                                                 | <b>Result</b> |
| <b>Power off consumption</b>       |                                                                                                                                   |               |
|                                    | Module is powered off                                                                                                             | 8uA           |

Note: 1. USB is disabled when testing airplane mode and standby mode.

## 5. Software Interface

### 5.1. Support tools

The M18QF/M18QA Series modules are compatible with the following support tools:

- WNC M18QF/M18QA Series Connection Manager (WNCCM)

### 5.2. USB interface

The M18QF/M18QA Series modules support 3GPP standard AT commands and proprietary AT commands; the MAL Manager SDK is also supported for Linux platforms. Refer to [WNC M18QF/M18QA Series] WNC MAL Manager Developer Guide for more information.

## 6. Mechanical and Environmental Certifications

### 6.1. PCBA Form Factor

M18QF/M18QA Series modules have the same dimensions:

31.32 mm (typ.) × 23.5 mm (typ.) × 2.3 mm (typ.)

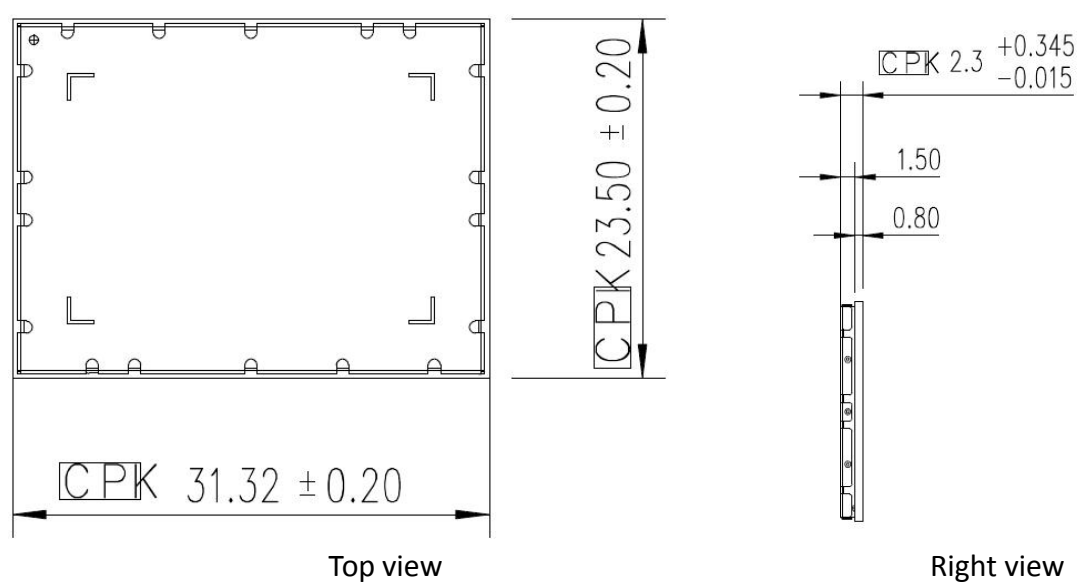


Figure 19. PCBA dimension

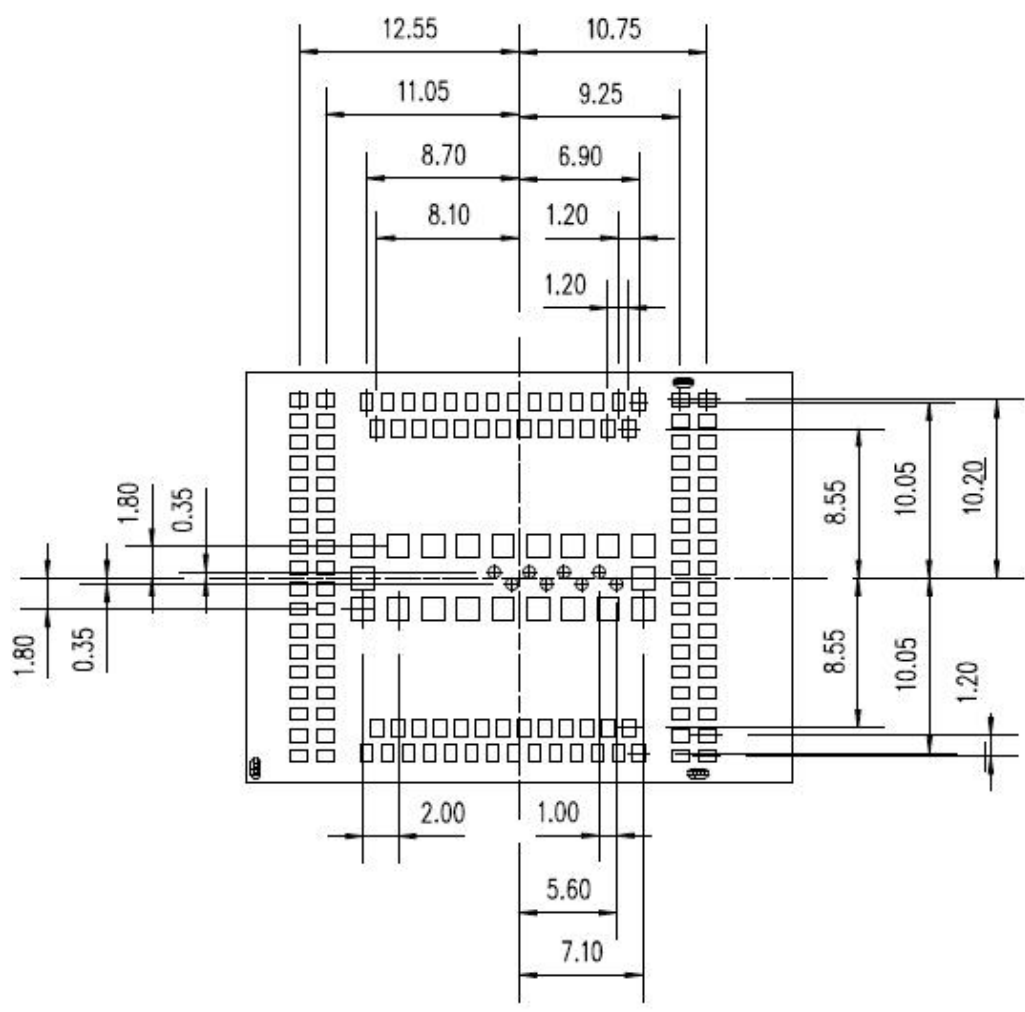
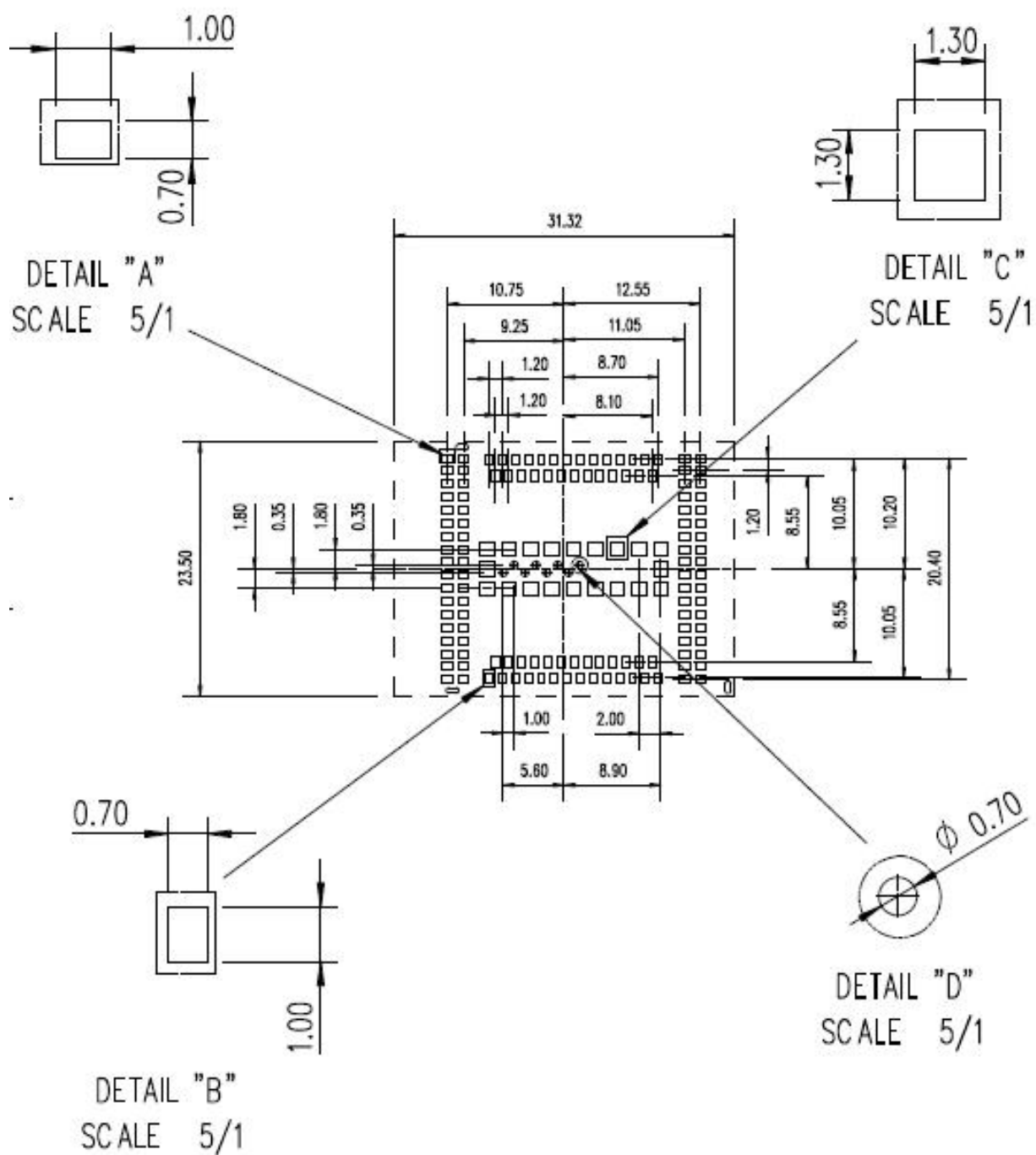


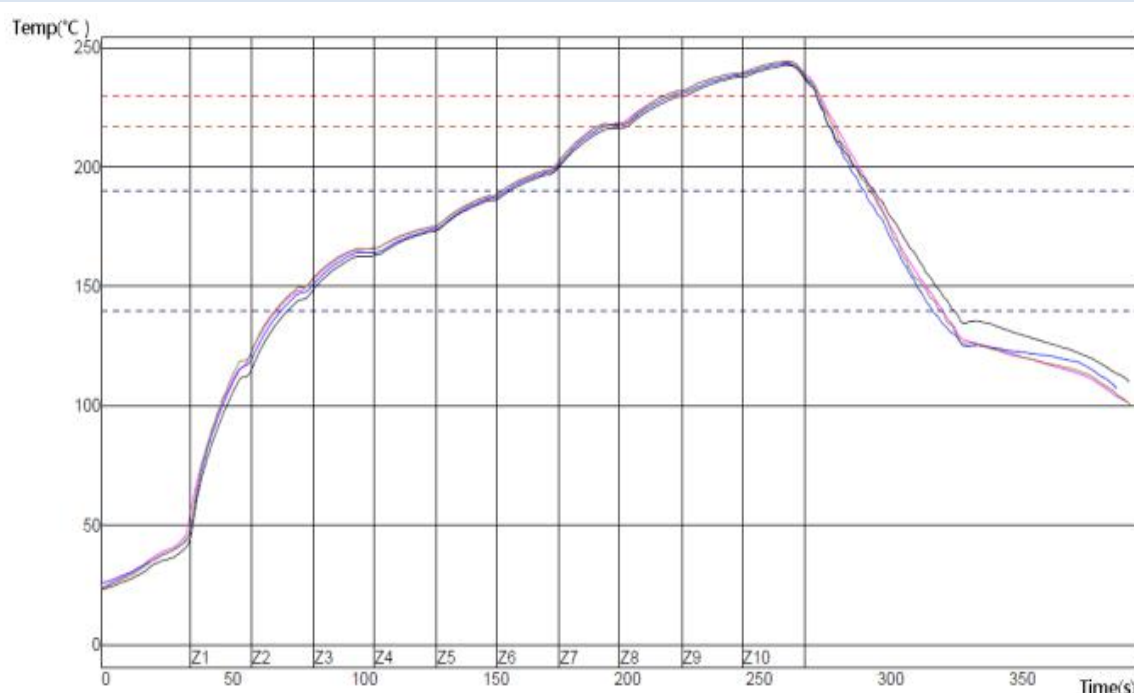
Figure 20. Pad dimension(Bottom view)



## 6.2. Reflow

This section details the recommended reflow profile when the module is mounted onto other boards.

| Temp. Region        | 1            | 2   | 3   | 4   | 5   | 6   | 7   | 8   | 9   | 10  |
|---------------------|--------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Upper temp. region  | 150          | 165 | 175 | 180 | 195 | 205 | 230 | 235 | 250 | 245 |
| Lower temp. region  | 150          | 165 | 175 | 180 | 195 | 205 | 230 | 235 | 250 | 245 |
| Conveyor band speed | 95 cm/minute |     |     |     |     |     |     |     |     |     |



| PWI = 91%              |  D31-1 |  D31-2 |  D31-3 |  D31-4 | Temp.<br>Difference |
|------------------------|-------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------|---------------------|
| Preheat from 140–190°C |                                                                                           |                                                                                           |                                                                                           |                                                                                             |                     |
| 85.34                  | 85.30                                                                                     | 86.06                                                                                     | 84.29                                                                                     | 1.77                                                                                        |                     |
| –12%                   | –13%                                                                                      | –8%                                                                                       | –18%                                                                                      |                                                                                             |                     |
| Melt-out Time/230°C    |                                                                                           |                                                                                           |                                                                                           |                                                                                             |                     |
| 59.07                  | 55.03                                                                                     | 58.70                                                                                     | 49.70                                                                                     | 9.37                                                                                        |                     |
| 91%                    | 50%                                                                                       | 87%                                                                                       | –3%                                                                                       |                                                                                             |                     |
| Max Temp               |                                                                                           |                                                                                           |                                                                                           |                                                                                             |                     |
| 244.27                 | 243.56                                                                                    | 244.33                                                                                    | 242.71                                                                                    | 1.62                                                                                        |                     |
| 43%                    | 36%                                                                                       | 43%                                                                                       | 27%                                                                                       |                                                                                             |                     |

|                              |       |       |       |       |
|------------------------------|-------|-------|-------|-------|
| <b>Total Time/217°C</b>      |       |       |       |       |
| 90.55                        | 85.88 | 90.09 | 76.90 | 13.65 |
| 22%                          | 4%    | 20%   | -32%  |       |
| <b>Gradient1 (100–150°C)</b> |       |       |       |       |
| 1.91                         | 1.83  | 1.93  | 1.78  | 0.15  |
| 27%                          | 22%   | 29%   | 19%   |       |

Process limit:

| <b>Solder Paste</b>                                                            | <b>Lead-free</b> |      |      |
|--------------------------------------------------------------------------------|------------------|------|------|
| Profile feature                                                                | Min.             | Max. | Unit |
| <b>Gradient1 (Target = 1.5) (100 °C–150 °C)</b><br><b>(Time period = 20 s)</b> | 0                | 3    | °C/S |
| <b>Preheat time from 140 °C to 190 °C</b>                                      | 70               | 105  | S    |
| <b>Time maintained above 230 °C</b>                                            | 40               | 60   | S    |
| <b>Peak package body temperature</b>                                           | 230              | 250  | °C   |
| <b>Time maintained above 217 °C</b>                                            | 60               | 110  | S    |

### 6.3. PCB pad design

Non solder mask defined (NSMD) type is recommended for the solder pads of the PCB on which M18QF/M18QA Series modules will be mounted, this kind of design is good to soldering reliability in SMT process.

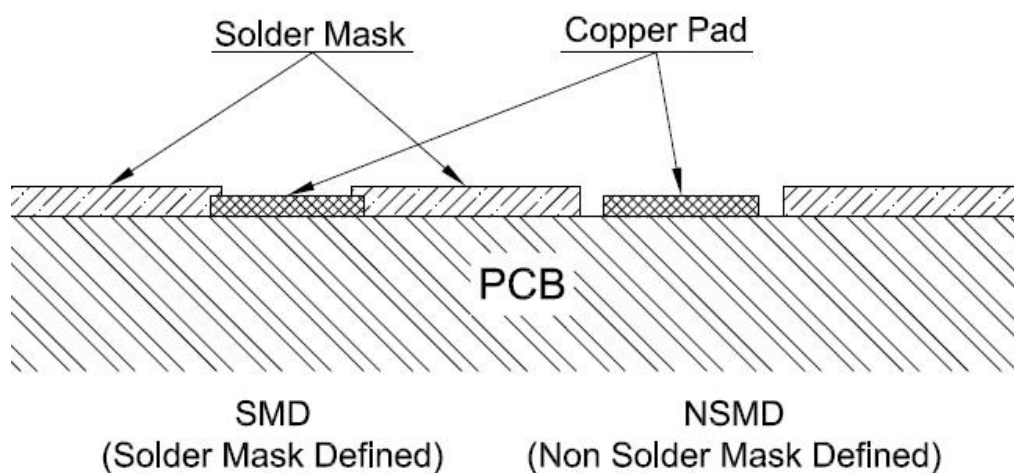
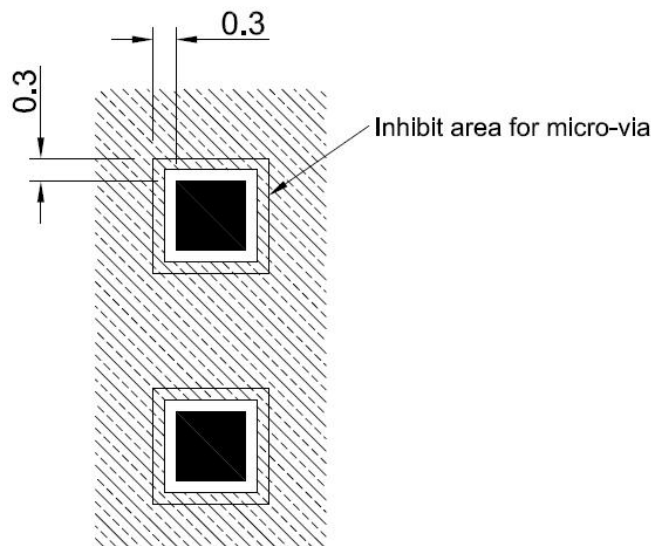


Figure 22. NSMD solder pad design

It is not recommended to place via or micro-via not covered by solder resist in an area of 0.3 mm around the pads unless it carries the same signal of the pad itself, see following figure.



Holes in pad are allowed only for blind holes and not for through holes.

6.4. Labeling

Figure26 shows label drawing of M18QF/M18QA Series modules.





Figure 23. Label drawing

## 6.5. SMT Voids control

### 6.5.1. Mother board PCB thickness

Thin mother board is prone to warping during SMT reflow, which creates voids when the module is soldered. Therefore, the thickness of the mother board needs to be larger than 1.2 mm, and the larger the size of the mother board, the larger the thickness. For example, 1.4mm, 1.6mm.

### 6.5.2. Stencil design

The thickness of the stencil is at least 0.15 mm, and the thickness of the stencil need to be increased depending on the actual situation. For example, there is open soldering still.

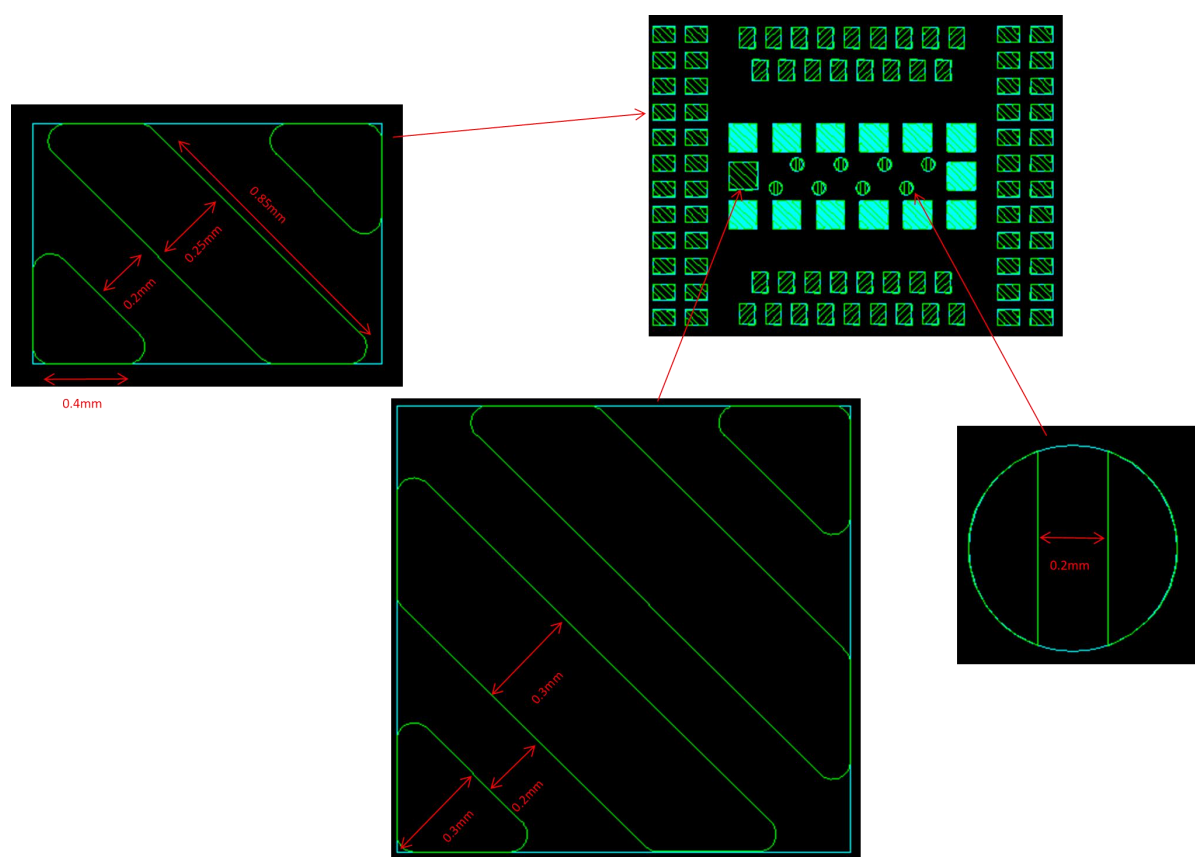


Figure 24. Stencil-foil drawing

## 6.6. Thermal considerations

| Grade      | Operating     | 3GPP compliant | Functional work | Storage        |
|------------|---------------|----------------|-----------------|----------------|
| Industrial | -40 °C~+85 °C | -20 °C~+60 °C  | -40 °C~+85 °C   | -40 °C ~+85 °C |

Note: The temperature above refers to ambient temperature.

The case temperature of module shielding cover must be < 85 °C when integrated to prevent damage.

Design points used to improve the thermal performance:

- It's better to add a naked copper area onto M18QF/M18QA Series modules' back side of the PCB. If the thermal performance becomes an issue in the customer's product, add thermal solutions for improvement such as a thermal pad or a heat sink.
- It's recommended to have a thermal pad or a heat sink on shielding cover to help

transfer heat.

- If systems with M18QF/M18QA Series modules embedded intend to work under ambient temperatures as low as -40°C, it's suggested that:
  1. SIM Card need to be well arranged to make sure it is functional at the condition of ambient temperature as low as -40°C.
  2. Adding heating circuit on board design, the circuit mainly consists of temperature sensing unit, heating element and control unit.

## 7. Regulatory Compliance and Certification

### 7.1. Certification testing

PTCRB, GCF, FCC, IC, AT&T TA and Verizon TA

8. Packaging

8.1. Tape-and-Reel Package

The M18QF/M18QA Series modules are delivered in tape and reel.

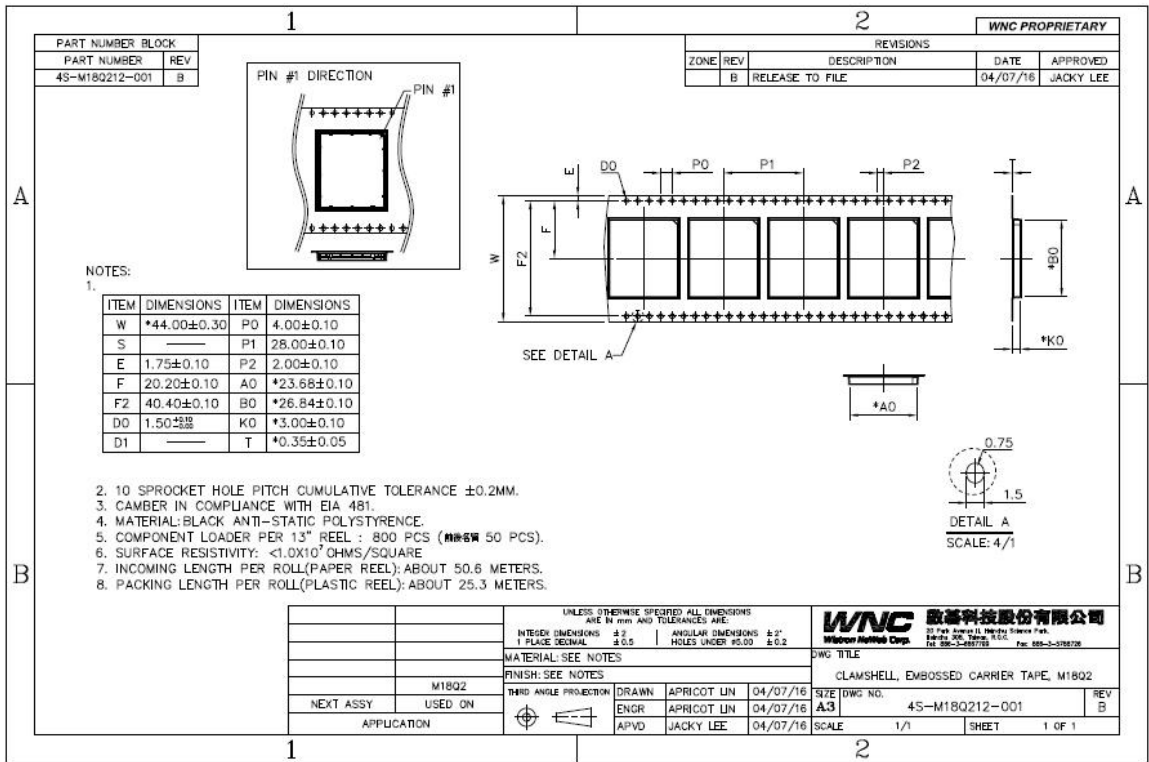


Figure 25. Packing--tape

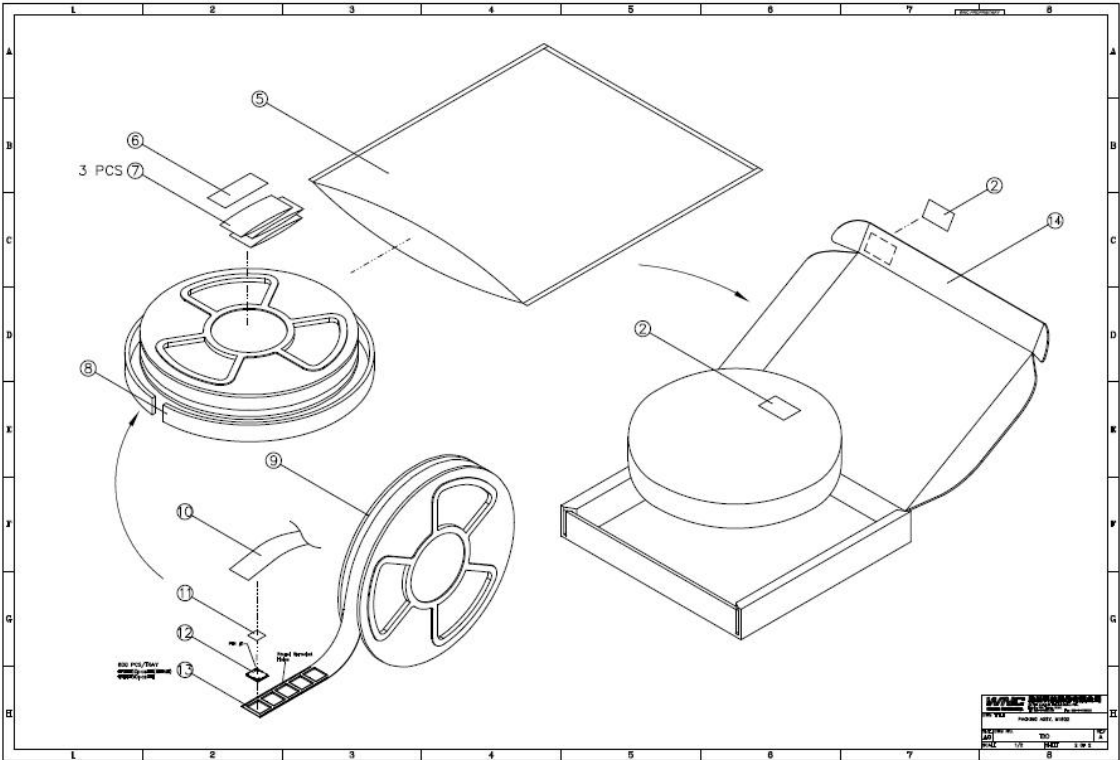


Figure 26. Packing—reel

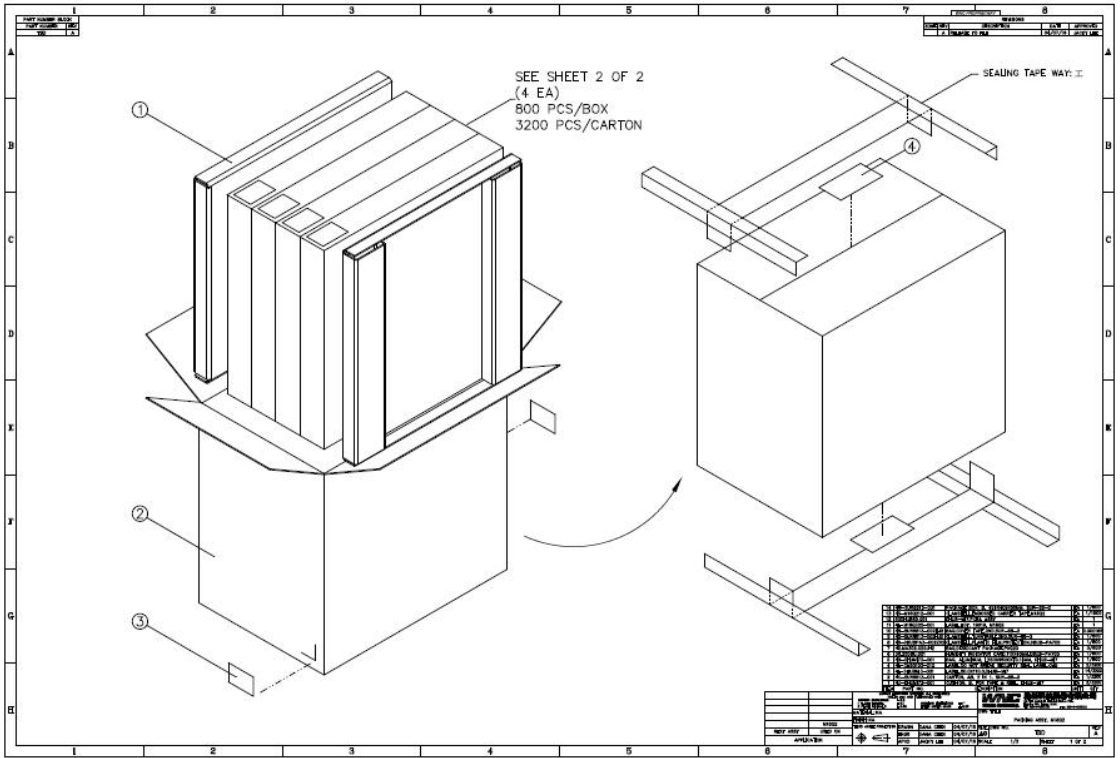
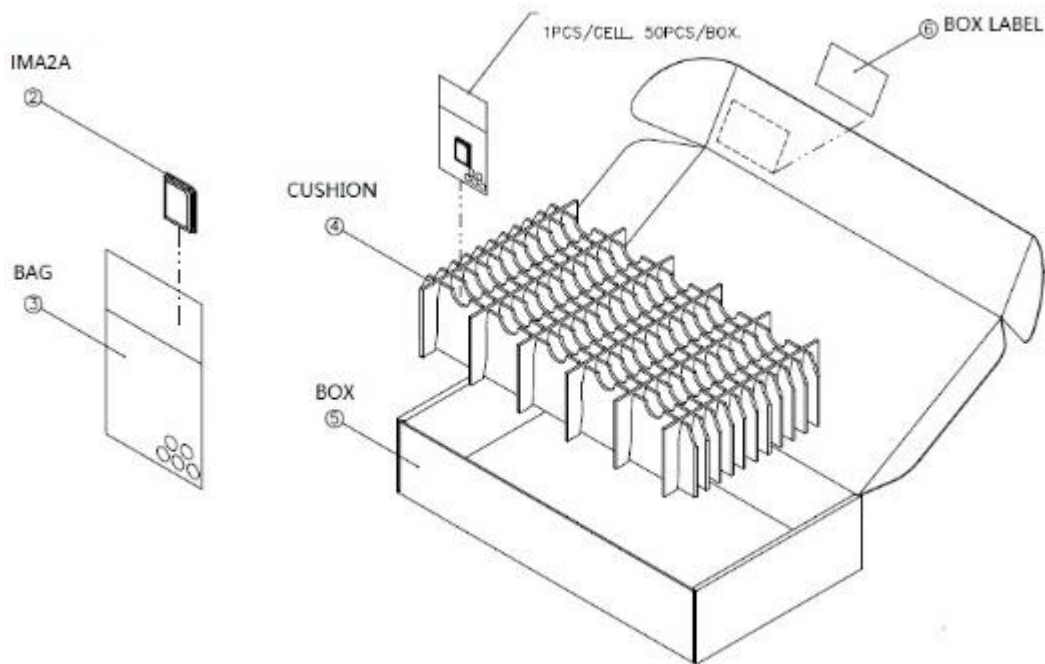


Figure 27. Packing—carton

## 8.2. Single Packaging for Samples

Samples are packaged at 50 pcs. /box. There is no vacuum packaging. Samples must be baked for 8 hours at least at 85 °C before SMT.



## 8.3. MSL level

The module MSL level is 3.

## 9. Safety Recommendation

Be sure the use of this product is allowed in the country and in the environment required.

The use of this product may be dangerous and must be avoided in the following areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, and aircraft
- Where there is a risk of explosion such as gasoline stations and oil refineries

It is the responsibility of the user to comply with his or her country's regulations and the specific environmental regulations.

Do not disassemble the product; any mark of tampering will compromise the warranty's validity.

We recommend following the instructions of the hardware user guides for a correct wiring of the product. The product must be supplied with a stabilized voltage source, and the wiring must conform to the security and fire-prevention regulations.

This product must be handled with care; avoid any contact with the pins because electrostatic discharge may damage the product. Same caution must be taken regarding the UIM card; carefully check the instructions for its use. Do not insert or remove the UIM when the product is in power-saving mode.

The system integrator is responsible of the functioning of the final product; therefore, care must be taken for the external components of the module as well as for project or installation issues—there may be a risk of disturbing the GSM network or external devices or of having an impact on device security. If you have any doubts, please refer to the technical documentation and the relevant regulations in force.

Every module must be equipped with a proper antenna with specific characteristics. The antenna must be installed with care in order to avoid any interference with other electronic devices.

### **Federal Communication Commission Interference Statement**

This device complies with Part 15 of the FCC Rules. Operation is subject to the

following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

**Radiation Exposure Statement:**

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

**This module is intended for OEM integrators only. Per FCC KDB 996369 D03 OEM Manual v01 guidance, the following conditions must be strictly followed when using this certified module:**

**KDB 996369 D03 OEM Manual v01 rule sections:****2.2 List of applicable FCC rules**

This module has been tested for compliance to FCC Part 15, 22, 24, 27, 90

**2.3 Summarize the specific operational use conditions**

The module is tested for standalone mobile RF exposure use condition. Any other usage conditions such as co-location with other transmitter(s) or being used in a portable condition will need a separate reassessment through a class II permissive change application or new certification.

**2.4 Limited module procedures**

Not applicable.

**2.5 Trace antenna designs**

Not applicable.

**2.6 RF exposure considerations**

This equipment complies with FCC mobile radiation exposure limits set forth for

an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20cm between the radiator & your body. If the module is installed in a portable host, a separate SAR evaluation is required to confirm compliance with relevant FCC portable RF exposure rules.

## 2.7 Antennas

The following antennas have been certified for use with this module; antennas of the same type with equal or lower gain may also be used with this module. The antenna must be installed such that 20 cm can be maintained between the antenna and users.

| For GPS            |                    |        |              |                                |                                |                  |                    |
|--------------------|--------------------|--------|--------------|--------------------------------|--------------------------------|------------------|--------------------|
| Antenn<br>a<br>No. | Brand              |        | Model        | Antenna Ne<br>t<br>Gain (dBi)  | Frequency<br>Range<br>(MHz)    | Antenna<br>Type  | Connector<br>Type  |
| GPS                | Master             |        | 98619ZSAX029 | 2.24                           | 1559~1606                      | Dipole           | SMA                |
| For WWAN           |                    |        |              |                                |                                |                  |                    |
| Antenn<br>a<br>No. | RF<br>Chain<br>No. | Brand  | Model        | Antenna Net<br>Gain (dBi)      | Frequency<br>Range (MHz)       | Antenn<br>a Type | Connecto<br>r Type |
| 1                  | Main               | Wieson | GY115        | Please refer to<br>below table | Please refer to<br>below table | Dipole           | SMA                |
| 2                  | Aux                | Wieson | GY115        | Please refer to<br>below table | Please refer to<br>below table | Dipole           | SMA                |

| Antenna gain list |                   |              |             |
|-------------------|-------------------|--------------|-------------|
| Band              | Freq. Range (MHz) | Gain (dBi)   |             |
|                   |                   | Ant 1 (Main) | Ant 2 (Aux) |
| WCDMA II (B2)     | 1850~1910         | 1.56         | 1.56        |

|               |           |      |      |
|---------------|-----------|------|------|
| WCDMA V (B5)  | 824~849   | 3.2  | 3.2  |
| LTE Band (2)  | 1850~1910 | 1.56 | 1.56 |
| LTE Band (4)  | 1710~1755 | 1.62 | 1.62 |
| LTE Band (5)  | 824~849   | 3.2  | 3.2  |
| LTE Band (12) | 698~716   | 1.49 | 1.49 |
| LTE Band (13) | 777~787   | 1.66 | 1.66 |
| LTE Band (14) | 788~798   | 1.60 | 1.60 |

## 2.8 Label and compliance information

The final end product must be labeled in a visible area with the following: "Contains FCC ID: **NKRM18QF**". The grantee's FCC ID can be used only when all FCC compliance requirements are met.

## 2.9 Information on test modes and additional testing requirements

This transmitter is tested in a standalone mobile RF exposure condition and any co-located or simultaneous transmission with other transmitter(s) or portable use will require a separate class II permissive change re-evaluation or new certification.

## 2.10 Additional testing, Part 15 Subpart B disclaimer

This transmitter module is tested as a subsystem and its certification does not cover the FCC Part 15 Subpart B (unintentional radiator) rule requirement applicable to the final host. The final host will still need to be reassessed for compliance to this portion of rule requirements if applicable.

As long as all conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

**IMPORTANT NOTE:** In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the FCC

authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

### **Manual Information To the End User**

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as show in this manual.

### **OEM/Host manufacturer responsibilities**

OEM/Host manufacturers are ultimately responsible for the compliance of the Host and Module. The final product must be reassessed against all the essential requirements of the FCC rule such as FCC Part 15 Subpart B before it can be placed on the US market. This includes reassessing the transmitter module for compliance with the Radio and EMF essential requirements of the FCC rules. This module must not be incorporated into any other device or system without retesting for compliance as multi-radio and combined equipment.

### **Industry Canada statement:**

This device complies with ISED's licence-exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Le présent appareil est conforme aux CNR d' ISED applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) le dispositif ne doit pas produire de brouillage préjudiciable, et (2) ce dispositif doit accepter tout brouillage reçu, y compris un brouillage susceptible de provoquer un fonctionnement

indésirable.

**Radiation Exposure Statement:**

This equipment complies with ISED radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with greater than 20cm between the radiator & your body.

**Déclaration d'exposition aux radiations:**

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé à plus de 20 cm entre le radiateur et votre corps.

**This device is intended only for OEM integrators under the following conditions: (For module device use)**

- 1) The antenna must be installed and operated with greater than 20cm between the antenna and users, and
- 2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as **2** conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

**Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)**

- 1) L'antenne doit être installée et exploitée avec plus de 20 cm entre l'antenne et les utilisateurs, et
- 2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les **2** conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

**IMPORTANT NOTE:**

In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the Canada authorization is no longer considered valid and the IC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

**NOTE IMPORTANTE:**

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

**End Product Labeling**

This transmitter module is authorized only for use in device where the antenna may be installed and operated with greater than 20cm between the antenna and users. The final end product must be labeled in a visible area with the following: "Contains IC: **4441A-M18QF**".

**Plaque signalétique du produit final**

Ce module émetteur est autorisé uniquement pour une utilisation dans un appareil où l'antenne peut être installée et utilisée à plus de 20 cm entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: **4441A-M18QF**".

**Manual Information To the End User**

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as show in this manual.

#### Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.

Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

This radio transmitter (IC: **4441A-M18QF** / Model: **M18QF**、**M18QA**、**M14QF**、**M14QA**) has been approved by ISED to operate with the antenna type listed below with maximum permissible gain indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Le présent émetteur radio (IC: **4441A-M18QF** / Model: **M18QF**、**M18QA**、**M14QF**、**M14QA**) a été approuvé par ISED pour fonctionner avec les types d'antenne énumérés ci-dessous et ayant un gain admissible maximal. Les types d'antenne non inclus dans cette liste, et dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

| For GPS            |                    |        |              |                                |                                |                  |                    |
|--------------------|--------------------|--------|--------------|--------------------------------|--------------------------------|------------------|--------------------|
| Antenn<br>a<br>No. | Brand              |        | Model        | Antenna Ne<br>t<br>Gain (dBi)  | Frequency<br>Range<br>(MHz)    | Antenna<br>Type  | Connector<br>Type  |
| GPS                | Master             |        | 98619ZSAX029 | 2.24                           | 1559~1606                      | Dipole           | SMA                |
| For WWAN           |                    |        |              |                                |                                |                  |                    |
| Antenn<br>a<br>No. | RF<br>Chain<br>No. | Brand  | Model        | Antenna Net<br>Gain (dBi)      | Frequency<br>Range (MHz)       | Antenn<br>a Type | Connecto<br>r Type |
| 1                  | Main               | Wieson | GY115        | Please refer to<br>below table | Please refer to<br>below table | Dipole           | SMA                |
| 2                  | Aux                | Wieson | GY115        | Please refer to<br>below table | Please refer to<br>below table | Dipole           | SMA                |

Antenna gain list

| Band          | Freq. Range<br>(MHz) | Gain (dBi)      |                |
|---------------|----------------------|-----------------|----------------|
|               |                      | Ant 1<br>(Main) | Ant 2<br>(Aux) |
| WCDMA II (B2) | 1850~1910            | 1.56            | 1.56           |
| WCDMA V (B5)  | 824~849              | 3.2             | 3.2            |
| LTE Band (2)  | 1850~1910            | 1.56            | 1.56           |
| LTE Band (4)  | 1710~1755            | 1.62            | 1.62           |
| LTE Band (5)  | 824~849              | 3.2             | 3.2            |
| LTE Band (12) | 698~716              | 1.49            | 1.49           |
| LTE Band (13) | 777~787              | 1.66            | 1.66           |
| LTE Band (14) | 788~798              | 1.60            | 1.60           |