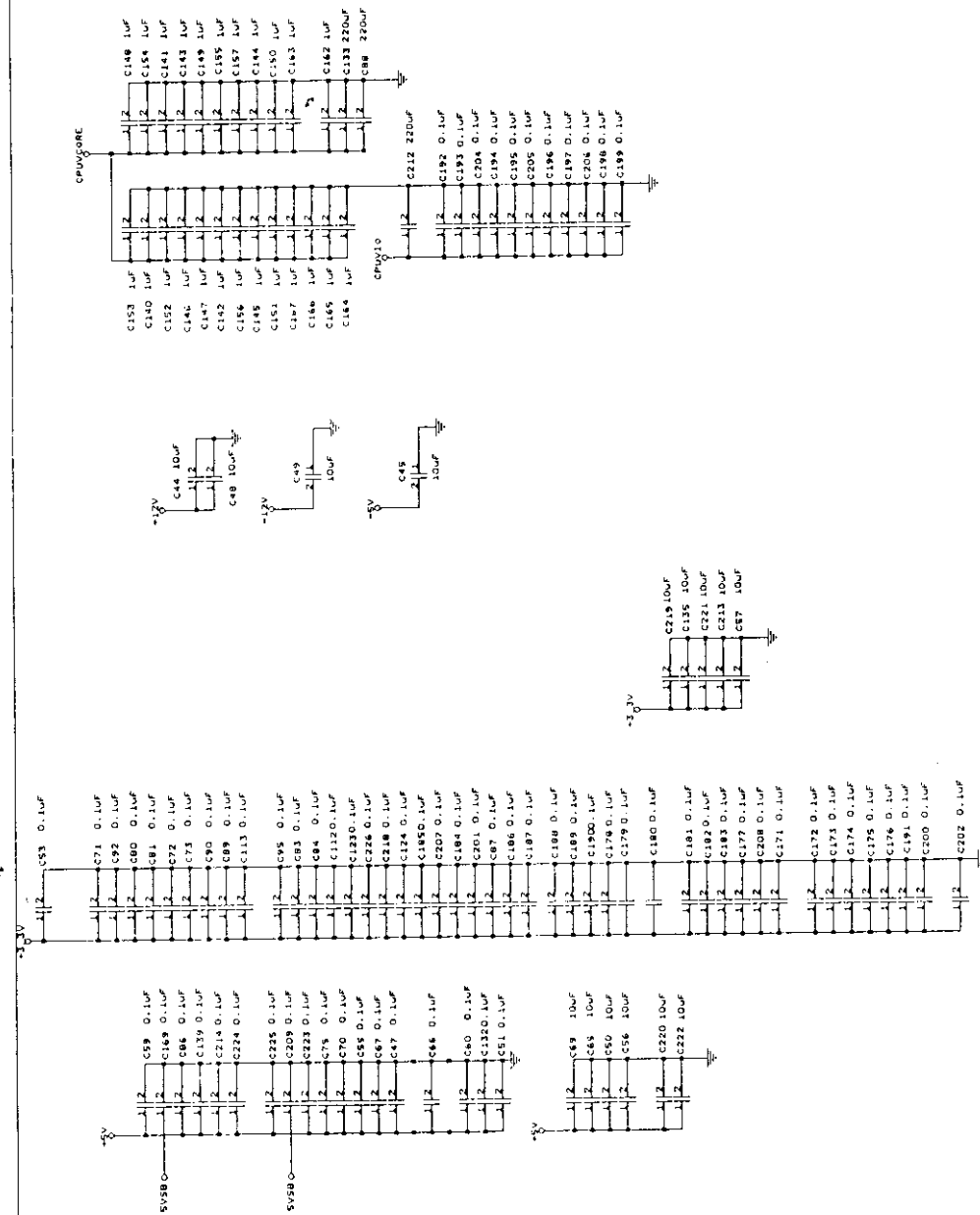
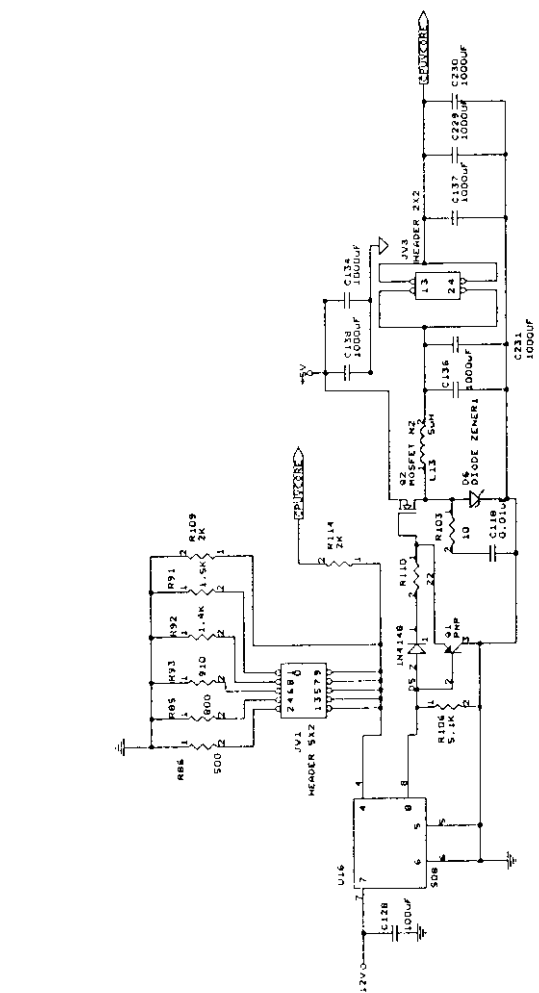
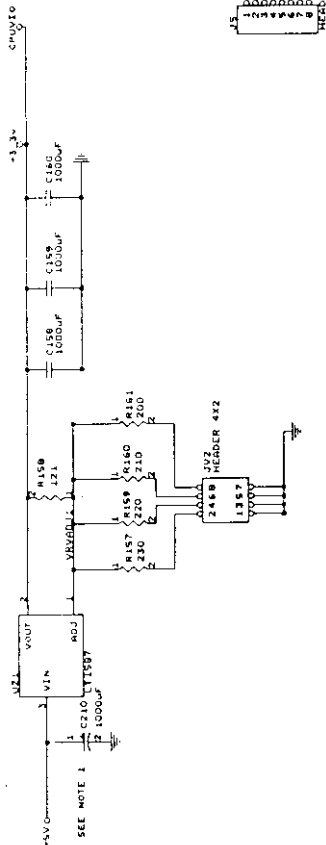
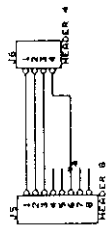
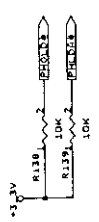
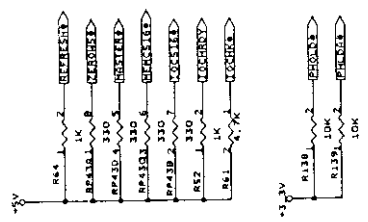
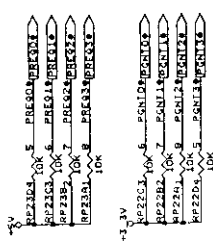
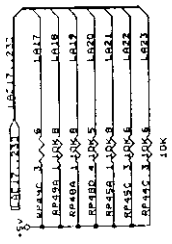
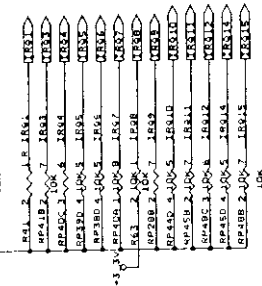
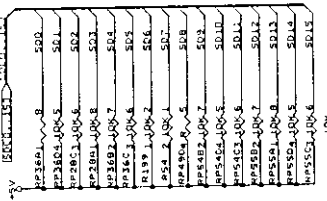
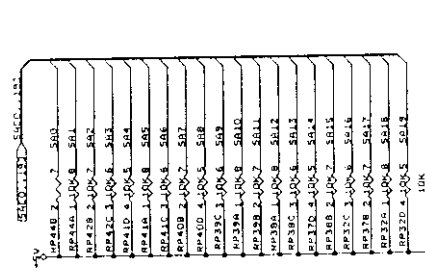
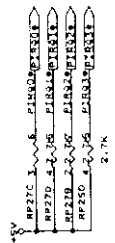






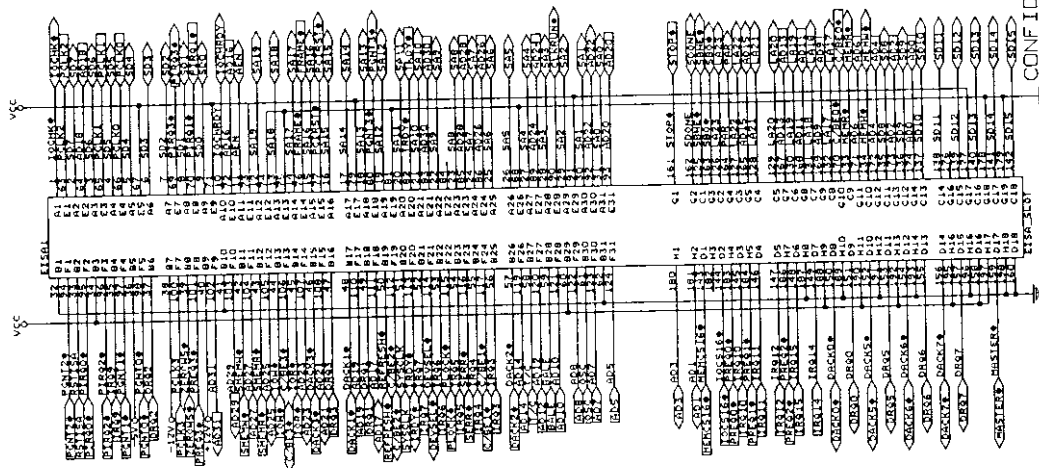
Heatstons are implemented as corner traces on inter layer:
 For 102, corner:
 Note 1: trace widths are 50 mils, 1.24" long.
 Note 2: trace widths are 50 mils, 0.82" long.





DO NOT REPRODUCE

ISA SLOTS 3&4



INTEL SECRET
CONFIDENTIAL INFORMATION

130

Platform : ATX

P54C,P55C,6X86,K5

SIMM : SOCKET 2 X 72 Pins

SIMM : 5V - EDO,FPM DRAM

CACHE : ON BOARD 256K/512K PBSRAM/M-CACHE

BIOS : 5V,12V FLASH ROM,2 Mbits FLASH ROM

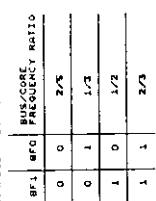
USB : 2

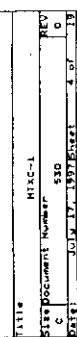
IO : SMC 37C672

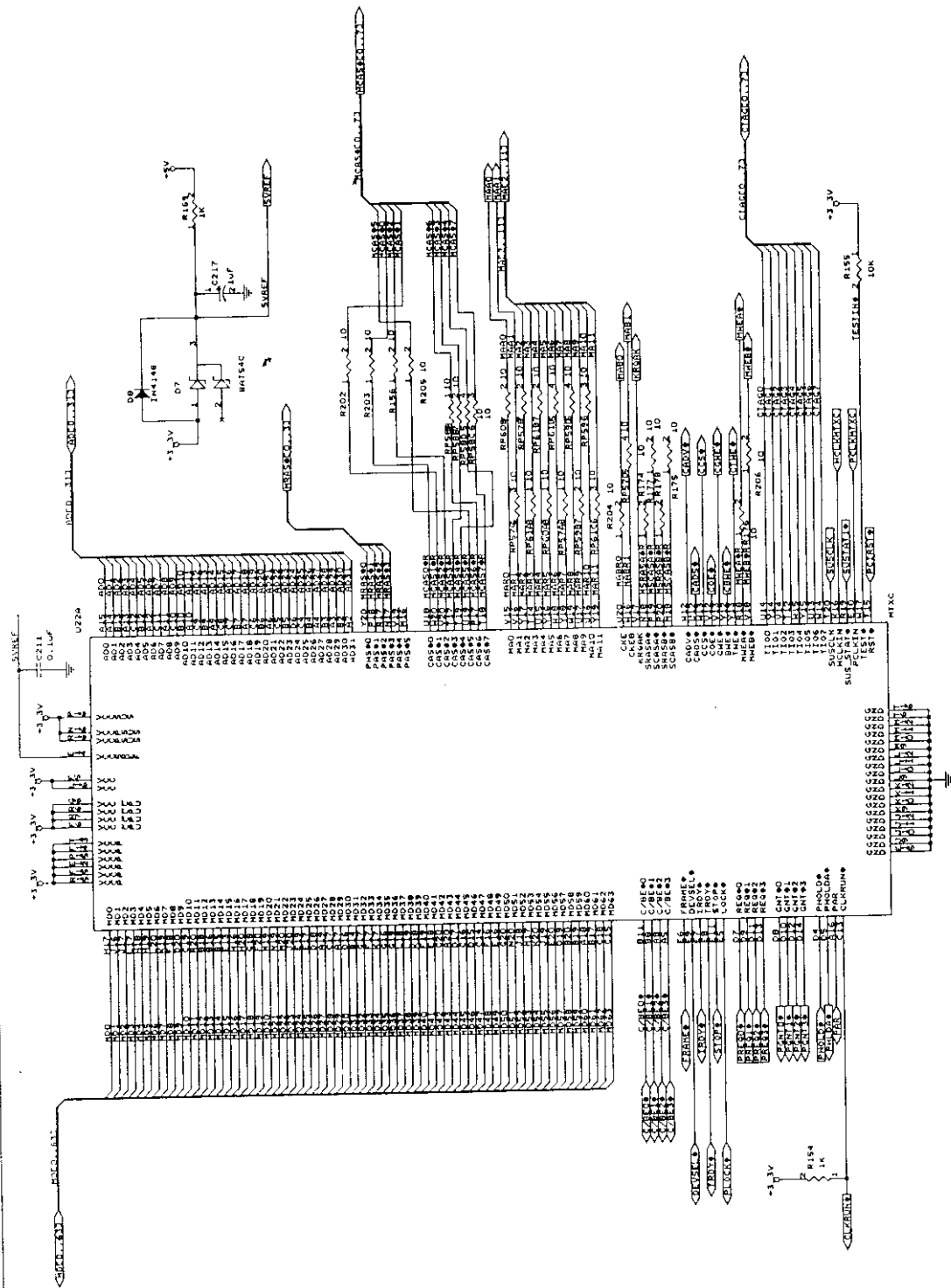
ULTRA DMA 33 IDE PORT X 2

ILINK
IP54C.SCH
ISYCLK.SCH
IMTXC_A.SCH
IMTXC_B.SCH
ICACHE.SCH
ISIMM.SCH
PIIX4_A.SCH
PIIX4_B.SCH
IDE&USB.SCH
ISUPER_IO.SCH
ICOM_PORT.SCH
IBIOS.SCH
IPOWER.SCH
IVOLT_REG.SCH
IDECOUP.SCH
IPULLUP.SCH
IRTC_KBC.SCH
IT2_ISA16.SCH

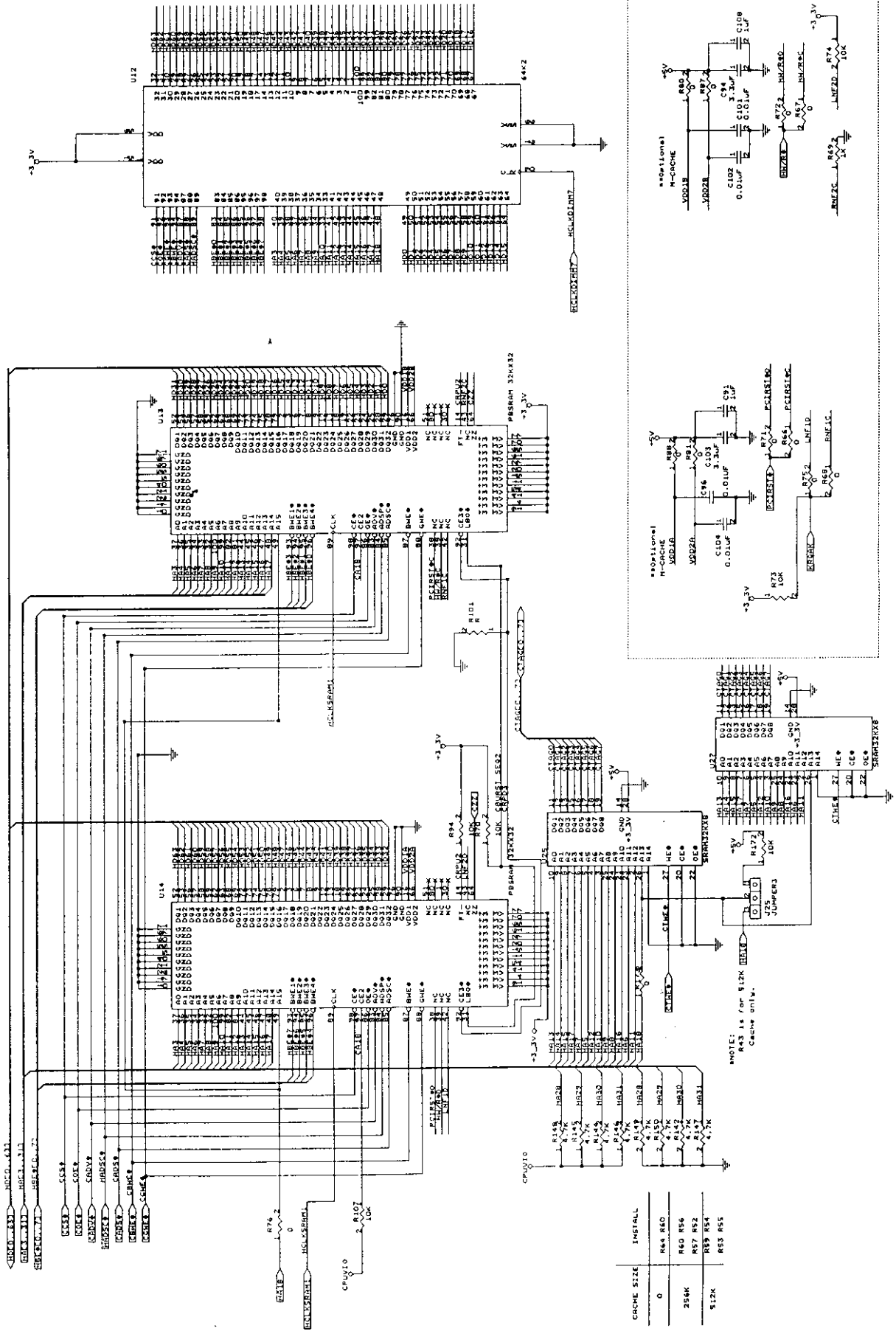
FILE		INDEX	
Star Document Number		REV	
C	1	0	0
Date		Date	
June 25, 1997		June 25, 1997	



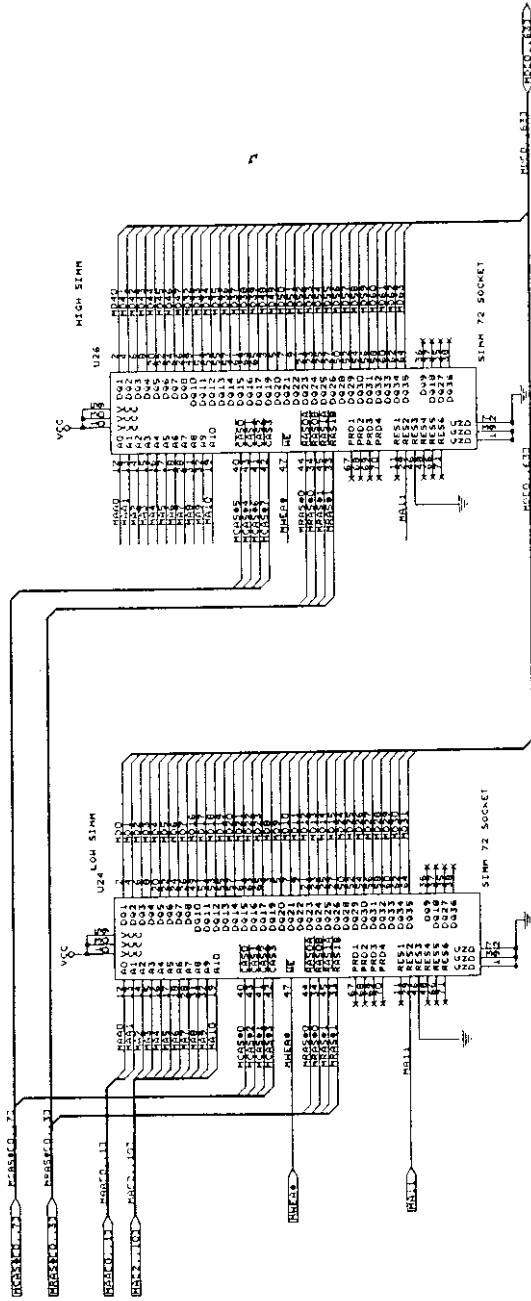




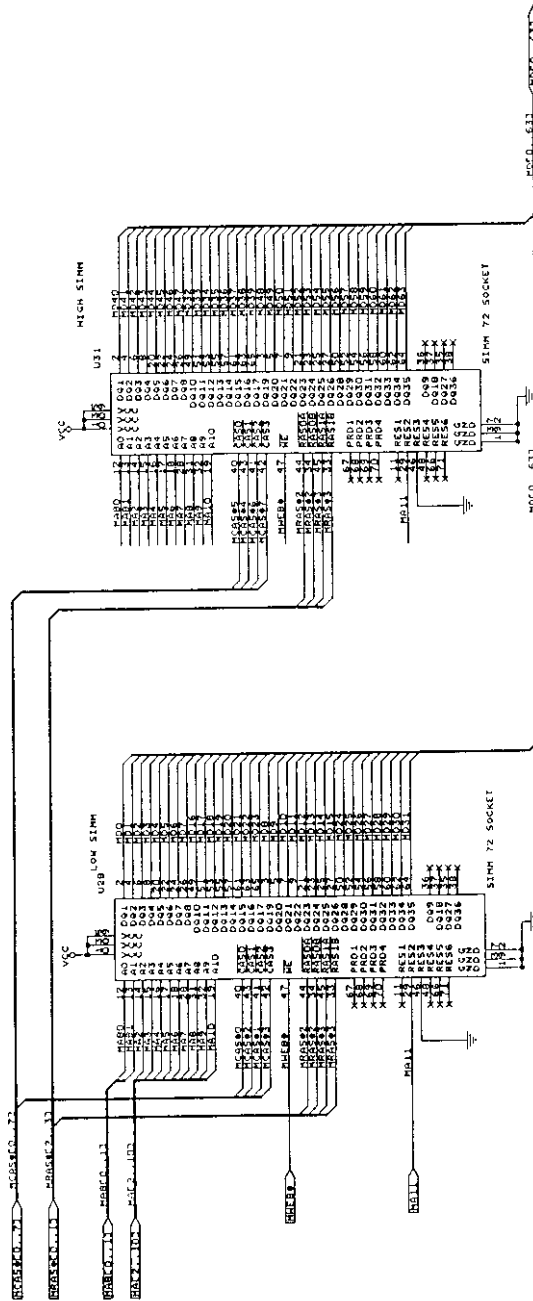
NOTE: PIN 16, 39, 42, 43 & 46 ARE NOCONNECTS FOR PM SRAM

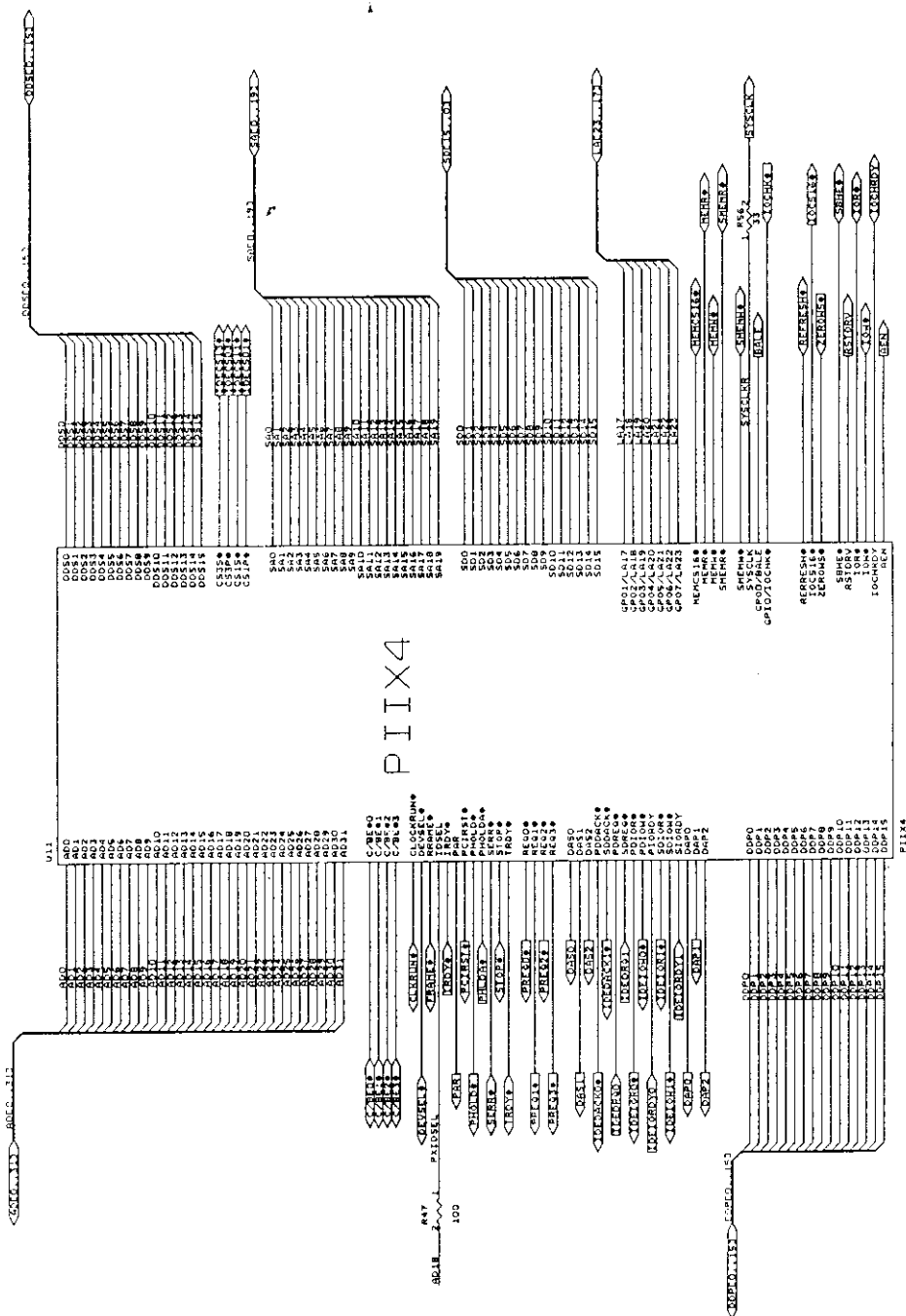


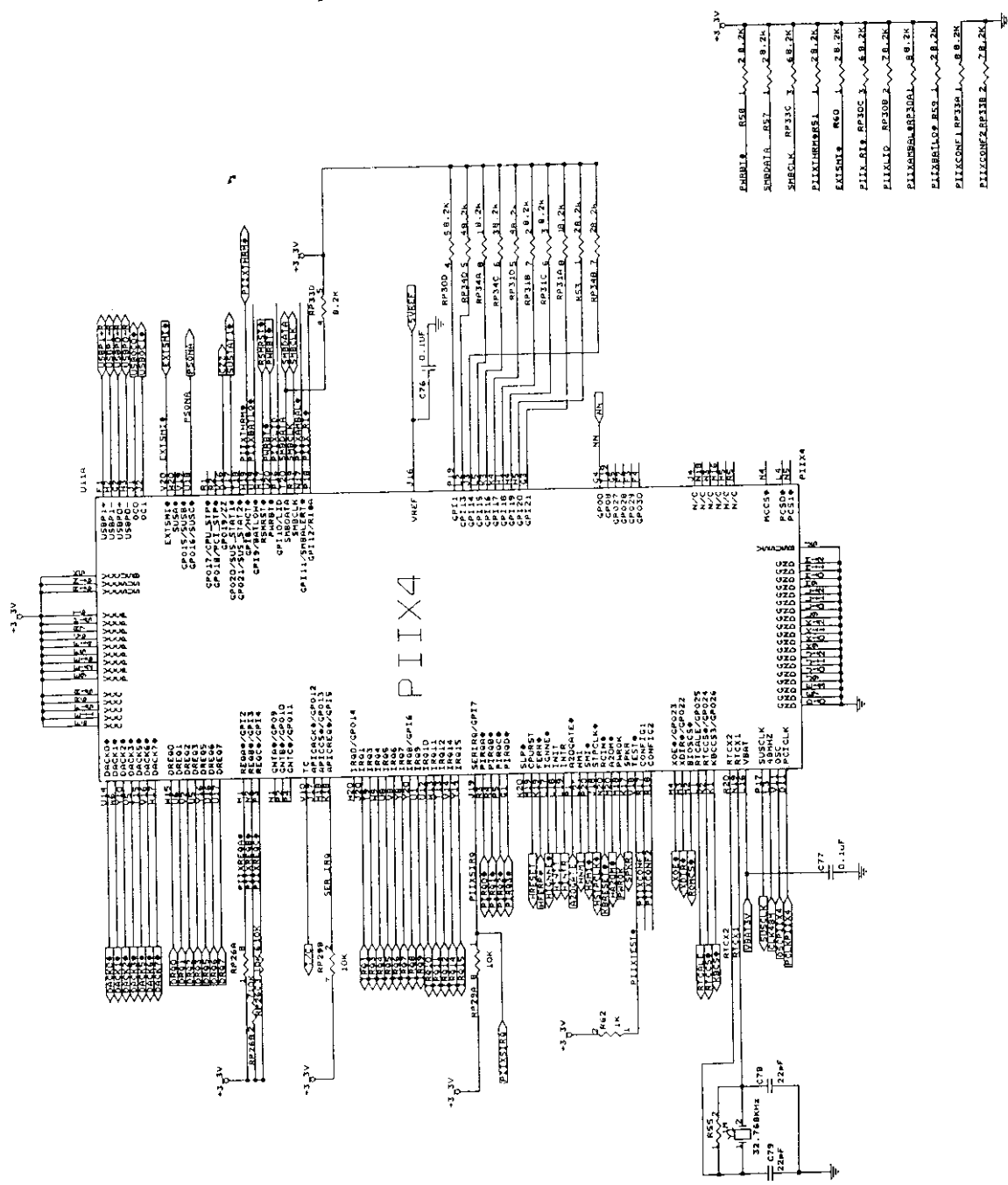
SIMM BANK 0

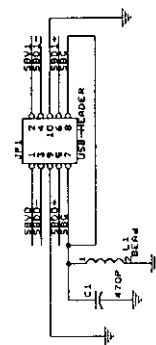
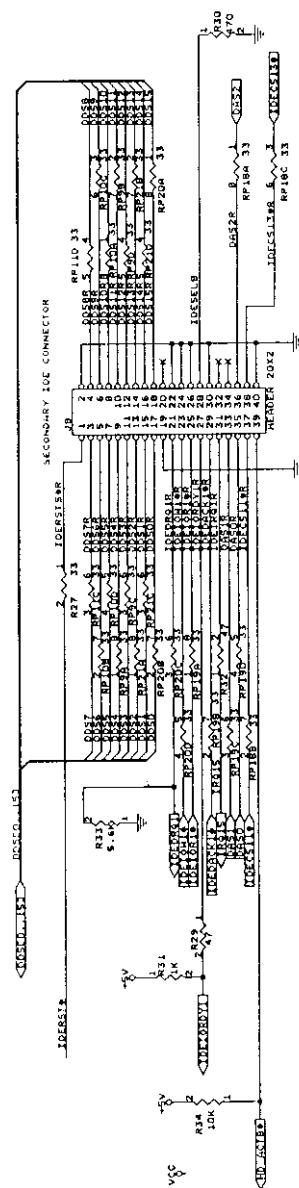
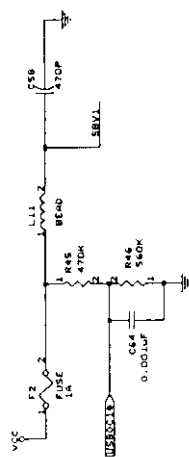
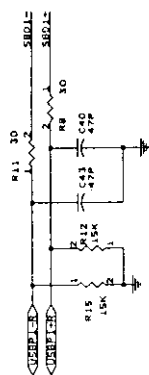
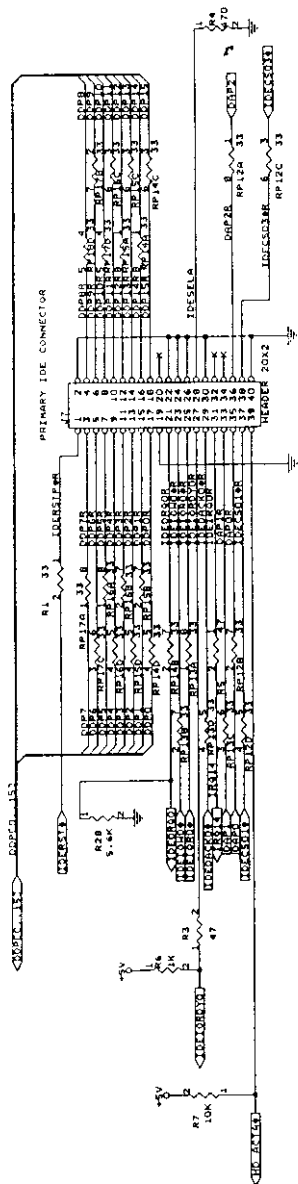


SIMM BANK 1

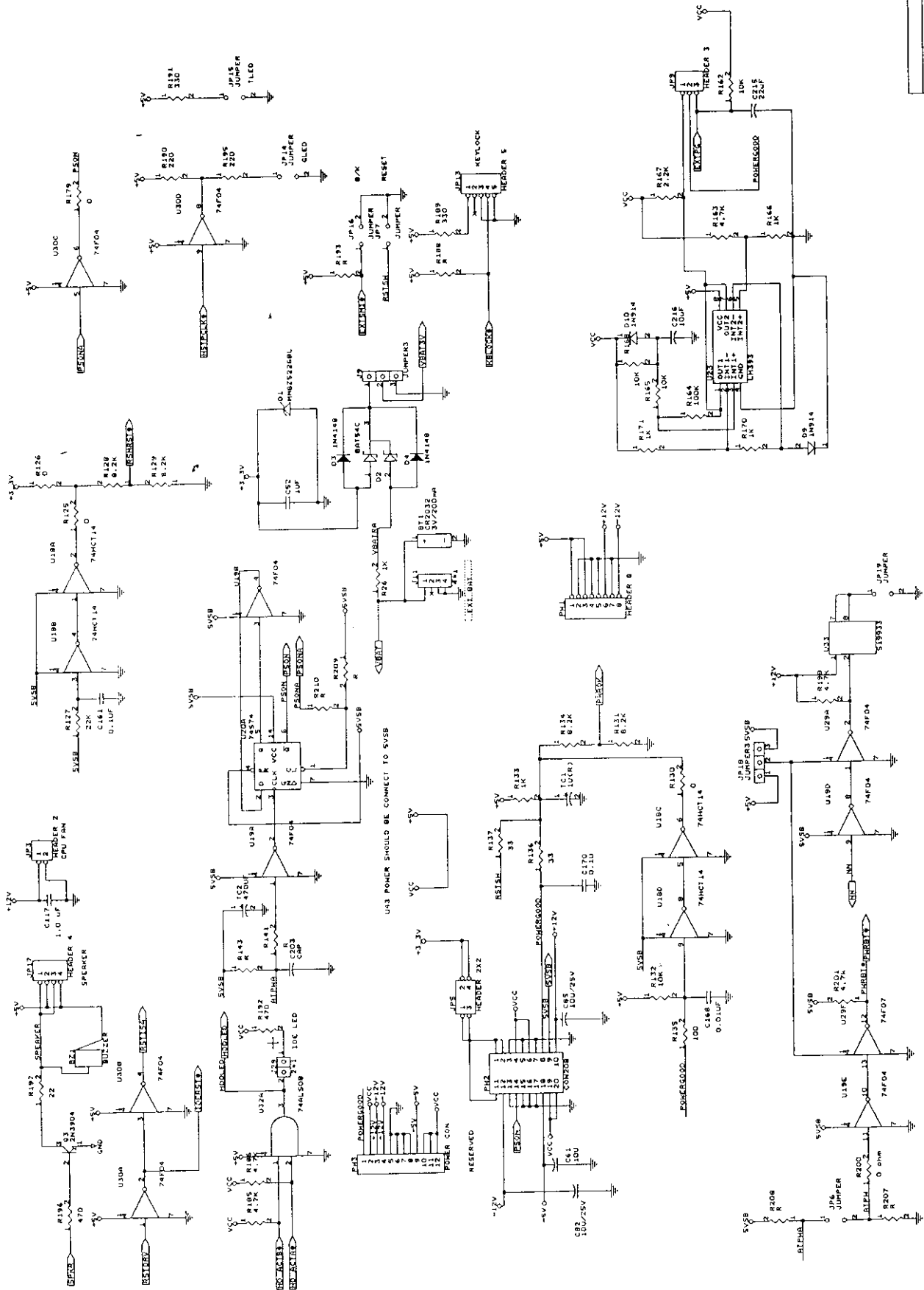






[illegible]

USB CONNECTOR



U43 POWER SHOULD BE CONNECT TO 5V5B

FILE	POWER
Sheet/Document Number	530
REV	0
DATE	2018-03-13
BY	14-07-18

