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Subject: GW-900T Circuit Description for FCC Approval

The GW900T transmitter circuit consists of three main functional areas: the user interface, the controller, and the RF section.

User Interface.

Meter data is read using a 3-wire interface on connector JP1. The clock required to interface the data is double-buffered by hex-inverter, U4. The switching regulator U5 provides the proper voltage to U4 and allows the processor to power-down the user interface during intervals when no data is scheduled for transmission. Transistor Q1 is used on some interface configurations to buffer voltage pulses from "generated" type meters.

Controller.

The control processor, U2, reads the data from the user interface and formats the data for transmission. The control processor sends the transmit data packet to the RF section via the Tx_Data signal line. The frequency hopping algorithm is implemented in the control processor, which controls a direct digital synthesizer in the RF Section to select the current hop frequency. The processor also controls the power wake-up and power shutdown timing of the transmitter. Crystal Y1 is the processor clock and determines the transmit data rate. Switch S1 is used during installation to initiate a test sequence. Connector location J1 is used during manufacture to program the device. Connectors J2 and J3 were used during development but are unused in the manufactured device. Integrated Circuits U1 and U7 are unused in the manufactured device.

RF Section.

The RF section consists of a FSK exciter, a power amplifier, the battery, and an integrated antenna. The FSK exciter, U3, accepts frequency control data and transmit data from the controller to generate a modulated signal between 902 and 928 MHz. The exciter uses an integral direct digital synthesizer (DDS) to generate an internal intermediate frequency which is multiplied by an integral fixed ratio phase-lock loop (PLL) to generate the final frequency. Components C13, C15, R11, and R13 comprise the external loop filter for the PLL. C3, L1, C9 and D2 form the resonator of the PLL's voltage controlled oscillator. The modulation is digitally induced via a frequency deviation register in the DDS. Crystal Y2 provides the reference for the DDS. The power amplifier, U6, amplifies the 5 milliwatt, 900 MHz output of U3 to 250 milliwatts. The keying of the power amplifier is controlled directly from the control processor. The output filter section consists of inductors L4, L7, L14 and capacitors C19, C21, C28, C29.

The output of the output filter induces RF currents on the battery case to form the radiating element of the antenna. Inductor L6 blocks RF currents from entering the DC power that is supplied from the battery to the integrated circuits. Capacitor C26 is an energy storage device that maintains proper voltage levels during transmissions.