

## WorldGate Communications

## Block Diagram Description

There are ten (10) major components in the SM2200: Microprocessor; Serial Interface; VBI Decoder; Audio/Video Processor; Dynamic Memory Controller; Program Memory; Audio/Video Selector; Dynamic Memory; and, Master Clock.

The Microprocessor, or CPU, is the principal component of the SM2200, providing the processing power to transform the set-top converter into an Internet terminal. The Serial Interface and Printer Interface provide the electrical interconnections respectively to the set-top converter's internal processor. The Program Memory stores the CPU instructions and data constants necessary for proper operation.

The Dynamic Memory (DRAM) serves two purposes: temporary, or variable, data for program operations; and audio and video data to be output to the external television receiver. All access to and from DRAM are managed by the Dynamic Memory Controller which schedules CPU access around the constant demand for audio and video data.

Audio and Video data from the DRAM are processed by the Audio/Video Processor. The audio is converted to a Pulse Width Modulation signal and routed to an integrator to produce analog audio signals. The video data is filtered and encoded and routed to a digital to analog converter to produce an analog composite video signal.

The VBI Decoder extracts digital data embedded in the video during the vertical blanking interval, and converts the data to a form readable by the CPU. The incoming video is routed, with audio, to the Audio/Video Selector which selects the source (television or Internet) signal to be output by the set-top converter (both, base-band and modulated RF).

The Master Clock is the source of all timing signals in the SM2200. The clock crystal controlled oscillator operating at a frequency eight (8) times the burst frequency of the desired video standard (NTSC, PAL/B/G/I, PAL/M, or PAL/Nc)

**WORLDGATE SERVICE MODULE  
SM2200**

**BLOCK DIAGRAM**

