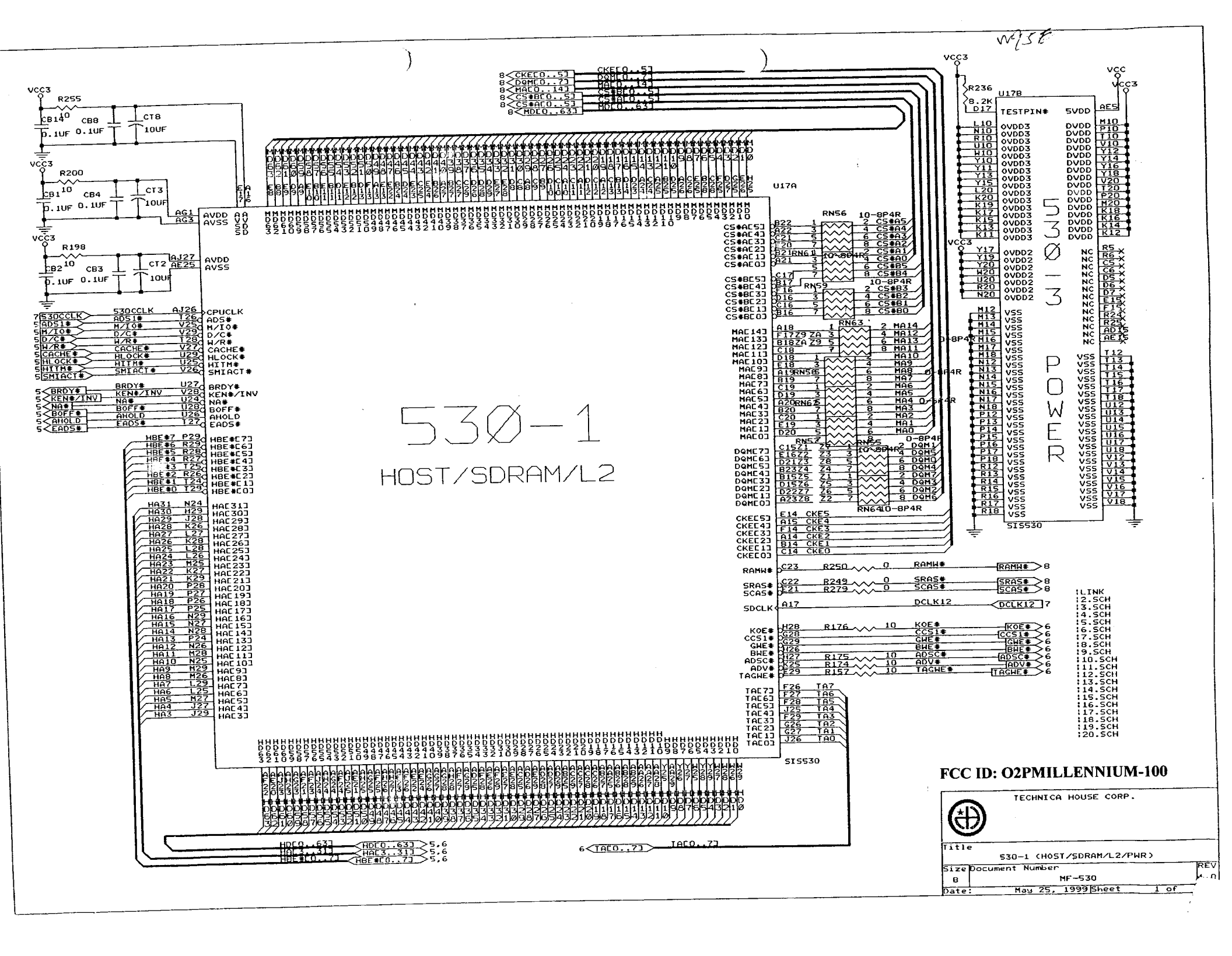
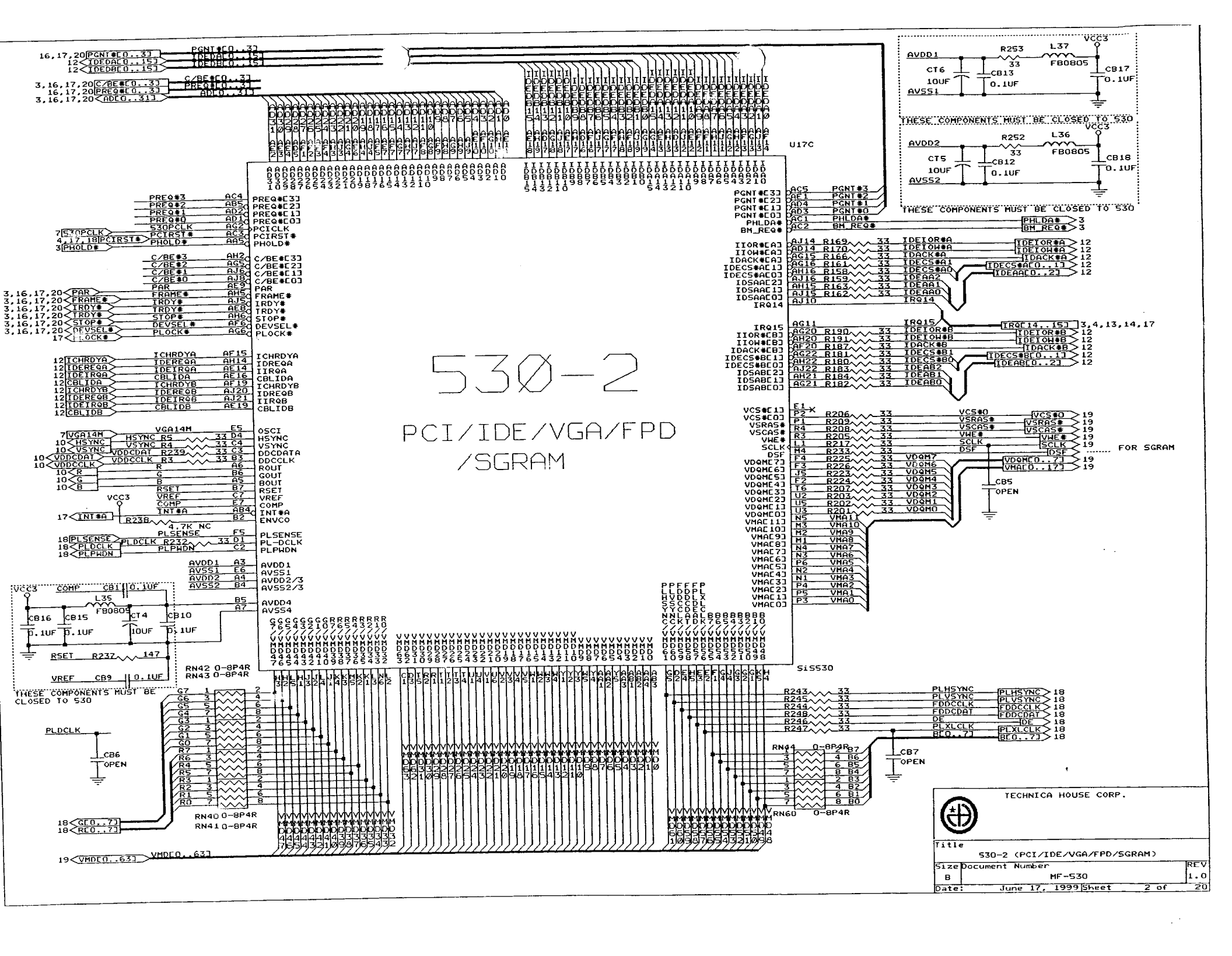
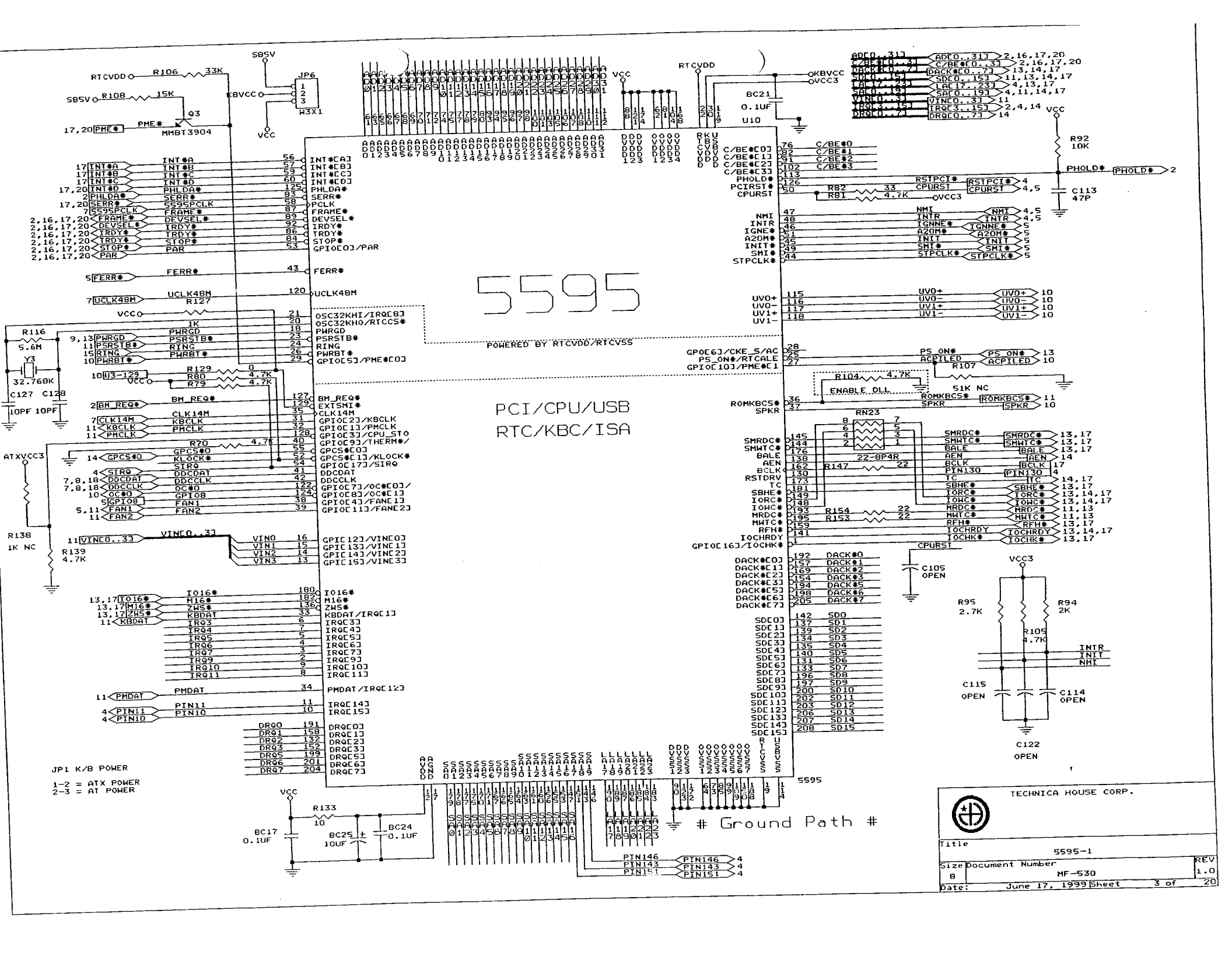


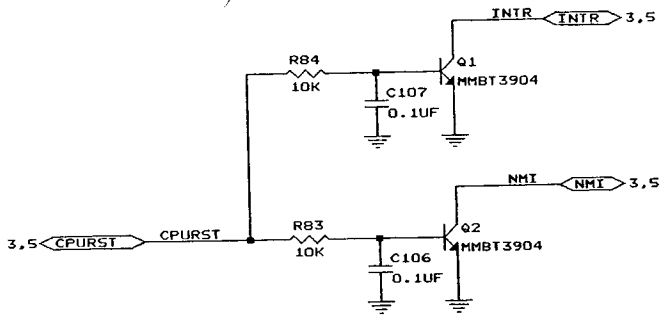
FCC ID: O2PMILLENNIUM-100

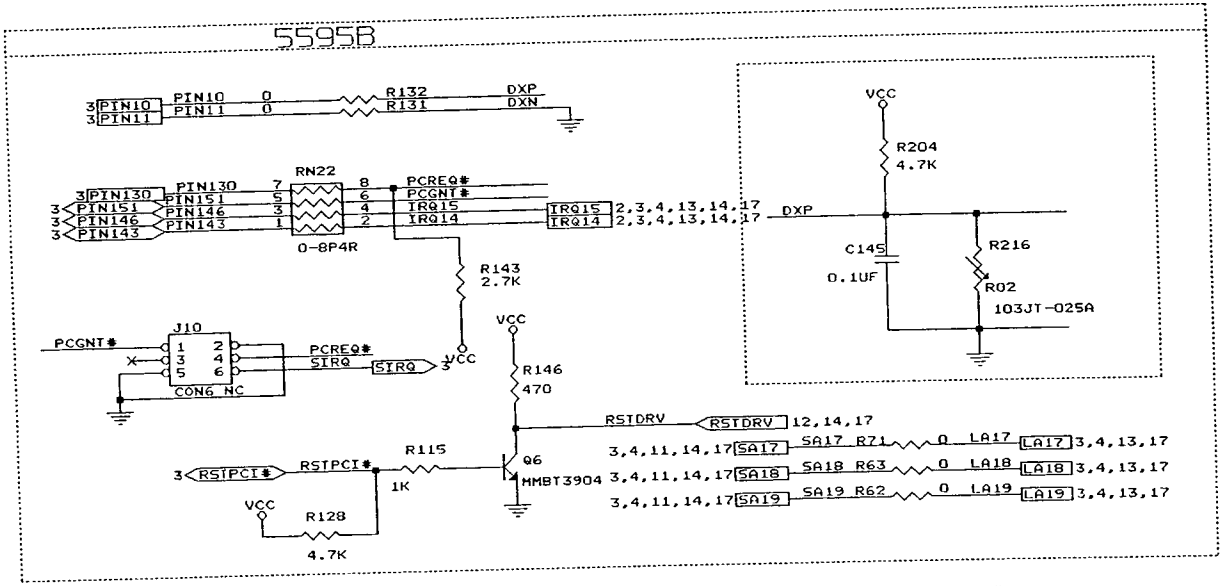
TECHNICA HOUSE CORP.

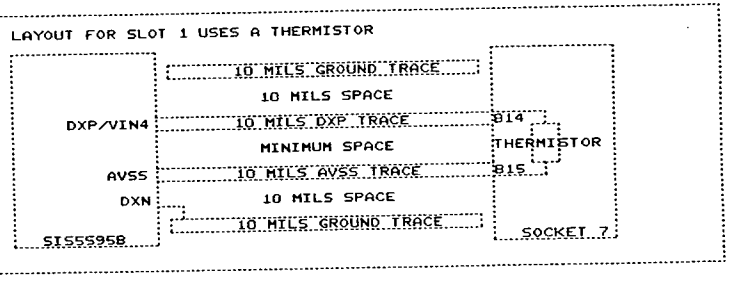
Title	530-1 (HOST/SDRAM/L2/PWR)	
Size: B	Document Number: MF-530	REV: A.0
Date: May 25, 1999	Sheet 1 of	

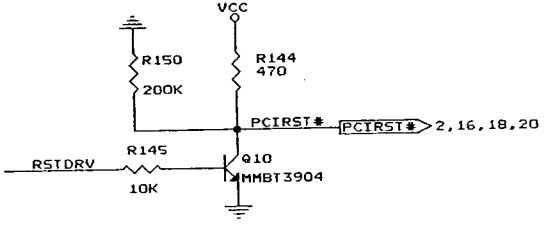

530-2
PCI/IDE/VGA/FPD
/SGRAM
SiS530
U17C
THESE COMPONENTS MUST BE CLOSED TO 530
THESE COMPONENTS MUST BE CLOSED TO 530
THESE COMPONENTS MUST BE CLOSED TO 530
FOR SGRAM
TECHNICA HOUSE CORP.
Title
530-2 (PCI/IDE/VGA/FPD/SGRAM)
Size B
Document Number MF-530
REV 1.0
Date: June 17, 1999
Sheet 2 of 20

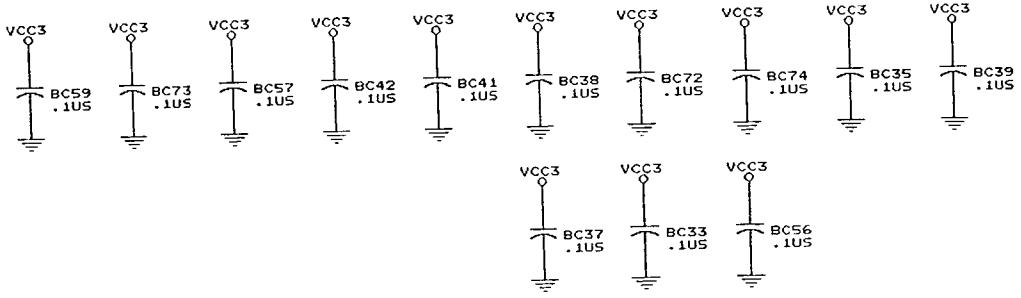

5595
PCI/CPU/USB
RTC/KBC/ISA
POWERED BY RTCVDD/RTCVSS
JP1 K/B POWER
1-2 = ATX POWER
2-3 = AT POWER
Ground Path
TECHNICA HOUSE CORP.
Title
5595-1
Size B
Document Number MF-530
REV 1.0
Date: June 17, 1999
Sheet 3 of 20





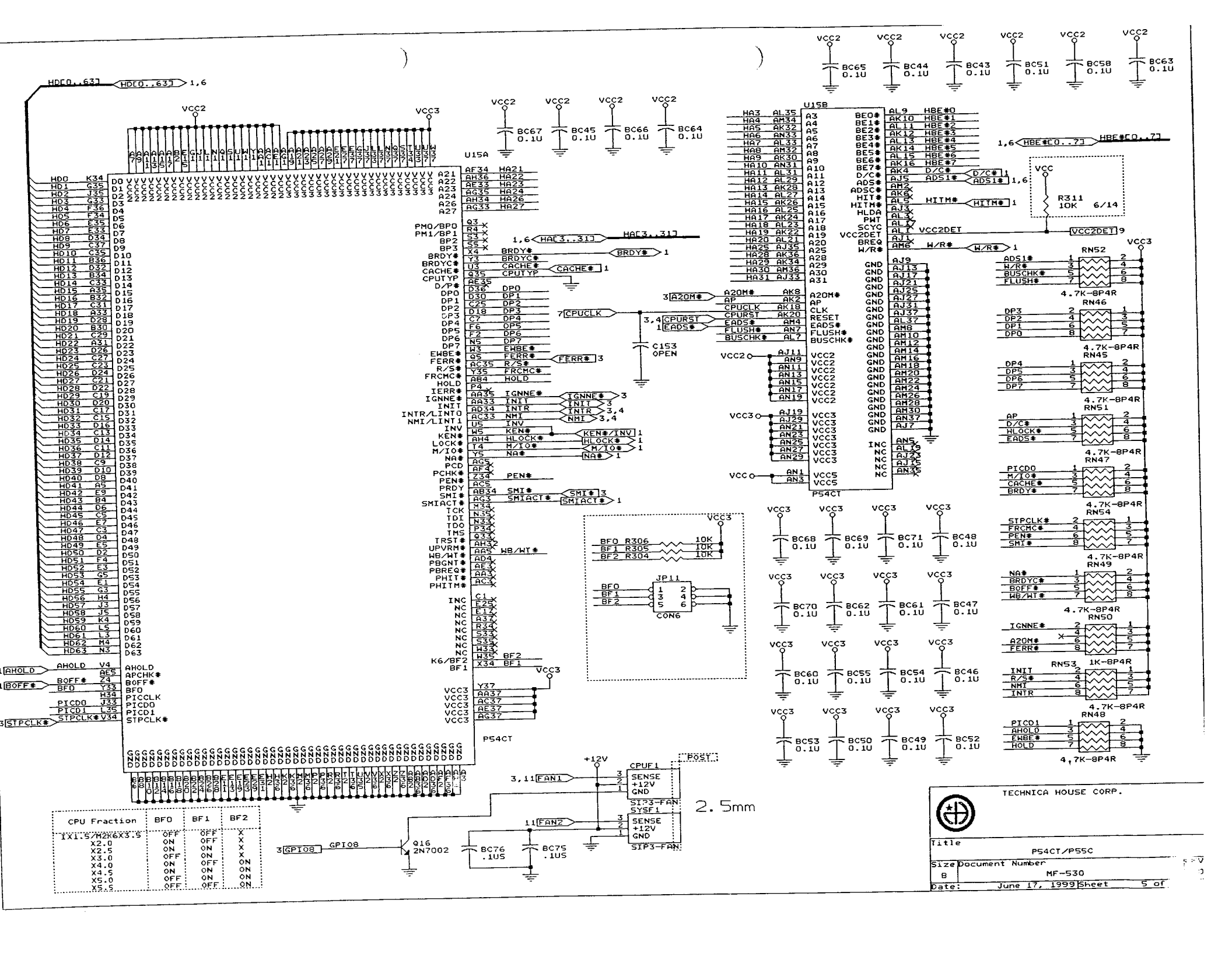




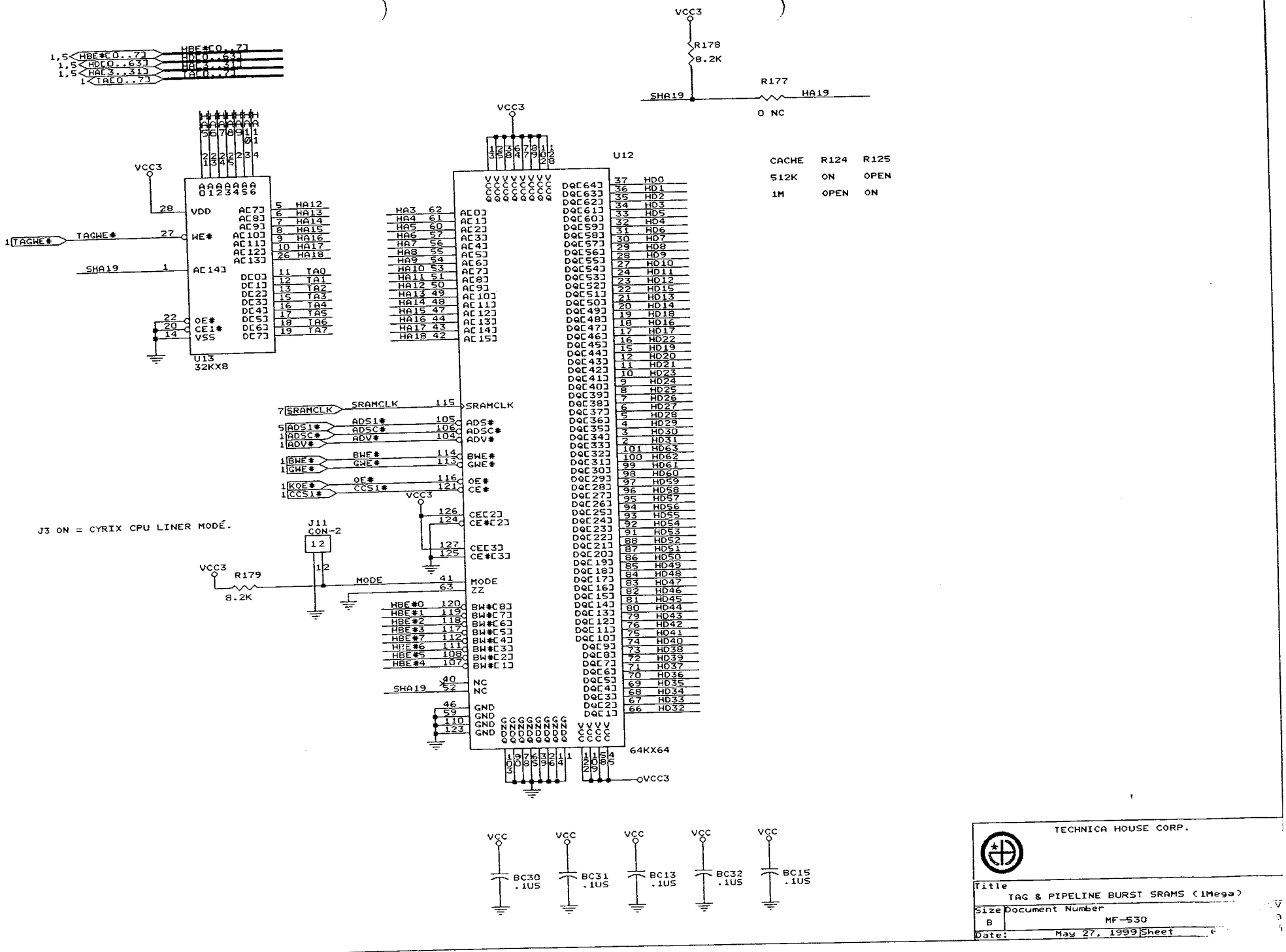


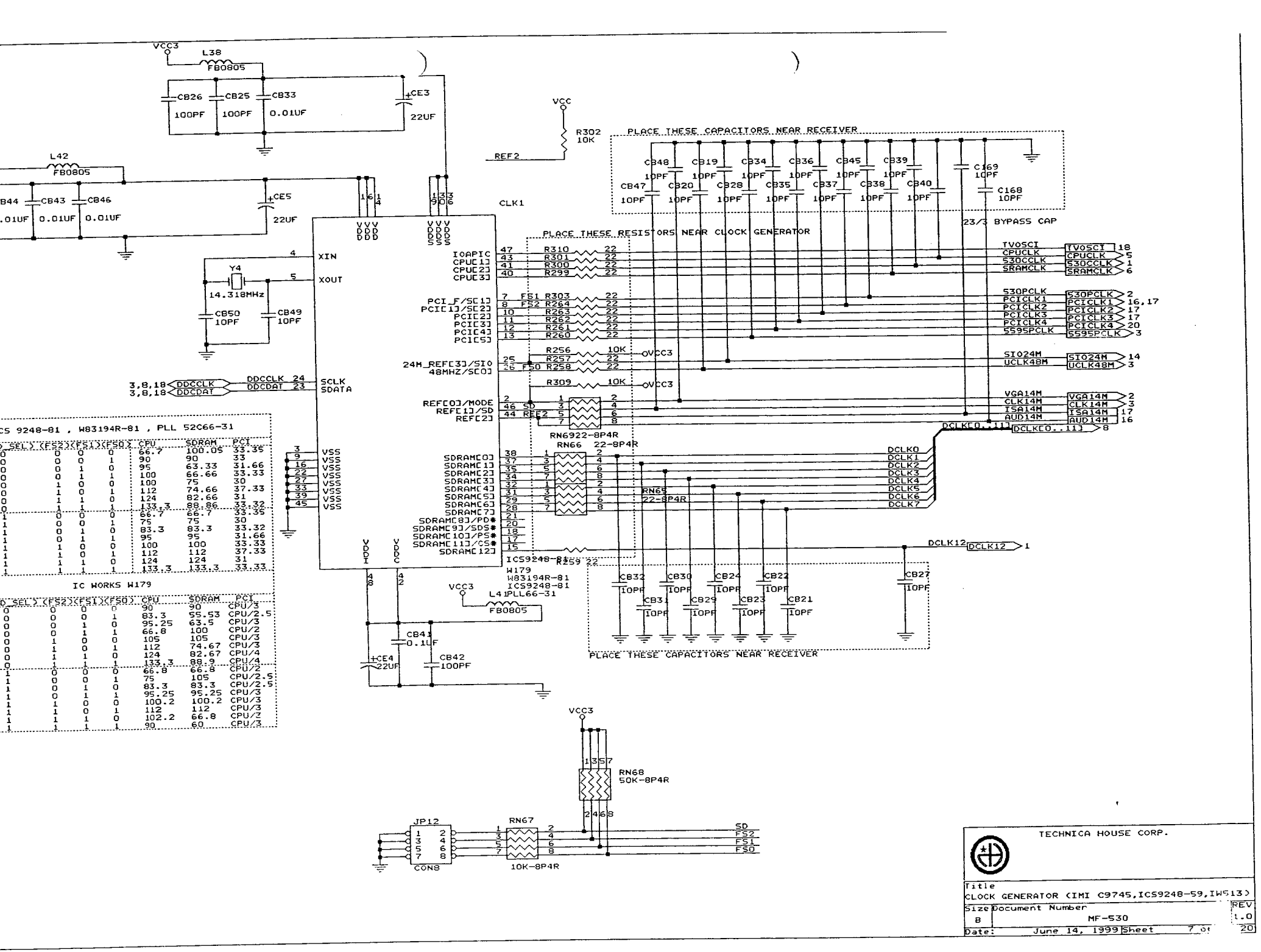
TECHNICA HOUSE CORP.

Title	5595-2	
Size B	Document Number MF-530	REV 1.0
Date: June 17, 1999	Sheet 4 of 20	



CPU Fraction	BF0	BF1	BF2
IX1.5/M2K6X3.5	OFF	OFF	X
X2.0	ON	OFF	X
X2.5	ON	ON	X
X3.0	OFF	ON	X
X4.0	ON	OFF	ON
X4.5	ON	ON	ON
X5.0	OFF	ON	ON
X5.5	OFF	OFF	ON


VCC3
R178
8.2K
R177
SHA19
HA19
0 NC
CACHE R124 R125
512K ON OPEN
1M OPEN ON
U12
64KX64
U13
32KX8
SRAMCLK
ADS1#
ADSC#
ADV#
BWE#
GWE#
OE#
CCS1#
MODE
J11
CON-2
R179
8.2K
J3 ON = CYRIX CPU LINER MODE.
BC30 .1US
BC31 .1US
BC13 .1US
BC32 .1US
BC15 .1US
TECHNICA HOUSE CORP.
Title
TAG & PIPELINE BURST SRAMS (1Mega)
Size B
Document Number MF-530
Date: May 27, 1999
Sheet



CS 9248-81 , W83194R-81 , PLL 52C66-31

SEL	FS2	FS1	FS0	CPU	SDRAM	PCI
0	0	0	0	66.7	100.05	33.35
0	0	0	1	90	90	33
0	0	1	0	95	63.33	31.66
0	0	1	1	100	66.66	33.33
0	1	0	0	100	75	30
0	1	0	1	112	74.66	37.33
0	1	1	0	124	82.66	31
0	1	1	1	133.3	88.86	33.32
1	0	0	0	66.7	66.7	33.35
1	0	0	1	75	75	30
1	0	1	0	83.3	83.3	33.32
1	0	1	1	95	95	31.66
1	1	0	0	100	100	33.33
1	1	0	1	112	112	37.33
1	1	1	0	124	124	31
1	1	1	1	133.3	133.3	33.33

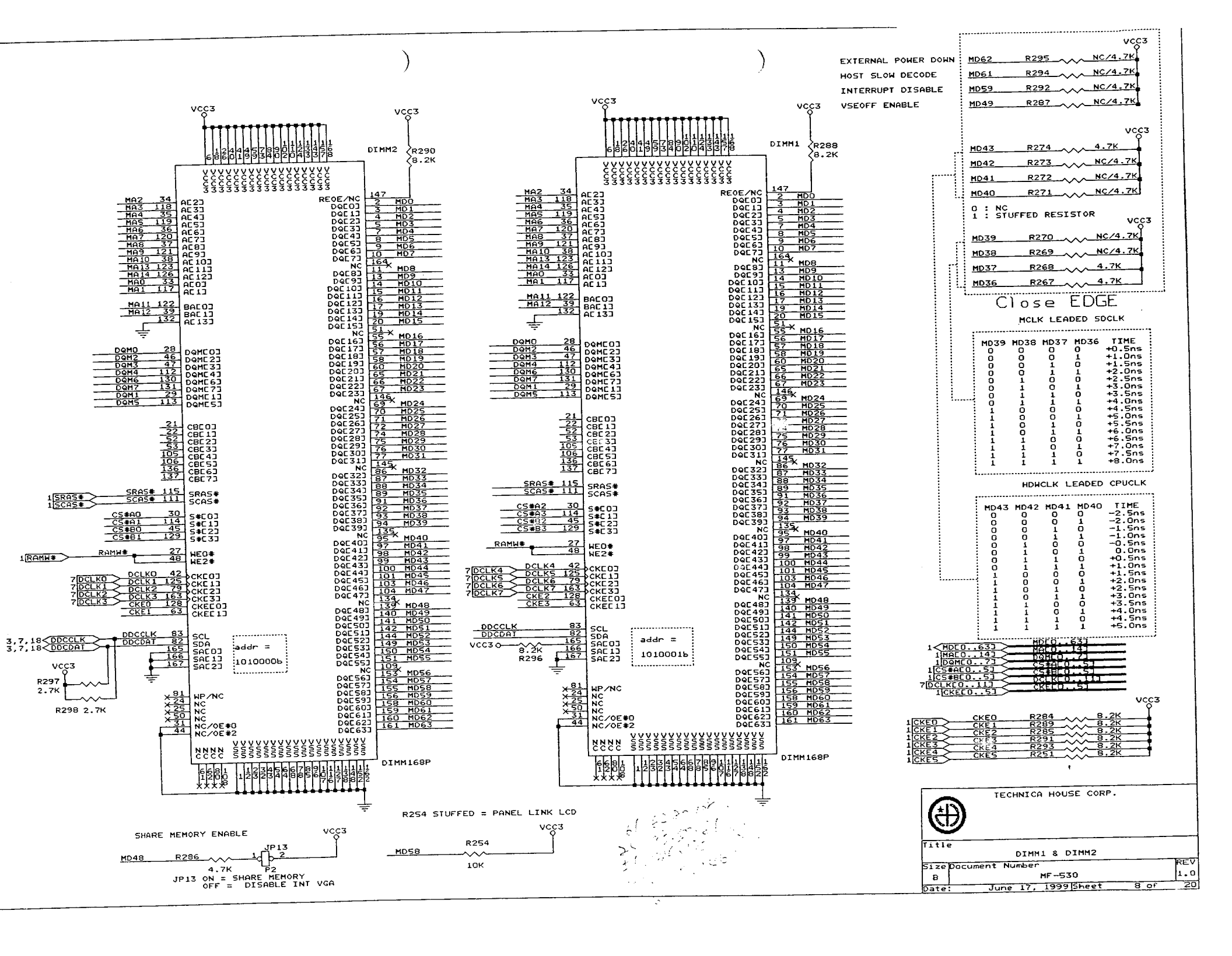
IC WORKS W179

SEL	FS2	FS1	FS0	CPU	SDRAM	PCI
0	0	0	0	90	90	CPU/3
0	0	0	1	83.3	55.53	CPU/2.5
0	0	1	0	95.25	63.5	CPU/3
0	0	1	1	66.8	100	CPU/2
0	1	0	0	105	105	CPU/3
0	1	0	1	112	74.67	CPU/3
0	1	1	0	124	82.67	CPU/4
0	1	1	1	133.3	88.9	CPU/4
1	0	0	0	66.8	66.8	CPU/2
1	0	0	1	75	105	CPU/2.5
1	0	1	0	83.3	83.3	CPU/2.5
1	0	1	1	95.25	95.25	CPU/3
1	1	0	0	100.2	100.2	CPU/3
1	1	0	1	112	112	CPU/3
1	1	1	0	102.2	66.8	CPU/2
1	1	1	1	90	60	CPU/3

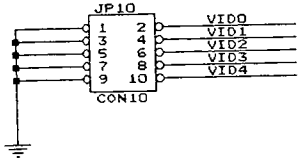
TECHNICA HOUSE CORP.

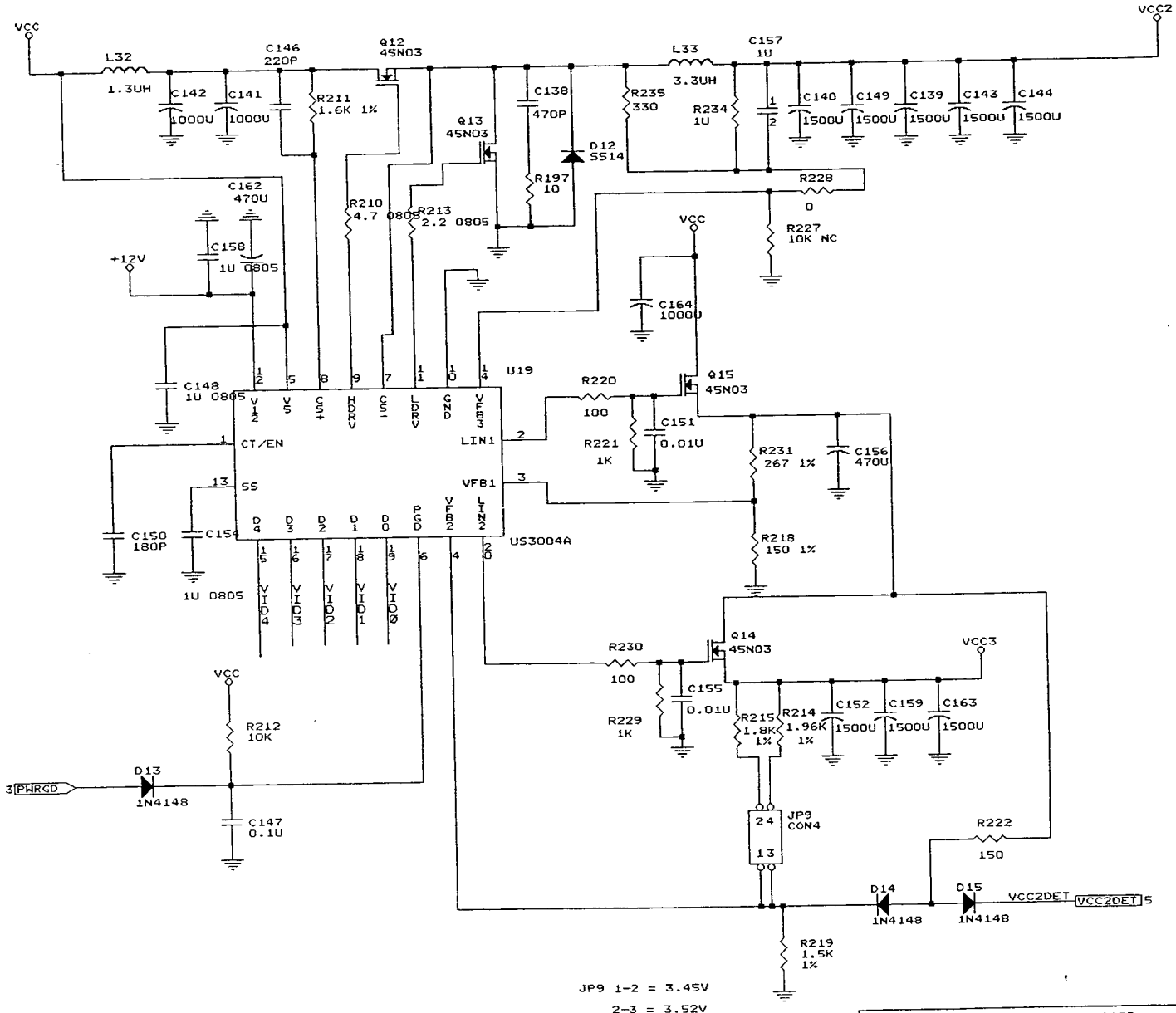
Title
CLOCK GENERATOR (IMI C9745,ICS9248-59,IW5133)

Size	Document Number	REV
B	MF-530	1.0
Date: June 14, 1999	Sheet 7 of 20	


EXTERNAL POWER DOWN
HOST SLOW DECODE
INTERRUPT DISABLE
VSEOFF ENABLE
MD62 R295 NC/4.7K
MD61 R294 NC/4.7K
MD59 R292 NC/4.7K
MD49 R287 NC/4.7K
MD43 R274 4.7K
MD42 R273 NC/4.7K
MD41 R272 NC/4.7K
MD40 R271 NC/4.7K
0 : NC
1 : STUFFED RESISTOR
MD39 R270 NC/4.7K
MD38 R269 NC/4.7K
MD37 R268 4.7K
MD36 R267 4.7K
Close EDGE
MCLK LEADED SDCLK
MD39 MD38 MD37 MD36 TIME
0 0 0 0 +0.5ns
0 0 0 1 +1.0ns
0 0 1 0 +1.5ns
0 0 1 1 +2.0ns
0 1 0 0 +2.5ns
0 1 0 1 +3.0ns
0 1 1 0 +3.5ns
0 1 1 1 +4.0ns
1 0 0 0 +4.5ns
1 0 0 1 +5.0ns
1 0 1 0 +5.5ns
1 0 1 1 +6.0ns
1 1 0 0 +6.5ns
1 1 0 1 +7.0ns
1 1 1 0 +7.5ns
1 1 1 1 +8.0ns
HDWCLK LEADED CPUCLK
MD43 MD42 MD41 MD40 TIME
0 0 0 0 -2.5ns
0 0 0 1 -2.0ns
0 0 1 0 -1.5ns
0 0 1 1 -1.0ns
0 1 0 0 -0.5ns
0 1 0 1 0.0ns
0 1 1 0 +0.5ns
0 1 1 1 +1.0ns
1 0 0 0 +1.5ns
1 0 0 1 +2.0ns
1 0 1 0 +2.5ns
1 0 1 1 +3.0ns
1 1 0 0 +3.5ns
1 1 0 1 +4.0ns
1 1 1 0 +4.5ns
1 1 1 1 +5.0ns
DIMM2
DIMM1
R290 8.2K
R288 8.2K
DIMM168P
addr = 1010000b
addr = 1010001b
R297 2.7K
R298 2.7K
R296 8.2K
R254 STUFFED = PANEL LINK LCD
SHARE MEMORY ENABLE
JP13
R286 4.7K
P2
JP13 ON = SHARE MEMORY
OFF = DISABLE INT VGA
R254 10K
CKE0 R284 8.2K
CKE1 R289 8.2K
CKE2 R285 8.2K
CKE3 R291 8.2K
CKE4 R293 8.2K
CKE5 R251 8.2K
TECHNICA HOUSE CORP.
Title
DIMM1 & DIMM2
Size B
Document Number MF-530
REV 1.0
Date: June 17, 1999
Sheet 8 of 20

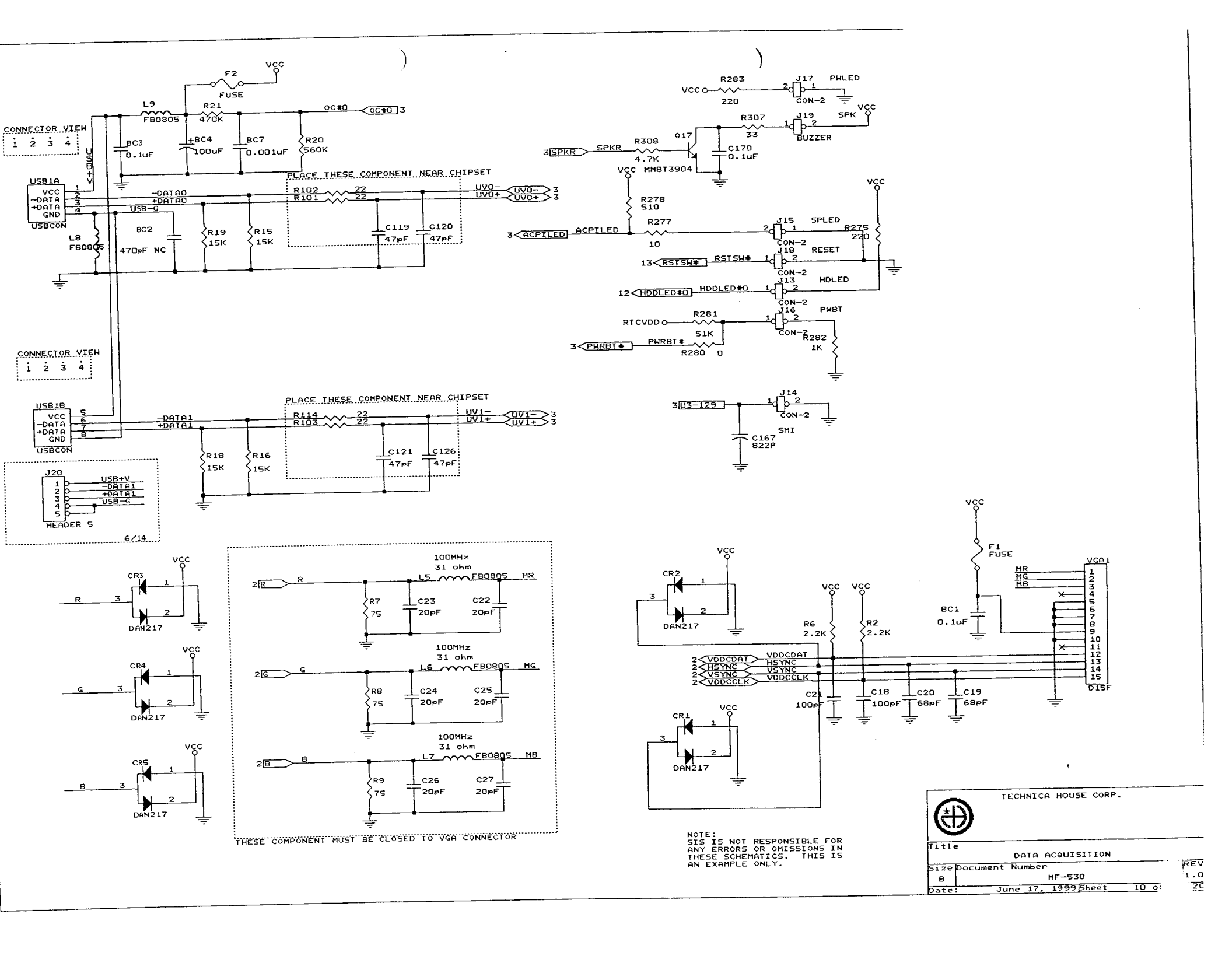
VCC2	1-2	3-4	5-6	7-8	9-10
1.8V	OFF	ON	OFF	ON	ON
2.0V	OFF	ON	ON	ON	ON
2.2V	OFF	ON	OFF	OFF	OFF
2.5V	ON	OFF	ON	OFF	OFF
2.8V	OFF	OFF	OFF	ON	OFF
2.9V	ON	OFF	OFF	ON	OFF
3.1V	ON	ON	OFF	ON	OFF
3.2V	OFF	OFF	ON	ON	OFF
3.3V	ON	OFF	ON	ON	OFF
3.5V	ON	ON	ON	ON	OFF

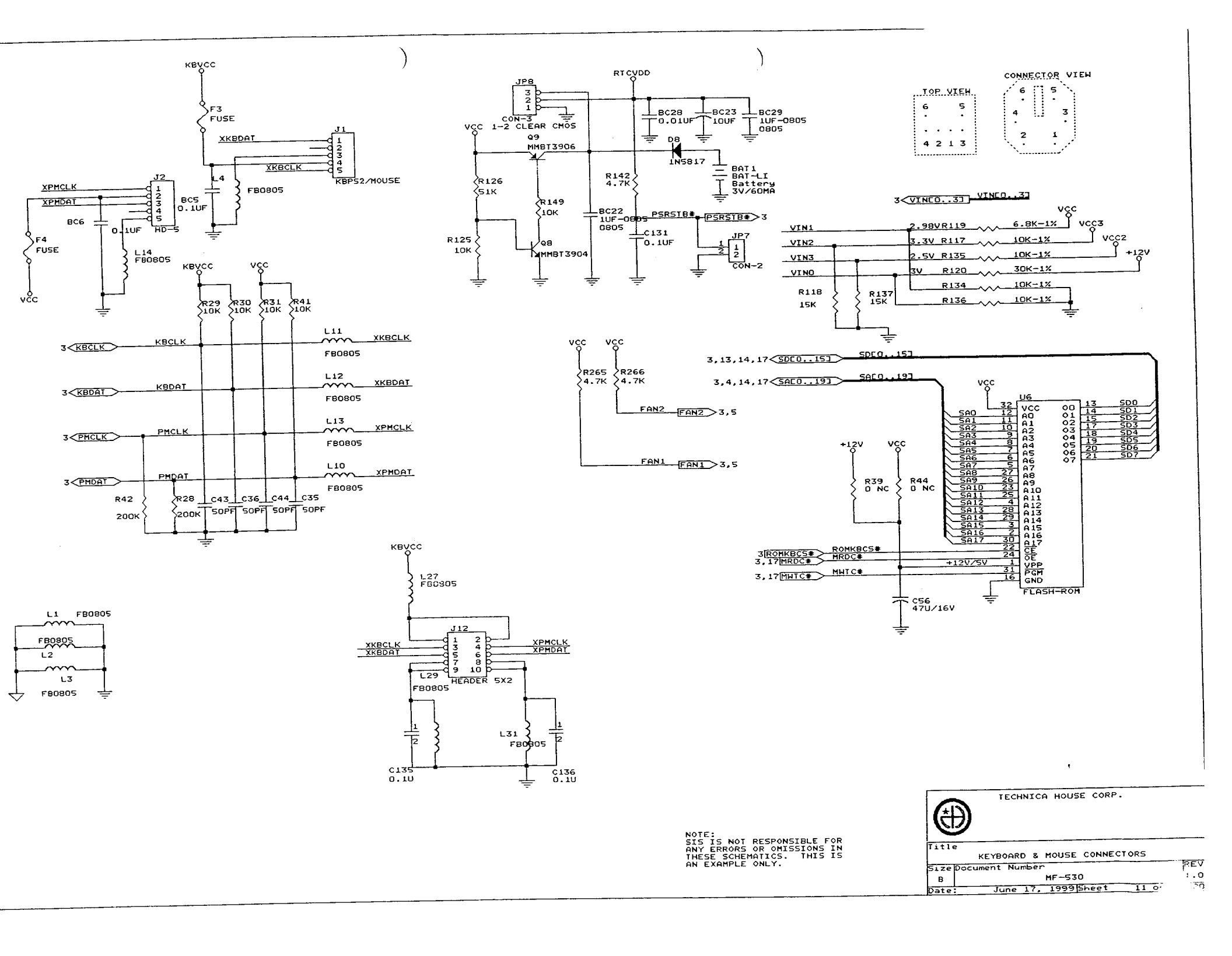




TECHNICA HOUSE CORP

Title	DC-DC CONVERTERS	
Size B	Document Number MF-530	REV 1.0
Date: June 17, 1999	Sheet 9	0


CONNECTOR VIEW
1 2 3 4
USB+V
F2
FUSE
VCC
L9
FB0805
R21
470K
OC#0
OC#0 3
BC3
0.1uF
BC4
100uF
BC7
0.001uF
R20
560K
USB1A
VCC
-DATA
+DATA
GND
USBCON
-DATA0
+DATA0
USB-G
PLACE THESE COMPONENT NEAR CHIPSET
R102 22
R101 22
UV0-
UV0+
UV0- 3
UV0+ 3
BC2
470pF NC
R19
15K
R15
15K
C119
47pF
C120
47pF
L8
FB0805
CONNECTOR VIEW
1 2 3 4
USB1B
VCC
-DATA
+DATA
GND
USBCON
-DATA1
+DATA1
PLACE THESE COMPONENT NEAR CHIPSET
R114 22
R103 22
UV1-
UV1+
UV1- 3
UV1+ 3
R18
15K
R16
15K
C121
47pF
C126
47pF
J20
USB+V
-DATA1
+DATA1
USB-G
HEADER 5
6/14
R283
220
J17
PWLED
CON-2
SPK
R307
33
J19
BUZZER
3 SPKR
SPKR
R308
4.7K
Q17
MMBT3904
C170
0.1uF
R278
510
R277
10
3 ACPILED
ACPILED
J15
SPLED
R275
220
13 RSTSW#
RSTSW#
J18
RESET
12 HDDLED#0
HDDLED#0
J13
HDLED
J16
PWBT
RTCVDD
R281
51K
R282
1K
3 PWRBT#
PWRBT#
R280
0
3 U3-129
J14
SMI
C167
822P
CR3
DAN217
CR4
DAN217
CR5
DAN217
100MHz
31 ohm
2 R
R
L5
FB0805
MR
R7
75
C23
20pF
C22
20pF
2 G
G
L6
FB0805
MG
R8
75
C24
20pF
C25
20pF
2 B
B
L7
FB0805
MB
R9
75
C26
20pF
C27
20pF
THESE COMPONENT MUST BE CLOSED TO VGA CONNECTOR
CR2
DAN217
CR1
DAN217
F1
FUSE
BC1
0.1uF
R6
2.2K
R2
2.2K
2 VDDCDAT
2 HSYNC
2 VSYNC
2 VDDCCLK
C21
100pF
C18
100pF
C20
68pF
C19
68pF
VGA1
MR
MG
MB
D15F
NOTE:
SIS IS NOT RESPONSIBLE FOR
ANY ERRORS OR OMISSIONS IN
THESE SCHEMATICS. THIS IS
AN EXAMPLE ONLY.
TECHNICA HOUSE CORP.
Title
DATA ACQUISITION
Size B
Document Number
MF-530
REV
1.0
Date: June 17, 1999
Sheet 10 o
2C

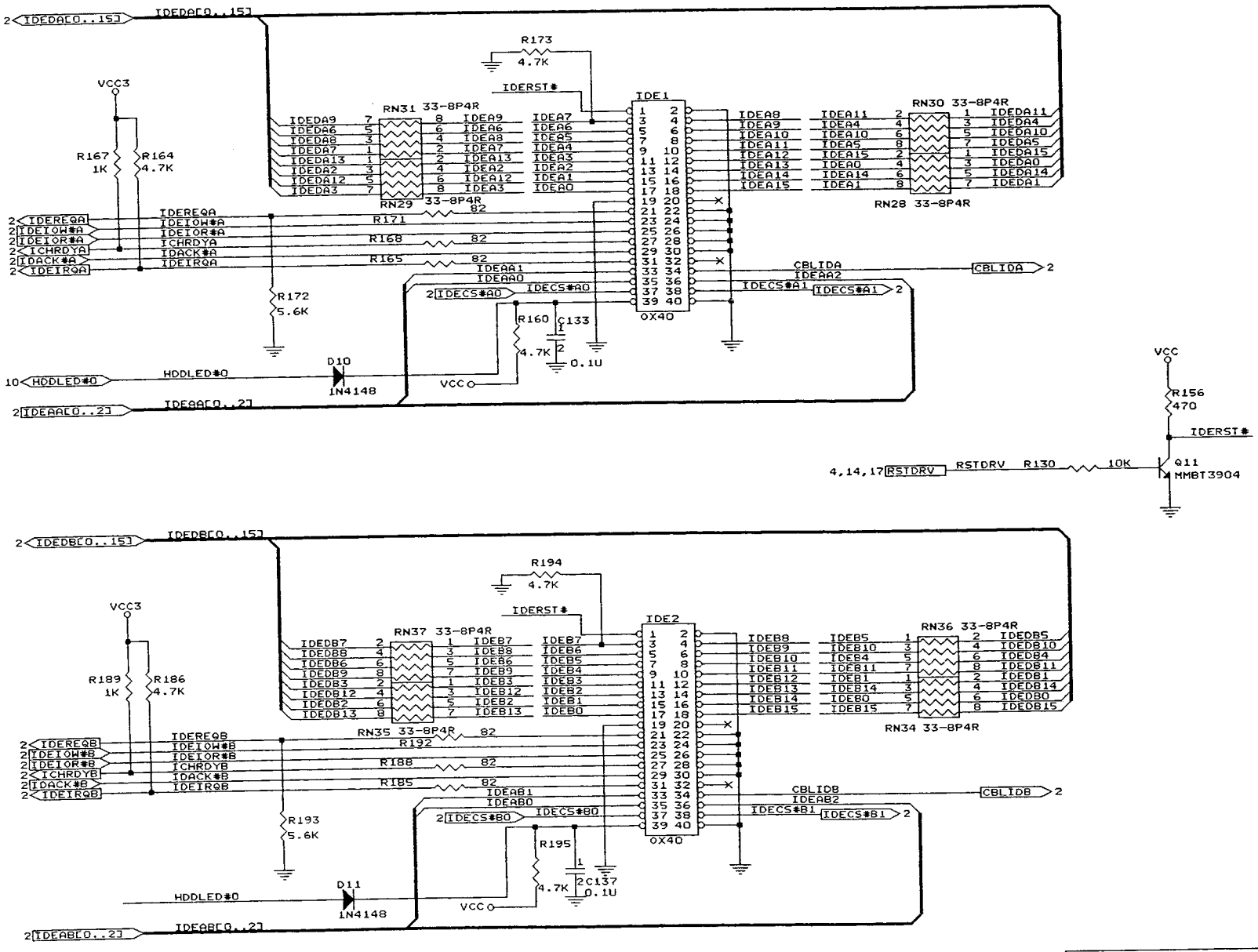


NOTE:
SIS IS NOT RESPONSIBLE FOR ANY ERRORS OR OMISSIONS IN THESE SCHEMATICS. THIS IS AN EXAMPLE ONLY.

TECHNICA HOUSE CORP.

Title: KEYBOARD & MOUSE CONNECTORS

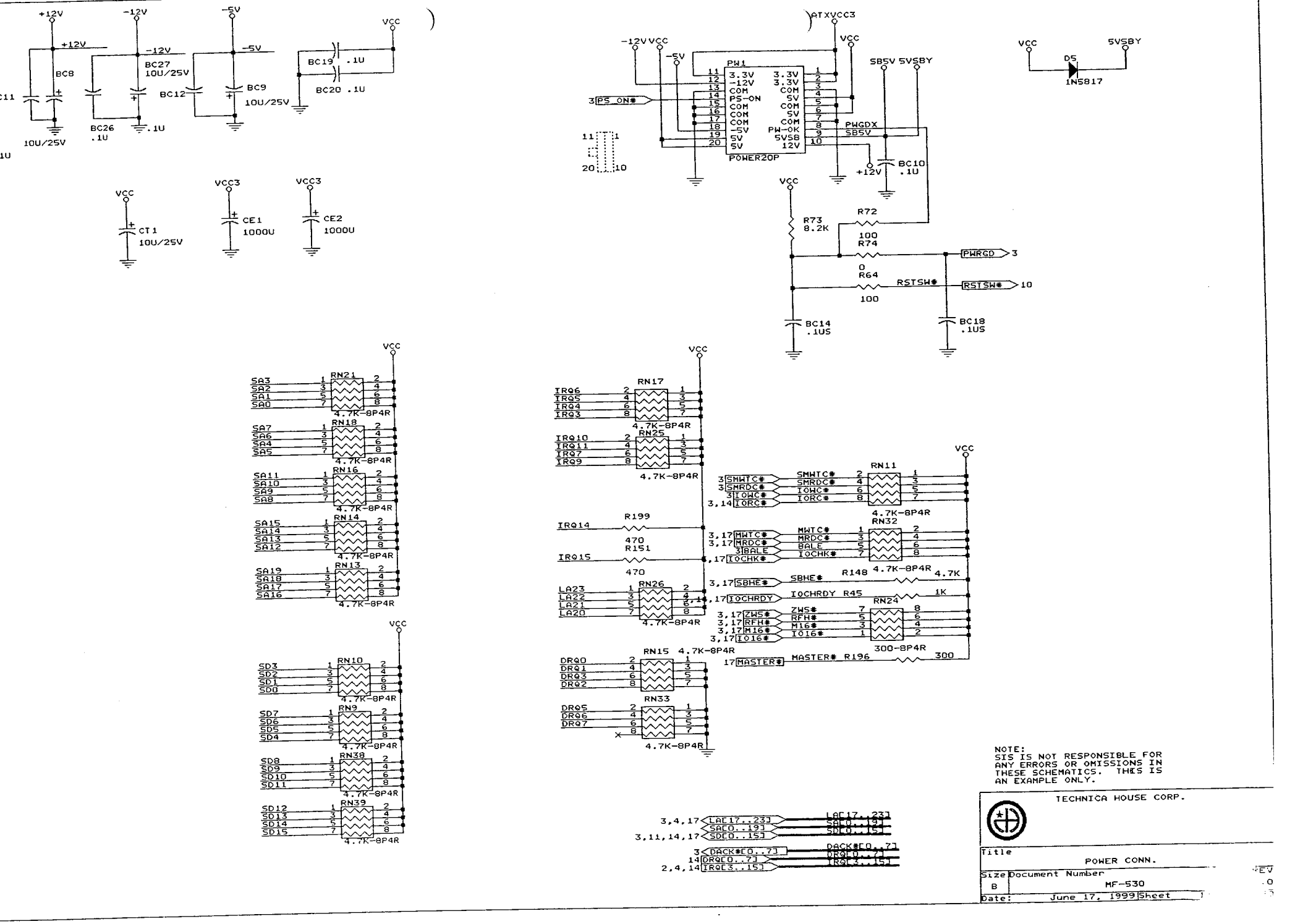
Size	Document Number	REV
B	MF-530	1.0
Date: June 17, 1999	Sheet 11 of 50	



NOTE:
SIS IS NOT RESPONSIBLE FOR ANY ERRORS OR OMISSIONS IN THESE SCHEMATICS. THIS IS AN EXAMPLE ONLY.

TECHNICA HOUSE CORP.

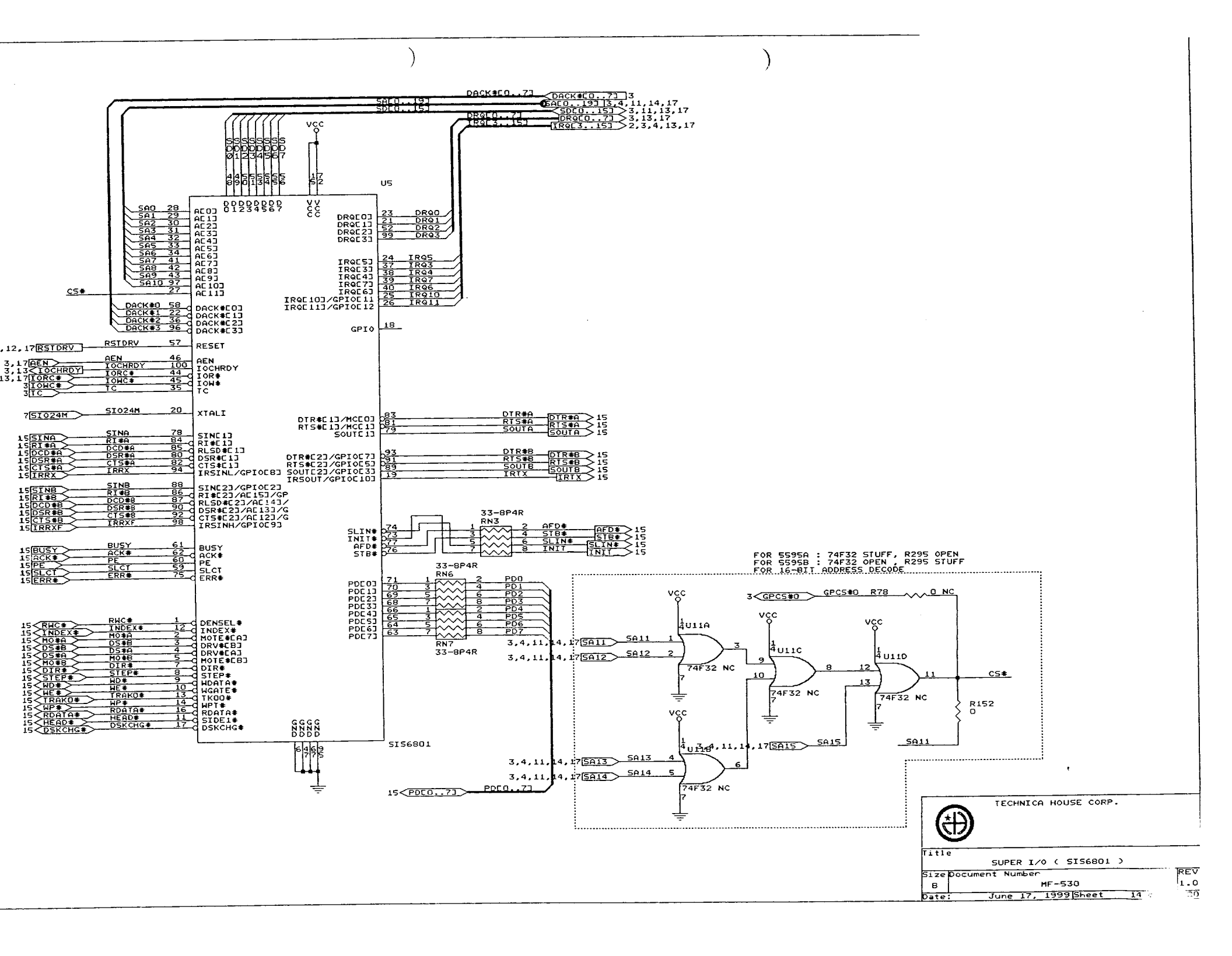
Title	IDE CONNECTORS	
Size B	Document Number MF-530	
Date: May 27, 1999	Sheet 12	

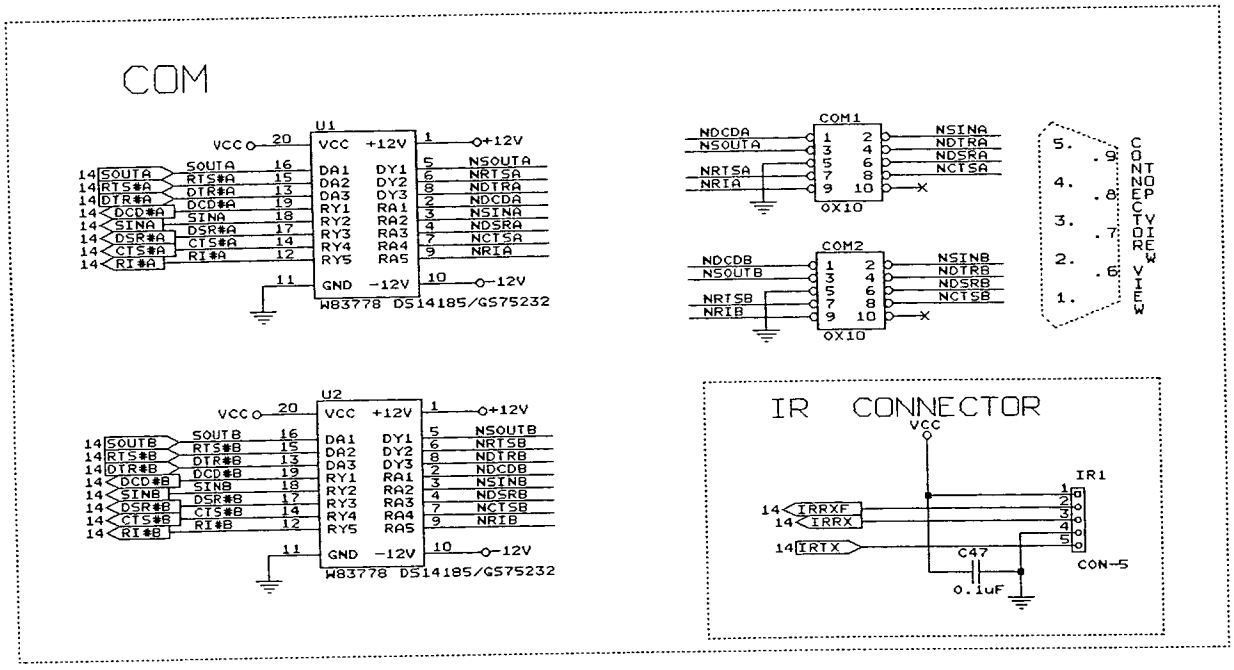


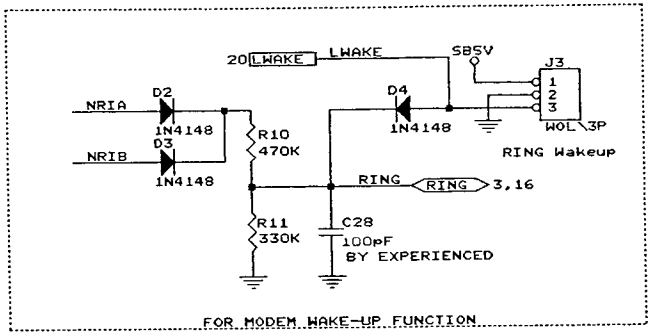
NOTE:
SIS IS NOT RESPONSIBLE FOR ANY ERRORS OR OMISSIONS IN THESE SCHEMATICS. THES IS AN EXAMPLE ONLY.

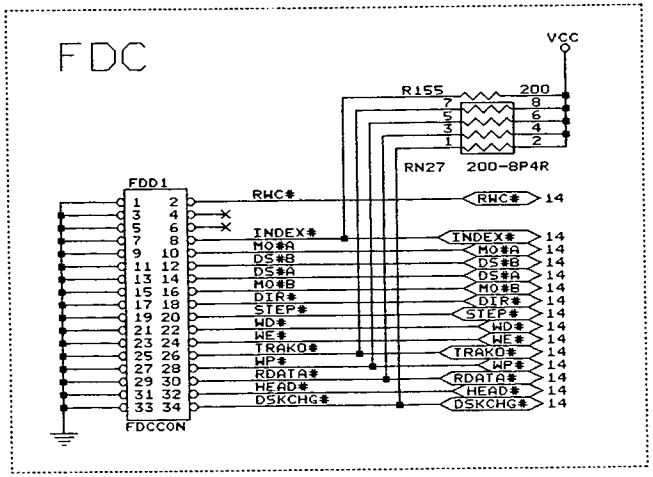
TECHNICA HOUSE CORP.

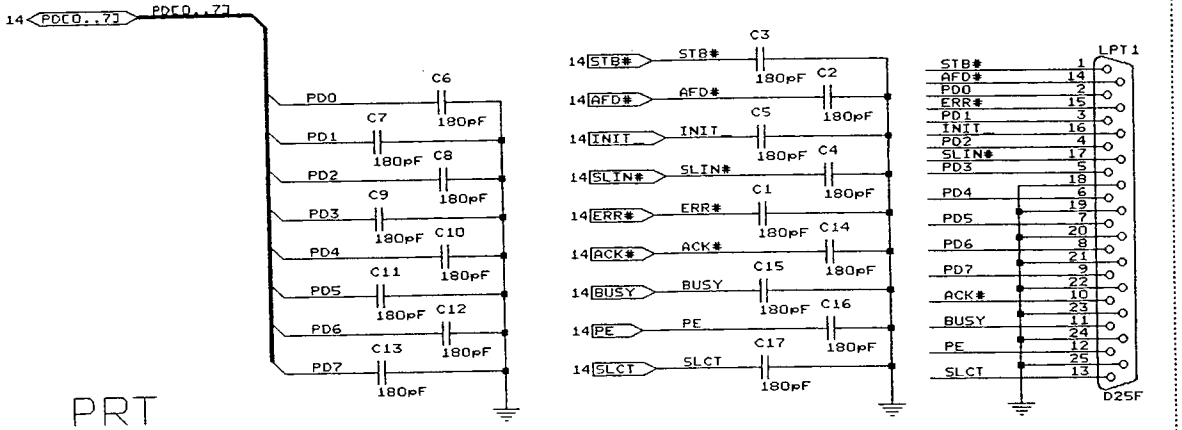
Title	POWER CONN.
Size B	Document Number MF-530
Date: June 17, 1999	Sheet

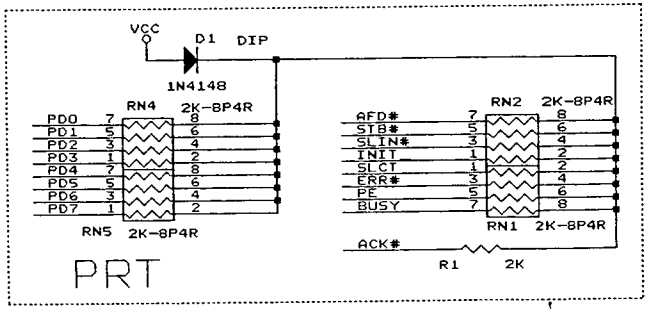

U5
SIS6801
RN3
33-8P4R
RN6
33-8P4R
RN7
33-8P4R
FOR 5595A : 74F32 STUFF, R295 OPEN
FOR 5595B : 74F32 OPEN , R295 STUFF
FOR 16-BIT ADDRESS DECODE
74F32 NC
R152
0
TECHNICA HOUSE CORP.
Title
SUPER I/O (SIS6801)
Size B
Document Number MF-530
REV 1.0
Date: June 17, 1999
Sheet 14

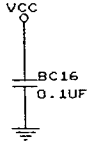






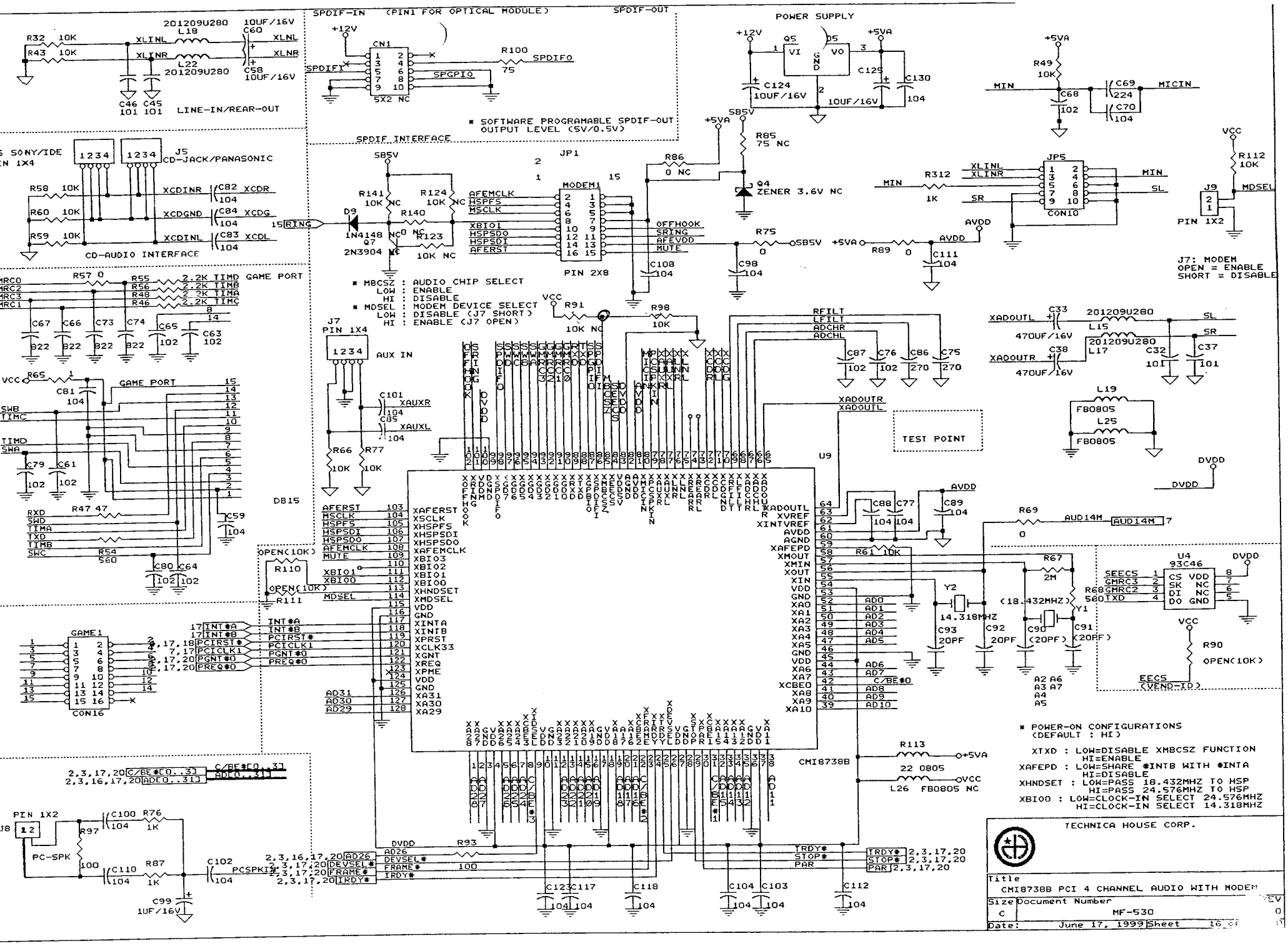






JET WAY INFORMATION

Title	SERIAL, PARALLEL, IR, & FLOPPY CONNECTORS	
Size B	Document Number MF-530	REV 1.0
Date: June 17, 1999	Sheet 15 of	


LINE-IN/REAR-OUT
SPDIF-IN (PIN1 FOR OPTICAL MODULE)
SPDIF-OUT
* SOFTWARE PROGRAMABLE SPDIF-OUT OUTPUT LEVEL (5V/0.5V)
SPDIF INTERFACE
POWER SUPPLY
CD-JACK/PANASONIC
CD-AUDIO INTERFACE
GAME PORT
AUX IN
PIN 1X4
PIN 2X8
CON10
CON16
TEST POINT
* MBCSZ : AUDIO CHIP SELECT
LOW : ENABLE
HI : DISABLE
* MDSEL : MODEM DEVICE SELECT
LOW : DISABLE (J7 SHORT)
HI : ENABLE (J7 OPEN)
J7: MODEM
OPEN = ENABLE
SHORT = DISABLE
* POWER-ON CONFIGURATIONS
(DEFAULT : HI)
XTXD : LOW=DISABLE XMBCSZ FUNCTION
HI=ENABLE
XAFEPD : LOW=SHARE *INTB WITH *INTA
HI=DISABLE
XHNDSET : LOW=PASS 18.432MHZ TO HSP
HI=PASS 24.576MHZ TO HSP
XBI00 : LOW=CLOCK-IN SELECT 24.576MHZ
HI=CLOCK-IN SELECT 14.318MHZ
CMI8738B
U9
U4 93C46
Y1
Y2
TECHNICA HOUSE CORP.
Title
CMI8738B PCI 4 CHANNEL AUDIO WITH MODEM
Size C
Document Number MF-530
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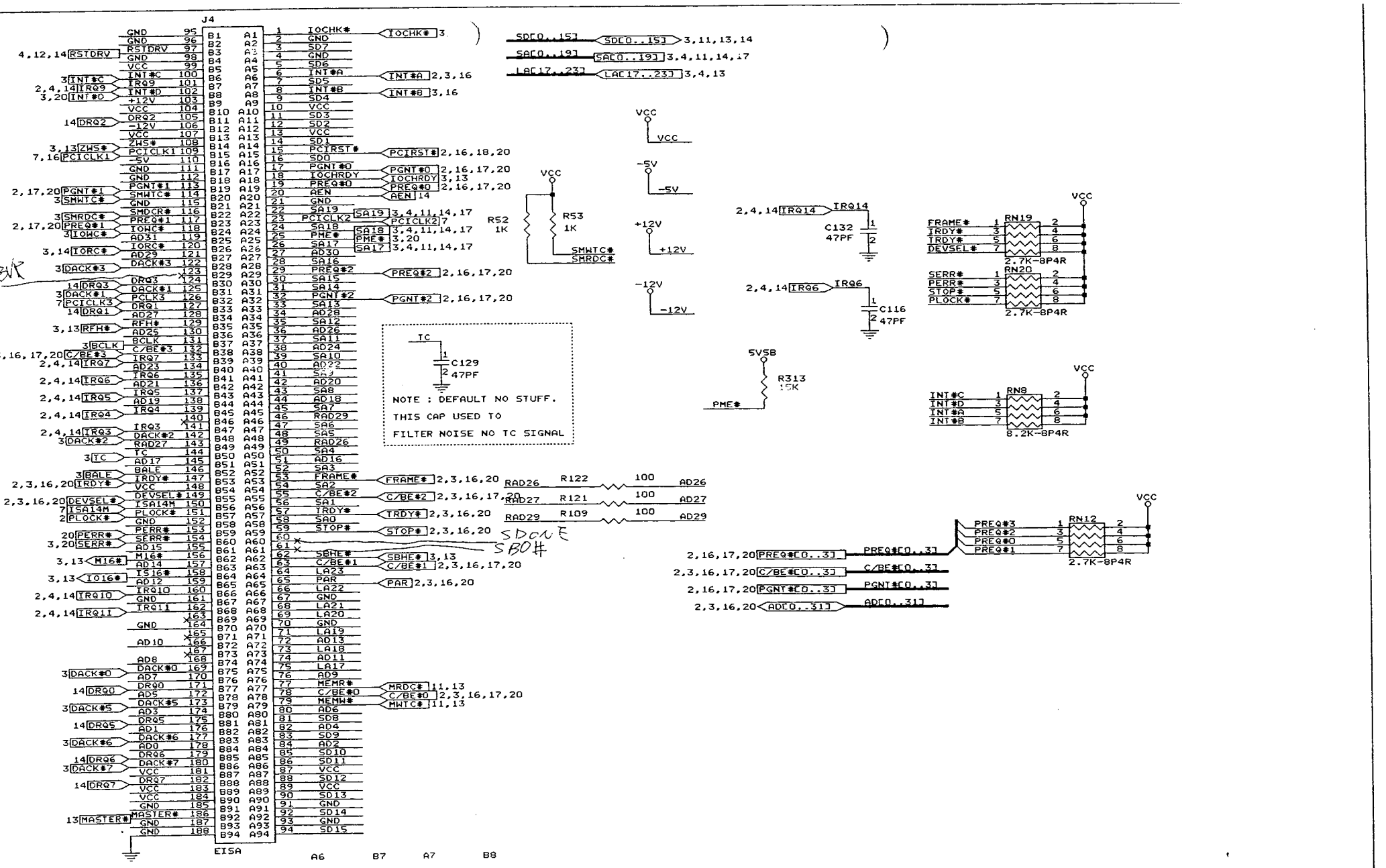
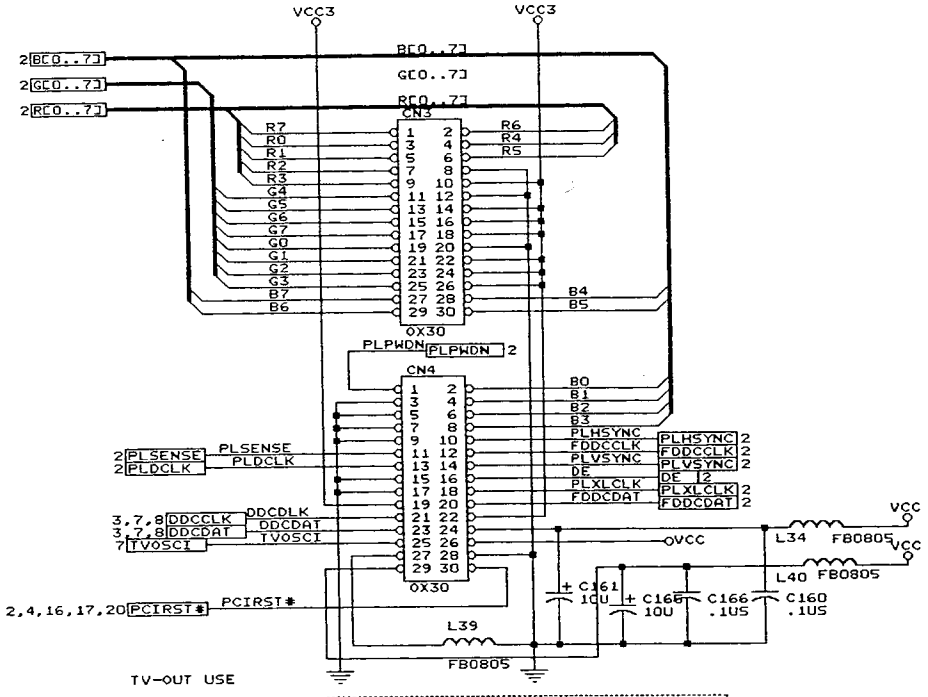
Date: June 17, 1999
Sheet 16 of



TECHNICA HOUSE CORP.

Title	ESIA SLOT		
Size B	Document Number MF-530		REV 1.0
Date: June 17, 1999	Sheet 1		20



TV-OUT USE

FOR 1. TV-OUT FOUNTION.
2. PANEL LINK FOUNTION.
3. LVDS FOUNTION.

THREE OPTIONS :

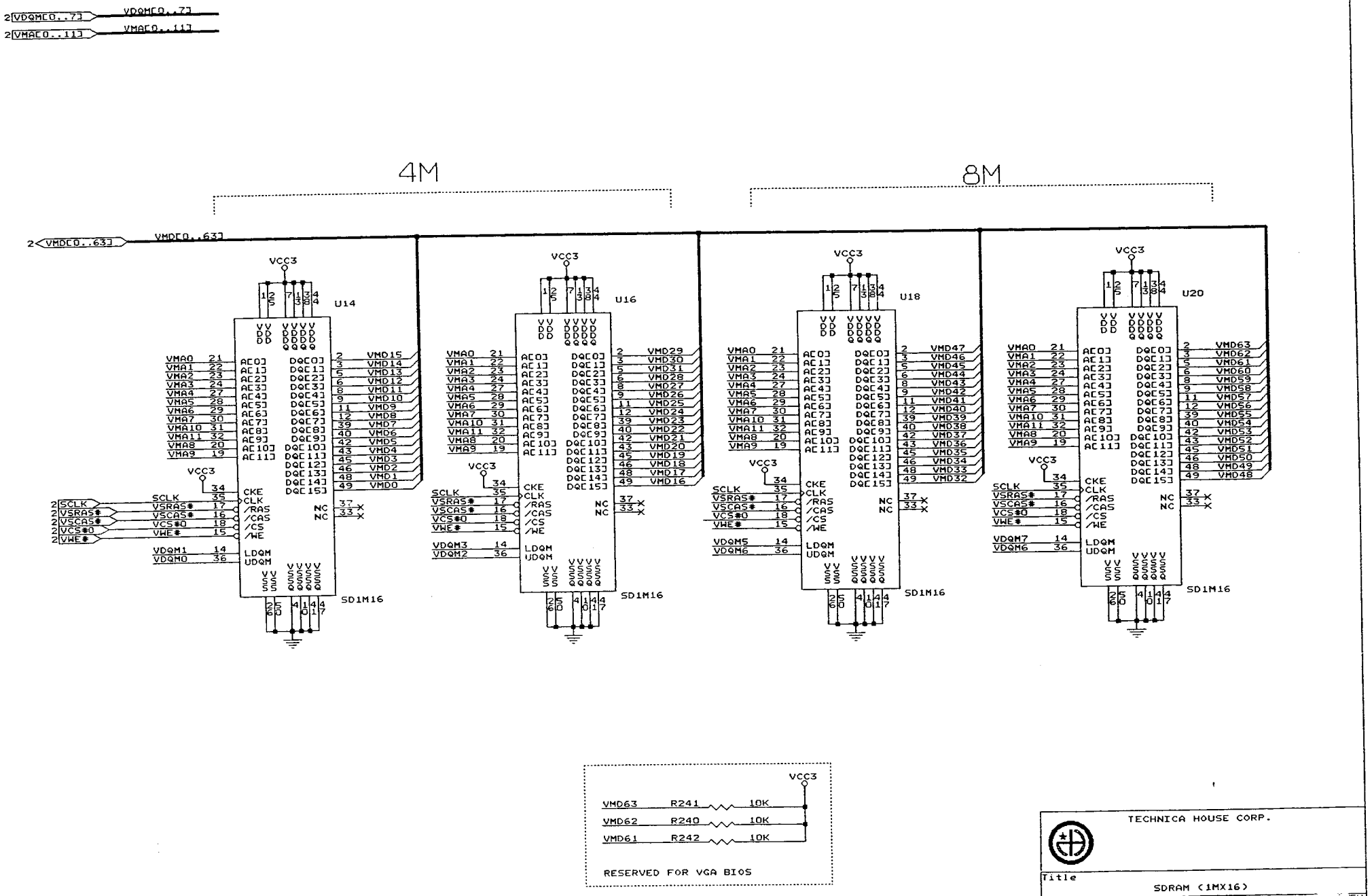
1 : You can use SiI140(TMDS) & DFP connector on board.

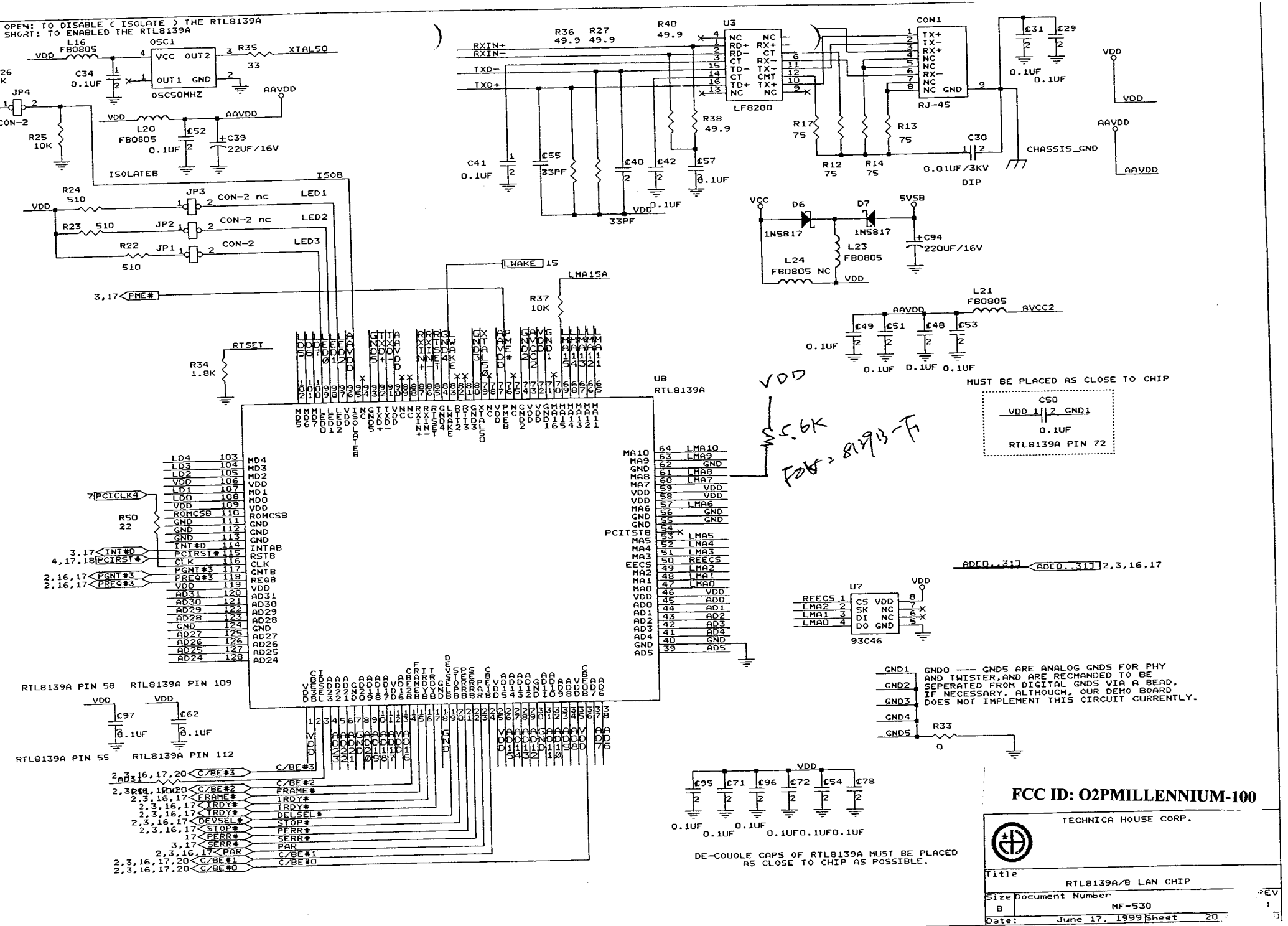
2 : You can use DS90CF561(LVDS) & 74F374 & DFP connector on board.

3: You can use SIS-DFP connector on board.

TECHNICA HOUSE CORP.

Title	SIS-DFP CONNECTOR	
Size B	Document Number MF-530	V 0
Date: June 17, 1999	Sheet	


2 VDQM[0..7]
2 VMA[0..11]
4M
8M
2 VMD[0..63]
VCC3
U14
U16
U18
U20
SD1M16
SCLK
VSRAS#
VSCAS#
VCS#0
VWE#
VDQM1
VDQM0
VDQM3
VDQM2
VDQM5
VDQM6
VDQM7
VDQM4
VMD63
R241
10K
VMD62
R240
10K
VMD61
R242
10K
RESERVED FOR VGA BIOS
TECHNICA HOUSE CORP.
Title
SDRAM (1MX16)
Size
B
Document Number
MF-530
Date:
June 14, 1999
Sheet
19 o
REV
.0

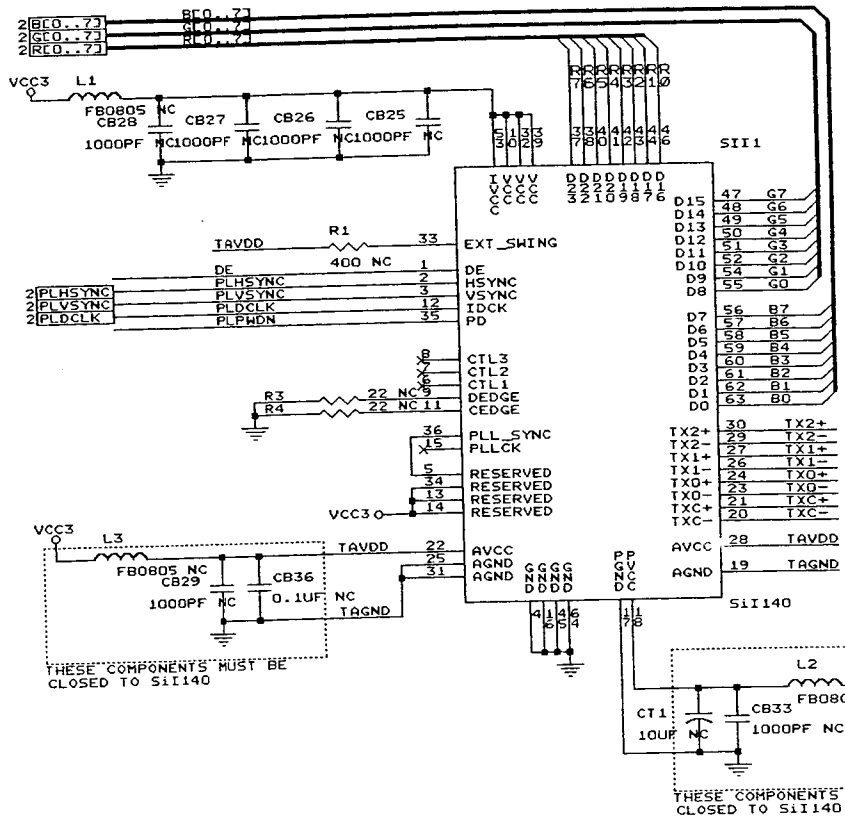

OPEN: TO DISABLE (ISOLATE) THE RTL8139A
SHORT: TO ENABLED THE RTL8139A
OSC1
OSC50MHZ
XTAL50
U3
LF8200
CON1
RJ-45
RXIN+
RXIN-
TXD-
TXD+
CHASSIS_GND
JP4
JP3
JP2
JP1
CON-2
CON-2 nc
LED1
LED2
LED3
ISOLATEB
ISOB
LWAKE
LMA15A
PME*
RTSET
U8
RTL8139A
PCICLK4
INT*D
PCIRST*
PGNT*3
PREQ*3
C/BE*3
C/BE*2
FRAME*
IRDY*
TRDY*
DELSEL*
DEVSEL*
STOP*
PERR*
SERR*
PAR
C/BE*1
C/BE*0
U7
93C46
REECS
LMA2
LMA1
LMA0
ADC0..31
GND1
GND2
GND3
GND4
GND5
GND0 --- GND5 ARE ANALOG GNDS FOR PHY AND TWISTER,AND ARE RECMANDED TO BE SEPERATED FROM DIGITAL GNDS VIA A BEAD, IF NECESSARY. ALTHOUGH, OUR DEMO BOARD DOES NOT IMPLEMENT THIS CIRCUIT CURRENTLY.
MUST BE PLACED AS CLOSE TO CHIP
C50
VDD 1 2 GND1
0.1UF
RTL8139A PIN 72
RTL8139A PIN 58
RTL8139A PIN 109
RTL8139A PIN 55
RTL8139A PIN 112
DE-COUOLE CAPS OF RTL8139A MUST BE PLACED AS CLOSE TO CHIP AS POSSIBLE.
FCC ID: O2PMILLENNIUM-100
TECHNICA HOUSE CORP.
Title
RTL8139A/B LAN CHIP
Size B
Document Number MF-530
Date: June 17, 1999 Sheet 20
REV 1

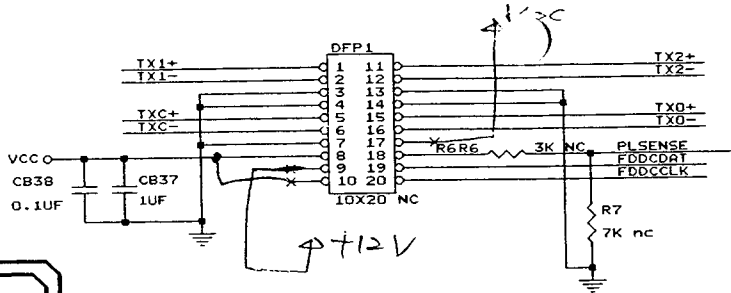
THREE OPTIONS :

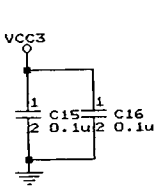
1 : You can use SiI140(TMDS) & DFP connector on board.

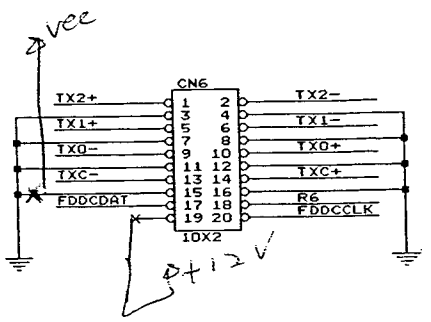
2 : You can use DS90CF561(LVDS) & 74F374 & DFP connector on board.

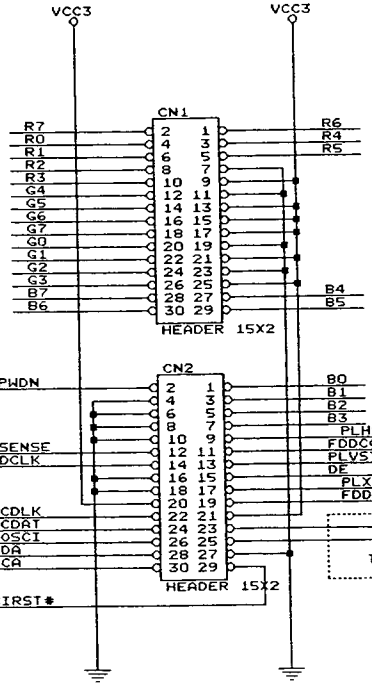
3 : You can use SiS-DFP connector on board.

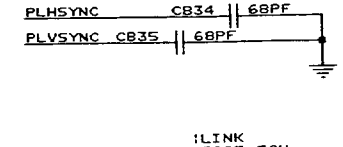


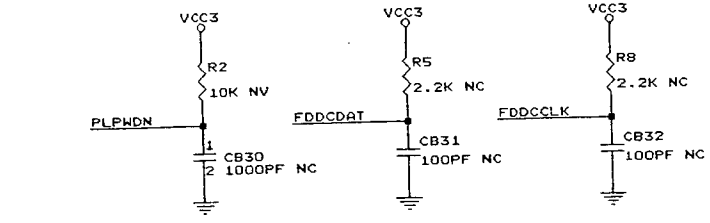












FOR DOT BOARD

TECHNICA HOUSE CORP.

Title	SiI140 & DFP PORT
Size B	Document Number MF-530DB
Date: June 17, 1999	Sheet 1