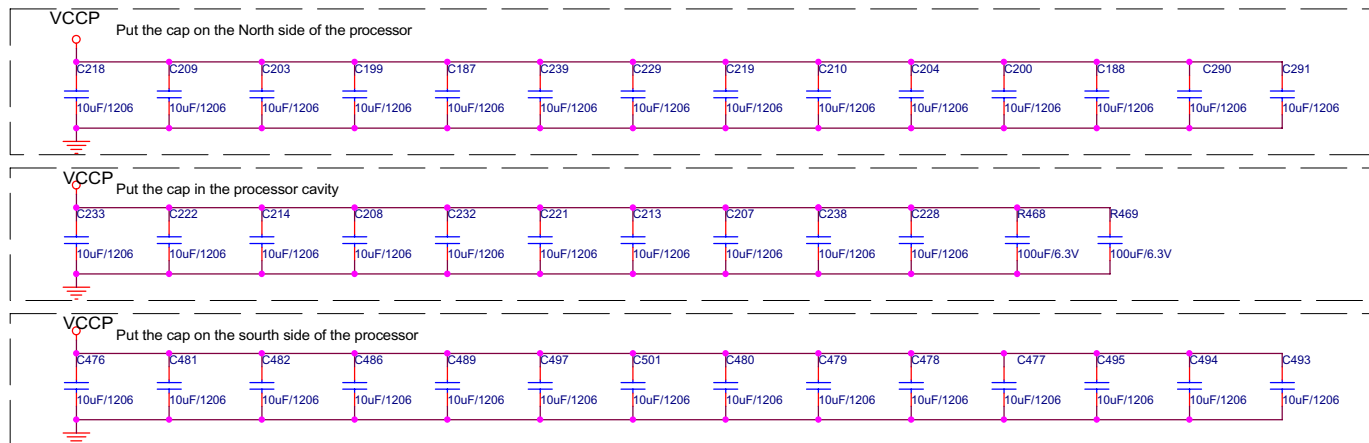




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Title		INTEL Brookdale_G_PE CHIPSET	
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Clock Synthesizer

TECHNICA

TECHNICA

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Title

INTEL Brookdale-B CHIPSET

Size

Document Number

ICS950201_Clock Genertor - 00006

Rev

0.9

Date

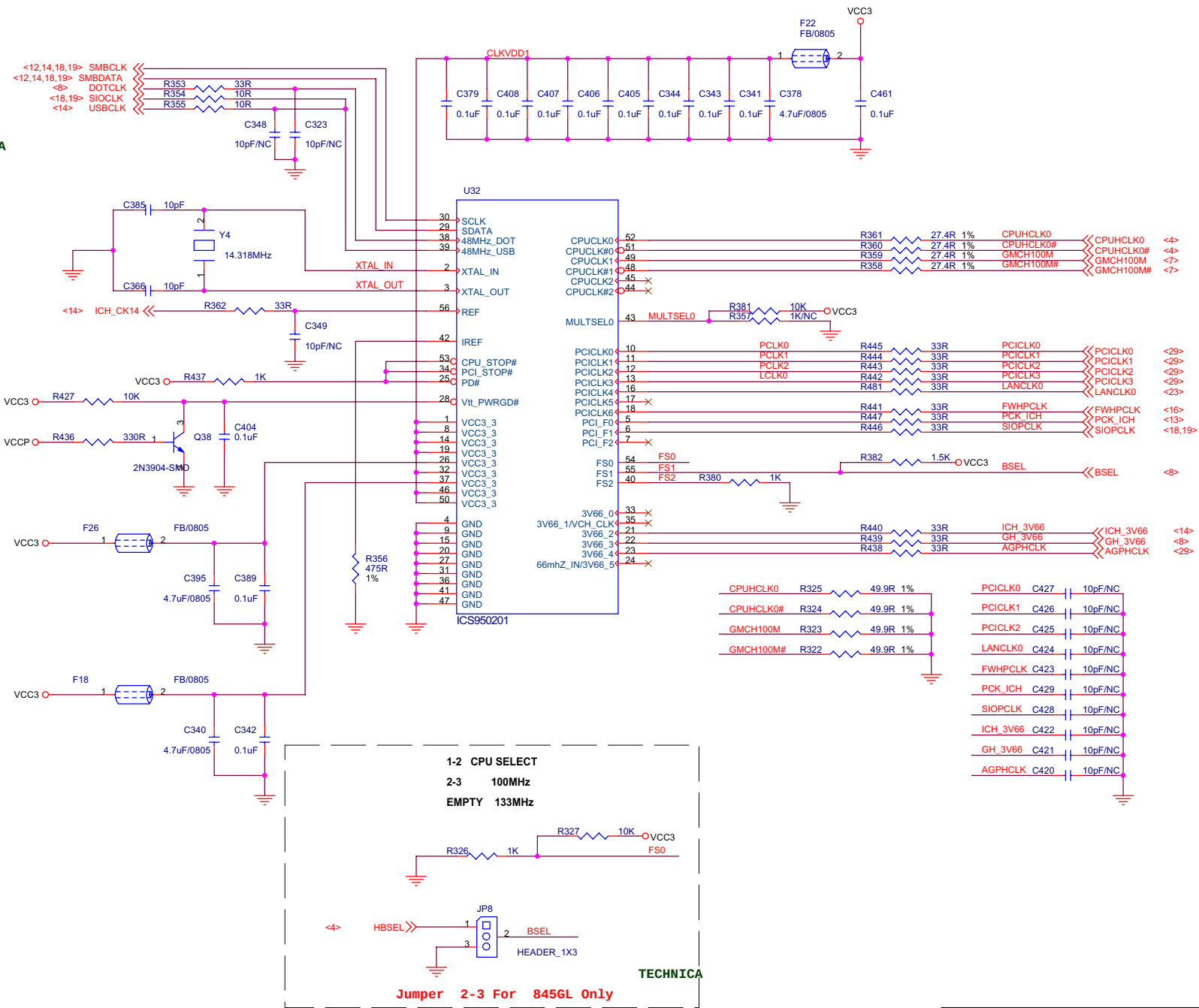
Tuesday, February 17, 2004

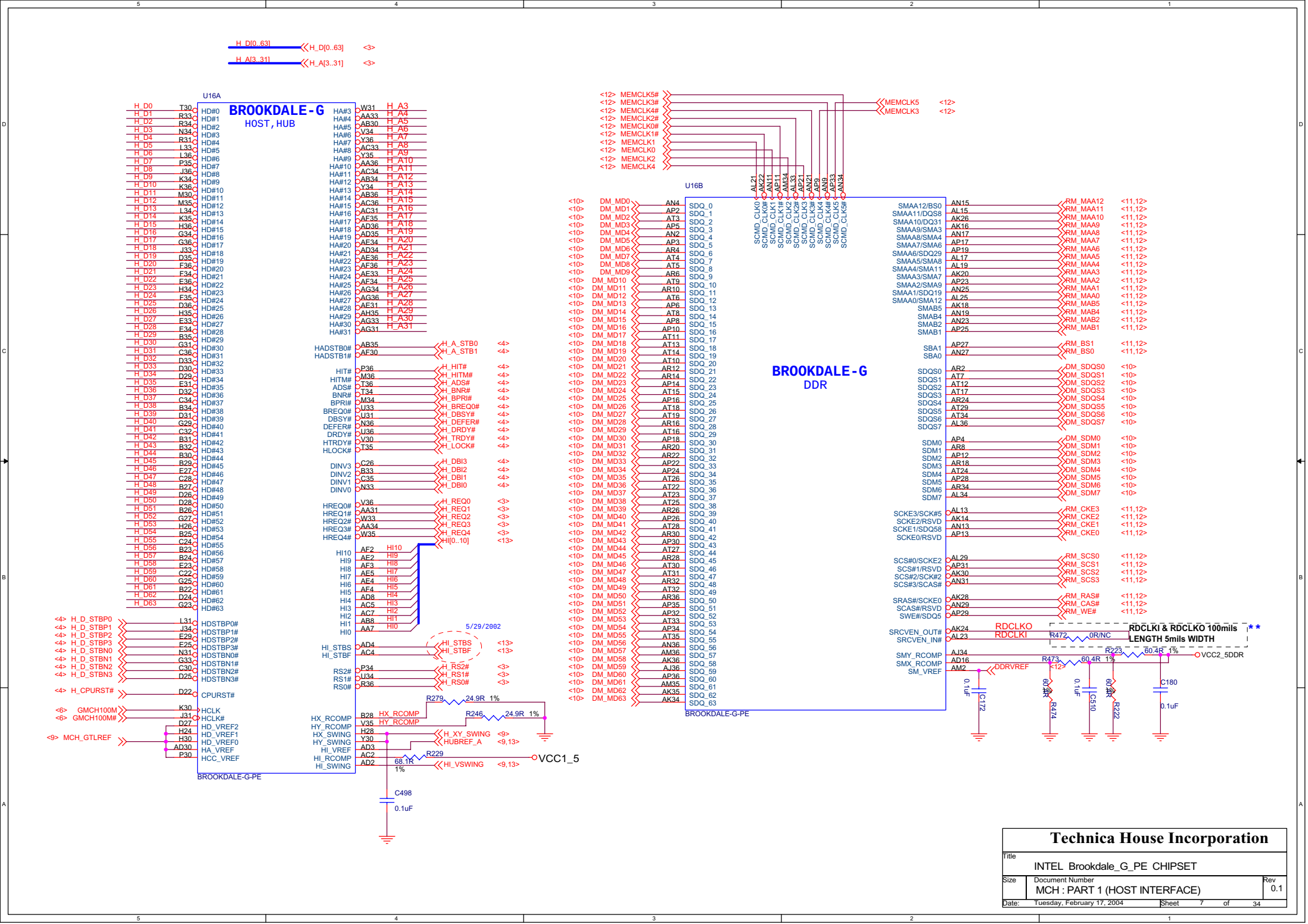
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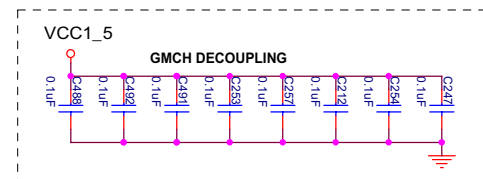
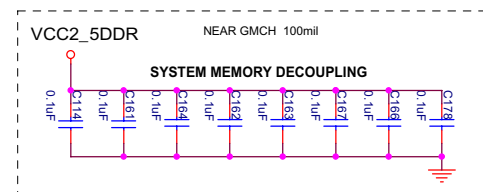
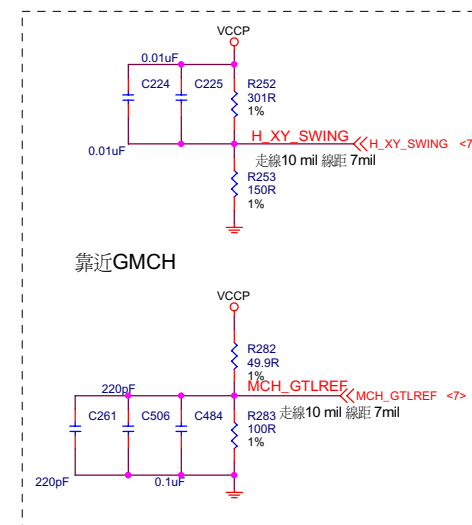
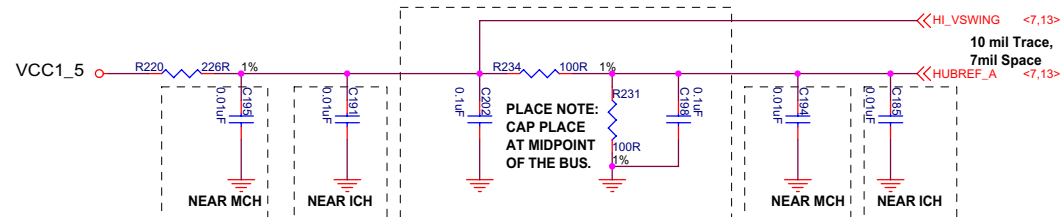
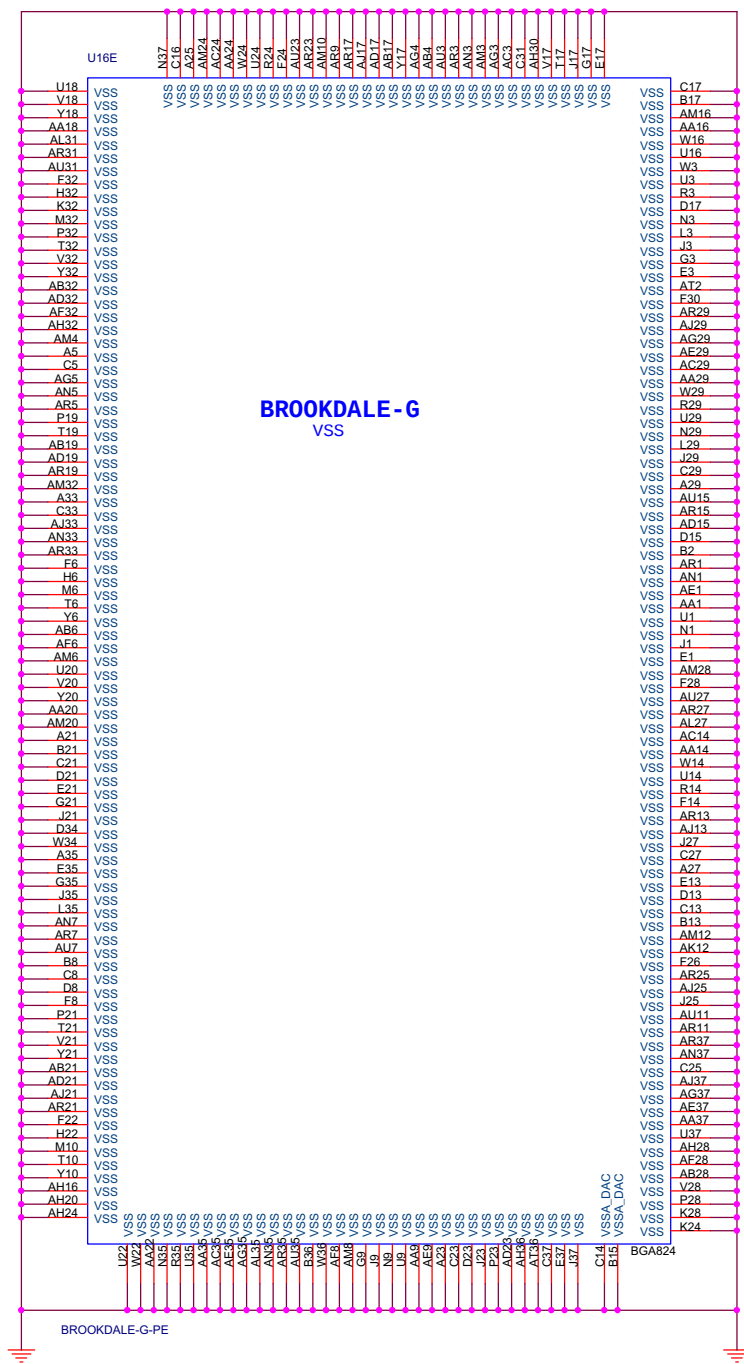
6

of

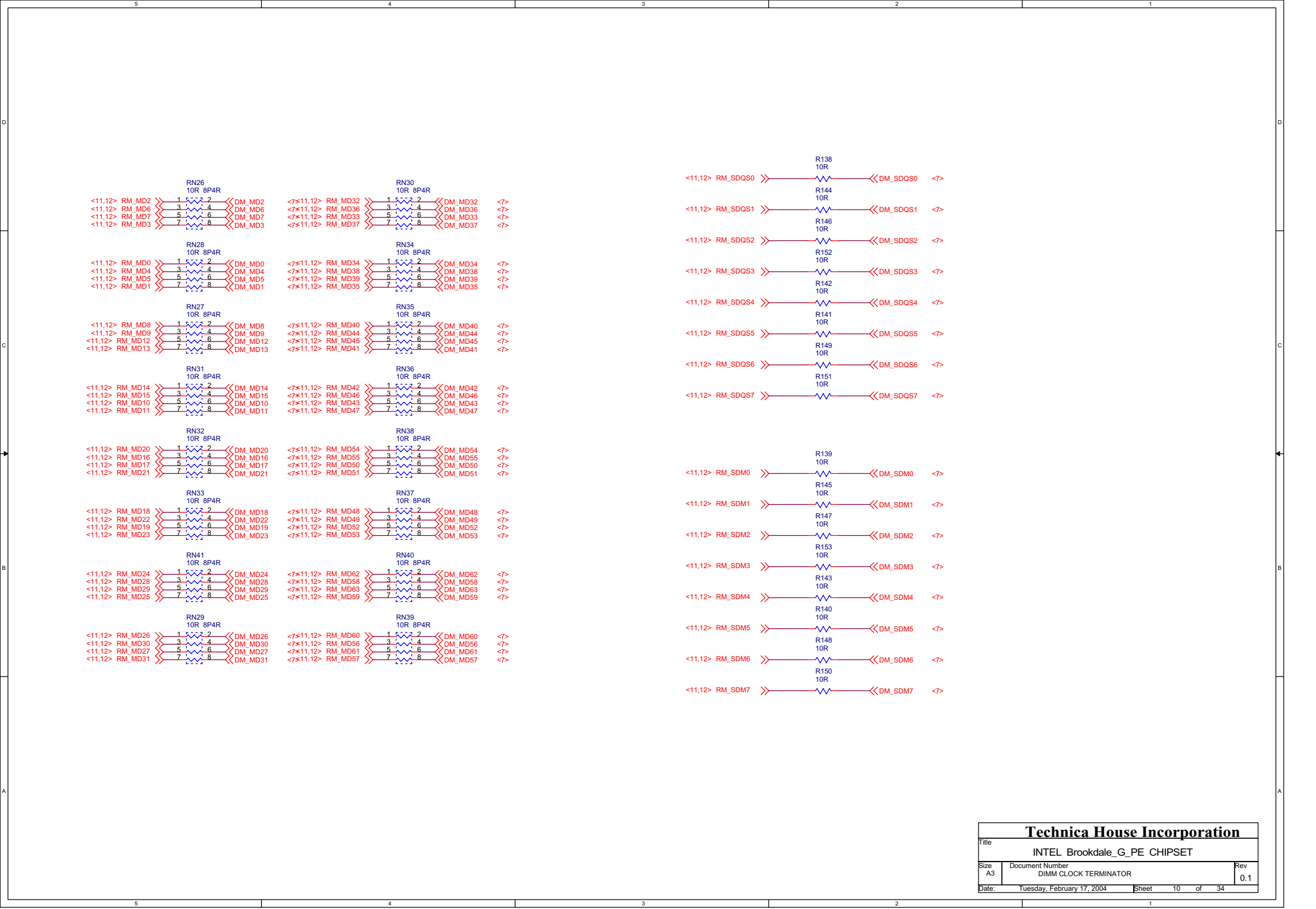
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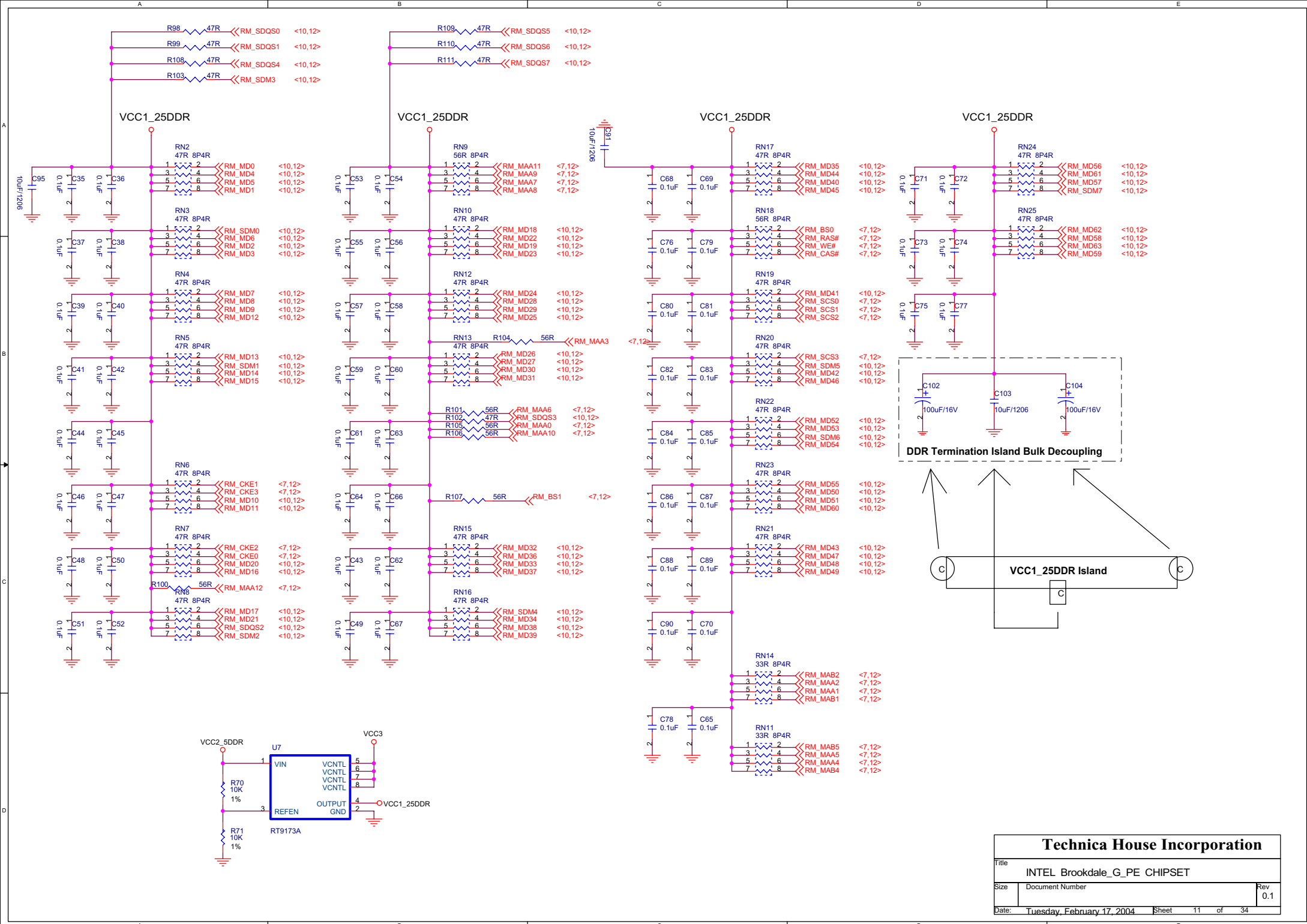


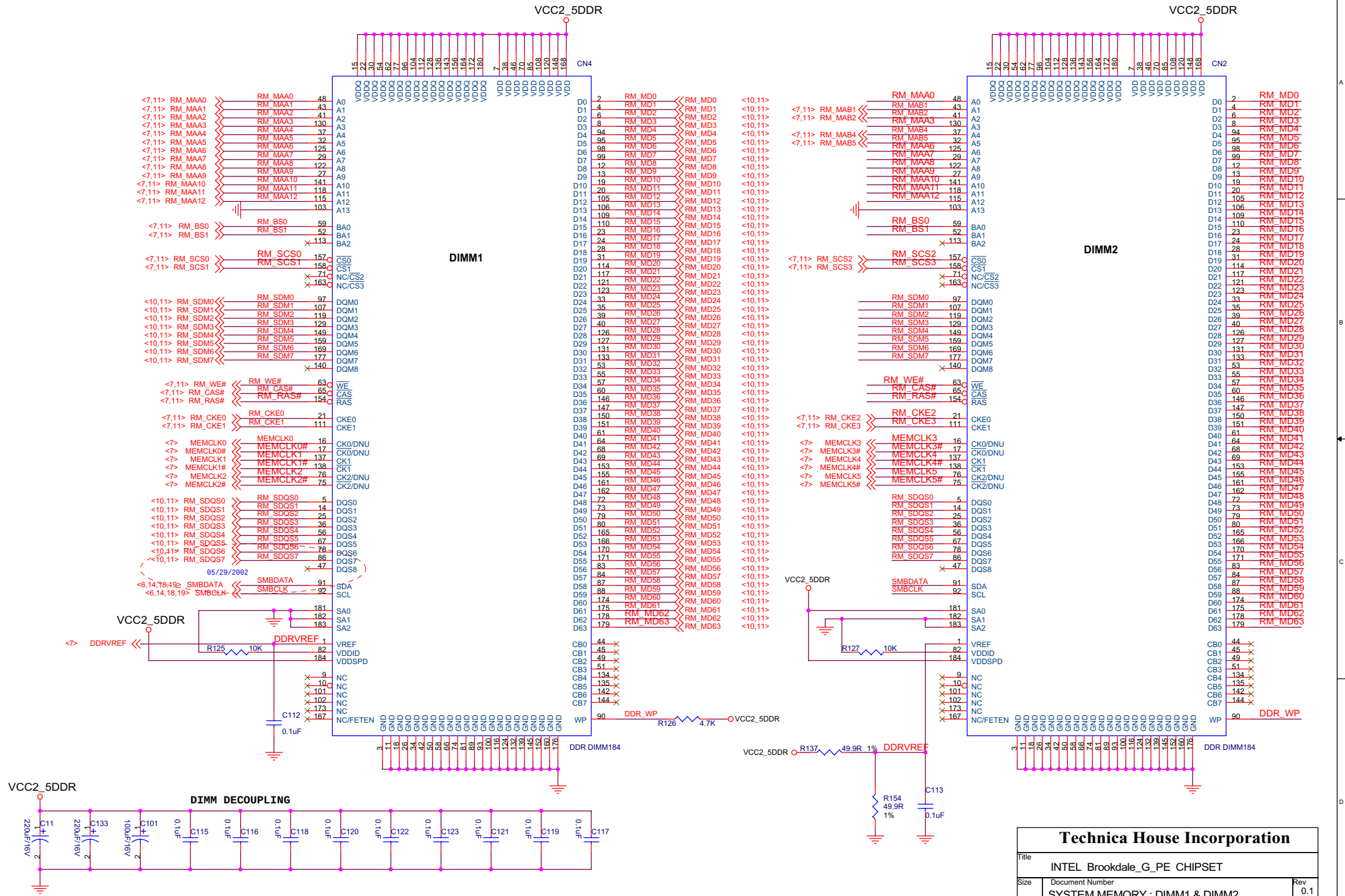




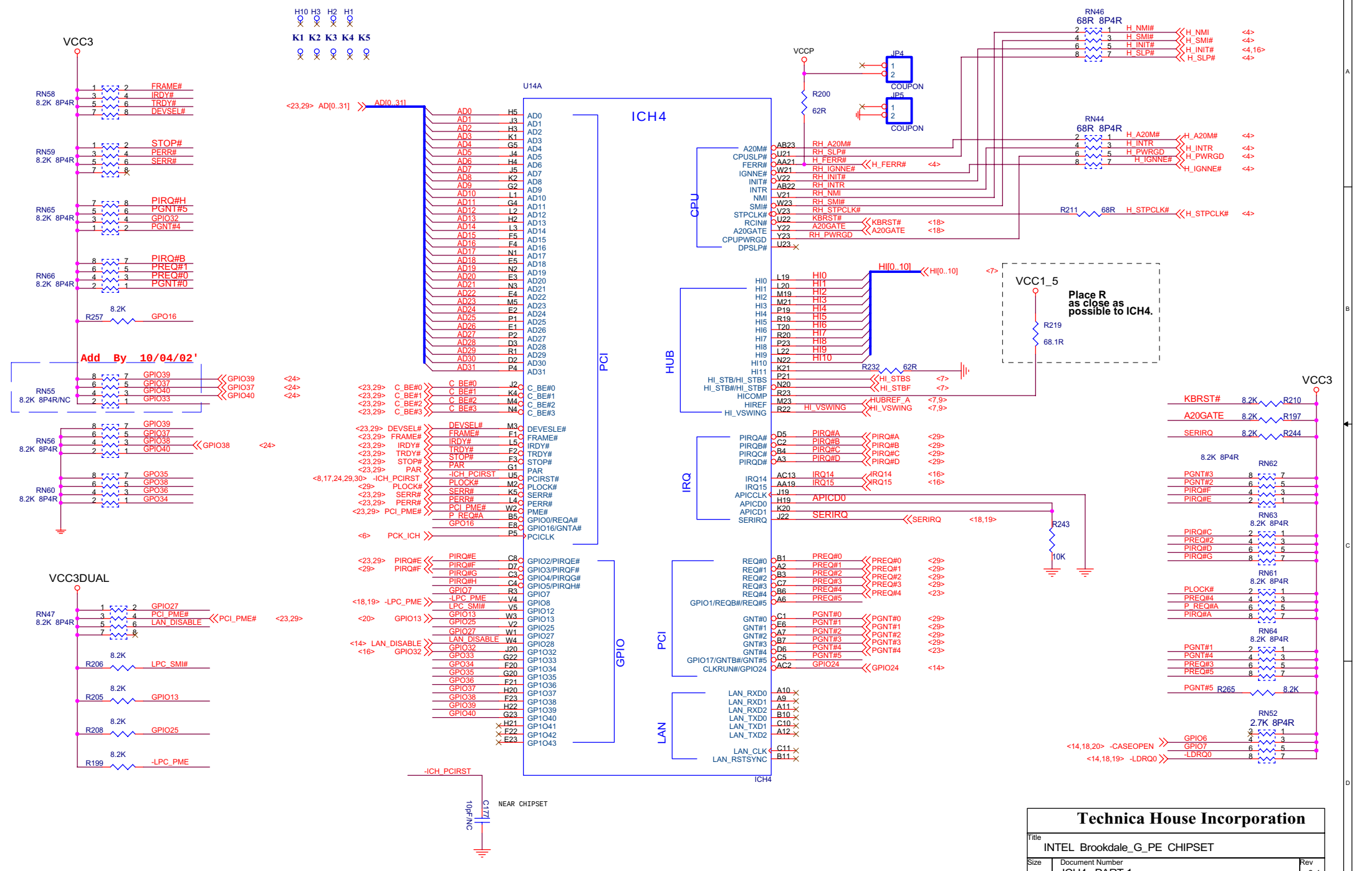
Technica House Incorporation		
Title INTEL Brookdale_G_PE CHIPSET		
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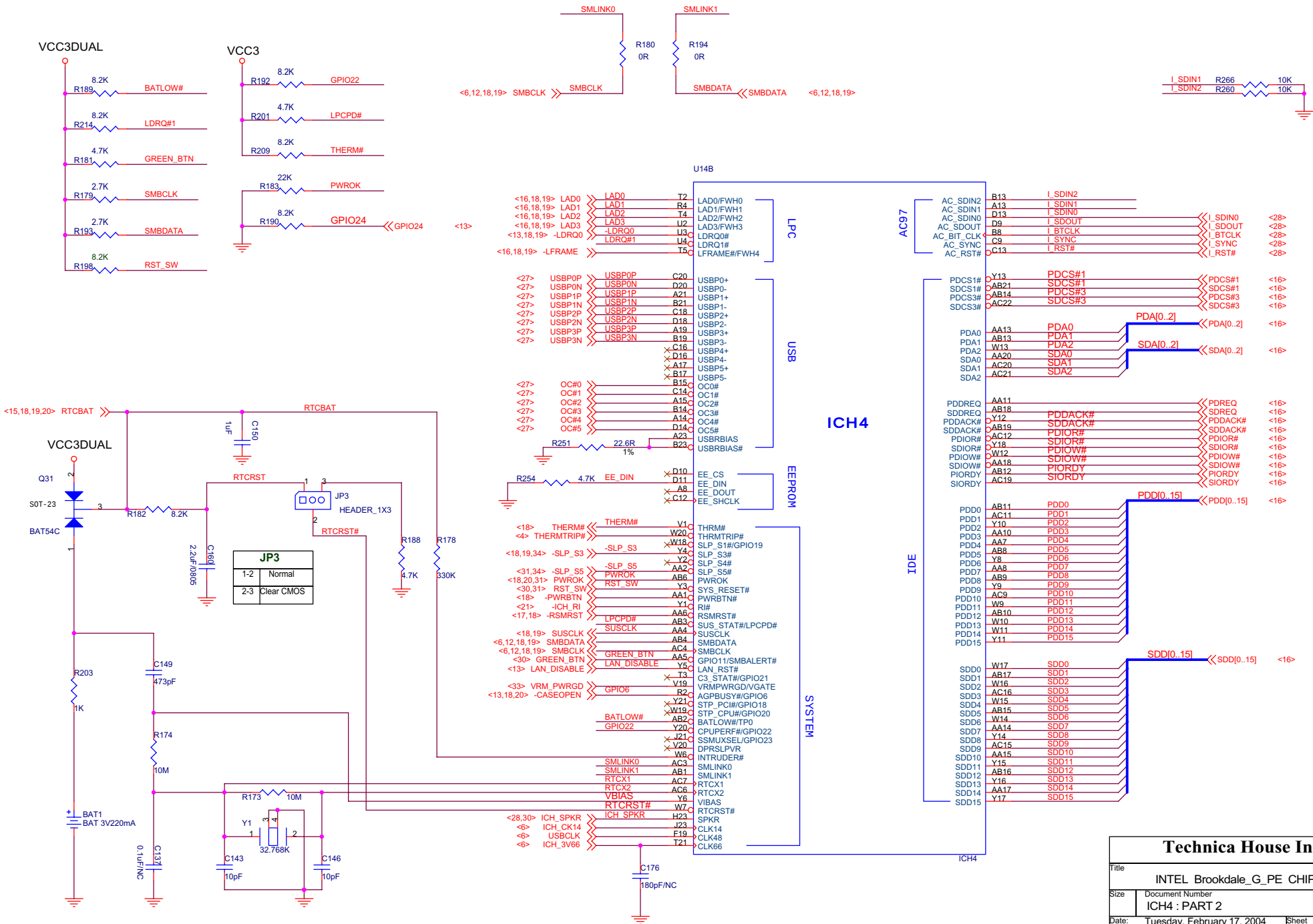




ICH4 PART1



ICH4 PART2



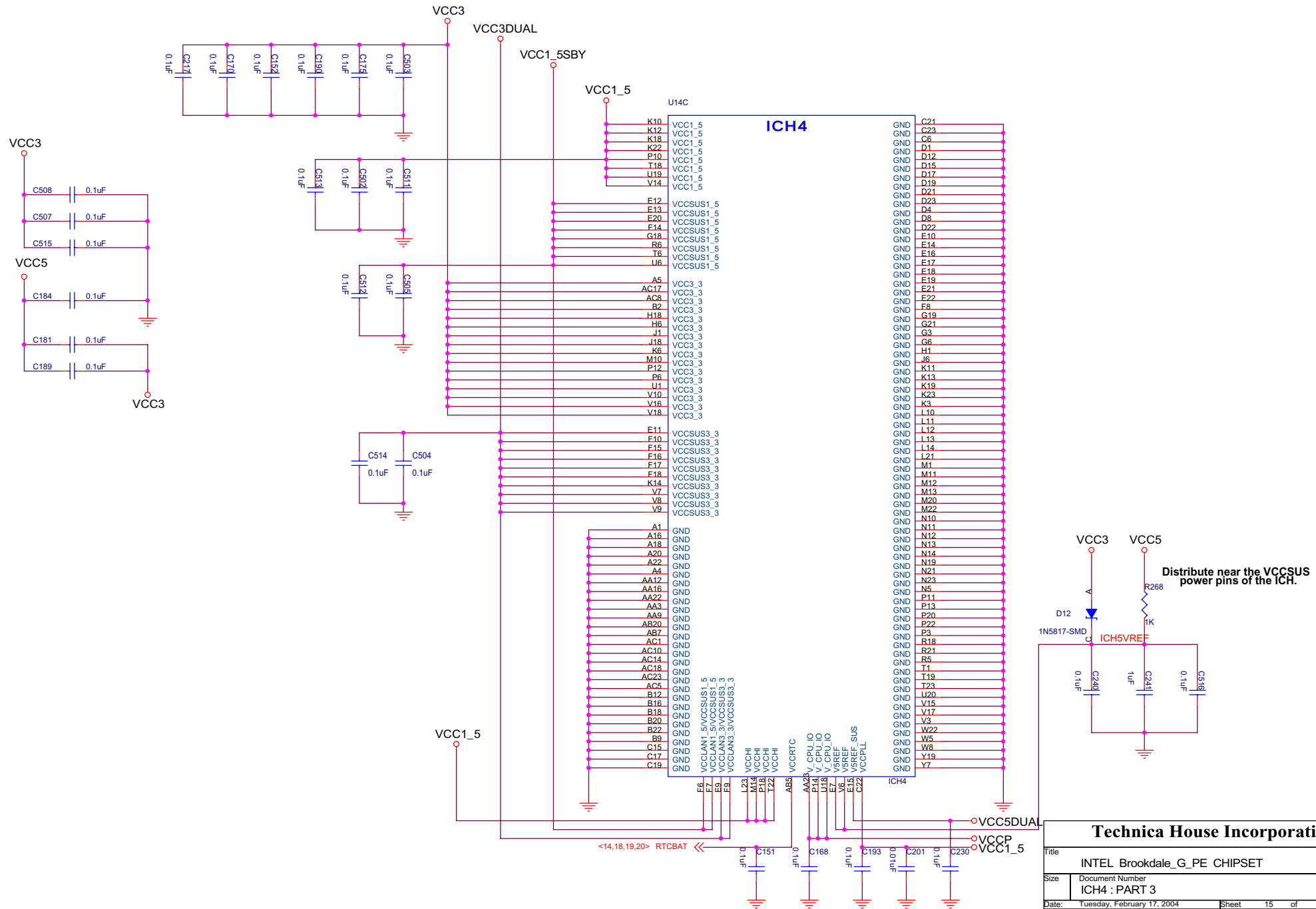
Technica House Incorporation

Title	INTEL Brookdale_G_PE CHIPSET
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Size	Document Number	Rev
	ICH4 : PART 2	0.1

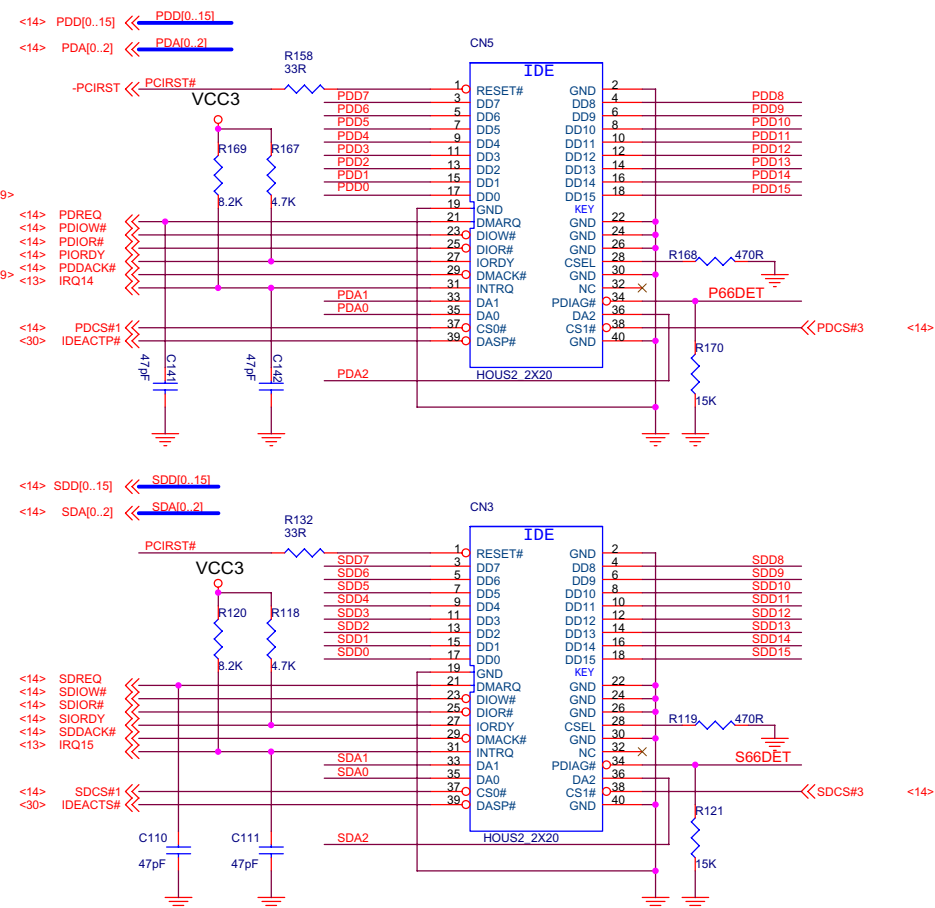
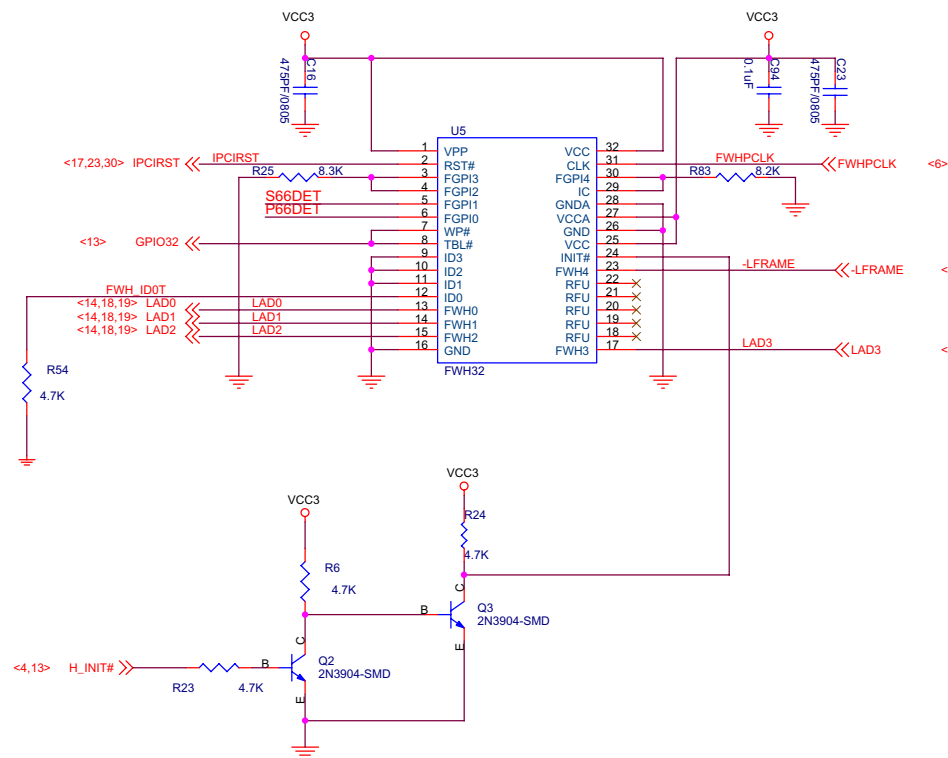
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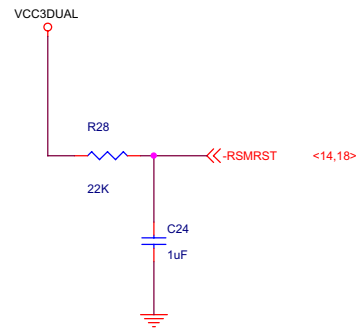
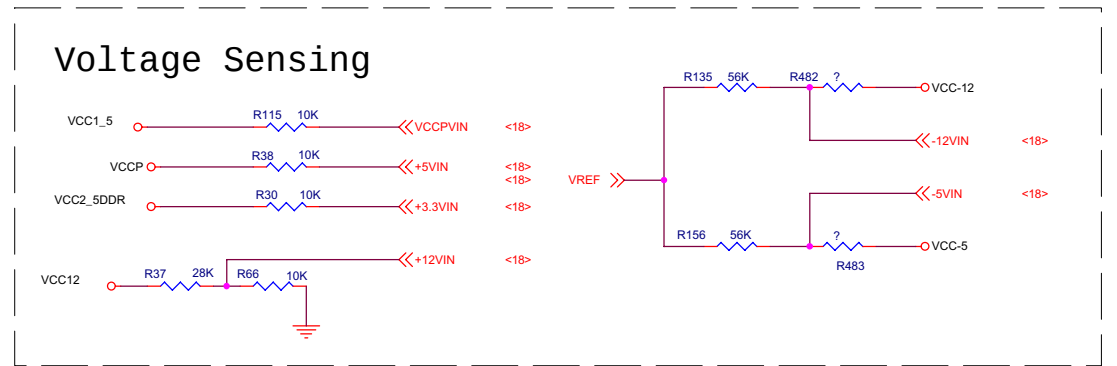
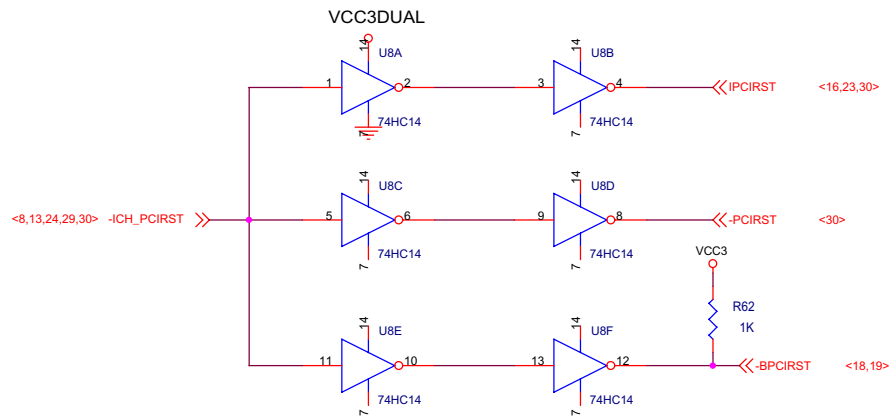
ICH4 PART3



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Title		
INTEL Brookdale_G_PE CHIPSET		
Size	Document Number	Rev
	ICH4 : PART 3	0.1
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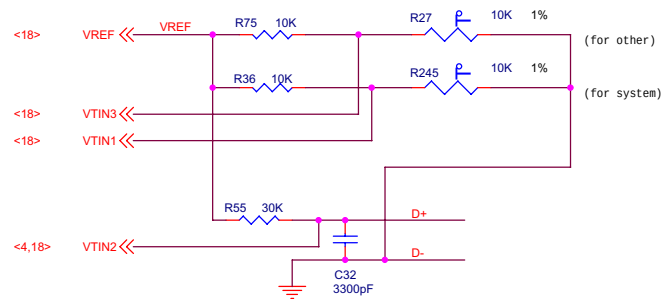
FirmWare Hub (FWH) Socket





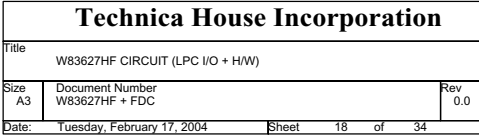
Hardware Monitor circuits

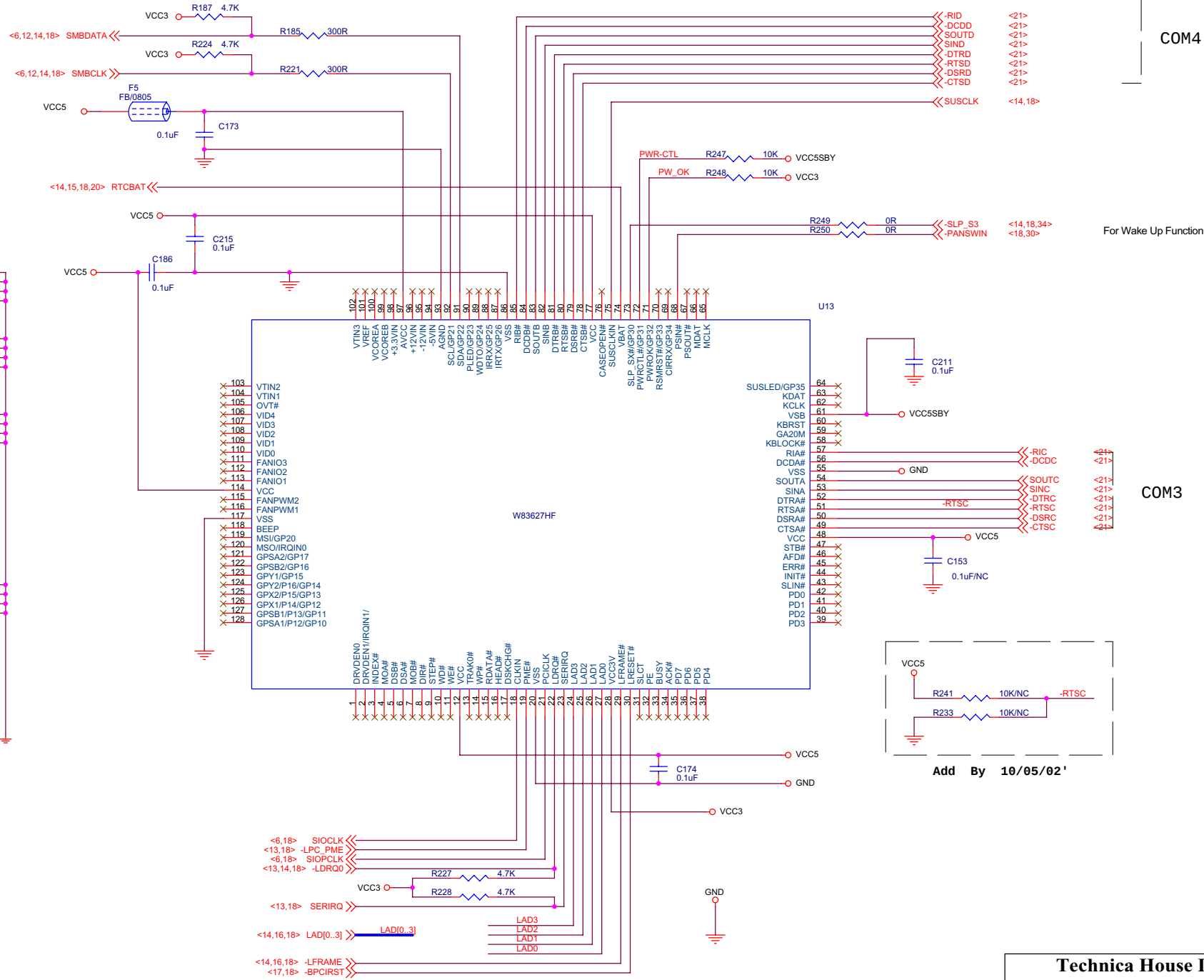
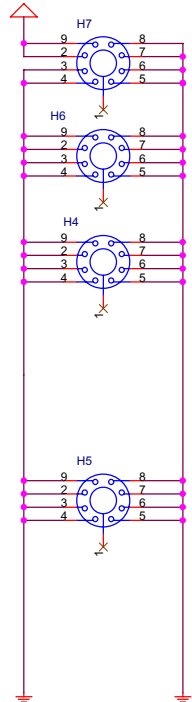
Temperature Sensing



Technica House Incorporation

Title			THERMISTOR, SMART CARD READER	
Size	A3	Document Number	ITTM-CG-99008	Rev
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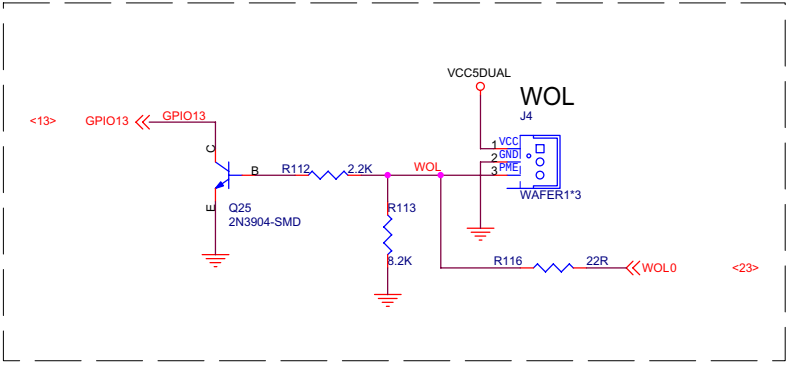
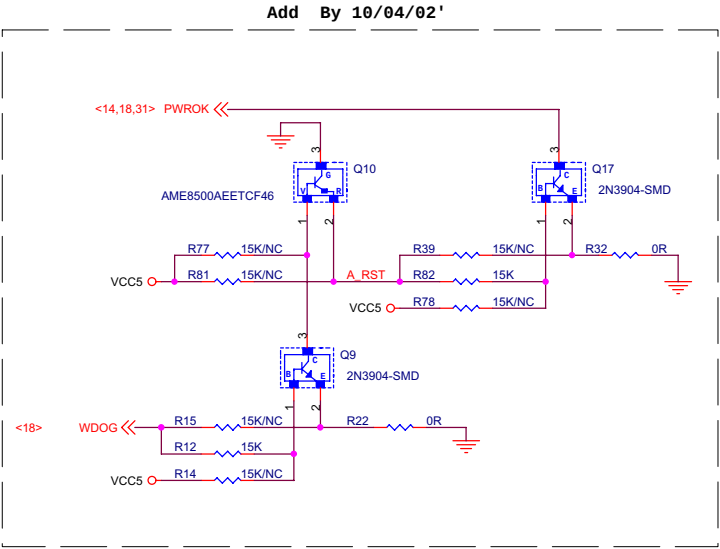
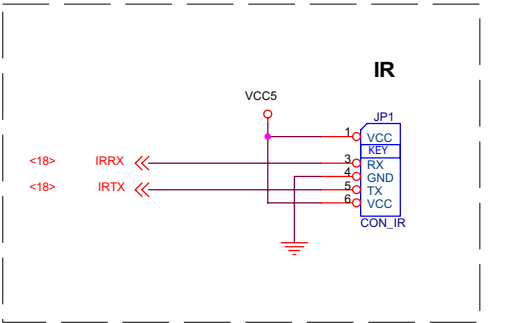
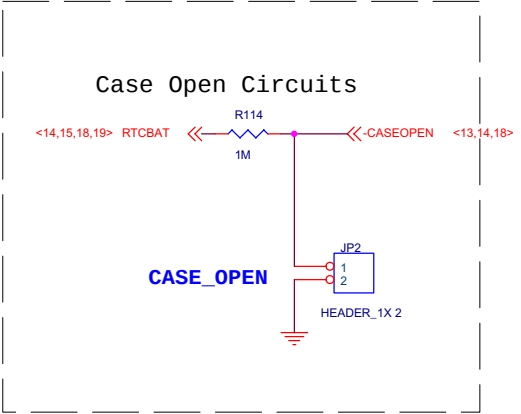
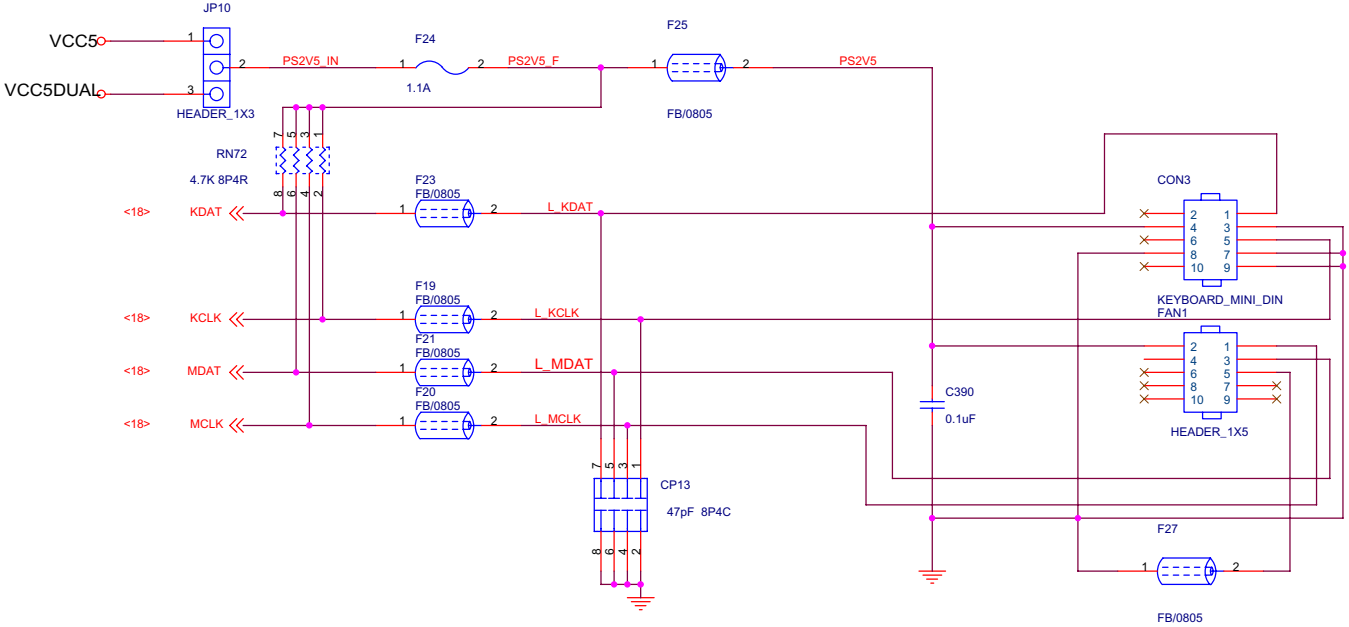




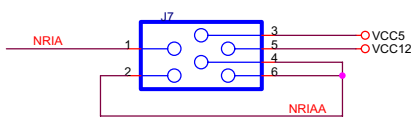
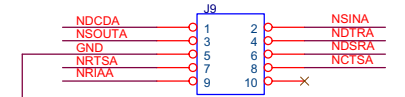
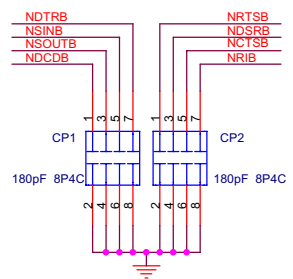
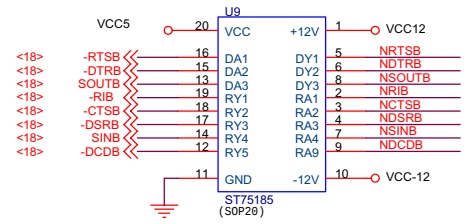
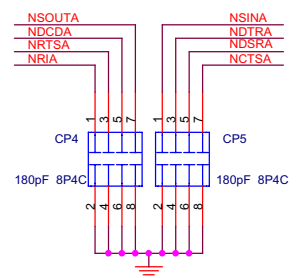
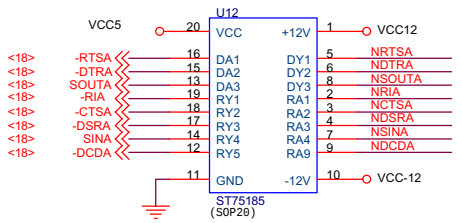
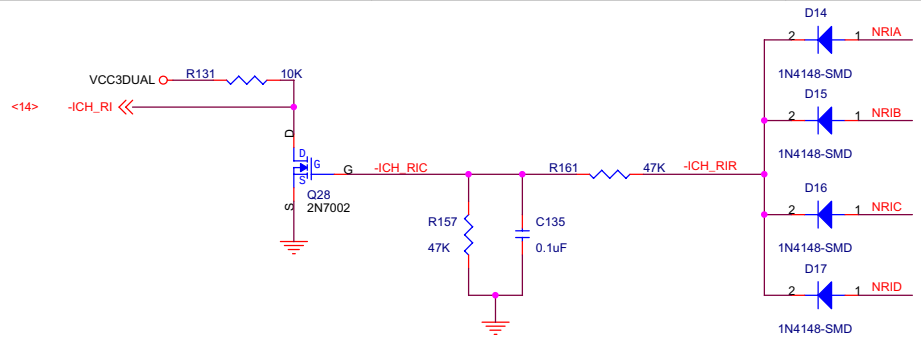
Technica House Incorporation

Title		W83627HF CIRCUIT (LPC I/O + H/W)
Size	Document Number	Rev
A3	W83627HF + FDC	0.0
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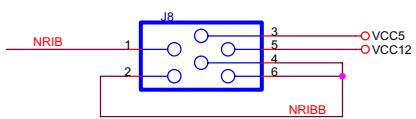
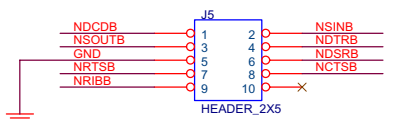
Serial Port/COM Headers



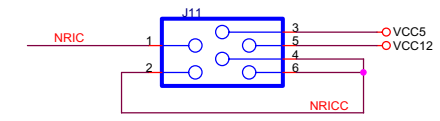
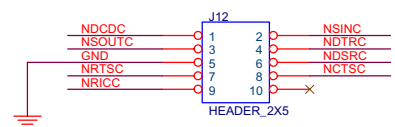
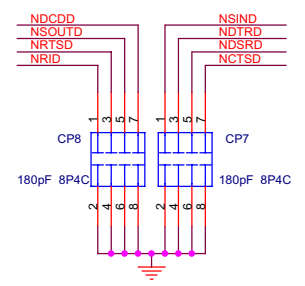
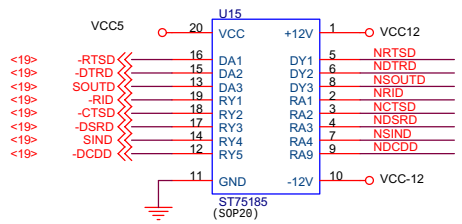
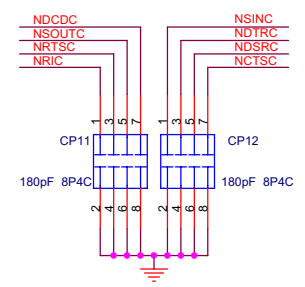
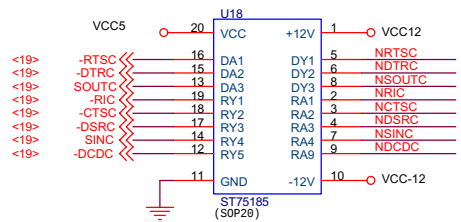
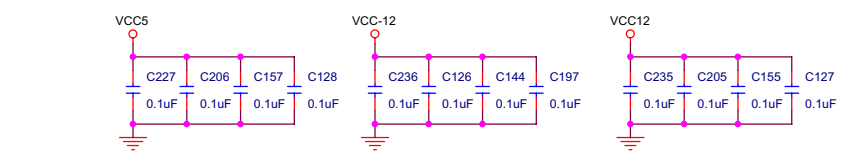
Technica House Incorporation			
Title INTEL Brookdale-G CHIPSET			
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SERIAL PORT/COM/IR/CIR HEADER		0.0	
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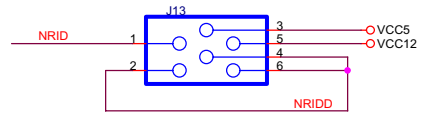
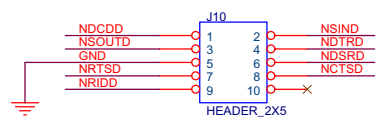
JUMPER SEL
 1-2 NORM
 3-4 SEL +5V
 5-6 SEL+12V



JUMPER SEL
 1-2 NORM
 3-4 SEL +5V
 5-6 SEL+12V



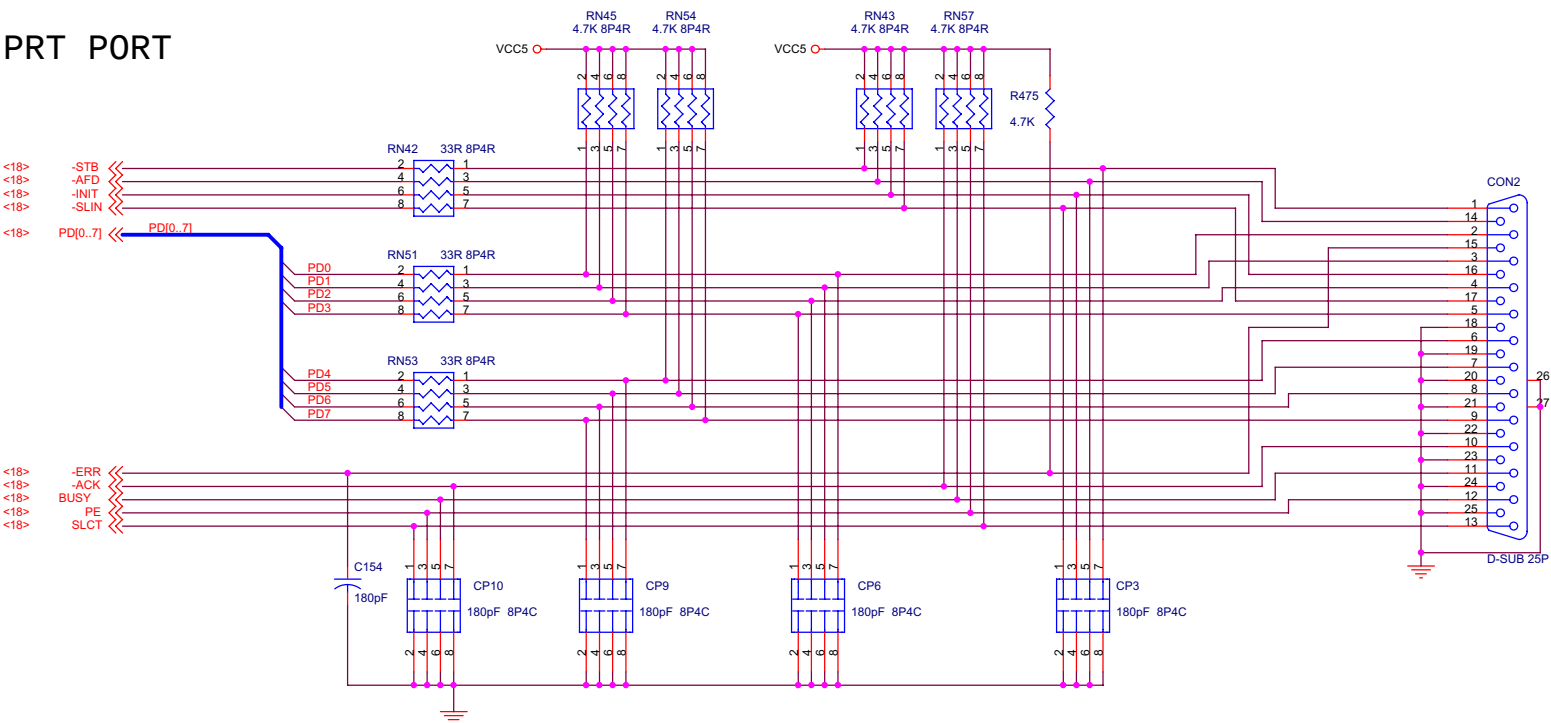
JUMPER SEL
 1-2 NORM
 3-4 SEL +5V
 5-6 SEL+12V



JUMPER SEL
 1-2 NORM
 3-4 SEL +5V
 5-6 SEL+12V

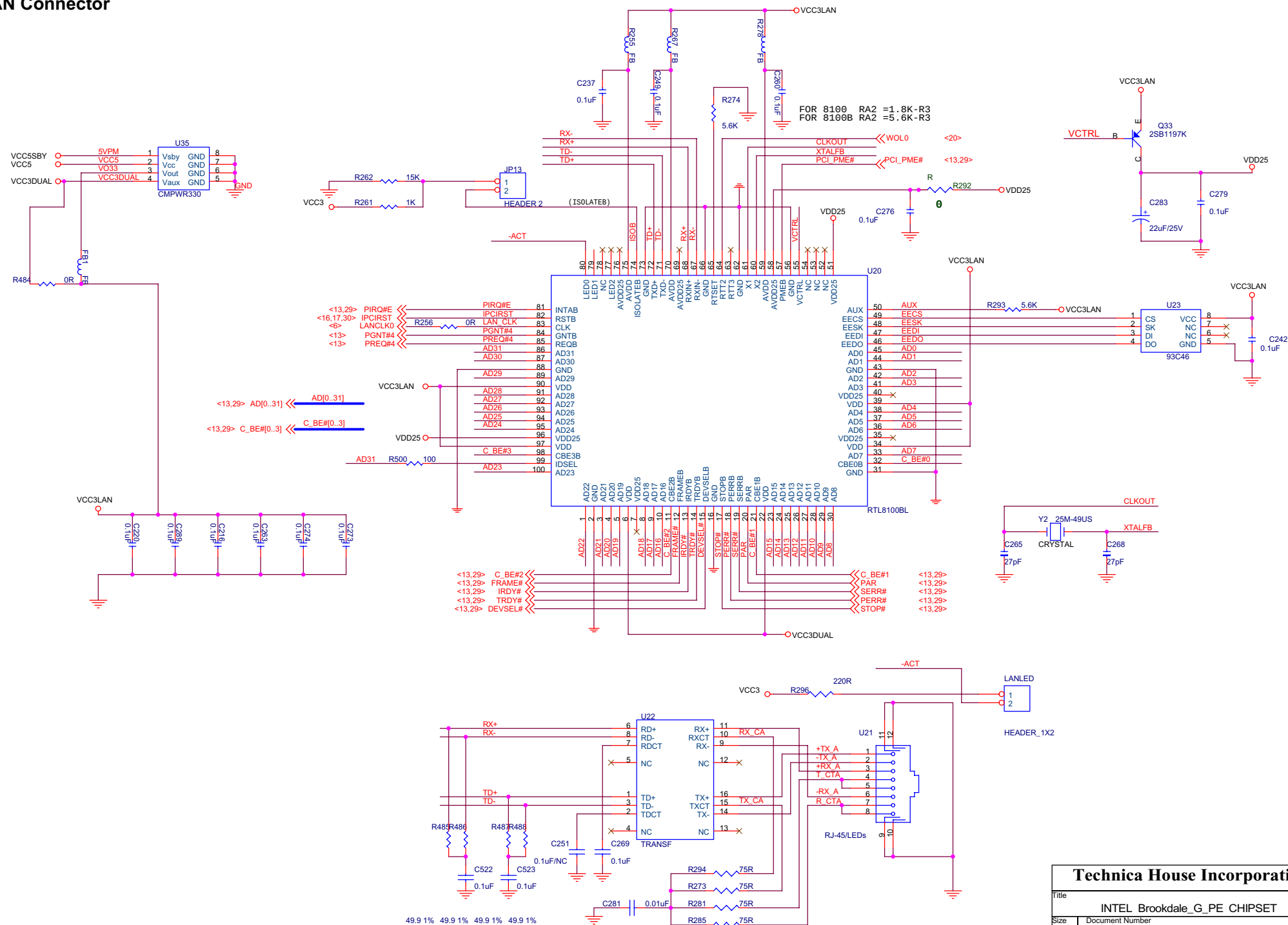
Parallel Port Header

PRT PORT



Technica House Incorporation			
Title			
INTEL Brookdale-G CHIPSET			
Size	Document Number	Rev	
	PARALLEL PORT / GAME PORT	0.0	
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LAN Connector

**Technica House Incorporation**

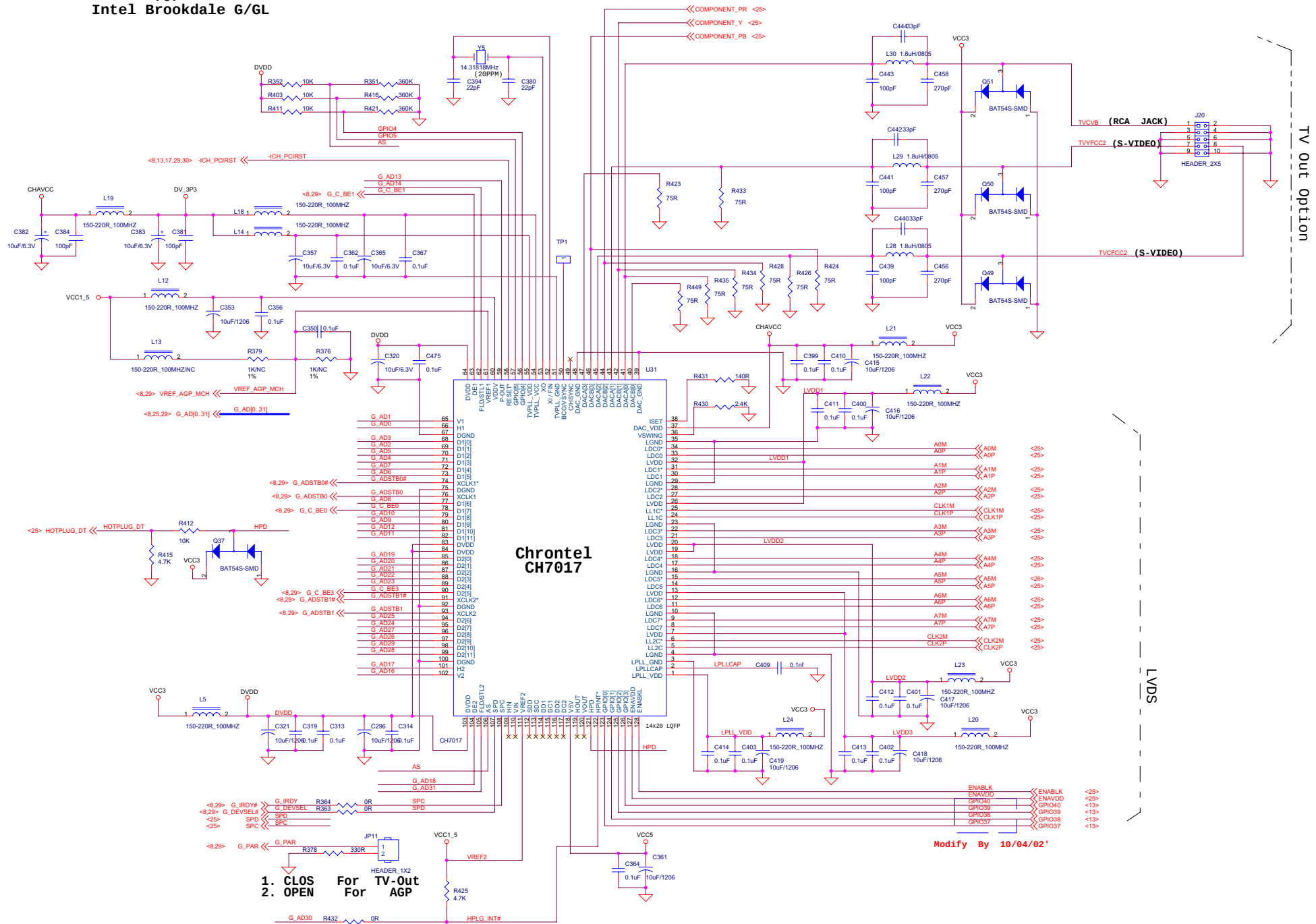
Title	INTEL Brookdale_G_PE CHIPSET
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Size	Document Number
	LAN CONNECTORS

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Preliminary Chronitel CH7017 reference design
for
Intel Brookdale G/GL



This Schematic is CHRONTEL Confidential and issue under NDA only

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Note:
Trace for LVDS signals should be closely-coupled and layout for 100 ohm differential impedance:
LVDS signals pairs : (A0x thru A7x , CLK1x and CLK2x)-

+3.3V Voltage Regulator circuit for CH7017's DAC_VDD and TVPLL

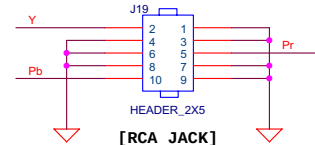
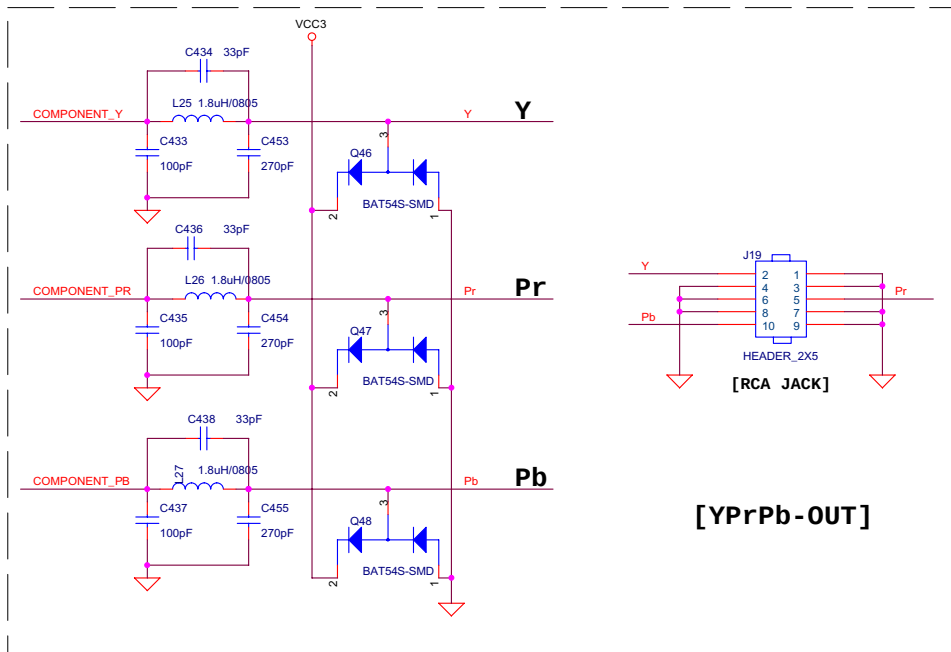
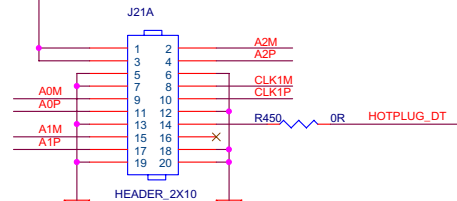
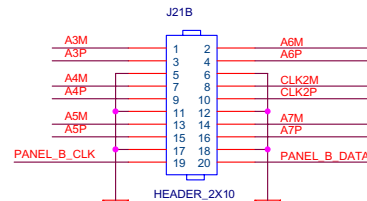
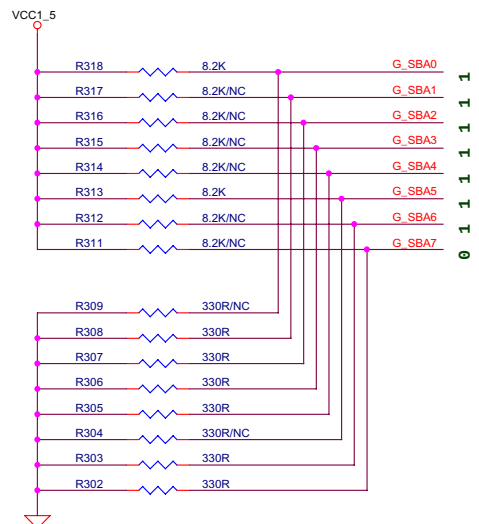
[LVDS Connector]

<24> HOTPLUG_DT >> HOTPLUG_DT
<24> A0M >> A0M
<24> A0P >> A0P
<24> A1M >> A1M
<24> A1P >> A1P
<24> A2M >> A2M
<24> A2P >> A2P
<24> CLK1M >> CLK1M
<24> CLK1P >> CLK1P
<24> A3M >> A3M
<24> A3P >> A3P
<24> A4M >> A4M
<24> A4P >> A4P
<24> A5M >> A5M
<24> A5P >> A5P
<24> A6M >> A6M
<24> A6P >> A6P
<24> A7M >> A7M
<24> A7P >> A7P
<24> CLK2M >> CLK2M
<24> CLK2P >> CLK2P
<24> ENABLK >> ENABLK
<24> ENAVDD >> ENAVDD

<24> COMPONENT_Y >> COMPONENT_Y
<24> COMPONENT_PR >> COMPONENT_PR
<24> COMPONENT_PB >> COMPONENT_PB

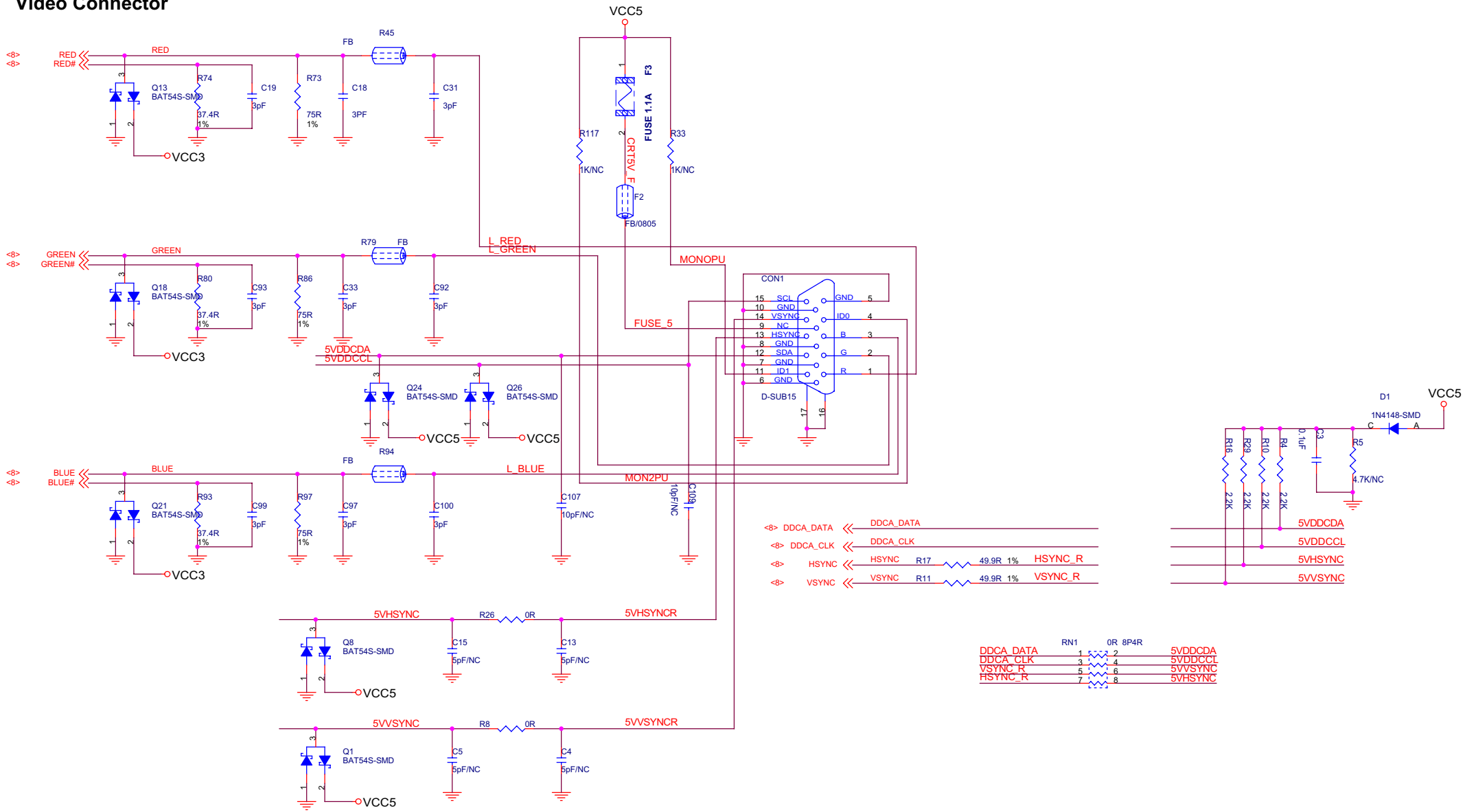
<8,29> G_SBA[0..7] >> G_SBA[0..7]

ADD ID Selector
It will be provided by
Intel regarding resistor
stuffing option.

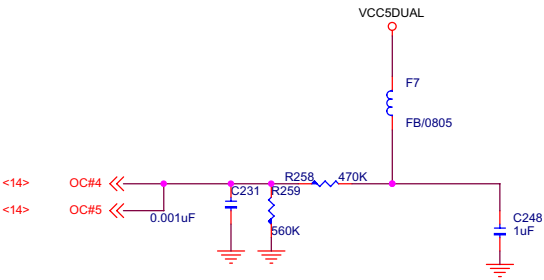
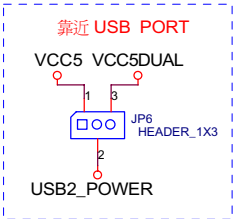
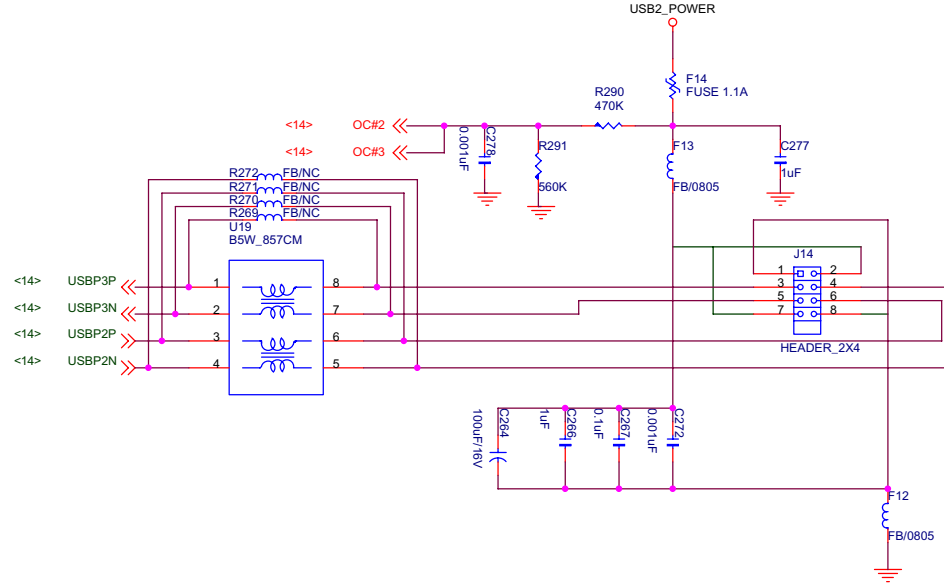
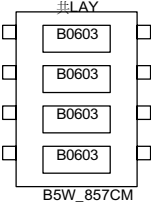
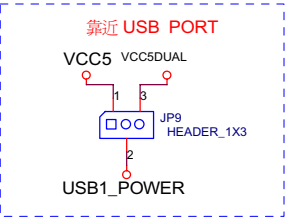
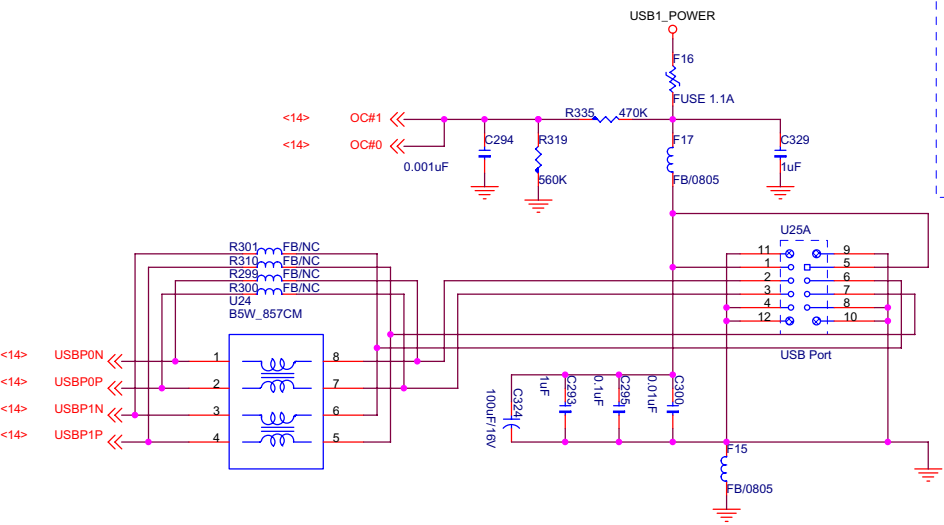


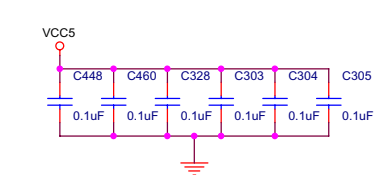
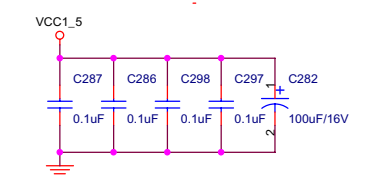
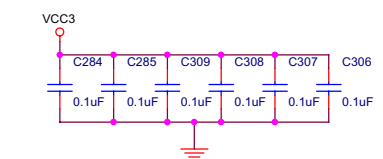
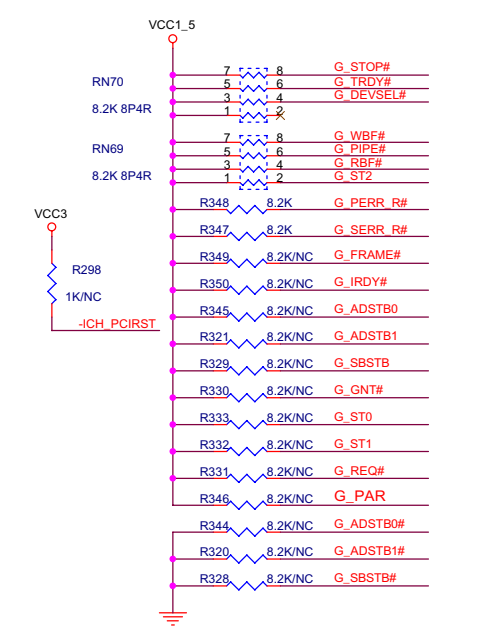
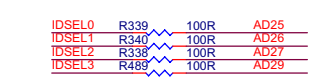
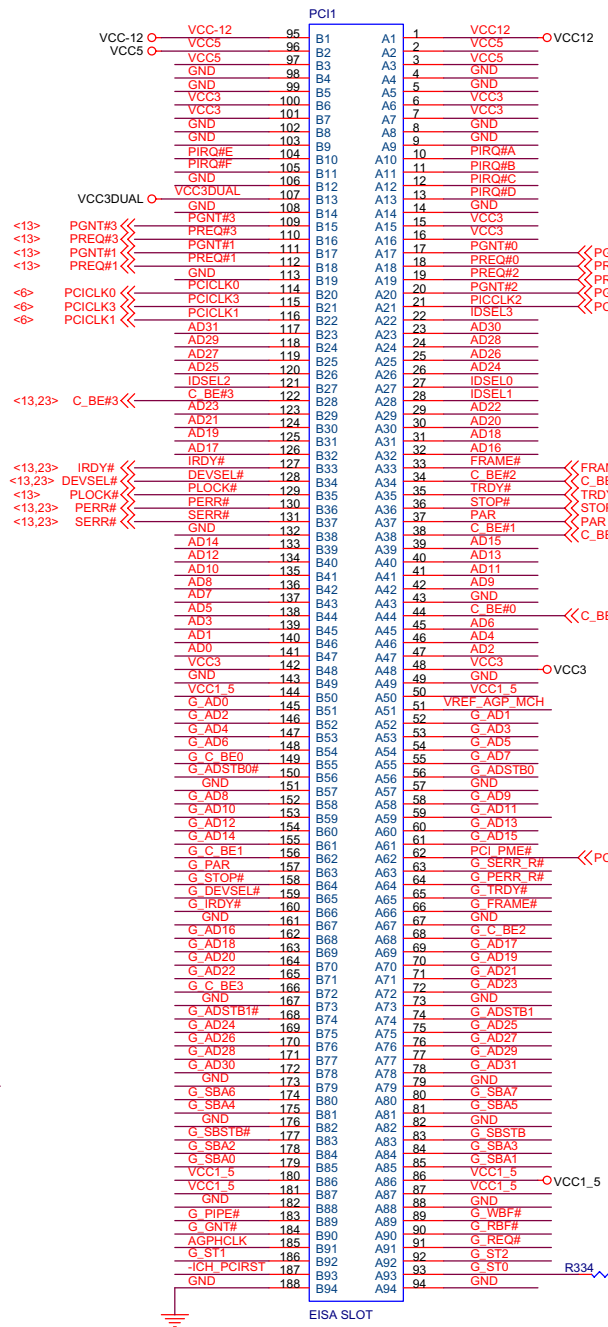
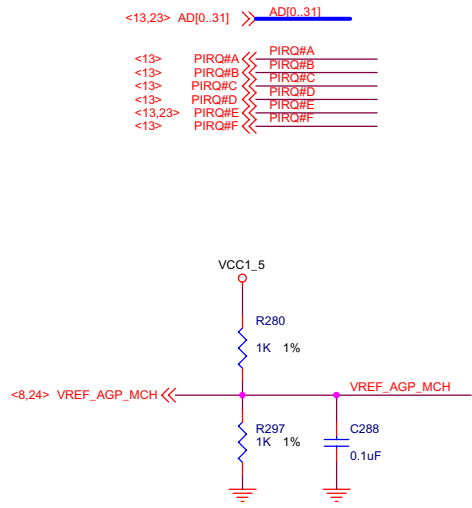
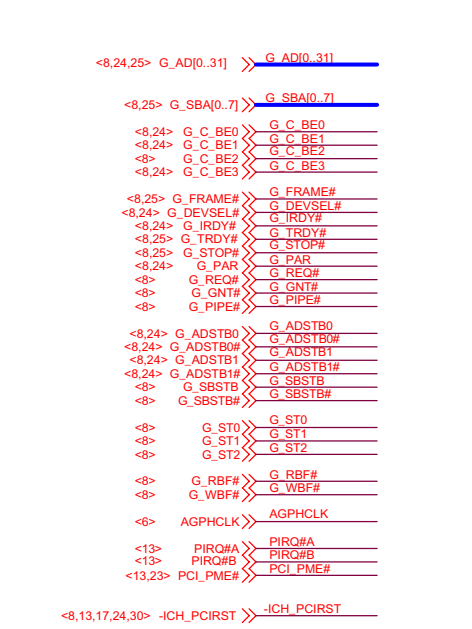
[YPrPb-OUT]

Video Connector



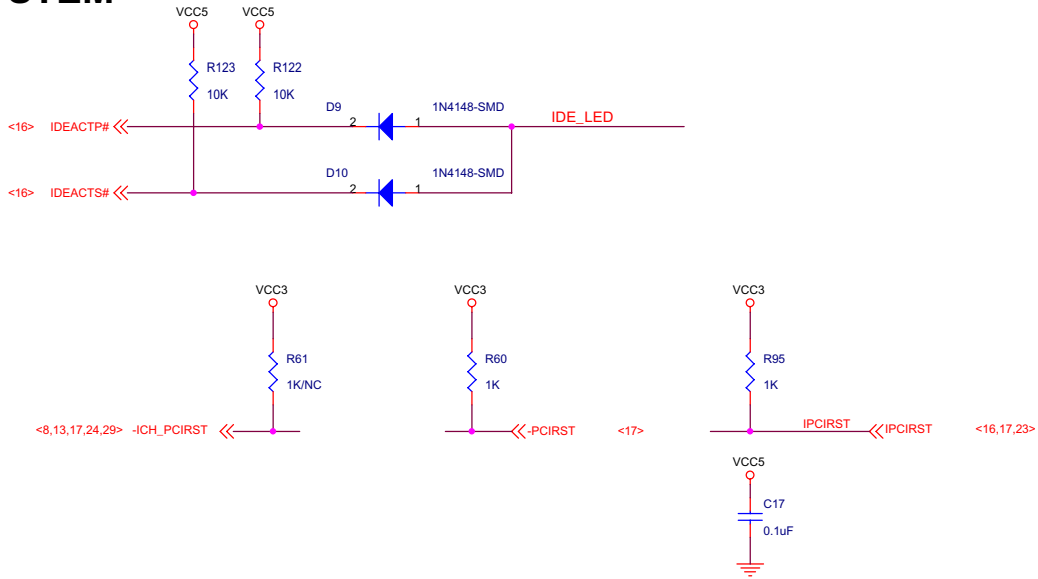
USB Connectors



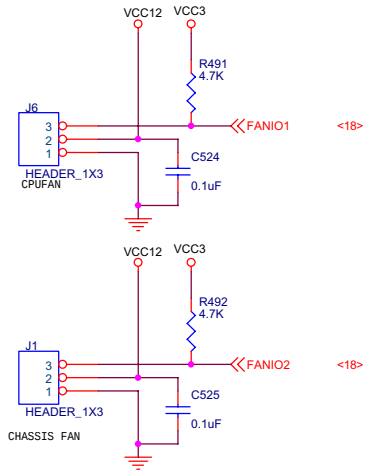


JET WAY INFORMATION			
Technica House Incorporation			
Title	PCI 1 & 2		
Size	Document Number	Rev	
Custom	610BS	A	
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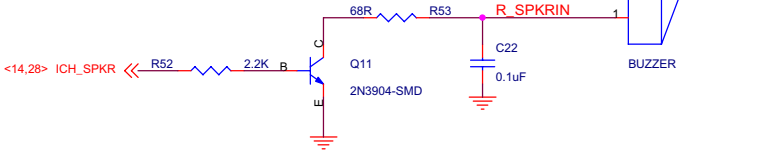
SYSTEM



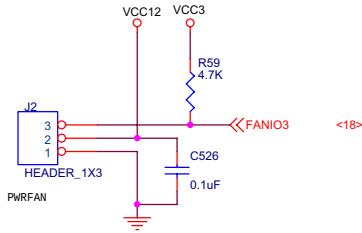
PWM Circuit for FAN speed control



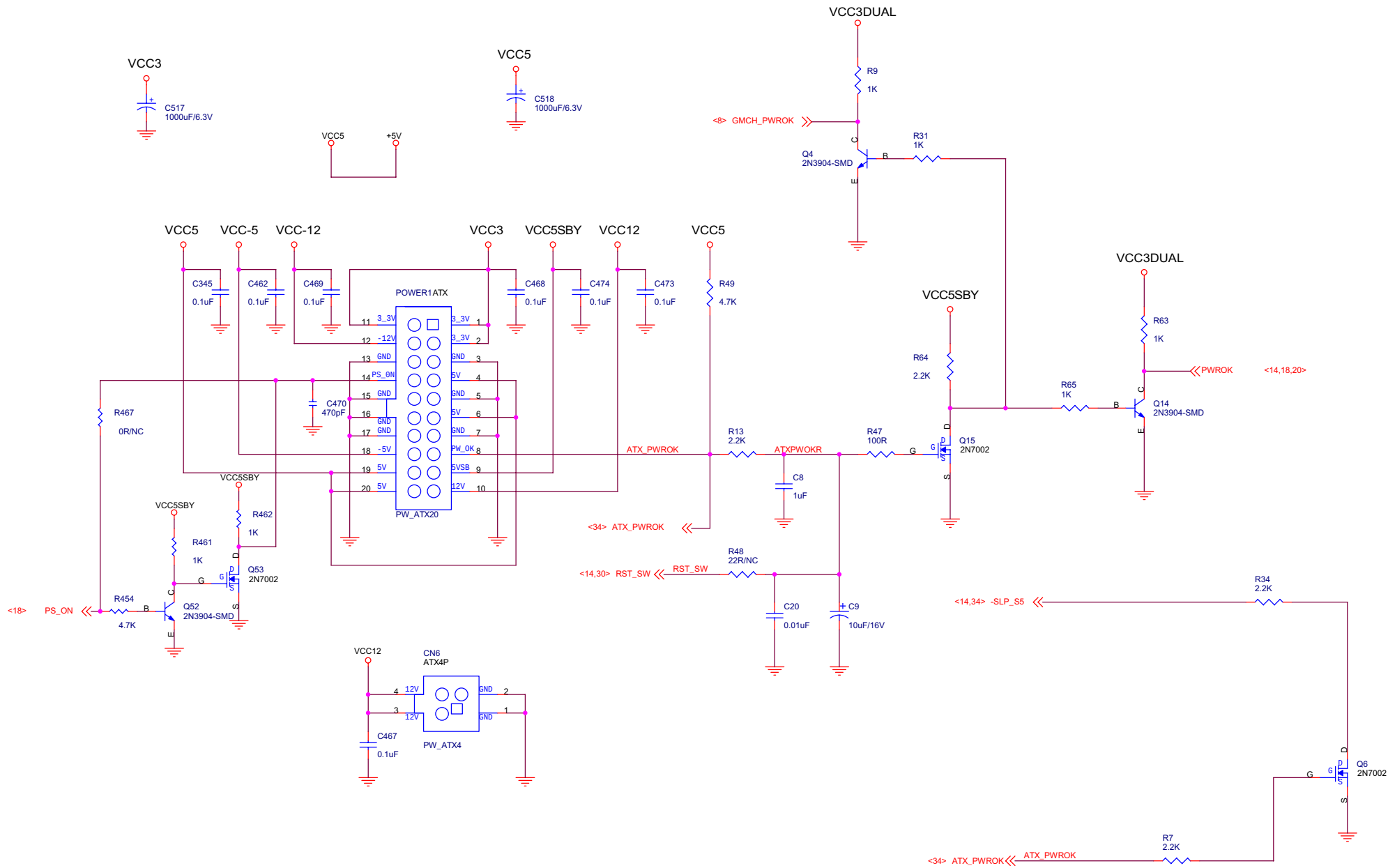
Speaker Circuit



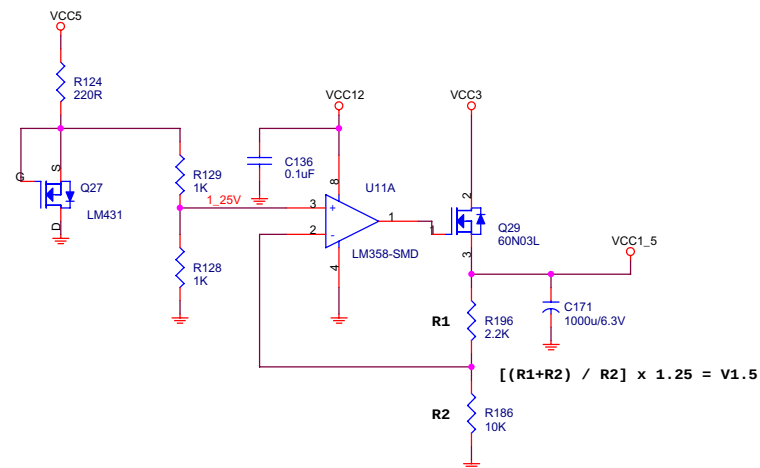
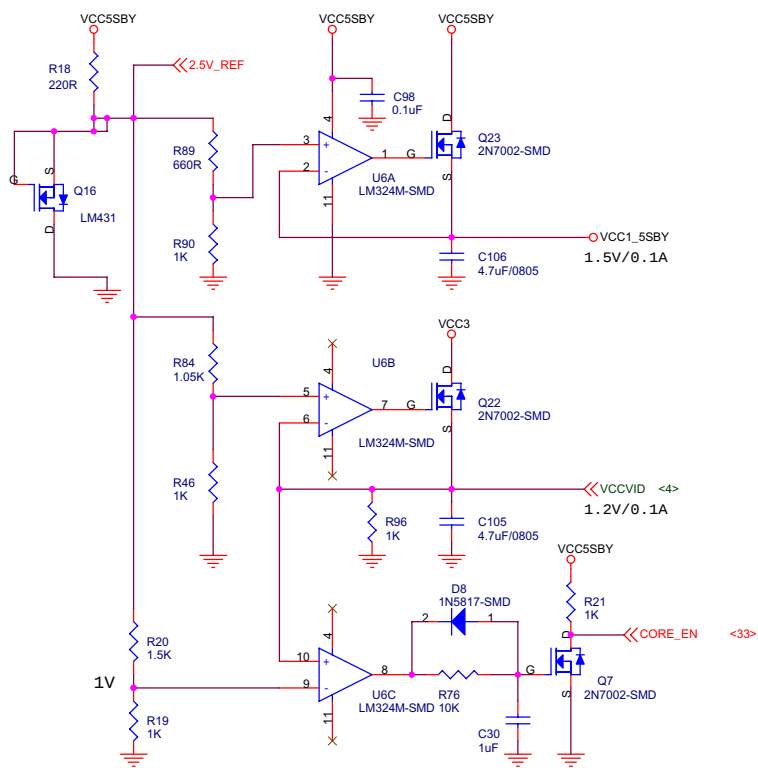
Fan Speed Input Circuit



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Voltage Regulators



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