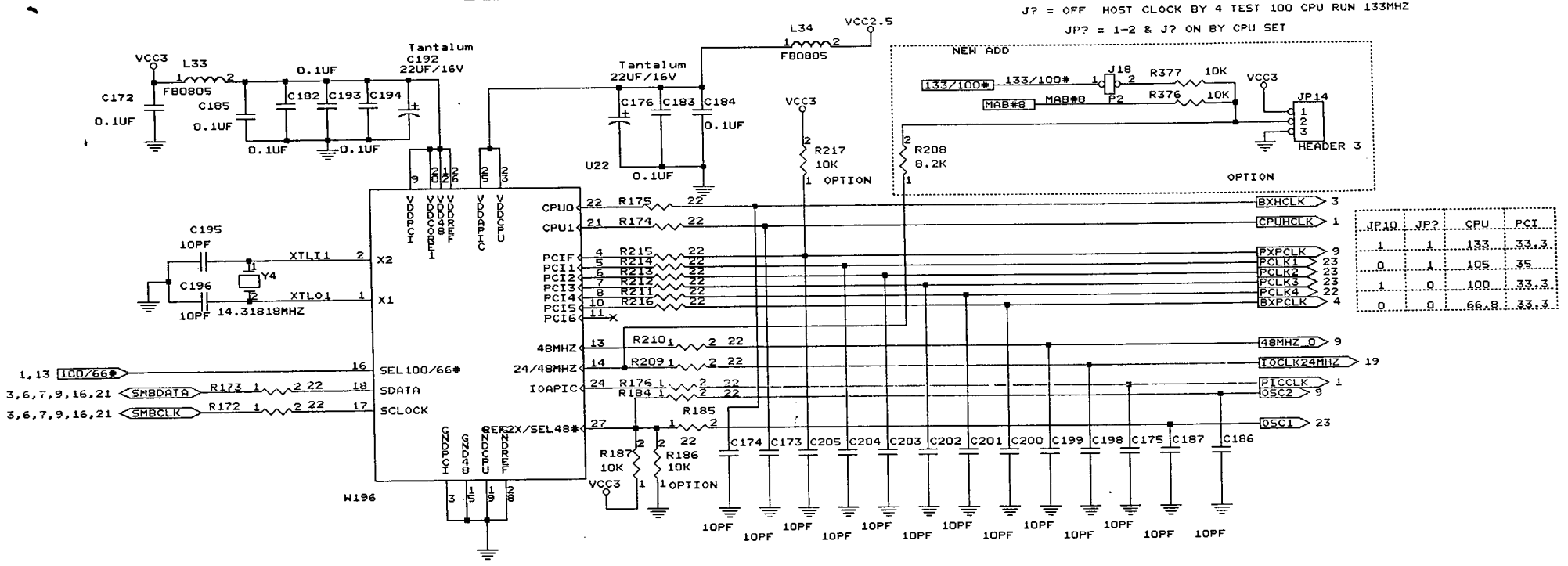
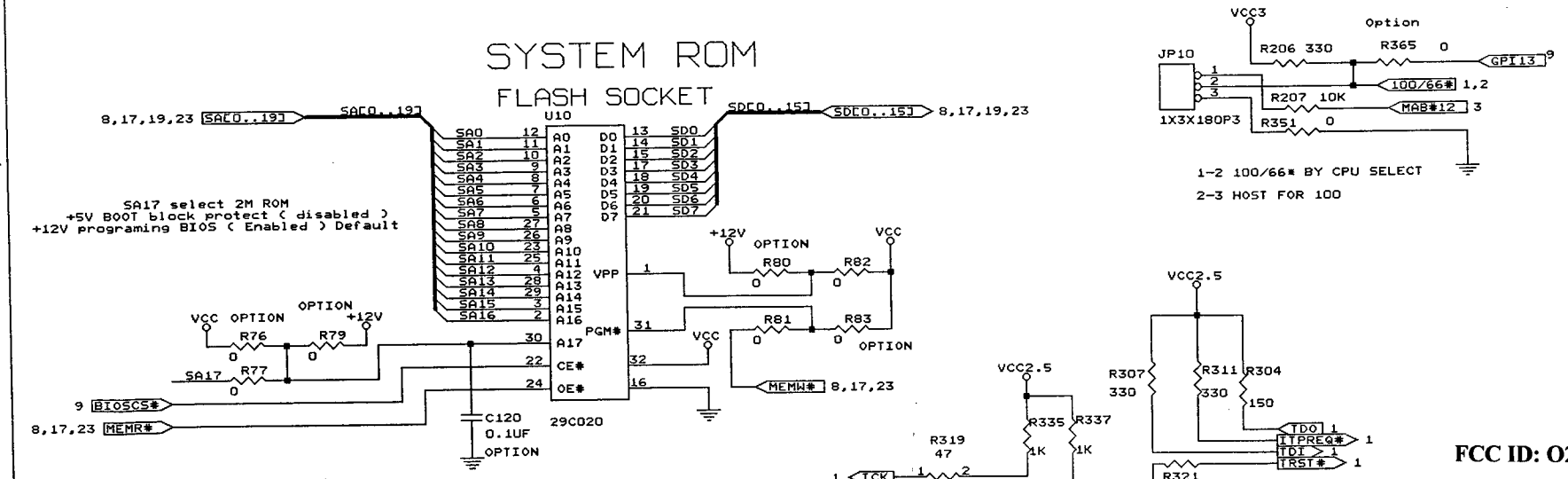
CLOCK SYNTHESIZER



JP10	JP?	CPU	PCI
1	1	133	33.3
0	1	105	35
1	0	100	33.3
0	0	66.8	33.3

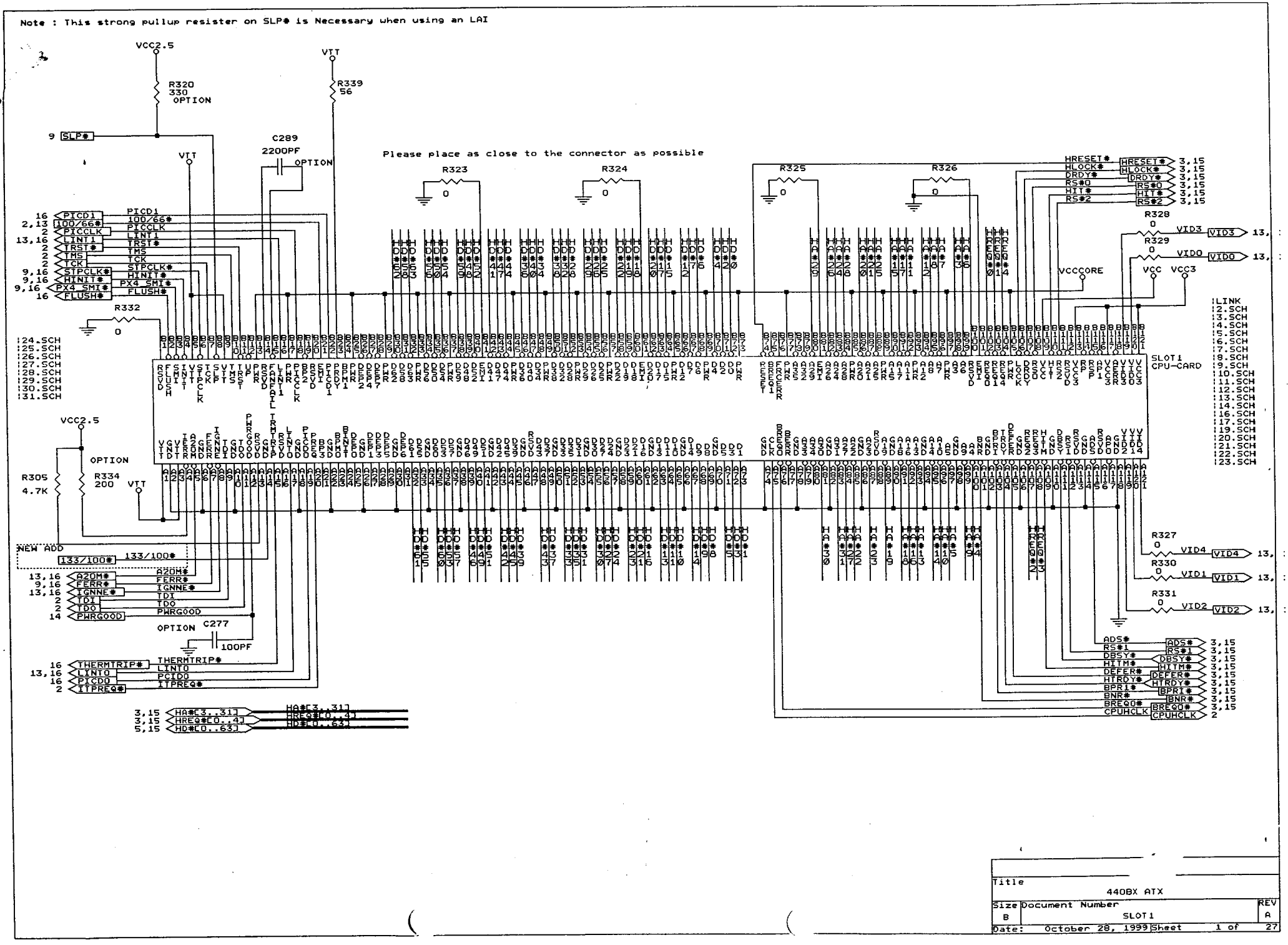
SYSTEM ROM

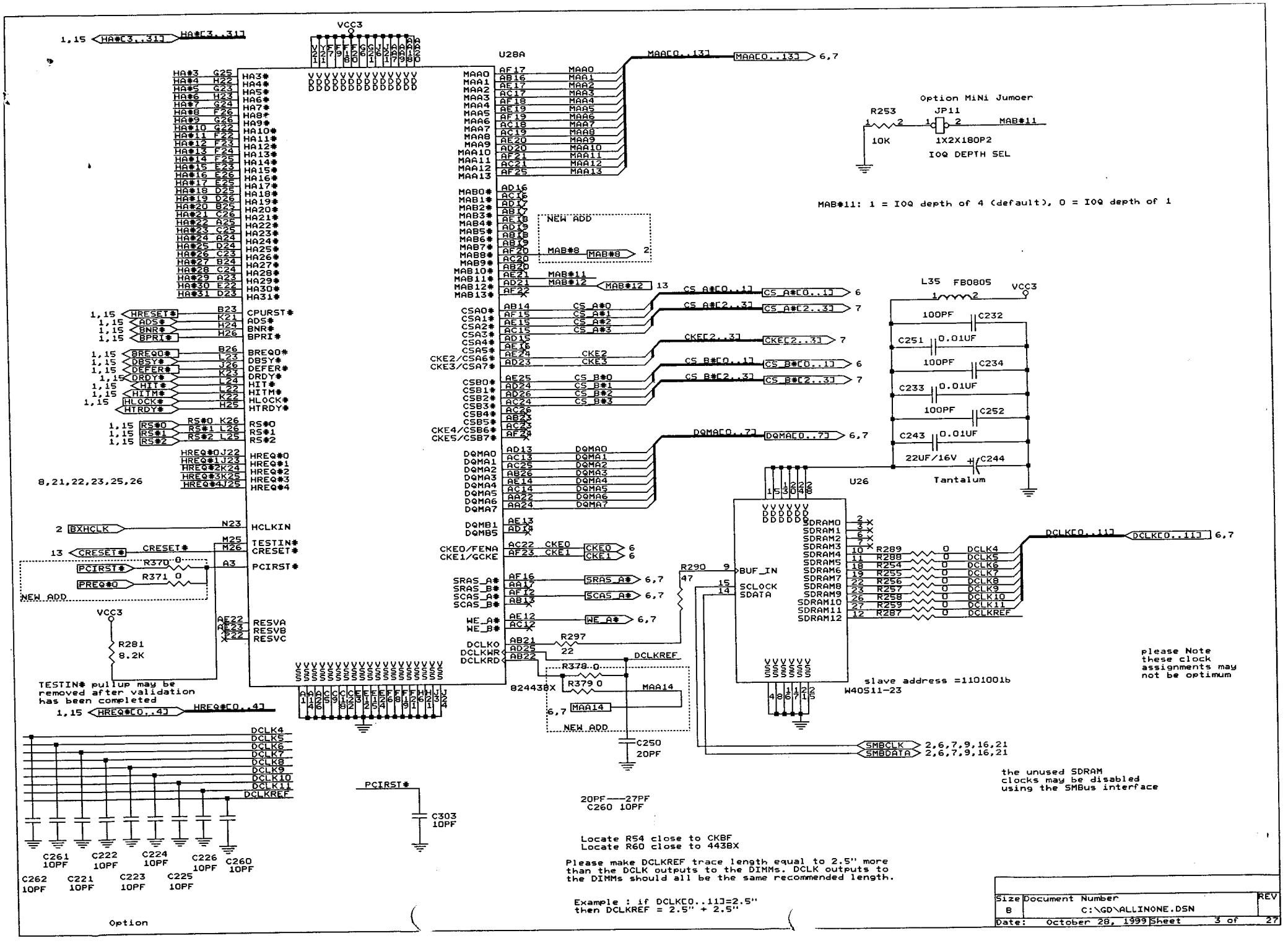
FLASH SOCKET

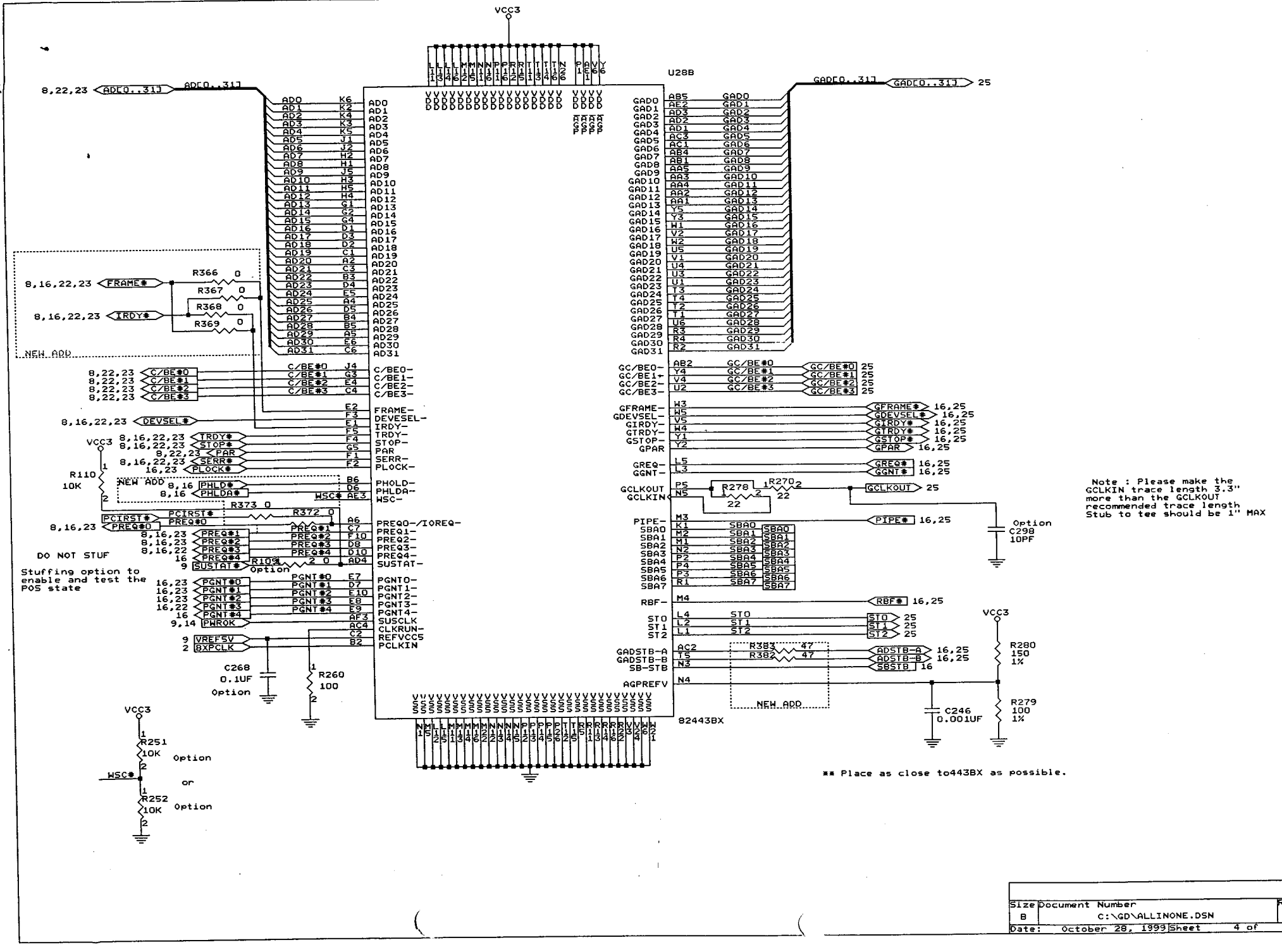


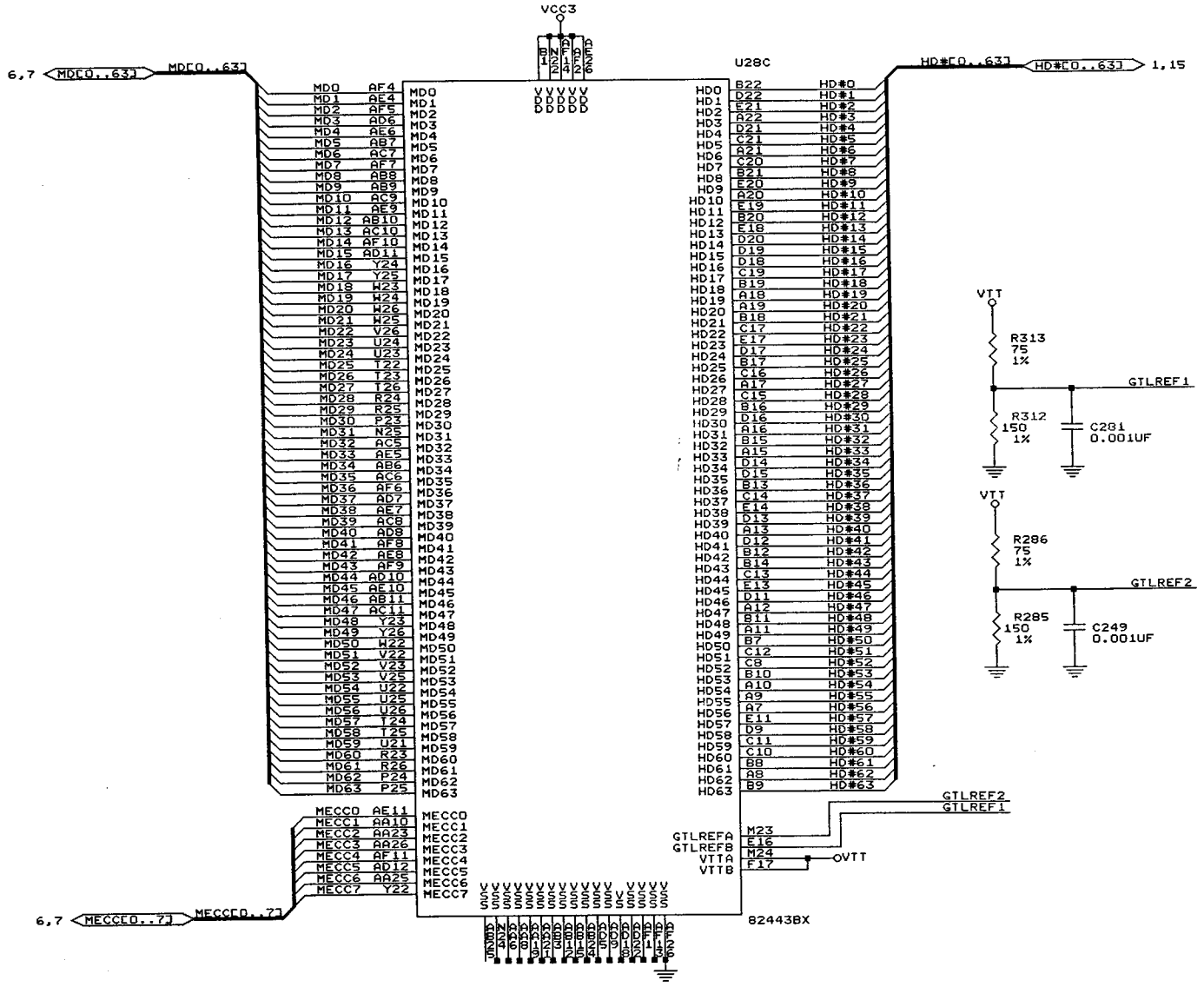
FCC ID: O2PMILLENNIUM-X

Size	Document Number	REV
B	C:\GD\ALLINONE.DSN	
Date: October 28, 1999	Sheet 2 of 27	


Note : This strong pullup resister on SLP# is Necessary when using an LAI
VCC2.5
VTT
R320
330
OPTION
R339
56
9 SLP#
C289
2200PF
OPTION
Please place as close to the connector as possible
R323
R324
R325
R326
R328
R329
R332
R305
4.7K
R334
200
OPTION
C277
100PF
OPTION
NEW ADD
133/100#
PICD1
100/66#
PICCLK
LINT1
TRST#
TMS
TCK
STPCLK#
HINIT#
PX4_SMI#
FLUSH#
A20M#
FERR#
IGNNE#
TDI
TDO
PWRGOOD
THERMTRIP#
LINT0
PCIDO
ITPREQ#
HA#[3..31]
HREQ#[0..4]
HD#[0..63]
HRESET#
HLOCK#
DRDY#
RS#0
HIT#
RS#2
VID3
VID0
VID4
VID1
VID2
VCCCORE
VCC
VCC3
SLOT1
CPU-CARD
ADS#
RS#1
DBSY#
HITM#
DEFER#
HTRDY#
BPRI#
BNR#
BREQ0#
CPUHCLK
LINK
2.SCH
3.SCH
4.SCH
5.SCH
6.SCH
7.SCH
8.SCH
9.SCH
10.SCH
11.SCH
12.SCH
13.SCH
14.SCH
16.SCH
17.SCH
19.SCH
20.SCH
21.SCH
22.SCH
23.SCH
24.SCH
25.SCH
26.SCH
27.SCH
28.SCH
29.SCH
30.SCH
31.SCH
Title
440BX ATX
Size B
Document Number SLOT1
REV A
Date: October 28, 1999
Sheet 1 of 27

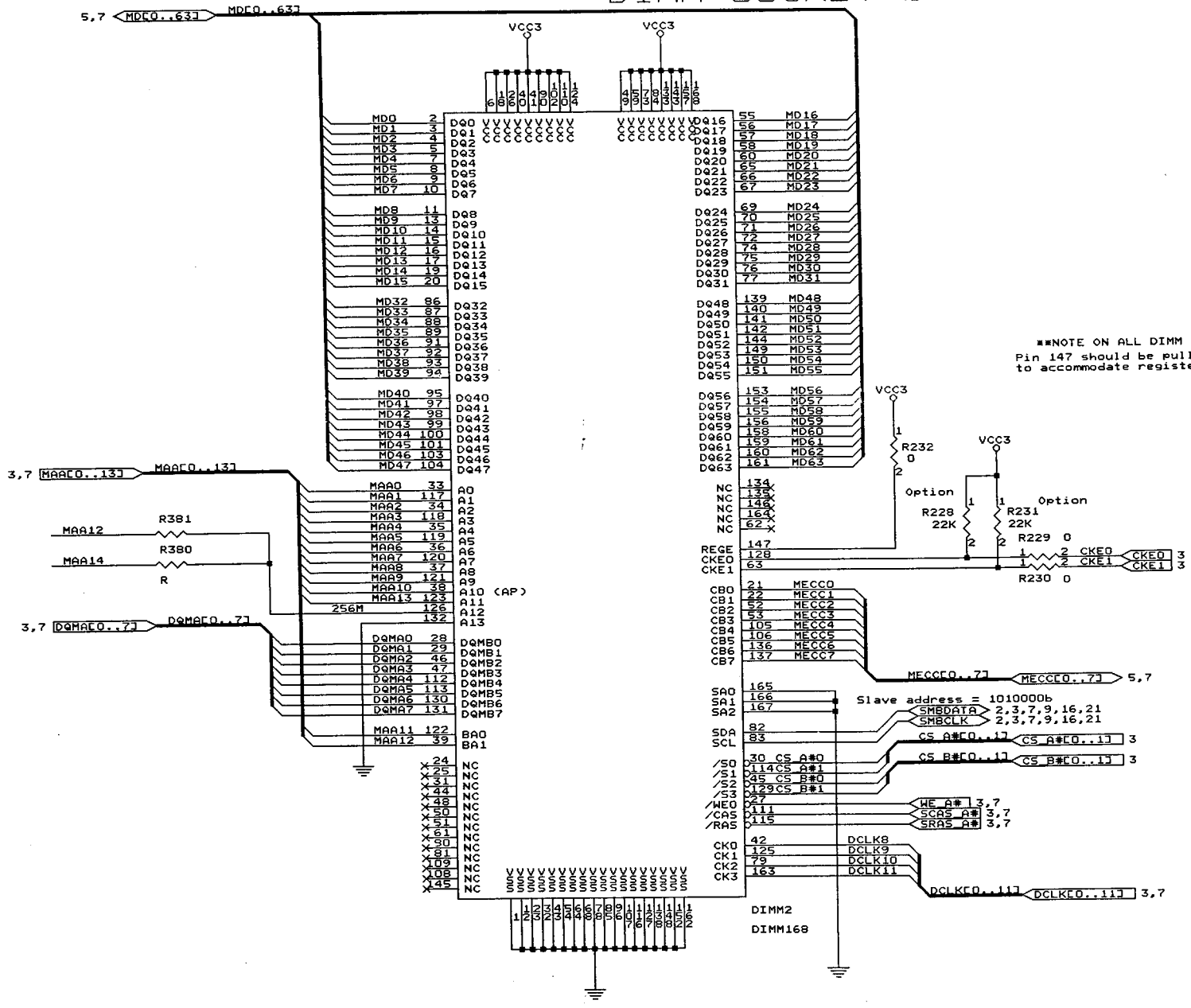

U28A
VCC3
Option MiNi Jumoer
R253
JP11
10K
1X2X180P2
IOQ DEPTH SEL
MAB#11: 1 = IOQ depth of 4 (default), 0 = IOQ depth of 1
NEW ADD
L35 FB0805
100PF C232
C251 0.01UF
100PF C234
C233 0.01UF
100PF C252
C243 0.01UF
22UF/16V C244
Tantalum
U26
R290
BUF_IN
SCLOCK
SDATA
SMBCLK
SMBDATA
slave address =1101001b
W40S11-23
please Note
these clock
assignments may
not be optimum
the unused SDRAM
clocks may be disabled
using the SMBus interface
R297
22
R378 0
R379 0
MAA14
C250
20PF
824430X
TESTIN# pullup may be
removed after validation
has been completed
R370 0
R371 0
R281
8.2K
C261 10PF
C222 10PF
C224 10PF
C226 10PF
C260 10PF
C262 10PF
C221 10PF
C223 10PF
C225 10PF
C303
10PF
20PF--27PF
C260 10PF
Locate R54 close to CKBF
Locate R60 close to 443BX
Please make DCLKREF trace length equal to 2.5" more
than the DCLK outputs to the DIMMs. DCLK outputs to
the DIMMs should all be the same recommended length.
Example : if DCLKE0..11]=2.5"
then DCLKREF = 2.5" + 2.5"
Option
Size B
Document Number C:\GD\ALLINONE.DSN
REV
Date: October 28, 1999
Sheet 3 of 27


VCC3
U28B
8,22,23 AD[0..31]
AD[0..31]
GAD[0..31]
25
AD0 K6
AD1 K2
AD2 K4
AD3 K3
AD4 K5
AD5 J1
AD6 J2
AD7 H2
AD8 H1
AD9 J5
AD10 H3
AD11 H5
AD12 H4
AD13 G1
AD14 G2
AD15 G4
AD16 D1
AD17 D3
AD18 D2
AD19 C1
AD20 A2
AD21 C3
AD22 B3
AD23 D4
AD24 E5
AD25 A4
AD26 D5
AD27 B4
AD28 B5
AD29 A5
AD30 E6
AD31 C6
GAD0 AB5
GAD1 AE2
GAD2 AD3
GAD3 AD2
GAD4 AD1
GAD5 AC3
GAD6 AC1
GAD7 AB4
GAD8 AB1
GAD9 AA5
GAD10 AA3
GAD11 AA4
GAD12 AA2
GAD13 AA1
GAD14 Y5
GAD15 Y3
GAD16 W1
GAD17 V2
GAD18 W2
GAD19 U5
GAD20 V1
GAD21 U4
GAD22 U3
GAD23 U1
GAD24 T3
GAD25 T4
GAD26 T2
GAD27 T1
GAD28 U6
GAD29 R3
GAD30 R4
GAD31 R2
NEW ADD
8,16,22,23 FRAME*
R366 0
R367 0
8,16,22,23 IRDY*
R368 0
R369 0
8,22,23 C/BE*0
8,22,23 C/BE*1
8,22,23 C/BE*2
8,22,23 C/BE*3
C/BE*0 J4
C/BE*1 G3
C/BE*2 E4
C/BE*3 C4
C/BE0- C/BE1- C/BE2- C/BE3-
GC/BE0- GC/BE1- GC/BE2- GC/BE3-
AB2 Y4 V4 U2
GC/BE*0 GC/BE*1 GC/BE*2 GC/BE*3
8,16,22,23 DEVSEL*
E2 FRAME-
F3 DEVESEL-
E1 IRDY-
F5 TRDY-
F4 STOP-
G5 PAR
F1 SERR-
F2 PLOCK-
GFRAME- GDEVSEL- GIRDY- GTRDY- GSTOP- GPAR
W3 H5 V5 H4 Y1 Y2
GFRAME* GDEVSEL* GIRDY* GTRDY* GSTOP* GPAR
16,25
8,16,22,23 TRDY*
8,16,22,23 STOP*
8,22,23 PAR
8,16,22,23 SERR*
16,23 PLOCK*
VCC3
R110 10K
NEW ADD
8,16 PHLD*
8,16 PHLDA*
B6 PHOLD-
D6 PHLDA-
WSC* AE3 WSC-
GREQ- GGNT-
L5 L3
GREQ* GGNT*
16,25
GCLKOUT GCLKIN
P5 N5
R278 22
R270 22
GCLKOUT
25
Option
C298
10PF
PCIRST*
PREQ*0
R373 0
R372 0
8,16,23 PREQ*0
A6 PREQ0-/IOREQ-
PREQ*1 C7 PREQ1-
PREQ*2 F10 PREQ2-
PREQ*3 D8 PREQ3-
PREQ*4 D10 PREQ4-
8,16,23 PREQ*1
8,16,23 PREQ*2
8,16,22 PREQ*3
16 PREQ*4
9 SUSTAT*
R109 0
Option
AD4 SUSTAT-
PIPE- M3
SBA0 K1
SBA1 M2
SBA2 M1
SBA3 N2
SBA4 P2
SBA5 P4
SBA6 P3
SBA7 R1
SBA0 SBA1 SBA2 SBA3 SBA4 SBA5 SBA6 SBA7
PIPE* 16,25
DO NOT STUF
Stuffing option to enable and test the POS state
16,23 PGNT*0
16,23 PGNT*1
16,23 PGNT*2
16,22 PGNT*3
16 PGNT*4
9,14 PWROK
PGNT*0 E7 PGNT0-
PGNT*1 D7 PGNT1-
PGNT*2 E10 PGNT2-
PGNT*3 E8 PGNT3-
PGNT*4 E9 PGNT4-
AF3 SUSCLK
AC4 CLKRUN-
RBF- M4
RBF* 16,25
STO L4
ST1 L2
ST2 L1
STO ST1 ST2
25
9 VREF5V
2 BXPCLK
C2 REFVCC5
B2 PCLKIN
GADSTB-A GADSTB-B SB-STB
AC2 T5 N3
R383 47
R382 47
ADSTB-A ADSTB-B SBSTB
16,25
16
AGPREFV N4
NEW ADD
C268 0.1UF Option
R260 100
VCC3
R280 150 1%
R279 100 1%
C246 0.001UF
82443BX
VCC3
R251 10K Option
WSC*
or
R252 10K Option
** Place as close to443BX as possible.
Note : Please make the GCLKIN trace length 3.3" more than the GCLKOUT recommended trace length Stub to tee should be 1" MAX
Size B
Document Number C:\GD\ALLINONE.DSN
REV
Date: October 28, 1999 Sheet 4 of 27



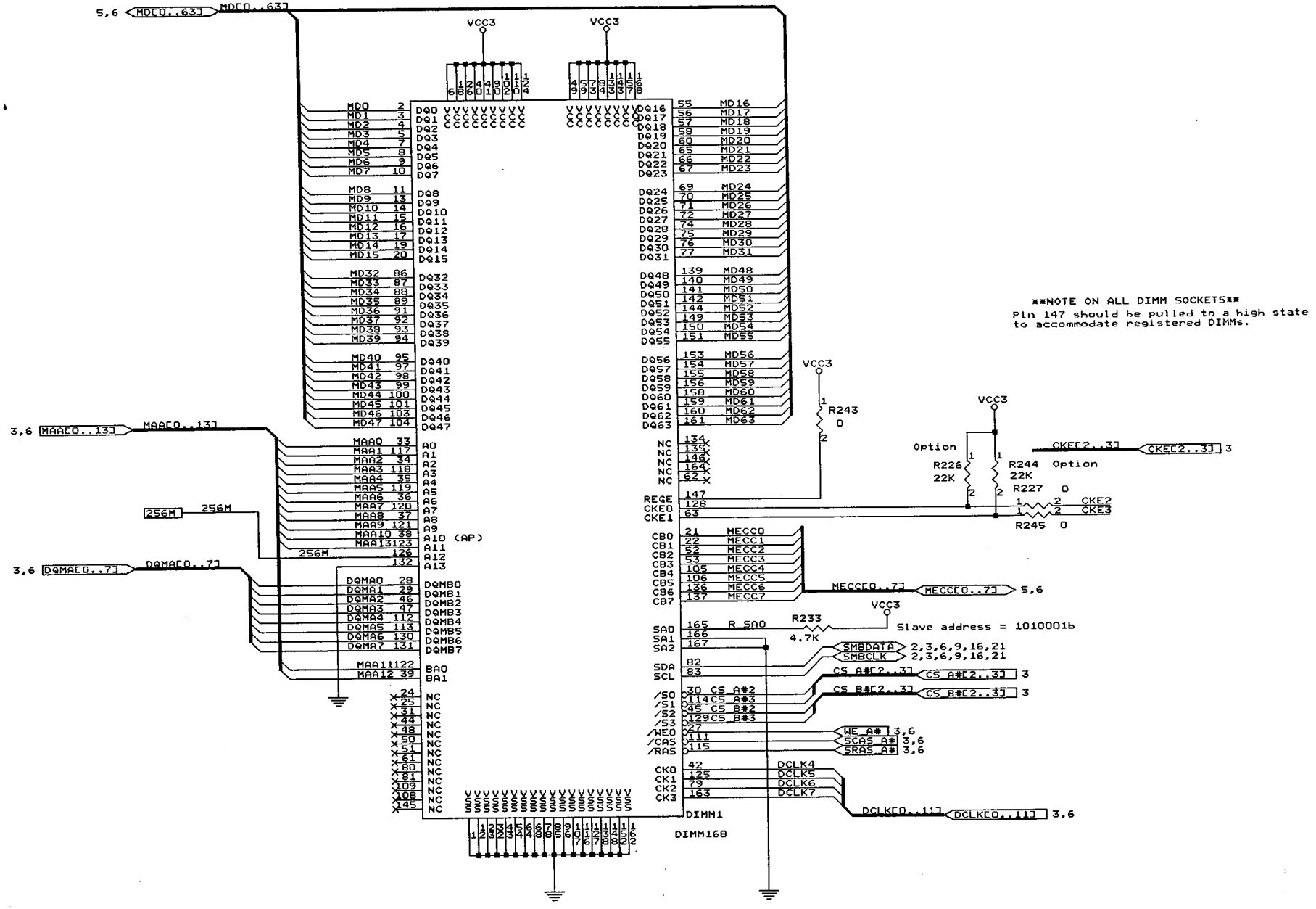
Size	Document Number	REV
B	C:\GD\ALLINONE.DSN	
Date: September 30, 1998	Sheet 5 of 27	

DIMM SOCKET Ø

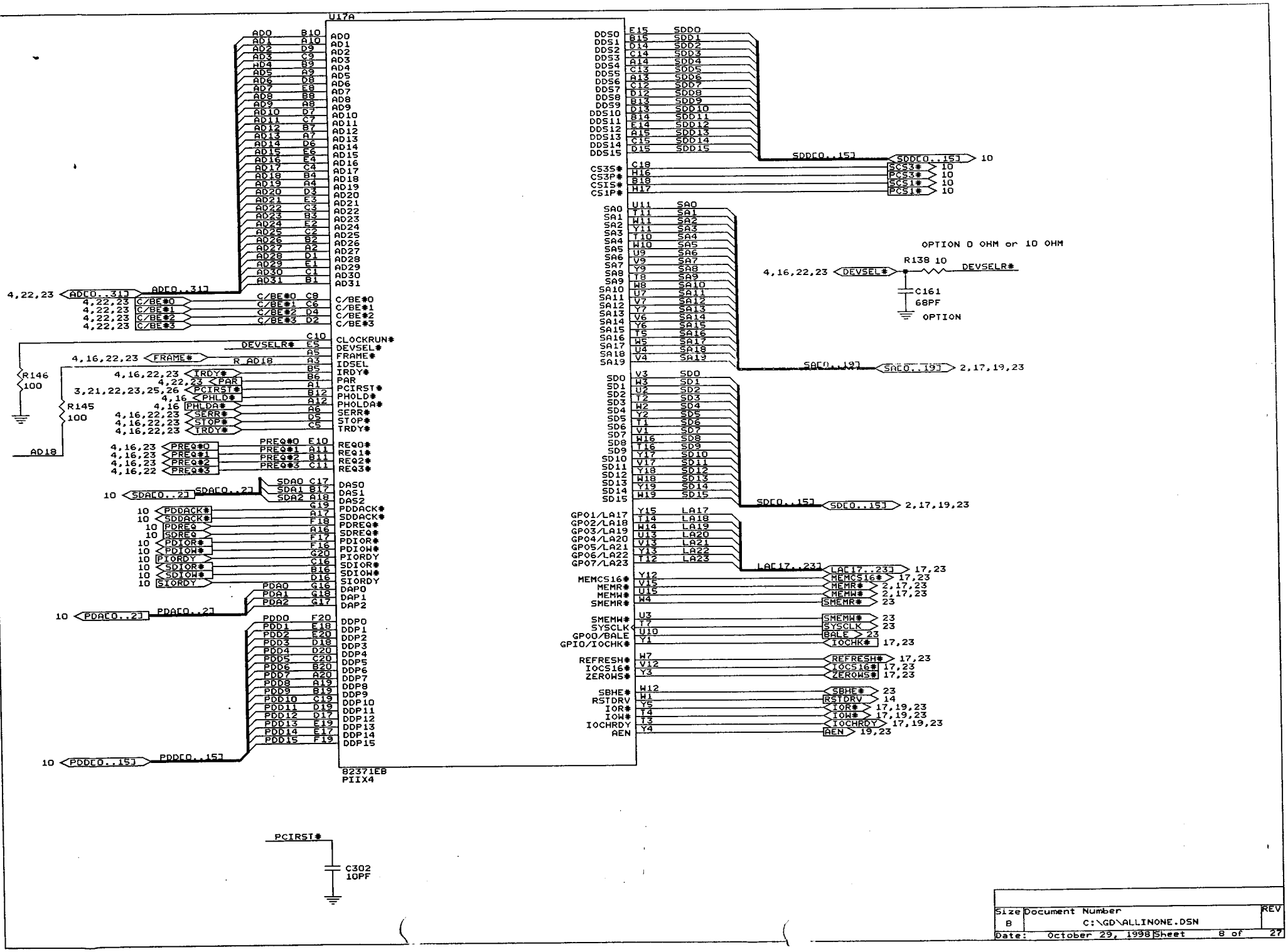


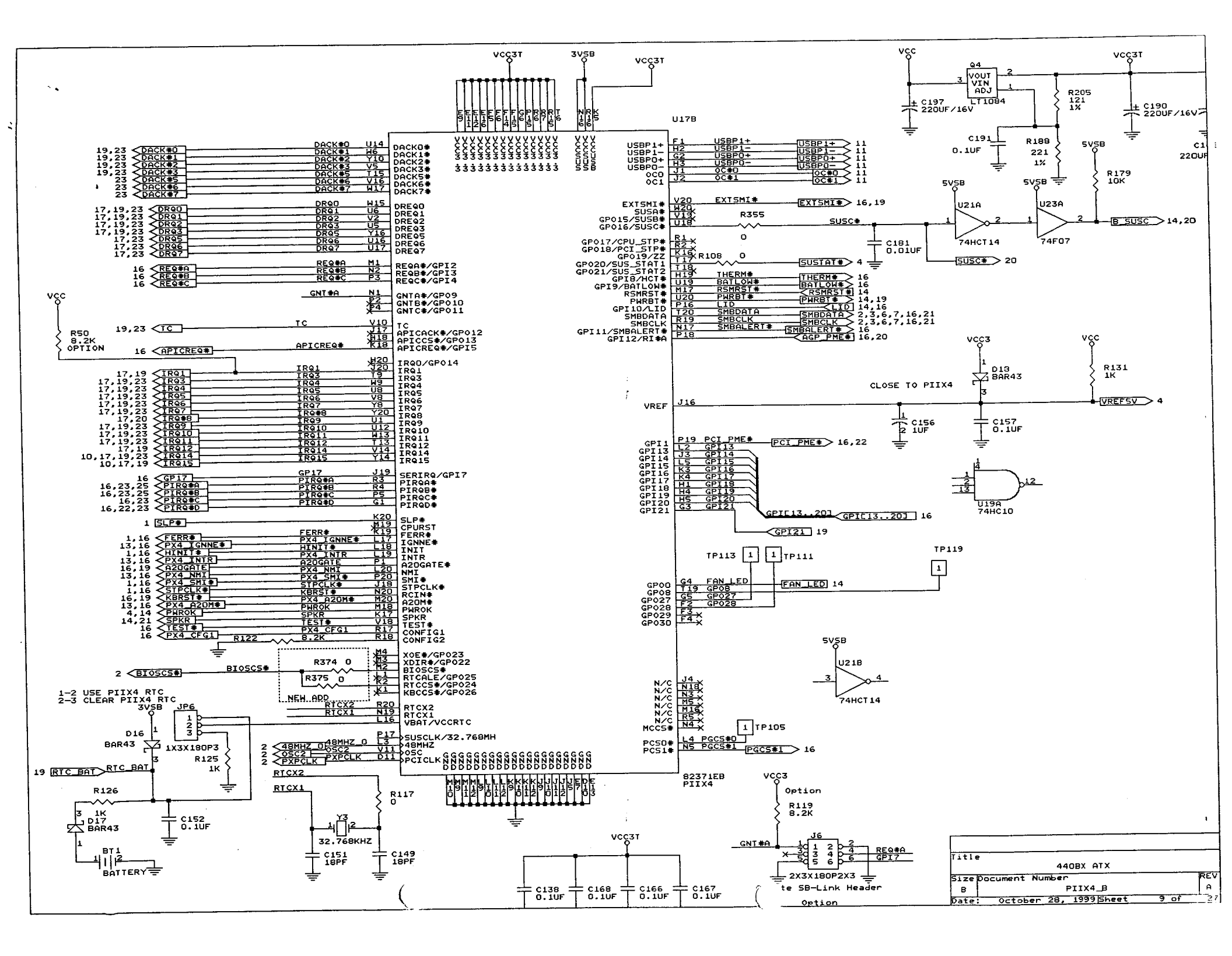
Size	Document Number	REV
B	C:\GD\ALLINONE.DSN	
Date: October 28, 1999	Sheet 6 of 27	

DIMM SOCKET 1

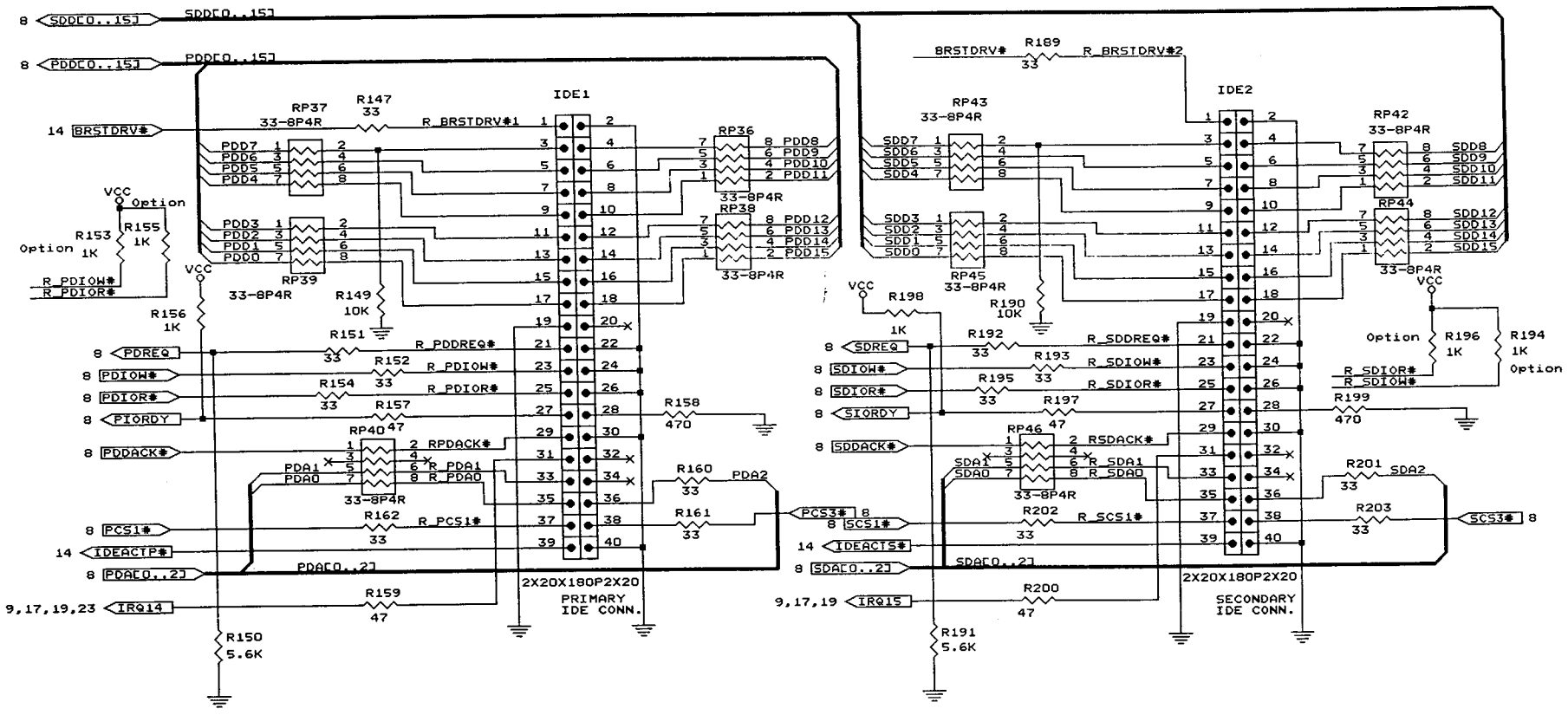


Size	Document Number	REV
B	C:\GD\ALLINONE.DSN	
Date: April 29, 1999	Sheet 7 of 27	


U17A
82371EB
PIIX4
OPTION 0 OHM or 10 OHM
R138 10
DEVSELR#
C161
68PF
OPTION
R146
100
R145
100
AD18
C302
10PF
PCIRST#
Size
B
Document Number
C:\GD\ALLINONE.DSN
REV
Date: October 29, 1998
Sheet 8 of 27

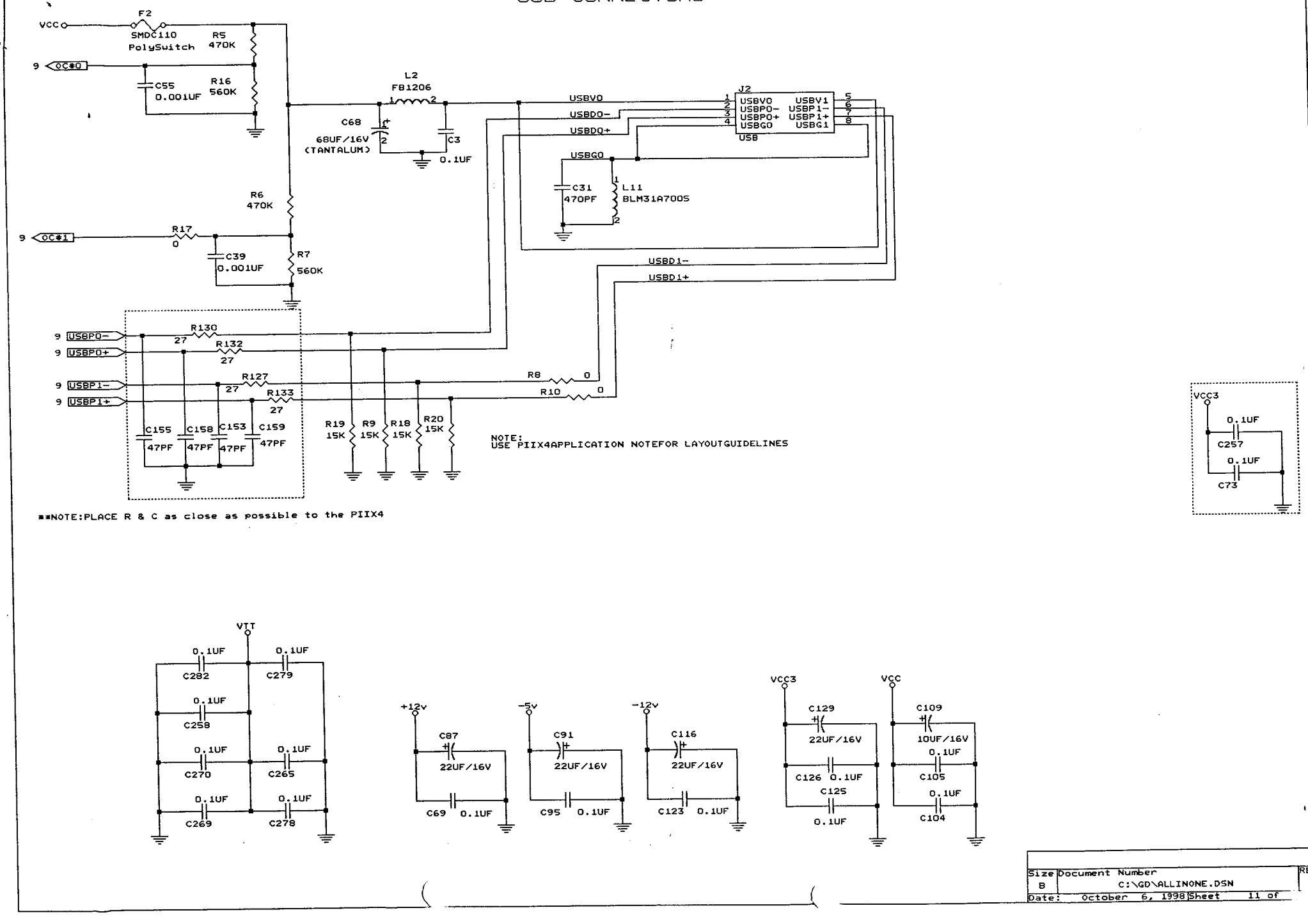

U17B
82371EB
PIIX4
U21A
74HCT14
U23A
74F07
U21B
74HCT14
U19A
74HC10
Q4
VOUT
VIN
ADJ
LT1084
C197
220UF/16V
C190
220UF/16V
R205
121
1%
R188
221
1%
R179
10K
R355
0
R108
0
C181
0.01UF
C191
0.1UF
D13
BAR43
CLOSE TO PIIX4
R131
1K
C156
1UF
C157
0.1UF
R50
8.2K
OPTION
R374 0
R375 0
NEW ADD
1-2 USE PIIX4 RTC
2-3 CLEAR PIIX4 RTC
JP6
D16
BAR43
1X3X180P3
R125
1K
R126
1K
D17
BAR43
BT1
BATTERY
Y3
32.768KHZ
C151
18PF
C149
18PF
R117
0
C152
0.1UF
R122
8.2K
TP113
TP111
TP119
TP105
R119
8.2K
Option
J6
2X3X180P2X3
te SB-Link Header
Option
C138
0.1UF
C168
0.1UF
C166
0.1UF
C167
0.1UF
Title
440BX ATX
Size
B
Document Number
PIIX4_B
REV
A
Date:
October 28, 1999
Sheet
9 of

IDE CONNECTORS



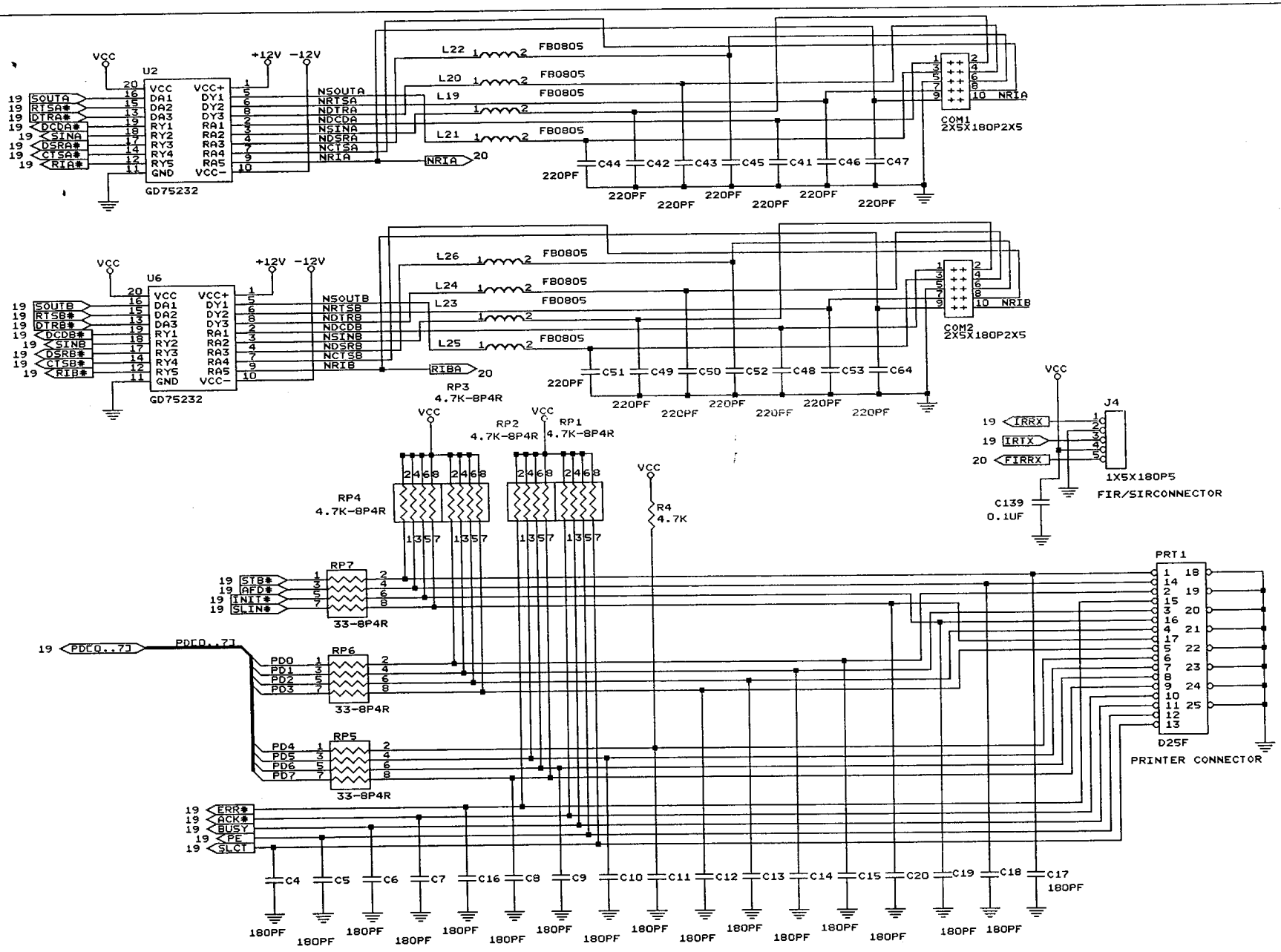
Size	Document Number	REV
B		A
Date: September 30, 1998	Sheet 10 of 27	

USB CONNECTORS



**NOTE:PLACE R & C as close as possible to the PIIX4

Size	Document Number	REV
B	C:\GD\ALLINONE.DSN	
Date: October 6, 1998	Sheet 11 of	



Size	Document Number	REV
B	C:\GD\ALLINONE.DSN	
Date: October 21, 1998	Sheet 12 of	

INPUT CHOKE IS OPTIONAL DEPENDED ON THE LAYOUT AND HOW FAR AWAY FROM THE POWERCONNECTOR

+12V
D22
1N5817
1A
C253
0.1UF
MUST BE VERY CLOSED TO PIN 9
D24
1N5817
1A
VCC
C239
1UF
R262
47K
25 MIL WIDE
U27
CS5165
VID0
VID1
VID2
VID3
VID4
ENABLE
PWRGD
COFF
SS
COMP
VDD
VGH
VGL
PGND
VFB
GATE TRACES MUST BE VERY SHORT
Q6
MiD50N03A
Q7
MiD50N03A
T50-52D
#AWG13
7 TURNS
L36
2UH
POWER IRON
PLACE 170MIL WIDE 1 INCH LONG TRACE AS A DROOP RESISTOR
C284
1200UF/6.3V
C286
1200UF/6.3V
C283
1200UF/6.3V
C285
1200UF/6.3V
C287
1200UF/6.3V
C290
1200UF/6.3V
C292
1200UF/6.3V
C291
1200UF/6.3V
C288
1200UF/6.3V
VCCCORE
T50-2
#AWG15
10 TURNS
L37
1UH
POWER IRON
C255
1000PF
C254
0.1UF
C237
0.33UF
C245
100PF
R291
3.3K
VCC3
RP29
4.7K-8P4R
SW1
SWDIP4
U15
74LVC3244
R135
10K
5VSB
CRESET#
U16A
74HCT14
R124
300
Option
VCC3
9,16 PX4_A20M#
9,16 PX4_IGNNE#
9,16 PX4_INTR
9,16 PX4_NMI
U18B
74F07
U18C
74F07
U18D
74F07
U18E
74F07
A20M# 1,16
IGNNE# 1,16
LINTO 1,16
LINT1 1,16
2.5V REGULATOR

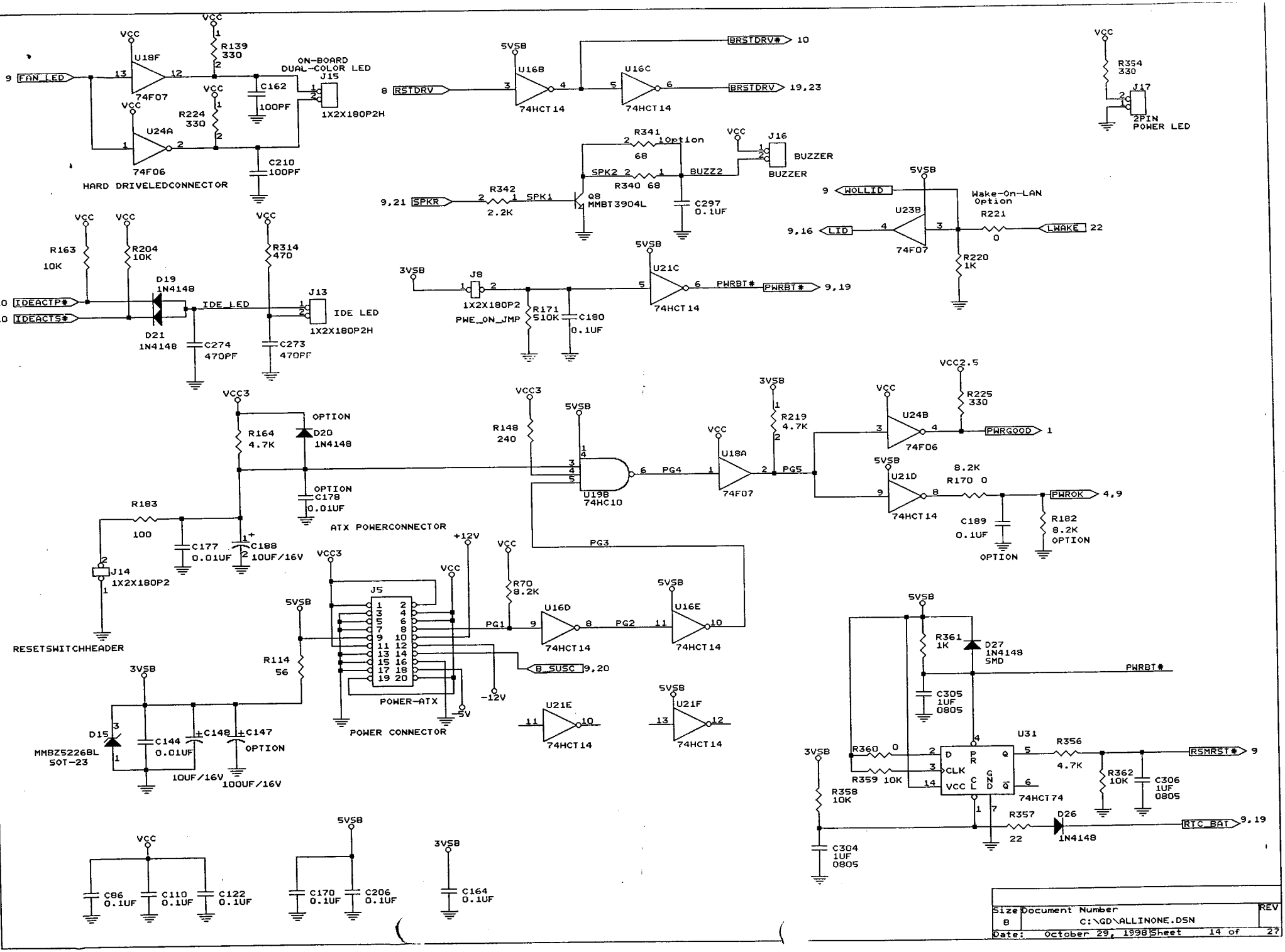
* ADDITIONAL STRAP CONFIGURATIONS MAY BENECESSARY TO SUPPORT THE DS1P.

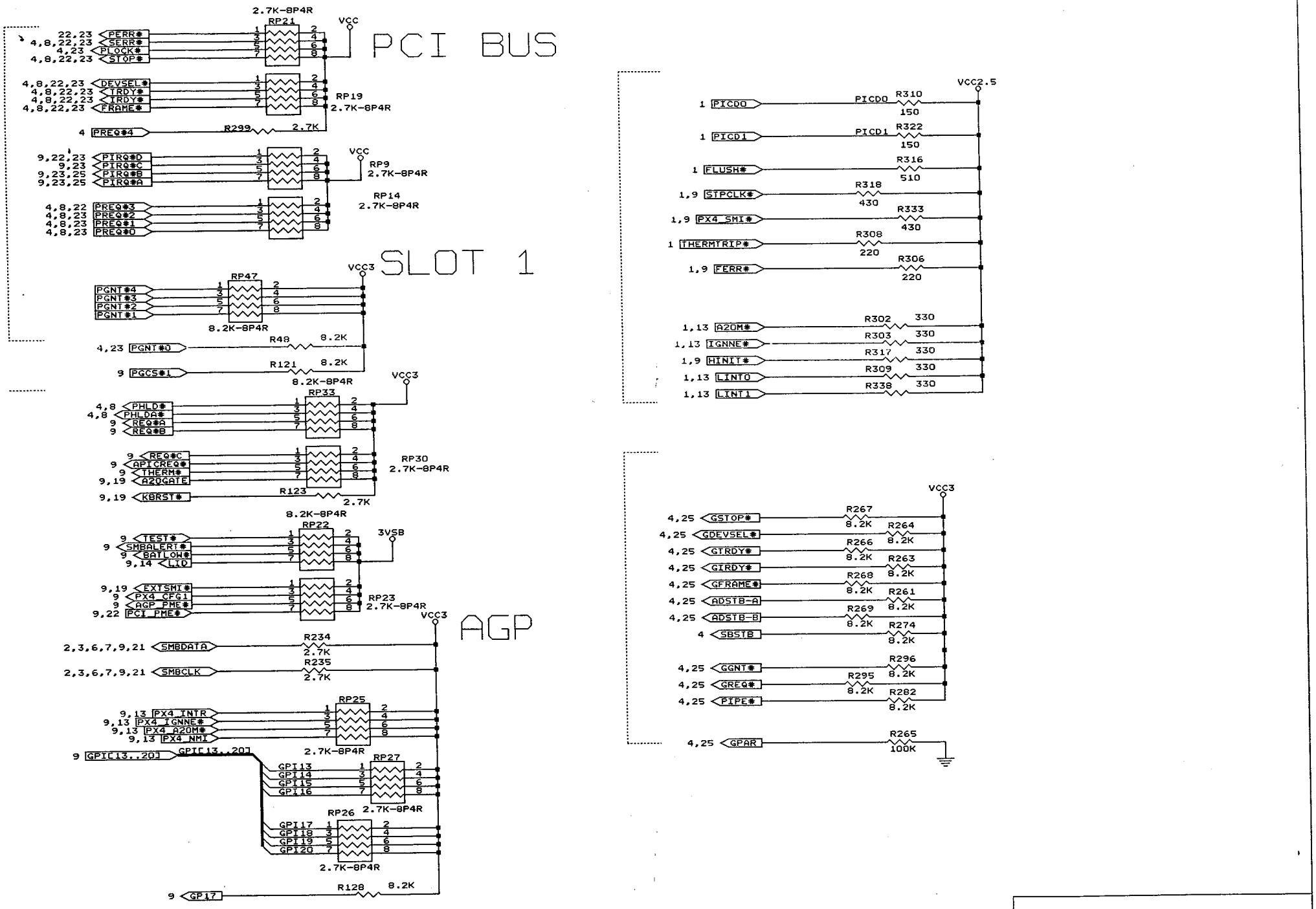
Frequency Multiplier: (System Bus to Process Core)	LINT1 KC7	LINTO KC5	IGNNE# KC3	A20M# KC1	
3	L	L	H	L	200
4	L	L	L	H	266
5	L	L	H	H	333
5/2	L	H	L	L	166
7/2	L	H	H	L	233
9/2	L	H	L	H	300

VTT REGULATOR
D25
Option
1N4002
VCC
U30
VOUT
VIN
ADJ
CS5205A
VTT
R301
124
1%
R300
23.2
1%
C263
10UF/16V
C276
0.1UFC0805
C266
22UF/16V
D23
Option
1N4002
VCC
U29
VOUT
VIN
ADJ
CS5201
R1
R277
124
1%
R2
R292
121.4
1%
C238
10UF/16V
C247
0.1UFC0805
VCC2.5
C240
22UF/16V
VOUT=VREF*(R1+R2 / R1)
VREF=1.263
VCCCORE
C293
1200UF/6.3V
C294
1200UF/6.3V
C295
1200UF/6.3V
C296
1200UF/6.3V

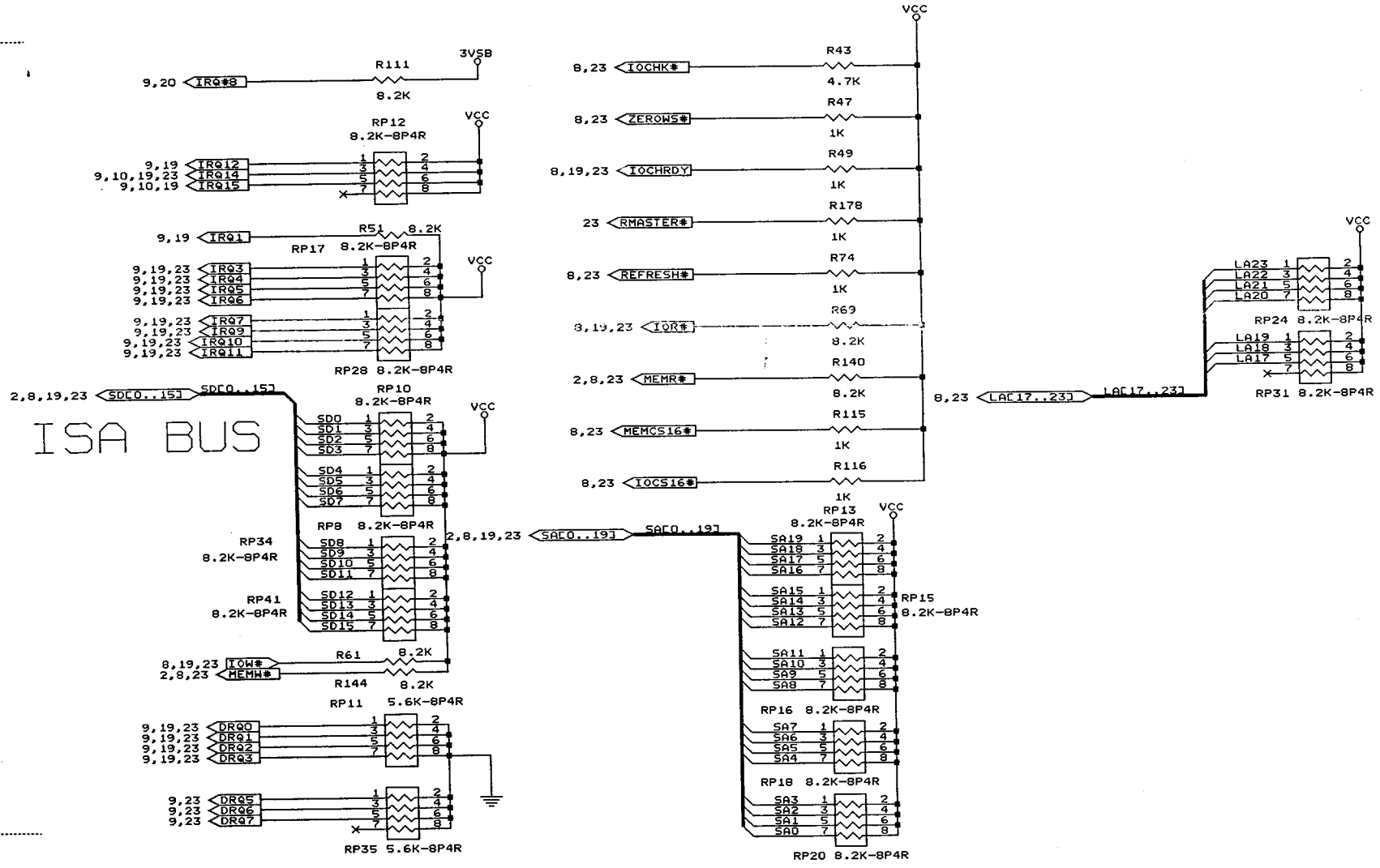
NOTE VOLTAGEREGULATOR SHOULDBE LOCATED NEARTHE 440BX

Size	Document Number	REV
B	C:\GD\ALLINONE.DSN	
Date: May 10, 1999	Sheet 13 of 27	

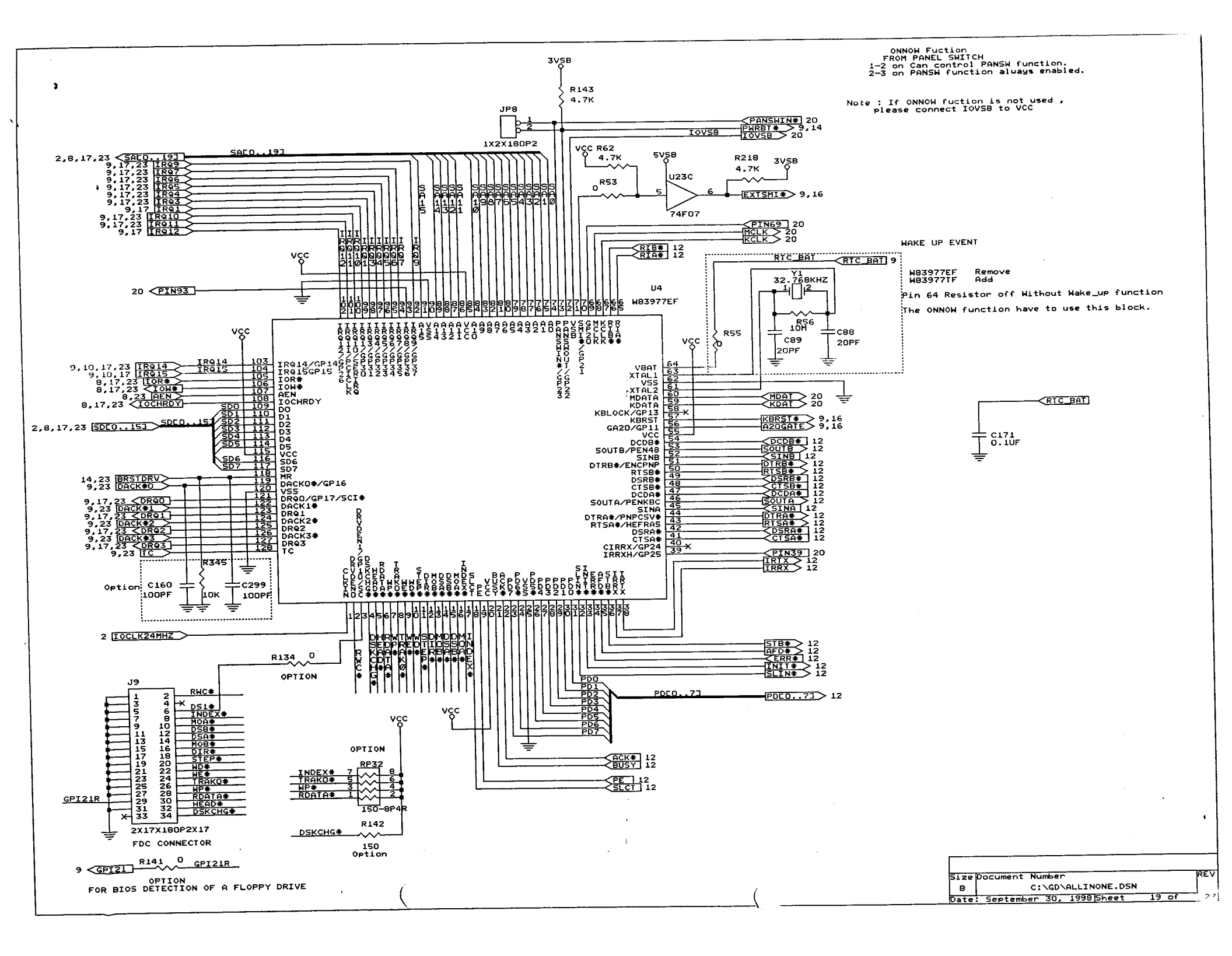

9 FAN_LED
U18F
74F07
R139 330
ON-BOARD DUAL-COLOR LED
J15
1X2X180P2H
C162 100PF
R224 330
U24A
74F06
C210 100PF
HARD DRIVELEDCONNECTOR
8 RSTDRV
U16B
74HCT14
U16C
74HCT14
BRSTDRV# 10
BRSTDRV 19,23
R354 330
J17
2PIN POWER LED
R341 10ption 68
SPK2
R340 68
BUZZ2
J16
BUZZER
9,21 SPKR
R342 2.2K
SPK1
Q8 MMBT3904L
C297 0.1UF
9 WOLLID
U23B
74F07
Wake-On-LAN Option
R221 0
9,16 LID
LWAKE 22
R220 1K
R163 10K
R204 10K
R314 470
D19 1N4148
D21 1N4148
10 IDEACTP#
10 IDEACTS#
IDE_LED
J13
IDE LED
1X2X180P2H
C274 470PF
C273 470PF
3VSB
J8
1X2X180P2
PWE_ON_JMP
R171 510K
C180 0.1UF
U21C
74HCT14
PWRBT#
PWRBT# 9,19
R164 4.7K
OPTION D20 1N4148
OPTION C178 0.01UF
ATX POWERCONNECTOR
R148 240
U19B 74HC10
PG4
PG5
U18A
74F07
R219 4.7K
U24B
74F06
R225 330
PWRGOOD 1
U21D
74HCT14
8.2K R170 0
PWROK 4,9
C189 0.1UF
OPTION
R182 8.2K
OPTION
R183 100
C177 0.01UF
C188 10UF/16V
J14
1X2X180P2
RESETSWITCHHEADER
PG3
J5
POWER-ATX
POWER CONNECTOR
PG1
PG2
U16D
74HCT14
U16E
74HCT14
R70 8.2K
B_SUSC 9,20
U21E
74HCT14
U21F
74HCT14
R114 56
D15 MMBZ5226BL SOT-23
C144 0.01UF
C148 10UF/16V
C147 OPTION 100UF/16V
R361 1K
D27 1N4148 SMD
PWRBT#
C305 1UF 0805
U31
74HCT74
R360 0
R359 10K
R358 10K
C304 1UF 0805
R356 4.7K
R362 10K
C306 1UF 0805
RSMRST# 9
R357 22
D26 1N4148
RTC_BAT 9,19
C86 0.1UF
C110 0.1UF
C122 0.1UF
C170 0.1UF
C206 0.1UF
C164 0.1UF
Size B
Document Number C:\GD\ALLINONE.DSN
REV
Date: October 29, 1998
Sheet 14 of 27

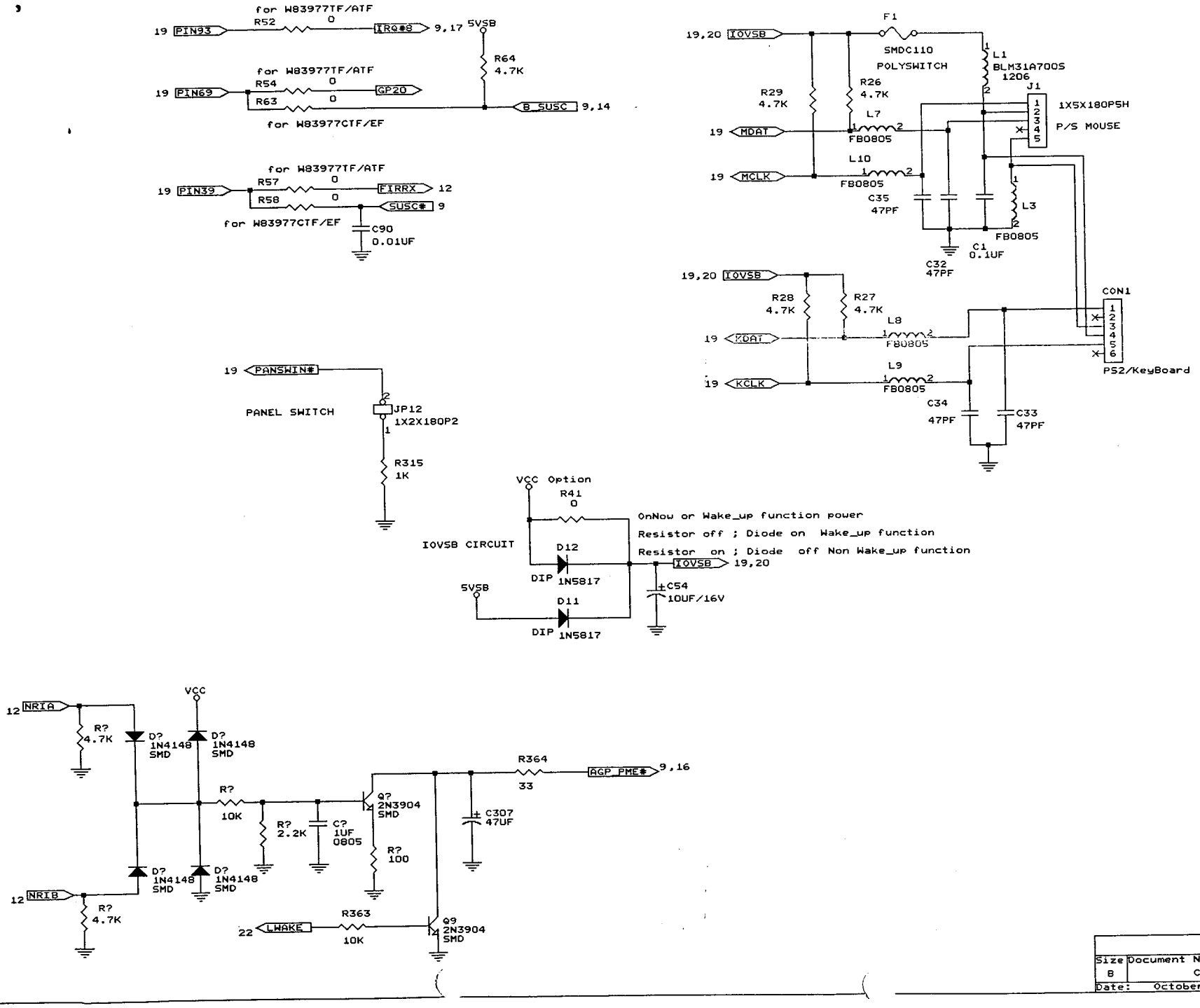


Size	Document Number	REV
B	C:\GD\ALLINONE.DSN	
Date: October 21, 1998	Sheet 16 of 27	

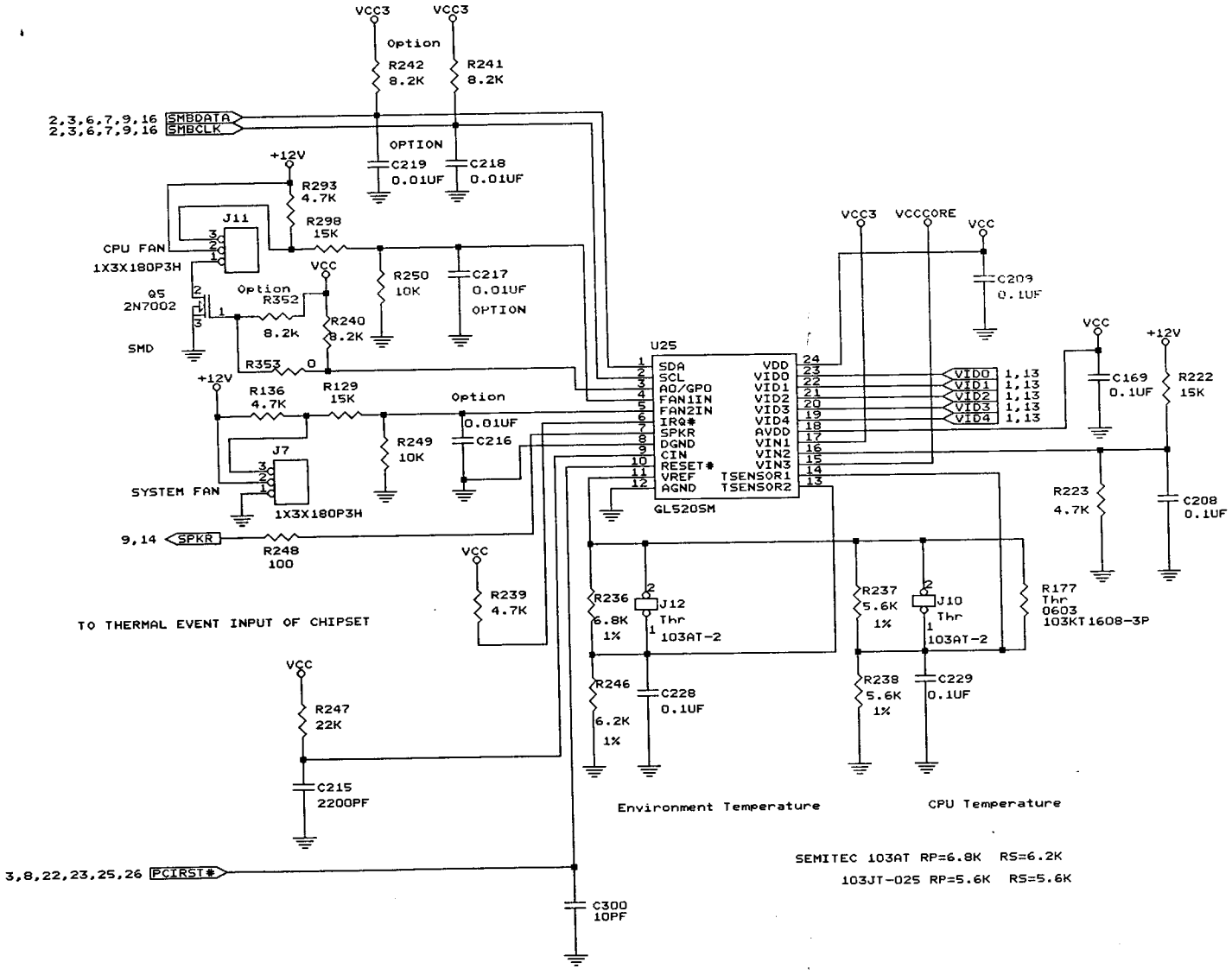


Size	Document Number	REV
B	C:\GD\ALLINONE.DSN	
Date: September 17, 1998	Sheet 17 of 27	

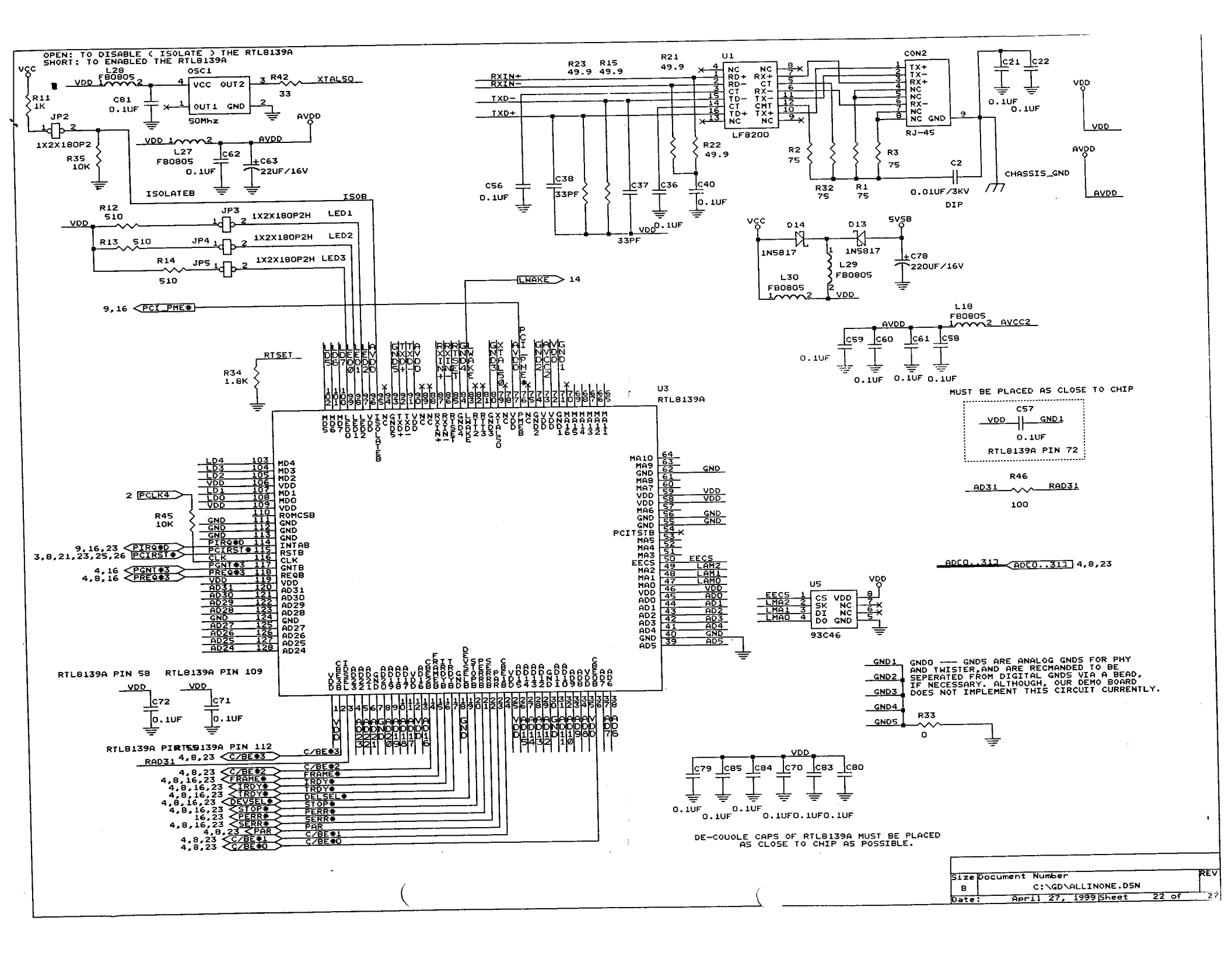

ONNOW Fuction
FROM PANEL SWITCH
1-2 on Can control PANSW function.
2-3 on PANSW function aluays enabled.
Note : If ONNOW fuction is not used , please connect IOVSB to VCC
3VSB
R143
4.7K
JP8
1X2X180P2
PANSWIN# 20
PWRBT# 9,14
IOVSB
IOVSB 20
VCC R62
4.7K
5VSB
U23C
74F07
R53
0
R218
4.7K
3VSB
EXTSMI# 9,16
PIN69 20
MCLK 20
KCLK 20
RIB# 12
RIA# 12
WAKE UP EVENT
RTC_BAT
RTC_BAT 9
Y1
32.768KHZ
R56
10M
C88
20PF
C89
20PF
R55
0
W83977EF Remove
W83977TF Add
Pin 64 Resistor off Without Wake_up function
The ONNOW function have to use this block.
U4
W83977EF
VCC
20 PIN93
2,8,17,23 SA[0..19]
9,17,23 IRQ9
9,17,23 IRQ7
9,17,23 IRQ6
9,17,23 IRQ5
9,17,23 IRQ4
9,17,23 IRQ3
9,17 IRQ1
9,17,23 IRQ10
9,17,23 IRQ11
9,17 IRQ12
9,10,17,23 IRQ14
9,10,17 IRQ15
8,17,23 IOR#
8,17,23 IOW#
8,23 AEN
8,17,23 IOCHRDY
2,8,17,23 SD[0..15]
14,23 BRSTDRV
9,23 DACK#0
9,17,23 DRQ0
9,23 DACK#1
9,17,23 DRQ1
9,23 DACK#2
9,17,23 DRQ2
9,23 DACK#3
9,17,23 DRQ3
9,23 TC
R345
Option
C160
100PF
10K
C299
100PF
2 IOCLK24MHZ
R134 0
OPTION
J9
RWC#
DS1#
INDEX#
MOA#
DSB#
DSA#
MOB#
DIR#
STEP#
WD#
WE#
TRAK0#
WP#
RDATA#
HEAD#
DSKCHG#
GPI21R
2X17X180P2X17
FDC CONNECTOR
9 GPI21
R141 0 GPI21R
OPTION
FOR BIOS DETECTION OF A FLOPPY DRIVE
OPTION
RP32
INDEX# TRAK0# WP# RDATA#
150-8P4R
R142
DSKCHG#
150
Option
VBAT
XTAL1
VSS
XTAL2
MDATA
KDATA
KBLOCK/GP13
KBRST
GA20/GP11
VCC
DCDB#
SOUTB/PEN48
SINB
DTRB#/ENCPNP
RTSB#
DSRB#
CTSB#
DCDA#
SOUTA/PENKBC
SINA
DTRA#/PNPCSV#
RTSA#/HEFRAS
DSRA#
CTSA#
CIRRX/GP24
IRRXH/GP25
MDAT 20
KDAT 20
KBRST# 9,16
A20GATE 9,16
DCDB# 12
SOUTB 12
SINB 12
DTRB# 12
RTSB# 12
DSRB# 12
CTSB# 12
DCDA# 12
SOUTA 12
SINA 12
DTRA# 12
RTSA# 12
DSRA# 12
CTSA# 12
PIN39 20
IRTX 12
IRRX 12
STB# 12
AFD# 12
ERR# 12
INIT# 12
SLIN# 12
PD[0..7]
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
ACK# 12
BUSY 12
PE 12
SLCT 12
C171
0.1UF
RTC_BAT
Size B
Document Number C:\GD\ALLINONE.DSN
REV
Date: September 30, 1998
Sheet 19 of

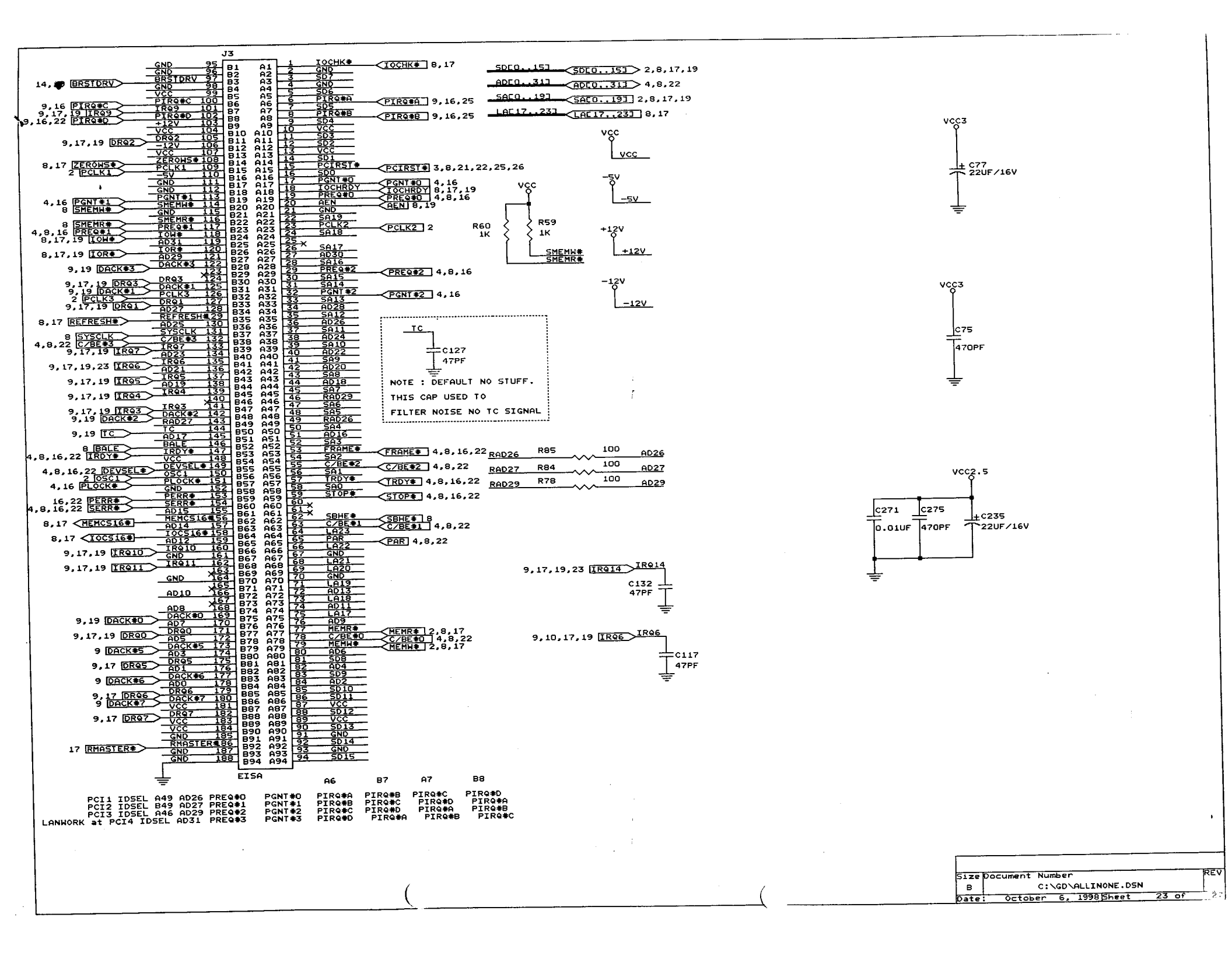


Size	Document Number	REV
B	C:\GD\ALLINONE.DSN	
Date: October 29, 1998	Sheet 20 of 27	



Size	Document Number	REV
B	C:\GD\ALLINONE.DSN	
Date: October 29, 1998	Sheet 21 of	


OPEN: TO DISABLE (ISOLATE) THE RTL8139A
SHORT: TO ENABLED THE RTL8139A
VCC
L28 FB0805
OSC1
VCC OUT2
OUT1 GND
50Mhz
R42 33
XTAL50
C81 0.1UF
R11 1K
JP2 1X2X180P2
R35 10K
AVDD
L27 FB0805
C62 0.1UF
C63 22UF/16V
ISOLATEB
ISOB
R12 510
R13 510
R14 510
JP3 1X2X180P2H LED1
JP4 1X2X180P2H LED2
JP5 1X2X180P2H LED3
VDD
LWAKE 14
9,16 PCI_PME#
RTSET
R34 1.8K
U3
RTL8139A
LD4 LD3 LD2 LD1 LD0 ROMCSB PIRQ#D PCIRST# CLK PGNT#3 PREQ#3 AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24
MD4 MD3 MD2 MD1 MD0 INTAB RSTB CLK GNTB REQB AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24
2 PCLK4
R45 10K
9,16,23 PIRQ#D
3,8,21,23,25,26 PCIRST#
4,16 PGNT#3
4,8,16 PREQ#3
MA10 MA9 MA8 MA7 MA6 MA5 MA4 MA3 MA2 MA1 MA0 AD0 AD1 AD2 AD3 AD4 AD5
GND VDD
PCITSTB
EECS LAM2 LAM1 LAM0
RTL8139A PIN 58
RTL8139A PIN 109
RTL8139A PIN 112
C72 0.1UF
C71 0.1UF
C/BE#3 RAD31 4,8,23
C/BE#2 4,8,23
FRAME# 4,8,16,23
IRDY# 4,8,16,23
TRDY# 4,8,16,23
DELSEL# 4,8,16,23
STOP# 4,8,16,23
PERR# 16,23
SERR# 4,8,16,23
PAR 4,8,23
C/BE#1 4,8,23
C/BE#0 4,8,23
U1
LF8200
NC RD+ RD- CT TD- CT TD+ NC
NC RX+ CT RX- TX- CMT TX+ NC
RXIN+ RXIN- TXD- TXD+
R23 49.9
R15 49.9
R21 49.9
R22 49.9
C56 0.1UF
C38 33PF
C37 C36 0.1UF
C40 0.1UF
33PF
CON2
RJ-45
TX+ TX- RX+ NC NC RX- NC NC GND
C21 0.1UF
C22 0.1UF
R2 75
R3 75
R32 75
R1 75
C2 0.01UF/3KV
DIP
CHASSIS_GND
VDD
AVDD
VCC
D14 1N5817
D13 1N5817
5VSB
L29 FB0805
L30 FB0805
C78 220UF/16V
L18 FB0805
AVCC2
C59 C60 C61 C58
0.1UF
MUST BE PLACED AS CLOSE TO CHIP
C57 0.1UF
RTL8139A PIN 72
R46 100
AD31 RAD31
ADC0..31 4,8,23
U5
93C46
EECS LMA2 LMA1 LMA0
CS SK DI DO VDD NC NC GND
GND1 GND2 GND3 GND4 GND5
GNDO —— GND5 ARE ANALOG GNDS FOR PHY AND TWISTER,AND ARE RECMANDED TO BE SEPERATED FROM DIGITAL GNDS VIA A BEAD, IF NECESSARY. ALTHOUGH, OUR DEMO BOARD DOES NOT IMPLEMENT THIS CIRCUIT CURRENTLY.
R33 0
C79 C85 C84 C70 C83 C80
0.1UF
DE-COUOLE CAPS OF RTL8139A MUST BE PLACED AS CLOSE TO CHIP AS POSSIBLE.
Size B
Document Number C:\GD\ALLINONE.DSN
REV
Date: April 27, 1999
Sheet 22 of 27



Size	Document Number	REV
B	C:\GD\ALLIN0NE.DSN	
Date: October 6, 1998	Sheet 23 of	