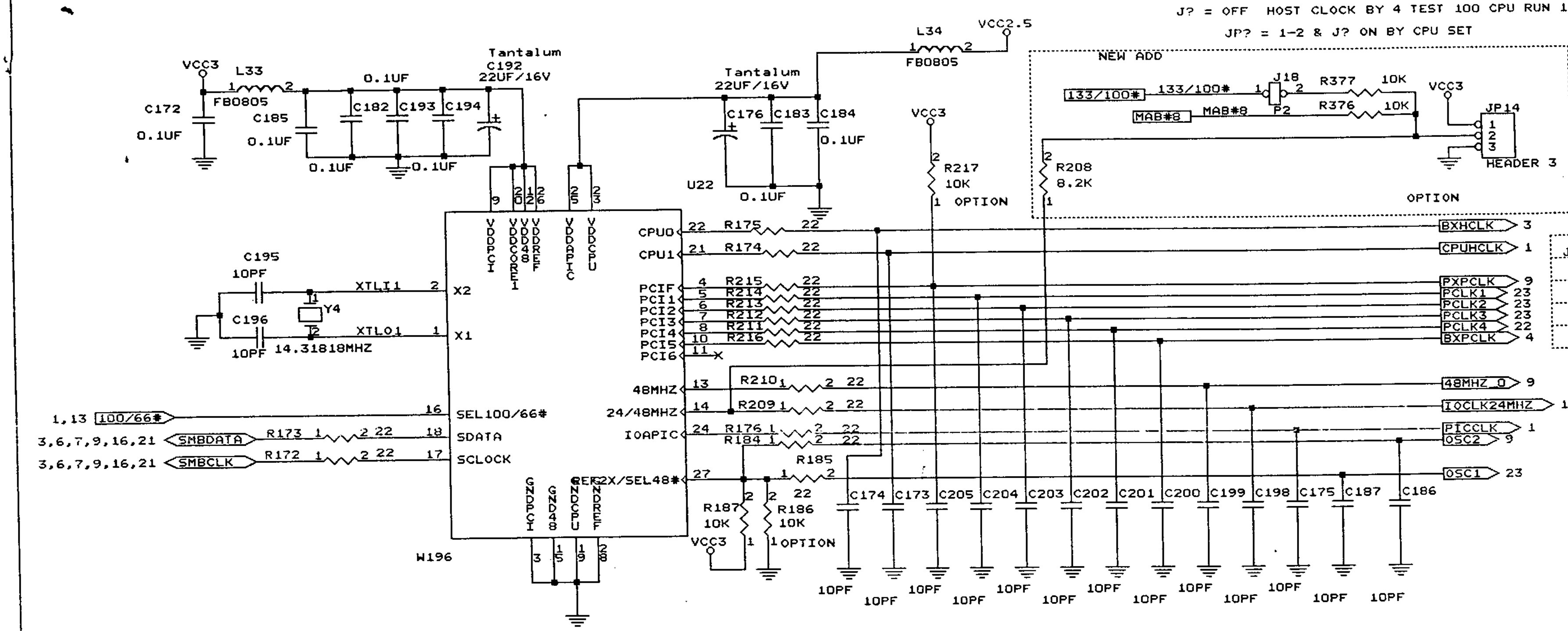
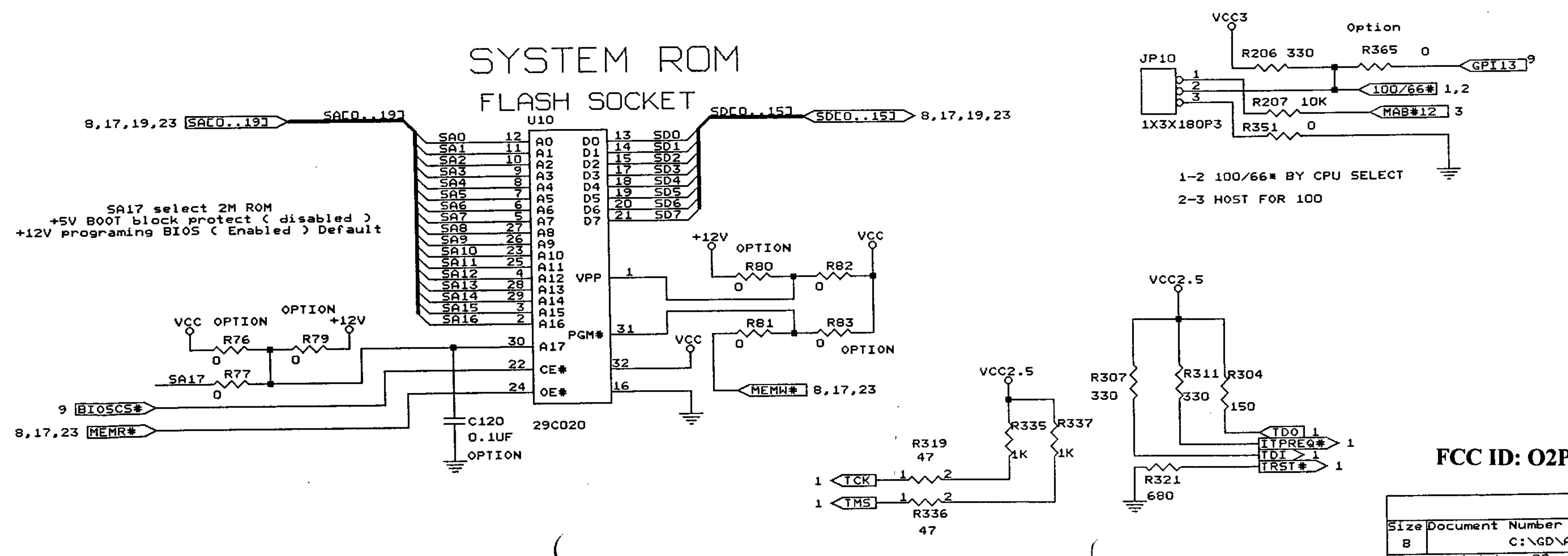
CLOCK SYNTHESIZER



JP10	JP?	CPU	PCI
1	1	133	33.3
0	1	105	35
1	0	100	33.3
0	0	66.8	33.3

SYSTEM ROM

FLASH SOCKET



FCC ID: O2PMILLENNIUM-X

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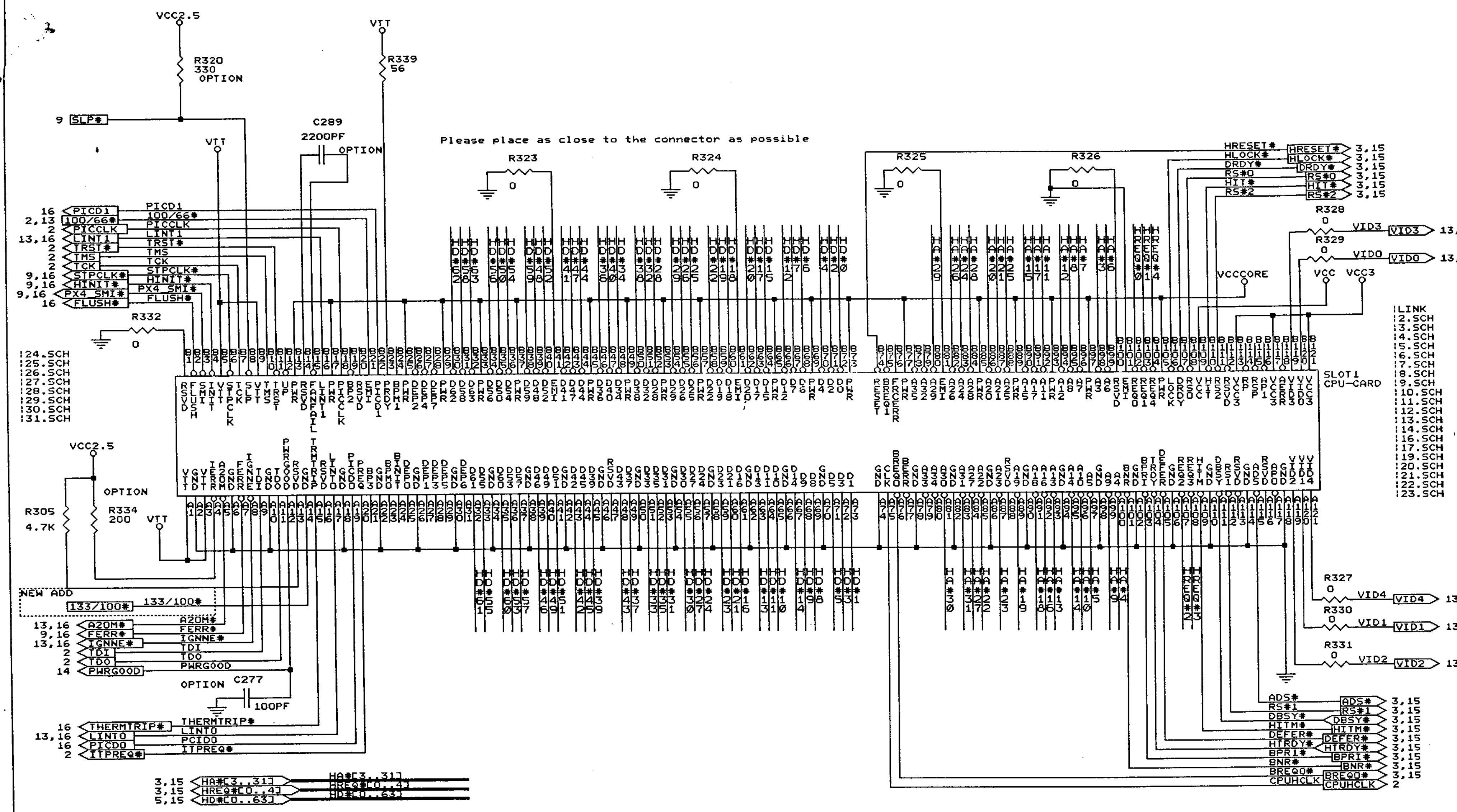
Note : This strong pullup resister on SLP# is Necessary when using an LAI



Title	440BX ATX		
Size B	Document Number SLOT1		REV A
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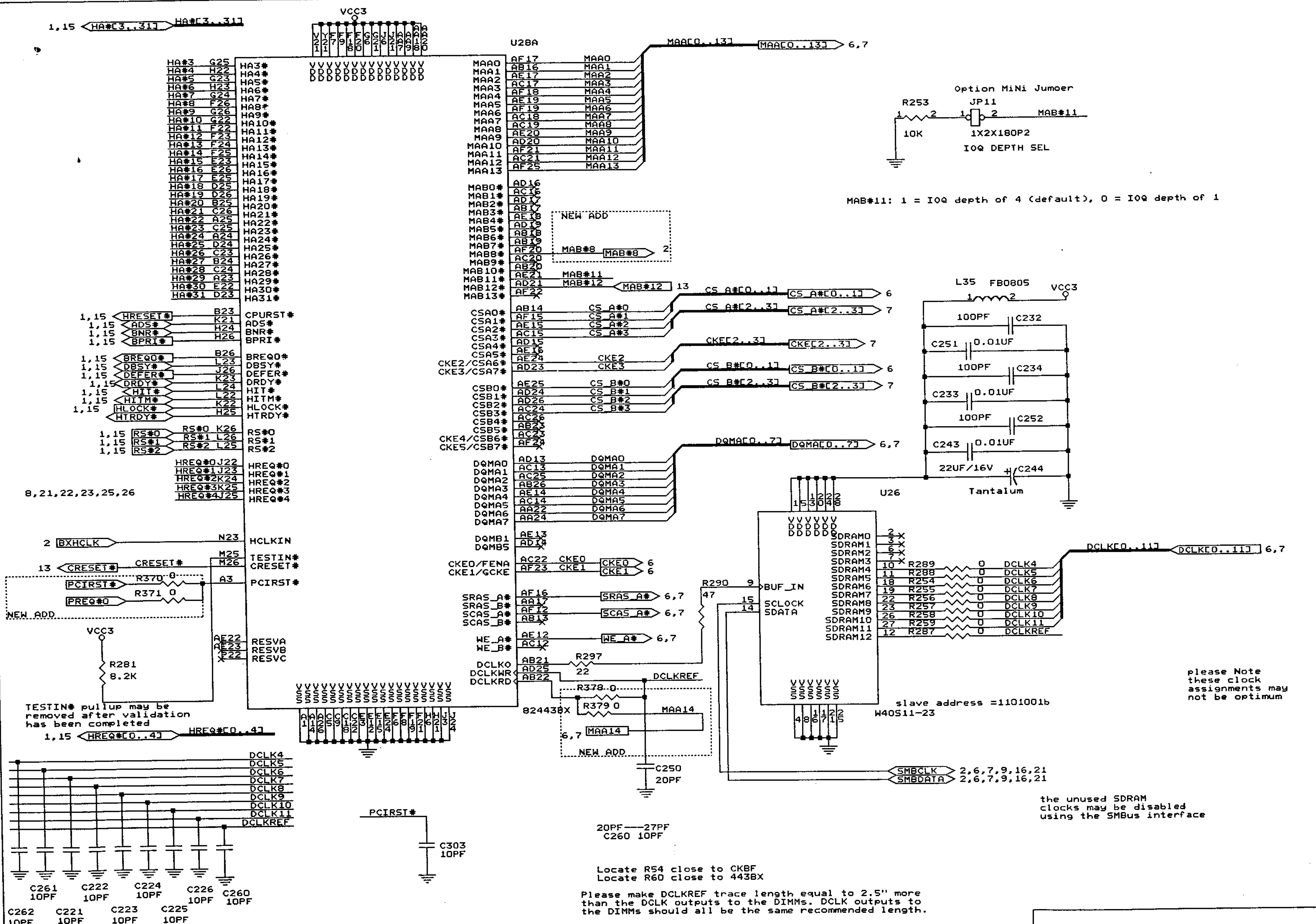

MAB#11: 1 = IOQ depth of 4 (default), 0 = IOQ depth of 1

TESTIN# pullup may be removed after validation has been completed

slave address =1101001b

please Note these clock assignments may not be optimum

the unused SDRAM clocks may be disabled using the SMBus interface

20PF----27PF
C260 10PF

Locate R54 close to CKBF
Locate R60 close to 443BX

Please make DCLKREF trace length equal to 2.5" more than the DCLK outputs to the DIMMs. DCLK outputs to the DIMMs should all be the same recommended length.

Example : if DCLK[0..11]=2.5"
then DCLKREF = 2.5" + 2.5"

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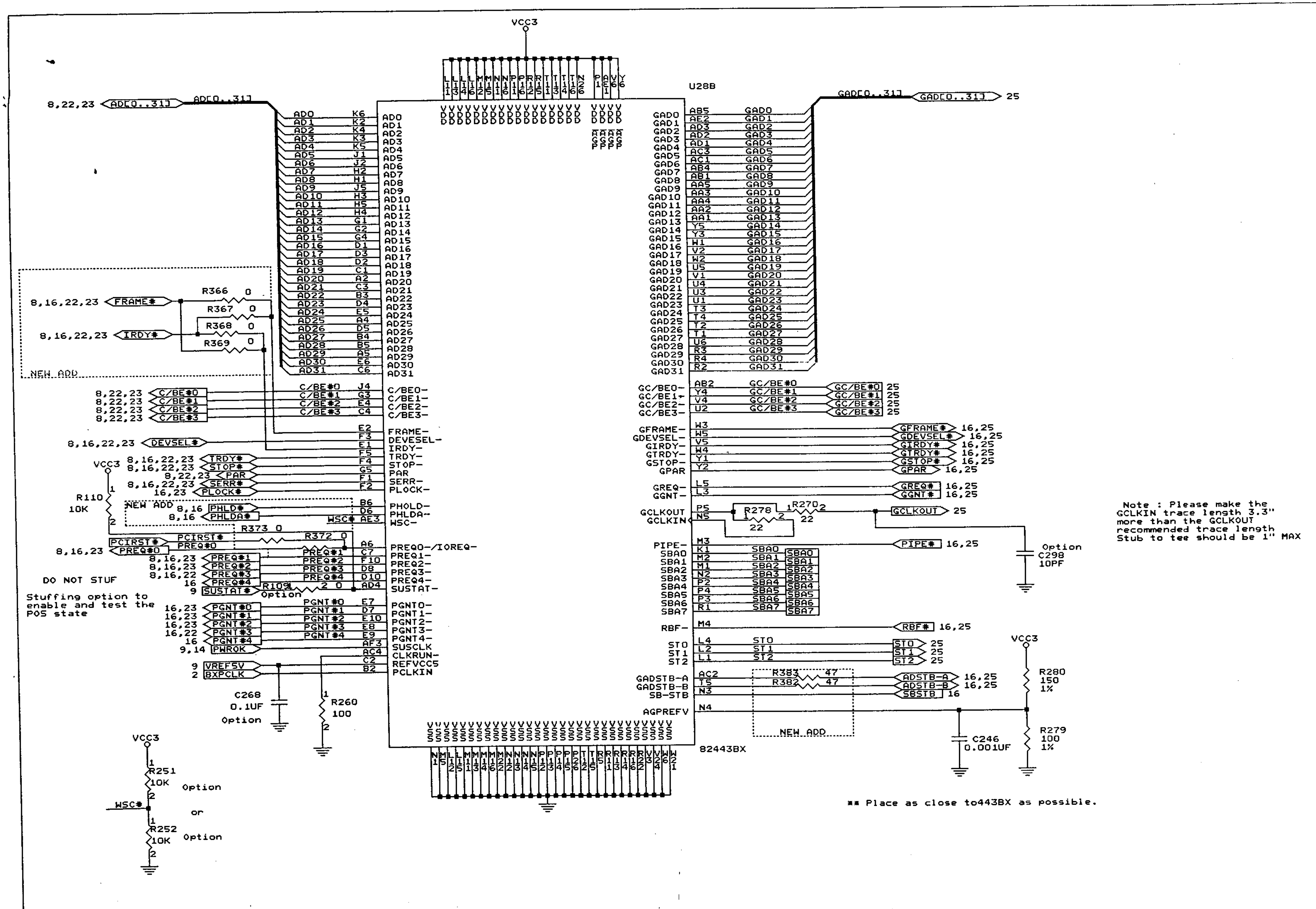

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B	C:\GD\ALLINONE.DSN		
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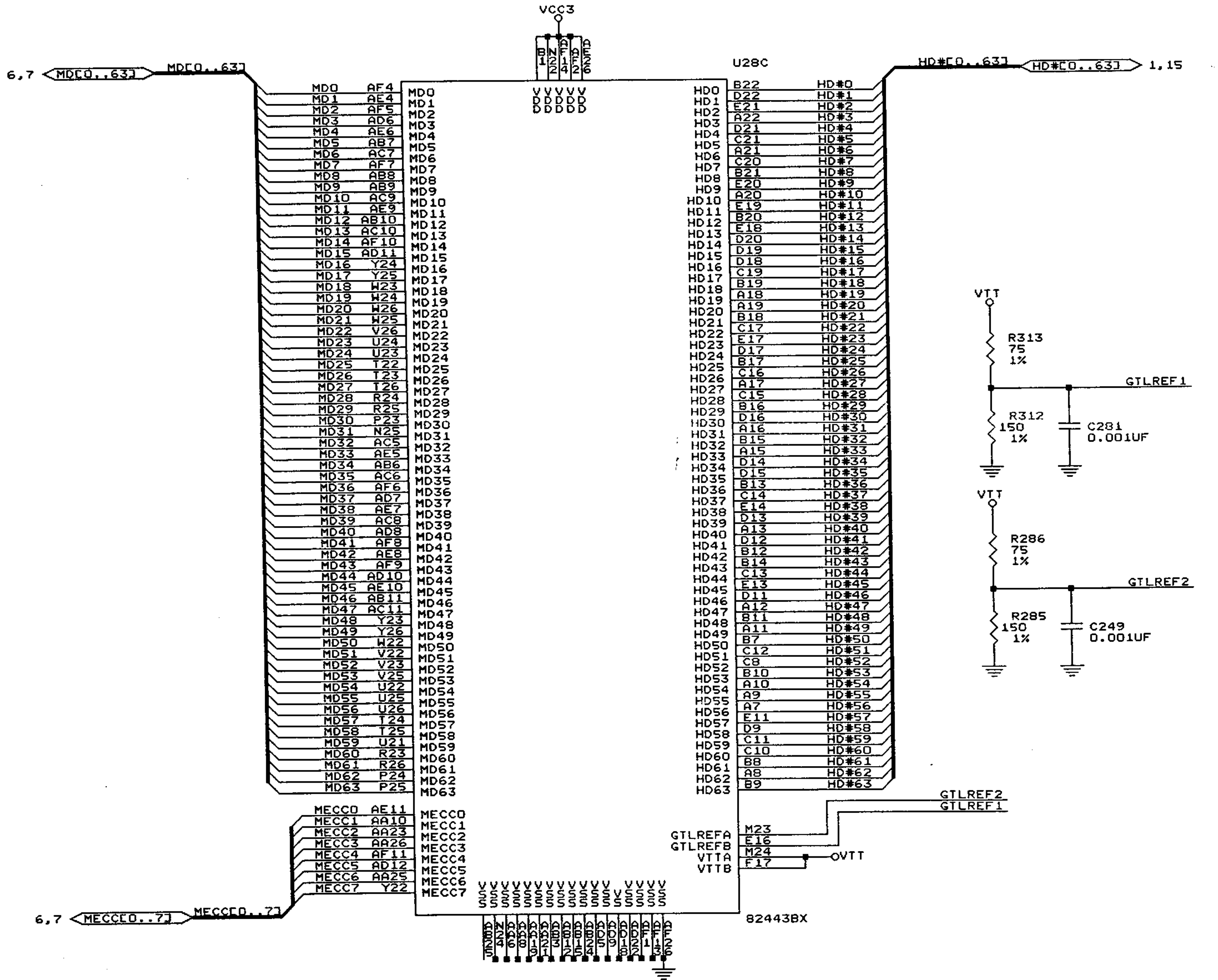

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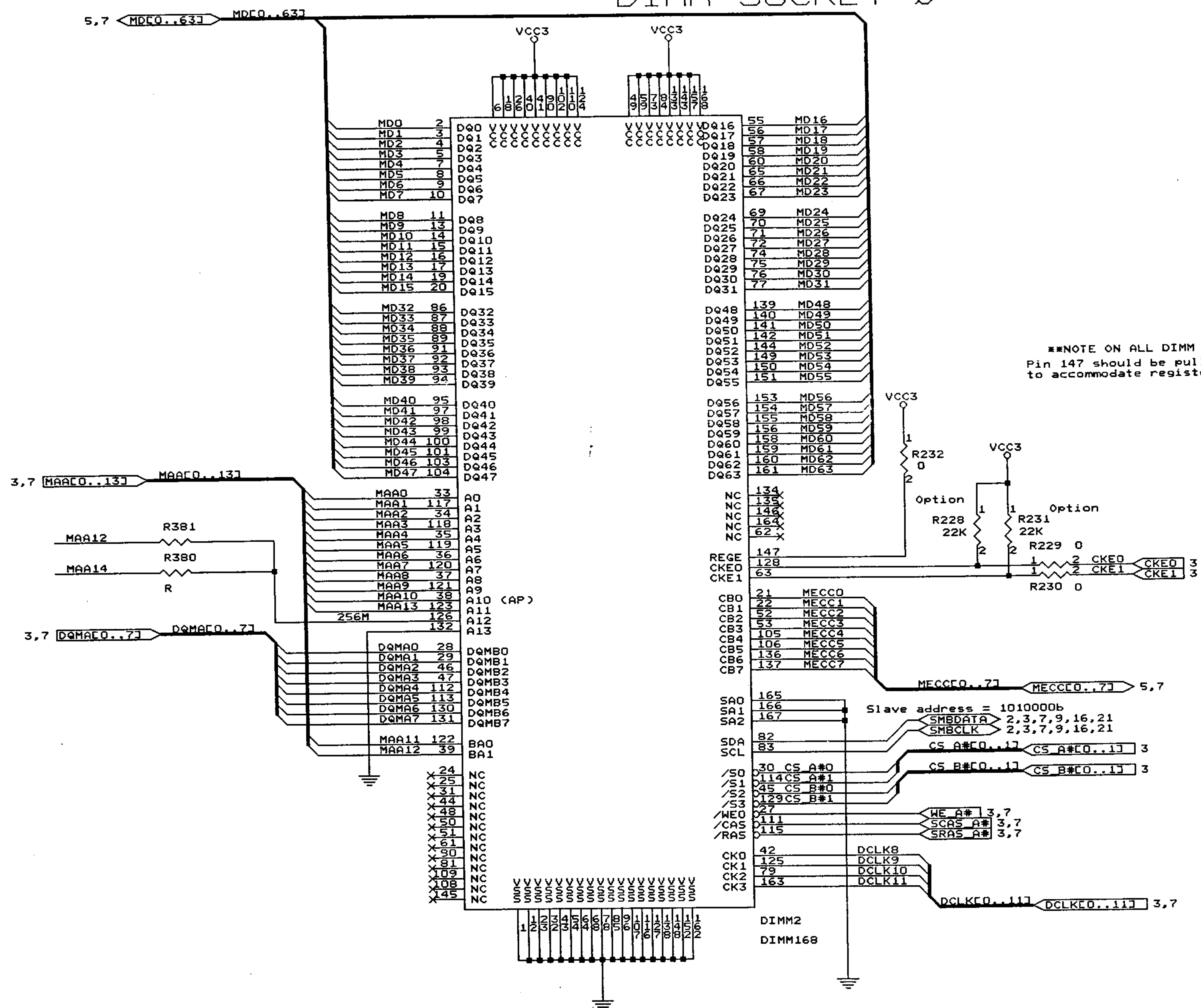
DIMM SOCKET Ø



NOTE ON ALL DIMM SOCKETS
Pin 147 should be pulled to a high state to accommodate registered DIMMs.

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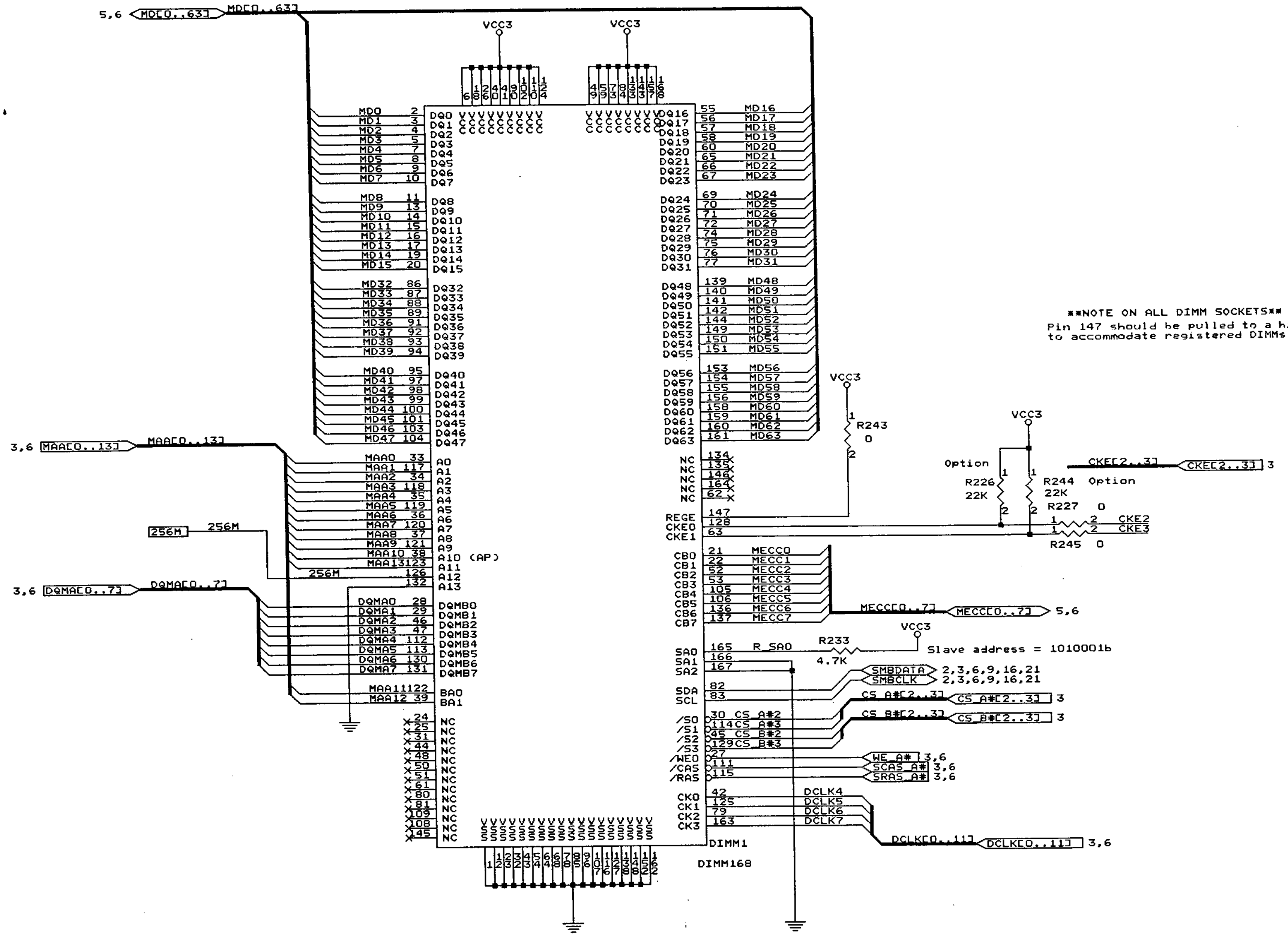
DIMM SOCKET 1



NOTE ON ALL DIMM SOCKETS
Pin 147 should be pulled to a high state to accommodate registered DIMMs.

Size	Document Number	REV
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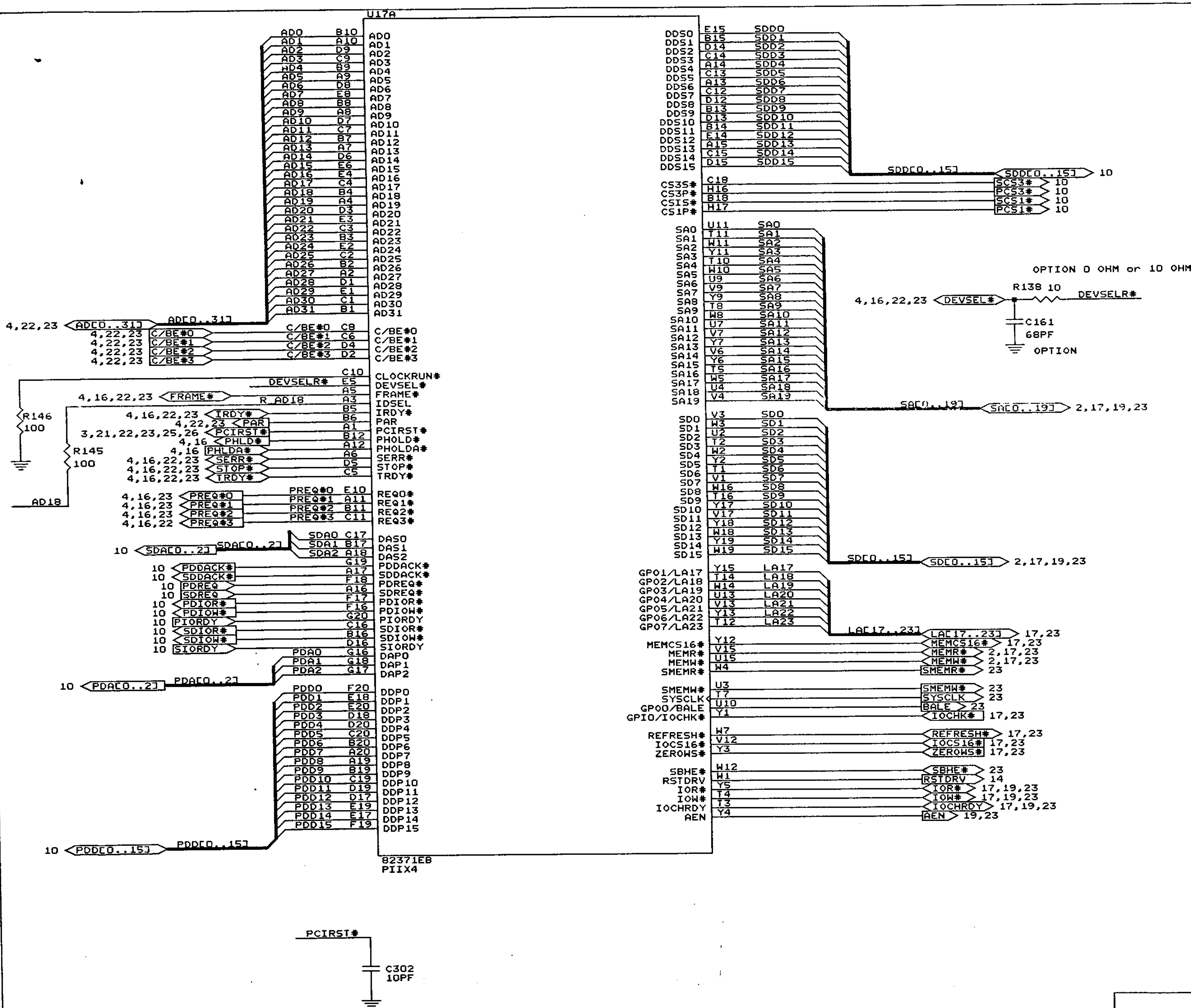

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B	C:\GD\ALLINONE.DSN	
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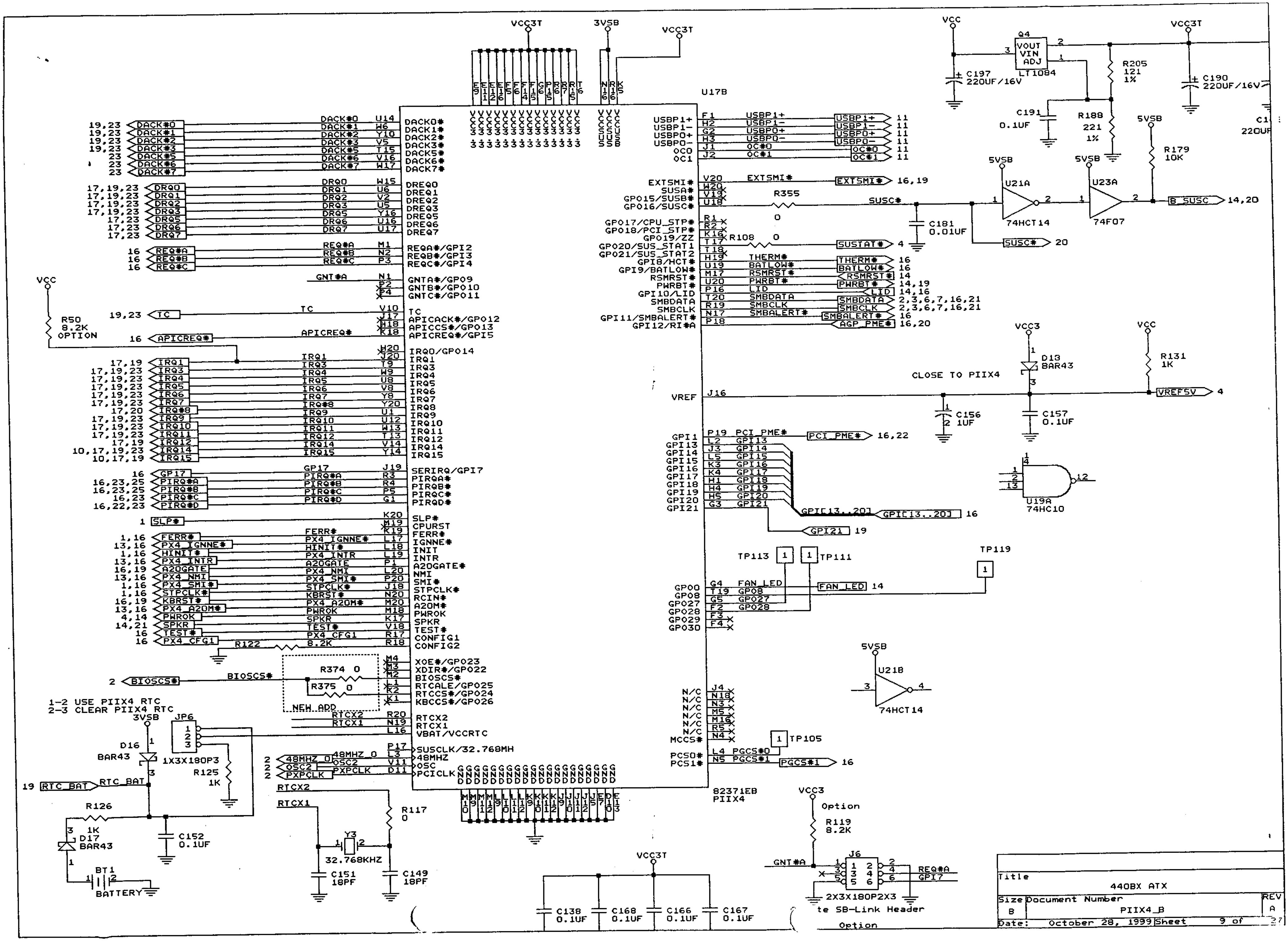

U17B
82371EB
PIIX4
VCC3T
3VSB
VCC
5VSB
VCC3
Q4
LT1084
VOUT
VIN
ADJ
C197
220UF/16V
C190
220UF/16V
R205
121
1%
R188
221
1%
C191
0.1UF
R179
10K
U21A
74HCT14
U23A
74F07
B_SUSC
14,20
SUSC#
20
R355
C181
0.01UF
EXTSMI#
16,19
SUSTAT#
R108
USBP1+
USBP1-
USBP0+
USBP0-
OC#0
OC#1
THERM#
BATLOW#
RSMRST#
PWRBT#
LID
SMBDATA
SMBCLK
SMBALERT#
AGP_PME#
2,3,6,7,16,21
16,20
14,19
14,16
CLOSE TO PIIX4
D13
BAR43
R131
1K
VREF
VREF5V
C156
1UF
C157
0.1UF
PCI_PME#
16,22
GPI[13..20]
GPI21
U19A
74HC10
TP113
TP111
TP119
FAN_LED
U21B
TP105
PGCS#1
DACK#0
DACK#1
DACK#2
DACK#3
DACK#5
DACK#6
DACK#7
DRQ0
DRQ1
DRQ2
DRQ3
DRQ5
DRQ6
DRQ7
REQ#A
REQ#B
REQ#C
GNT#A
TC
APICREQ#
R50
8.2K
OPTION
IRQ1
IRQ3
IRQ4
IRQ5
IRQ6
IRQ7
IRQ#8
IRQ9
IRQ10
IRQ11
IRQ12
IRQ14
IRQ15
GPI7
PIRQ#A
PIRQ#B
PIRQ#C
PIRQ#D
SLP#
FERR#
PX4_IGNNE#
HINIT#
PX4_INTR
A20GATE
PX4_NMI
PX4_SMI#
STPCLK#
KBRST#
PX4_A20M#
PWROK
SPKR
TEST#
PX4_CFG1
R122
8.2K
BIOSCS#
R374 0
R375 0
NEW ADD
1-2 USE PIIX4 RTC
2-3 CLEAR PIIX4 RTC
JP6
1X3X180P3
R125
1K
D16
BAR43
RTC_BAT
R126
1K
D17
BAR43
BT1
BATTERY
C152
0.1UF
48MHZ_0
OSC2
PXPCLK
RTCX1
RTCX2
R117
0
Y3
32.768KHZ
C151
18PF
C149
18PF
C138
0.1UF
C168
0.1UF
C166
0.1UF
C167
0.1UF
R119
8.2K
Option
J6
2X3X180P2X3
te SB-Link Header
Title
440BX ATX
Size B
Document Number
PIIX4_B
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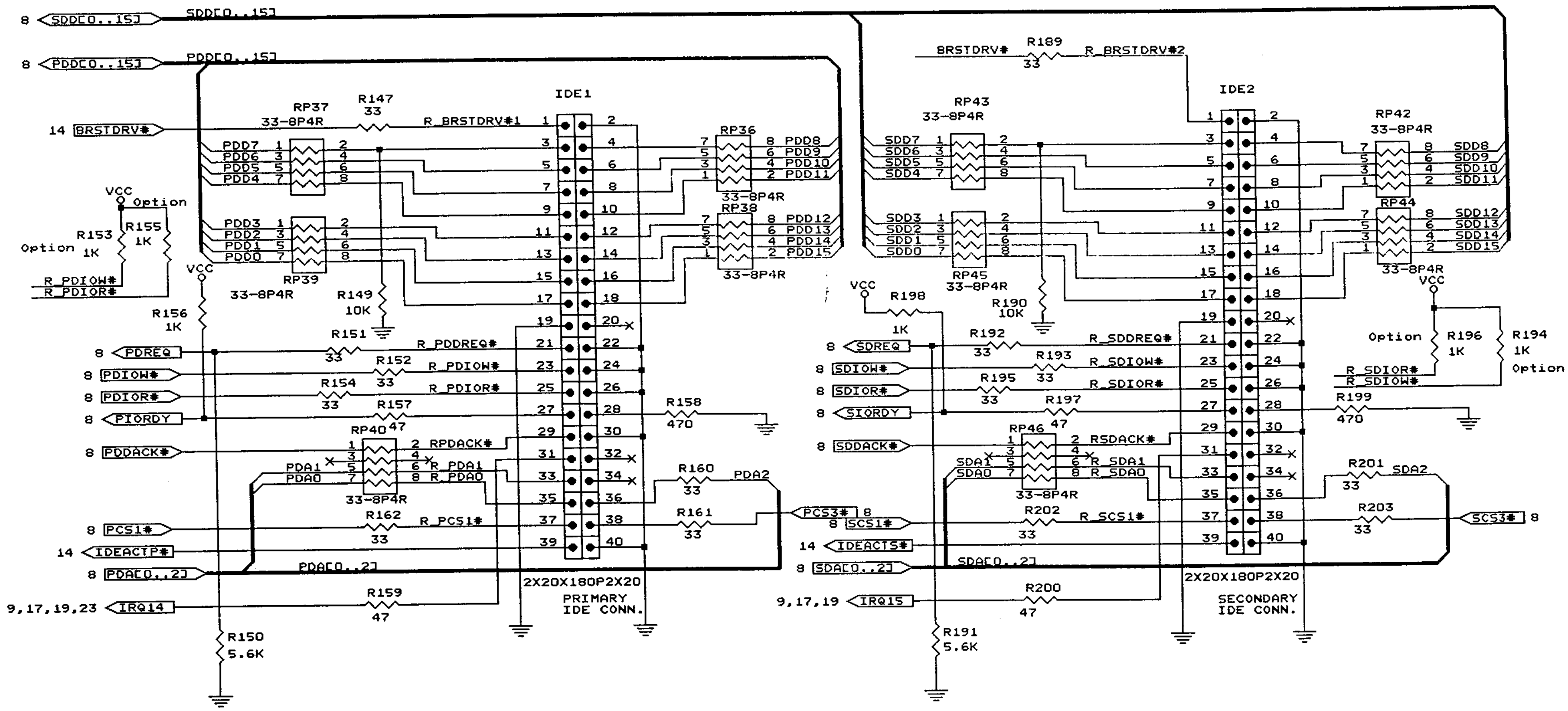
IDE CONNECTORS



Size	Document Number	REV
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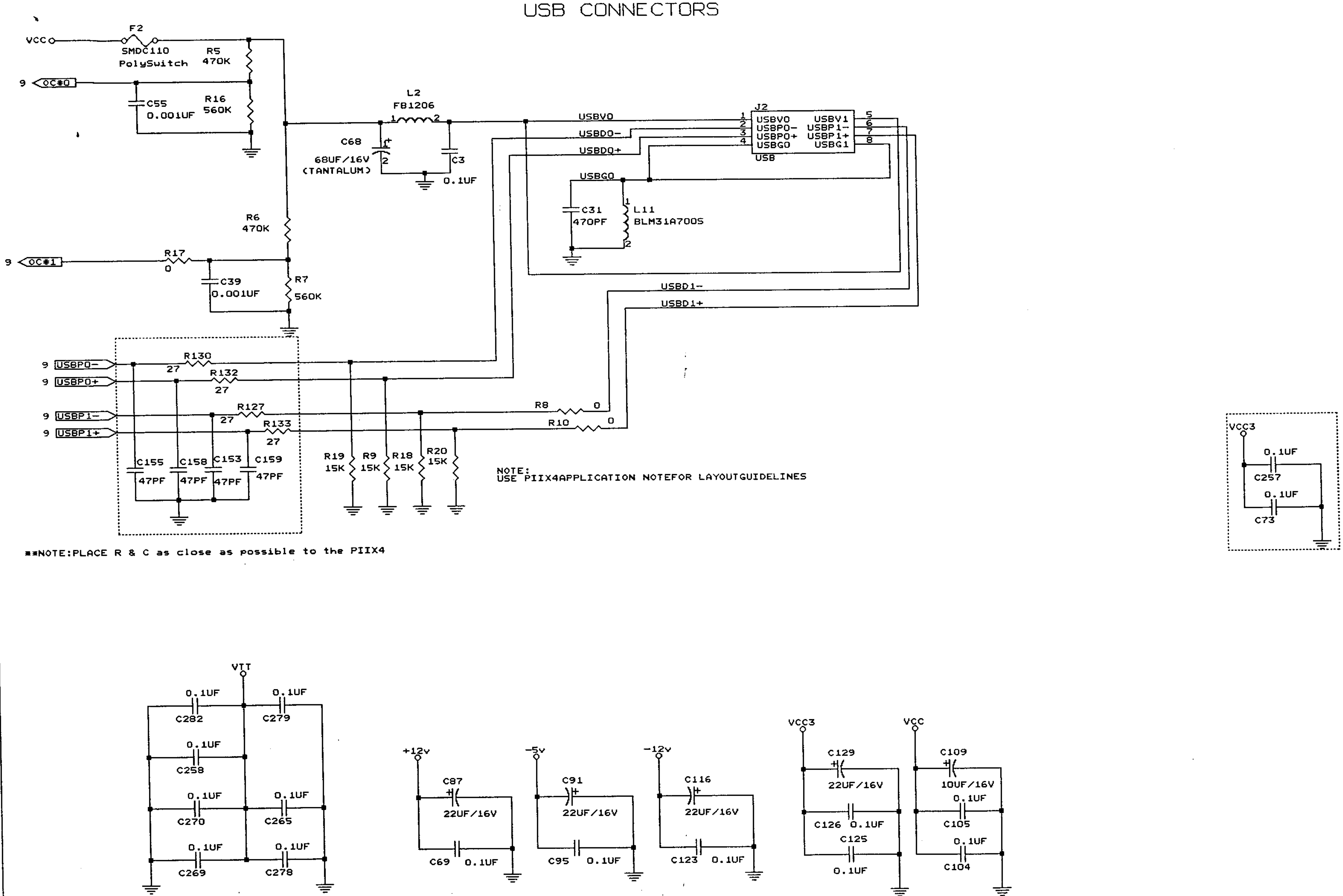
USB CONNECTORS



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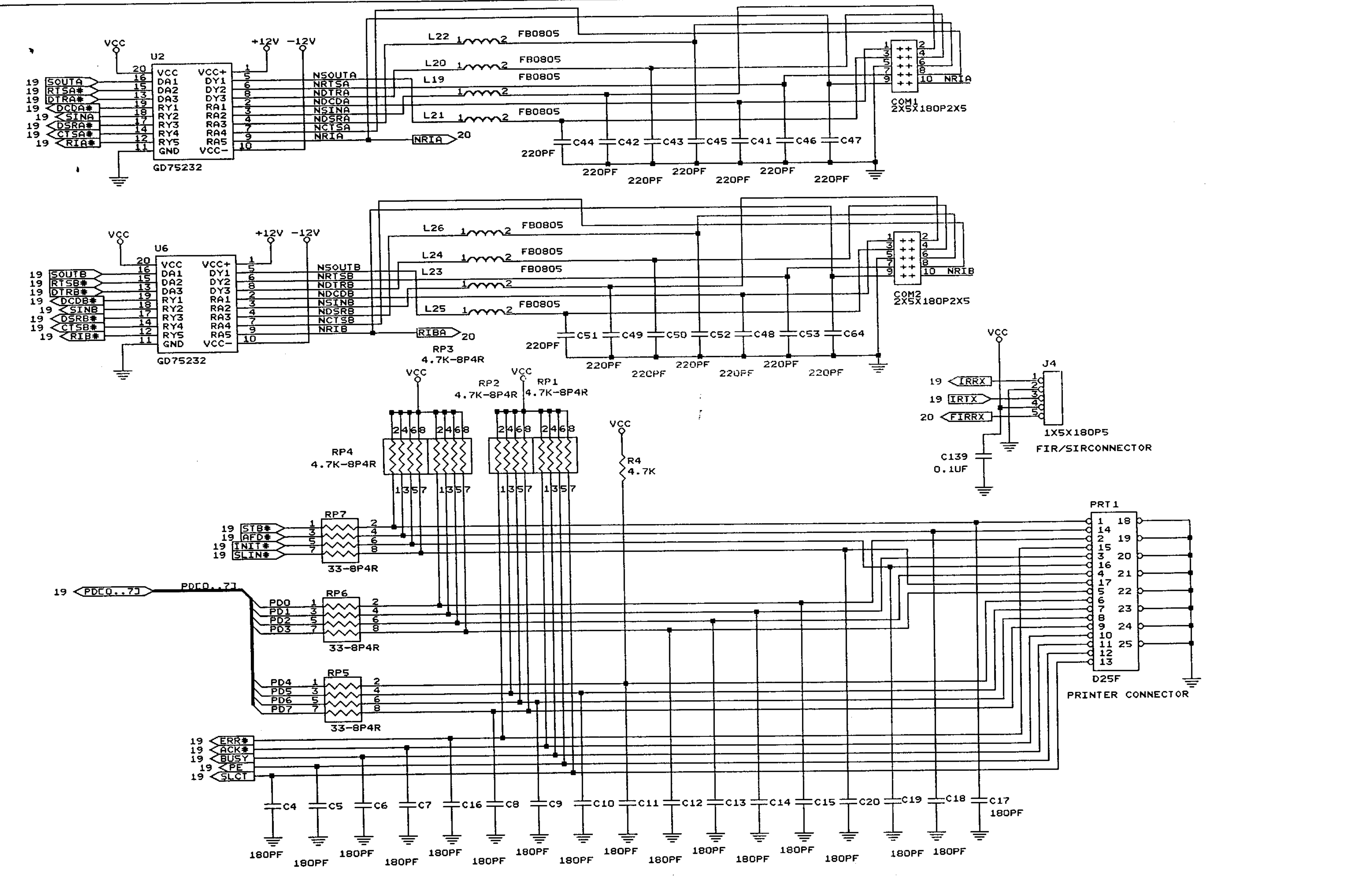

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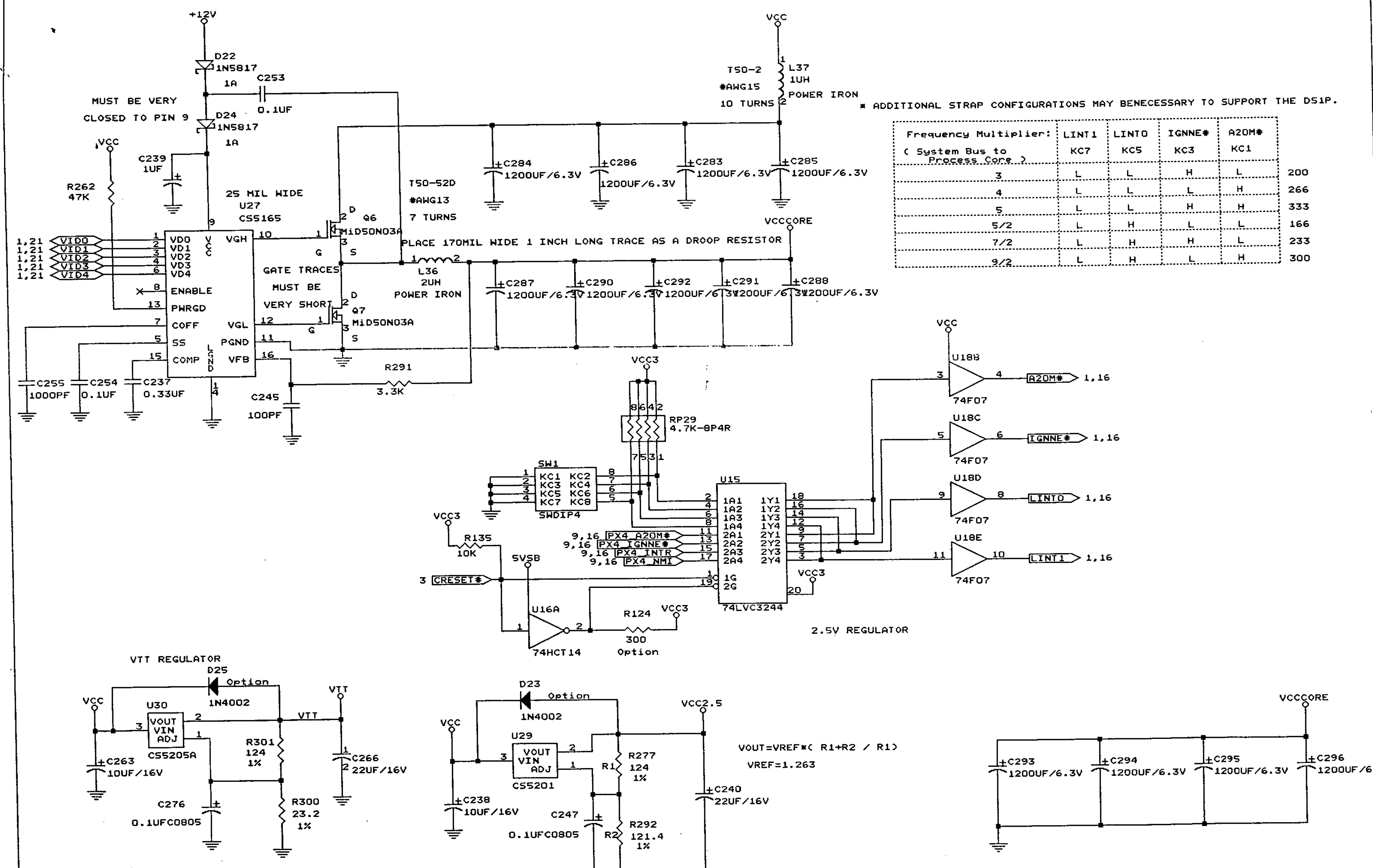
INPUT CHOKE IS OPTIONAL DEPENDED ON THE LAYOUT AND HOW FAR AWAY FROM THE POWERCONNECTOR



* ADDITIONAL STRAP CONFIGURATIONS MAY BENECESSARY TO SUPPORT THE DS1P.

Frequency Multiplier: (System Bus to Process Core)	LINT1 KC7	LINT0 KC5	IGNNE# KC3	A20M# KC1	
3	L	L	H	L	200
4	L	L	L	H	266
5	L	L	H	H	333
5/2	L	H	L	L	166
7/2	L	H	H	L	233
9/2	L	H	L	H	300

VOUT=VREF*(R1+R2 / R1)
VREF=1.263

NOTE VOLTAGEREGULATOR SHOULDBE LOCATED NEARTHE 440BX

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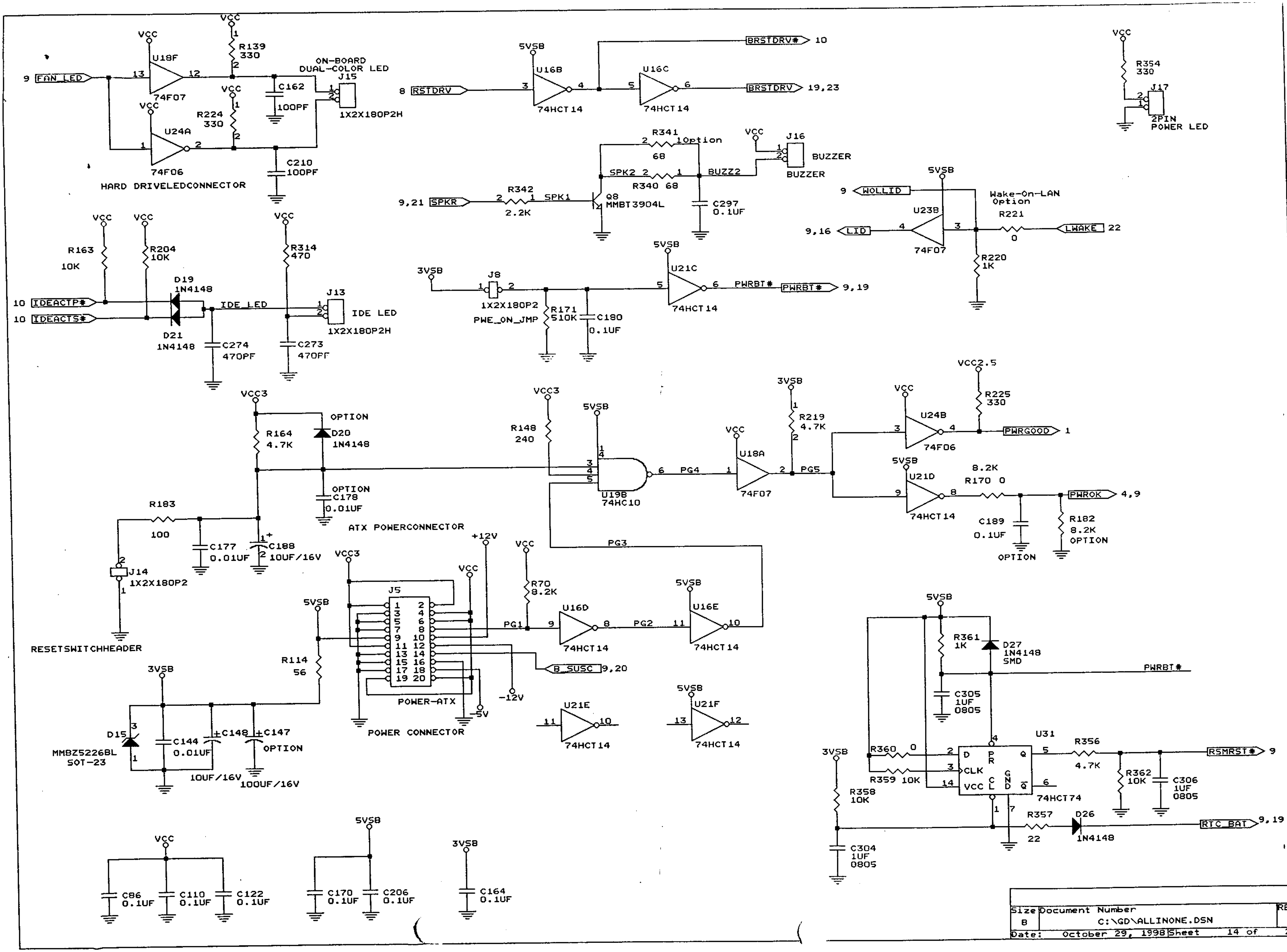
HARD DRIVELEDCONNECTOR
FAN_LED
U18F 74F07
U24A 74F06
R139 330
R224 330
C162 100PF
C210 100PF
ON-BOARD DUAL-COLOR LED
J15 1X2X180P2H
RSTDRV
U16B 74HCT14
U16C 74HCT14
BRSTDRV# 10
BRSTDRV 19,23
R354 330
J17 2PIN POWER LED
R341 10ption 68
R340 68
SPK2
BUZZ2
J16 BUZZER
BUZZER
SPKR
R342 2.2K
SPK1
Q8 MMBT3904L
C297 0.1UF
WOLLID
Wake-On-LAN Option
U23B 74F07
R221 0
LWAKE 22
LID
R220 1K
R163 10K
R204 10K
R314 470
D19 1N4148
D21 1N4148
IDEACTP#
IDEACTS#
IDE_LED
J13 1X2X180P2H IDE LED
C274 470PF
C273 470PF
3VSB
J8 1X2X180P2
PWE_ON_JMP
R171 510K
C180 0.1UF
U21C 74HCT14
PWRBT#
VCC3
R164 4.7K
D20 1N4148 OPTION
C178 0.01UF OPTION
R148 240
U19B 74HC10
PG4
U18A 74F07
PG5
R219 4.7K
VCC2.5
R225 330
U24B 74F06
PWRGOOD 1
U21D 74HCT14
R170 0 8.2K
PWROK 4,9
C189 0.1UF OPTION
R182 8.2K OPTION
R183 100
C177 0.01UF
C188 10UF/16V
J14 1X2X180P2
RESETSWITCHHEADER
ATX POWERCONNECTOR
+12V
J5 POWER-ATX
POWER CONNECTOR
R70 8.2K
PG1
U16D 74HCT14
PG2
U16E 74HCT14
PG3
B_SUSC 9,20
-12V
-5V
R114 56
5VSB
D15 MMBZ5226BL SOT-23
C144 0.01UF
C148 10UF/16V
C147 OPTION 100UF/16V
U21E 74HCT14
U21F 74HCT14
R361 1K
D27 1N4148 SMD
C305 1UF 0805
U31 74HCT74
R360 0
R359 10K
R356 4.7K
R362 10K
C306 1UF 0805
RSMRST# 9
R358 10K
C304 1UF 0805
R357 22
D26 1N4148
RTC_BAT 9,19
C86 0.1UF
C110 0.1UF
C122 0.1UF
C170 0.1UF
C206 0.1UF
C164 0.1UF
Size B
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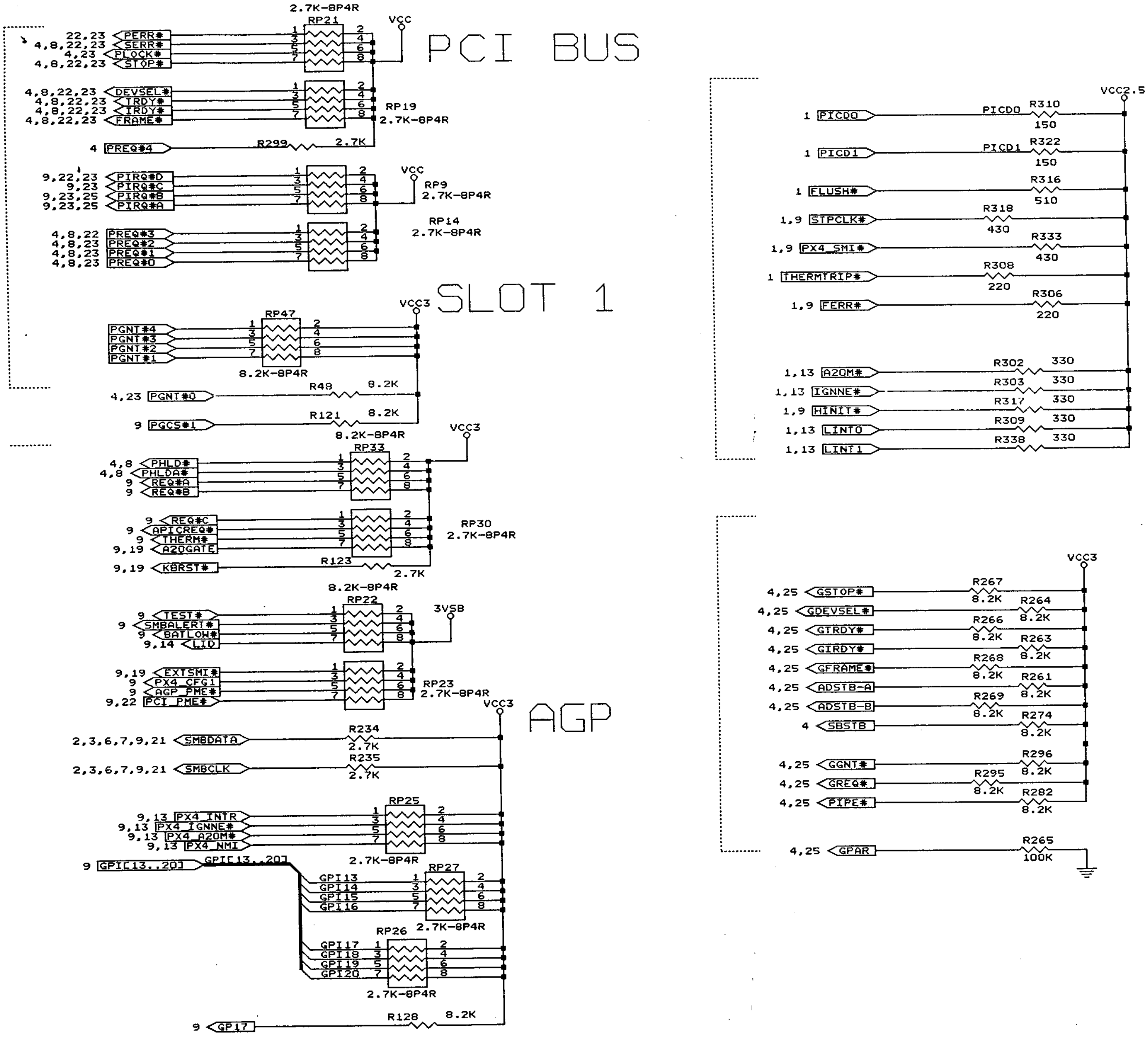

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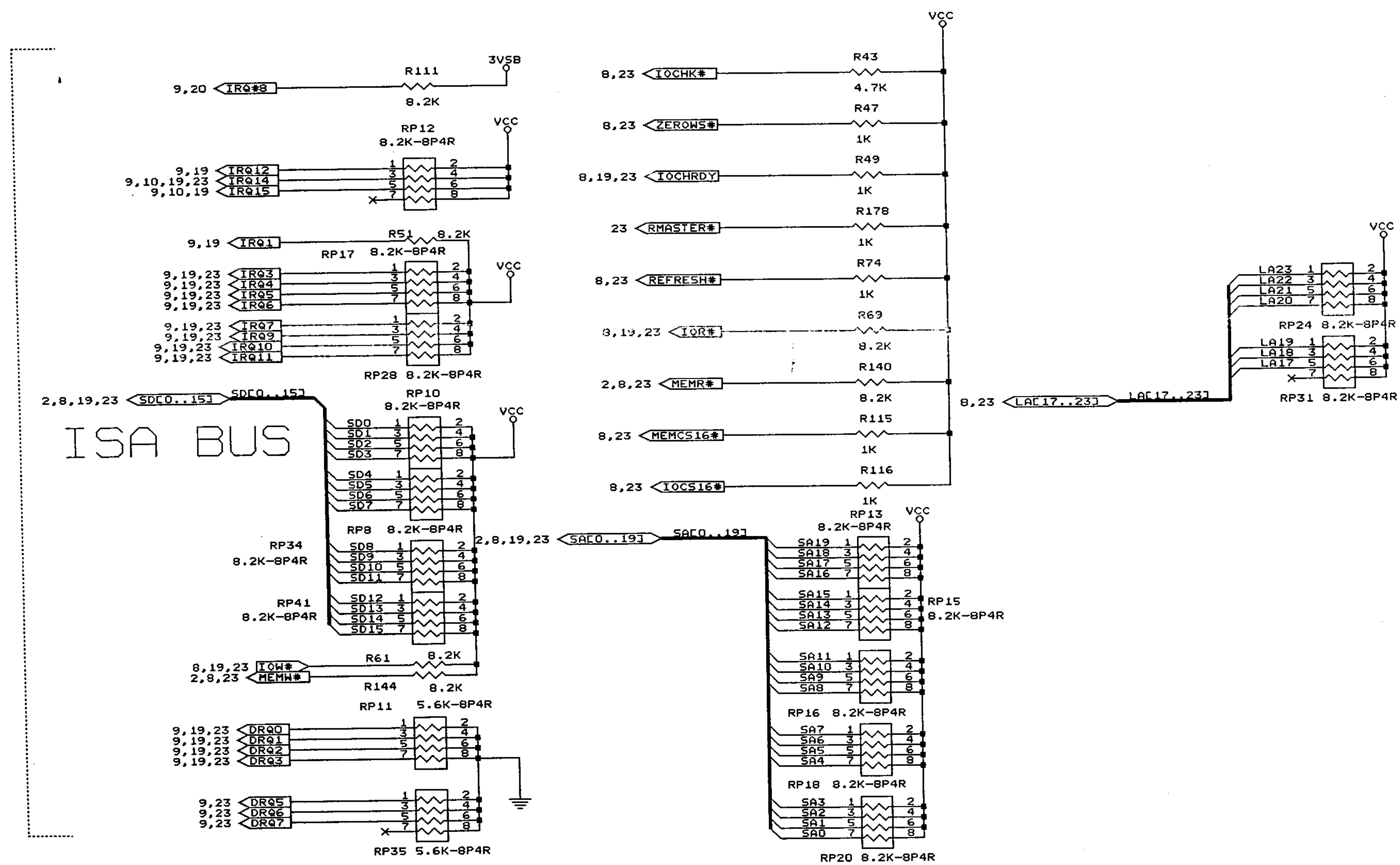

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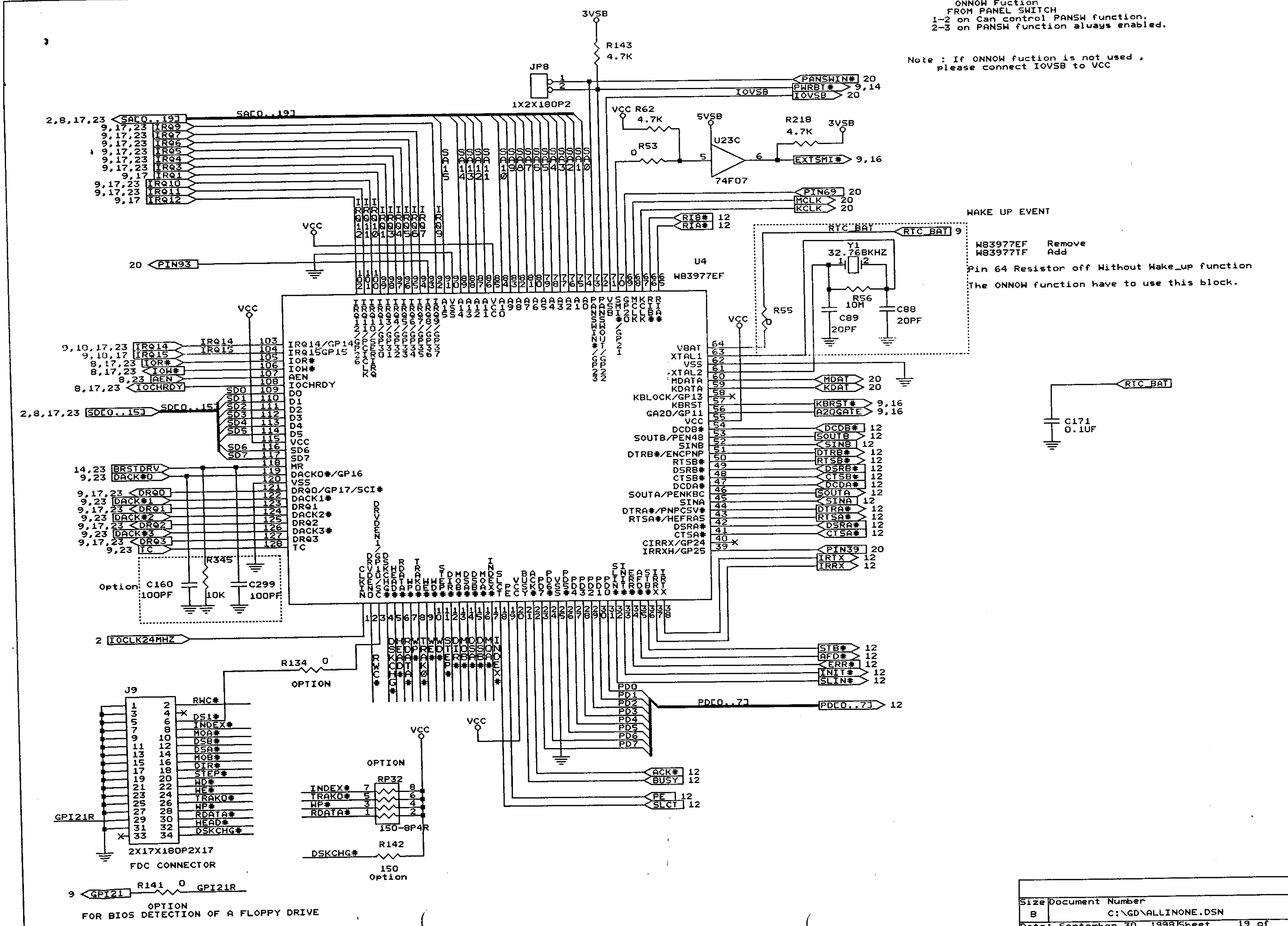
ONNOW Fuction
FROM PANEL SWITCH
1-2 on Can control PANSW function.
2-3 on PANSW function always enabled.

Note : If ONNOW fuction is not used ,
please connect IOVSB to VCC



WAKE UP EVENT

W83977EF Remove
W83977TF Add

Pin 64 Resistor off Without Wake_up function

The ONNOW function have to use this block.

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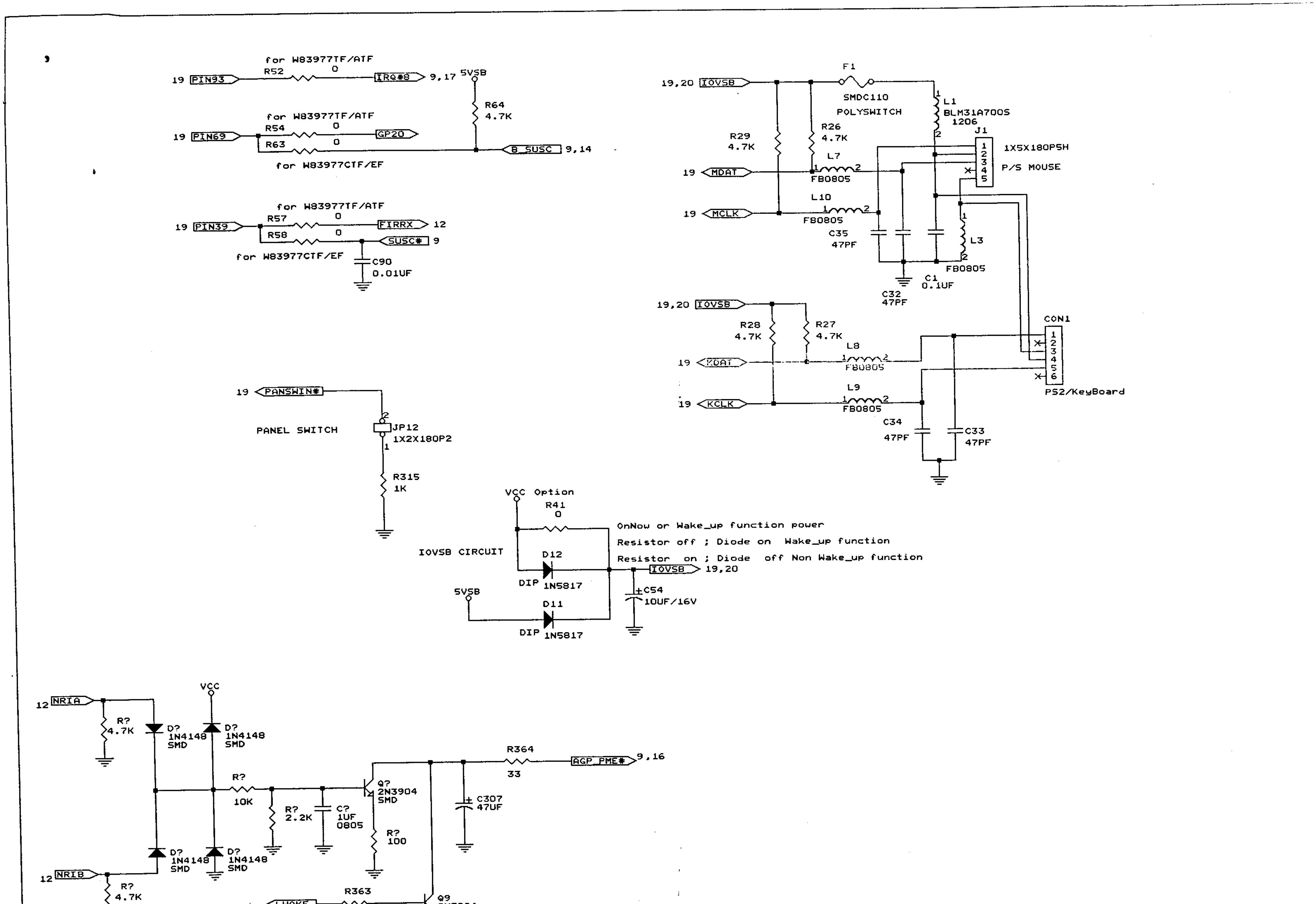

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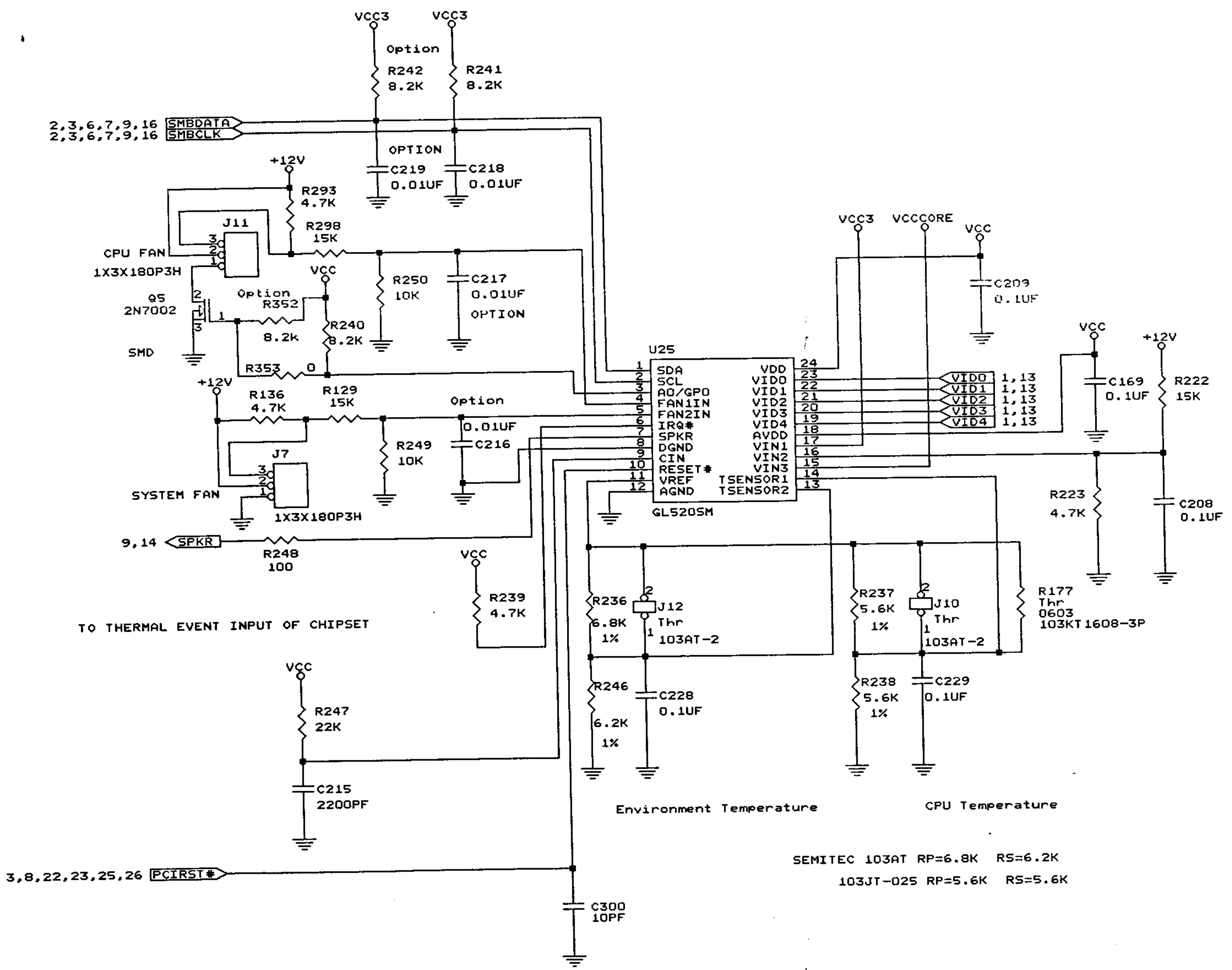

Size	Document Number		REV
B	C:\GD\ALLINONE.DSN		
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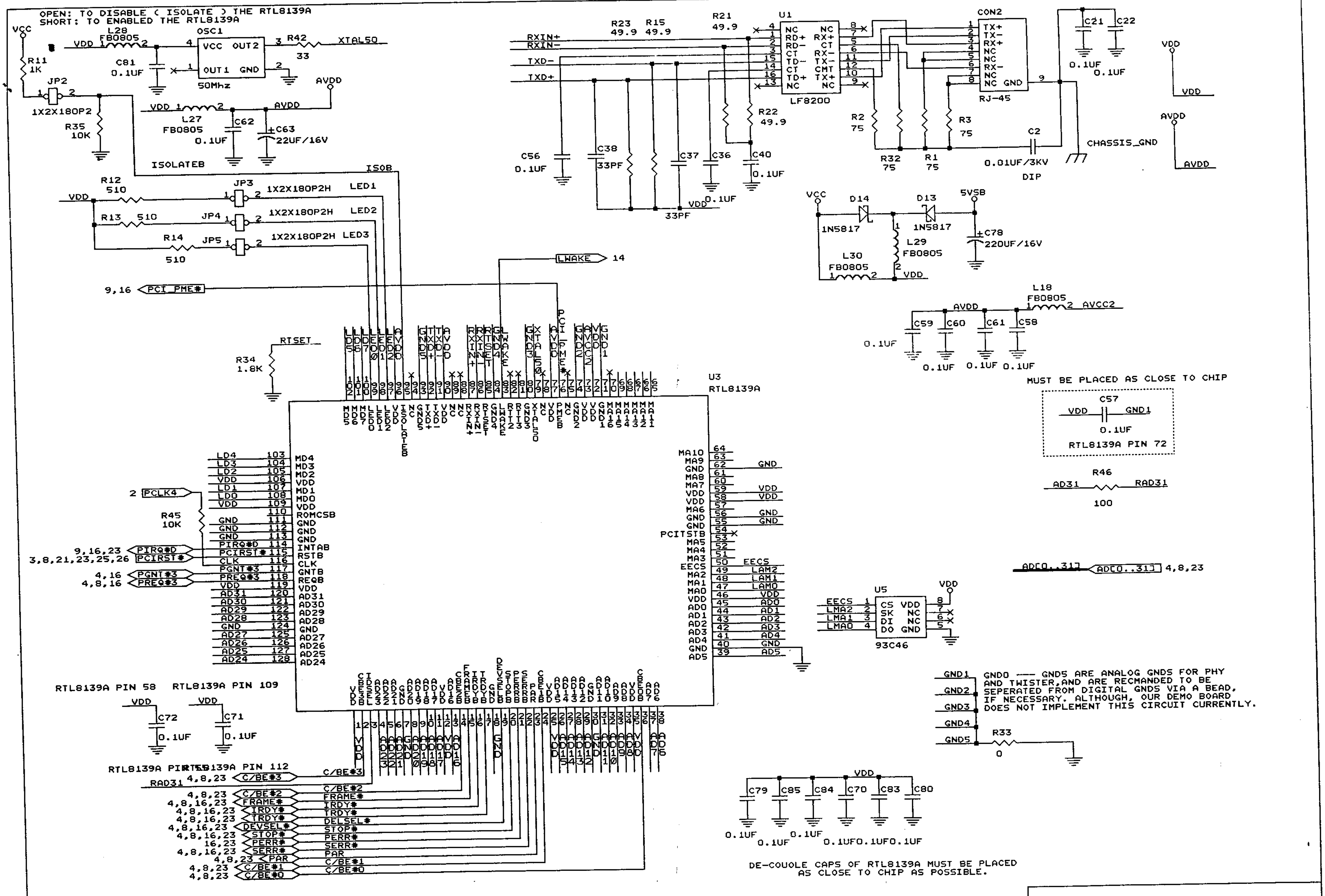

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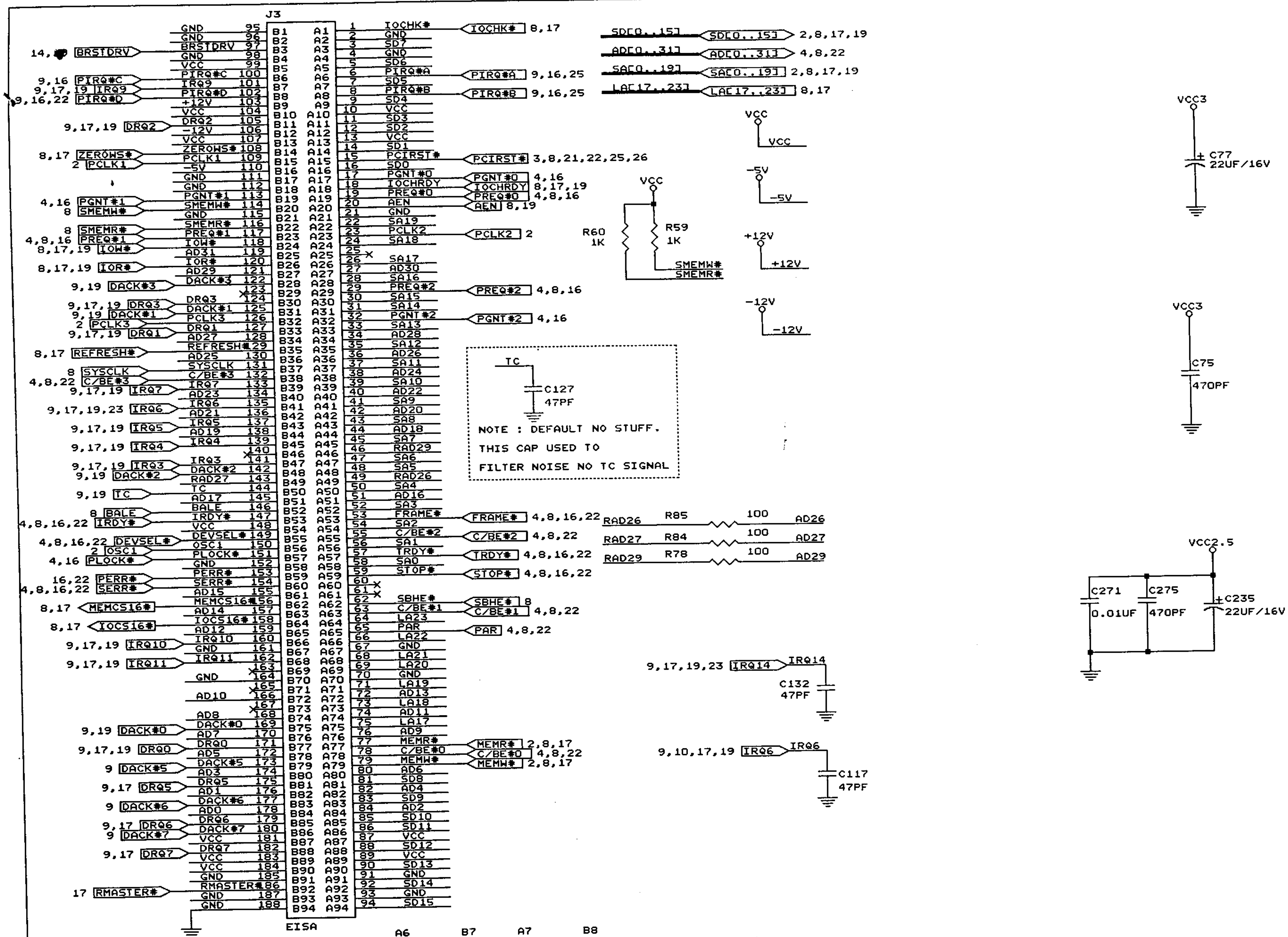

					A6	B7	A7	B8
PCI1 IDSEL	A49	AD26	PREQ#0	PGNT#0	PIRQ#A	PIRQ#B	PIRQ#C	PIRQ#D
PCI2 IDSEL	B49	AD27	PREQ#1	PGNT#1	PIRQ#B	PIRQ#C	PIRQ#D	PIRQ#A
PCI3 IDSEL	A46	AD29	PREQ#2	PGNT#2	PIRQ#C	PIRQ#D	PIRQ#A	PIRQ#B
LANWORK at PCI4 IDSEL		AD31	PREQ#3	PGNT#3	PIRQ#D	PIRQ#A	PIRQ#B	PIRQ#C

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