

Telink

User Manual for TL3225B Development Board

UM-TL3225B-E1

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Keyword

TL3225B, Bluetooth[®] LE, 2.4 GHz, Channel Sounding, CAN, LIN

Brief

This document is the development board user manual of Telink multi-standard wireless SoC TL3225B. It mainly introduces the development board block diagram, development board features, various peripheral interfaces and detailed function descriptions.

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1 Overview

The TL3225B development board is designed based on the TL3225B chip and is used to verify the TL3225x series chips. It can be used to verify the following chips:

- TL3225B
- TL3225C

The TL3225B is a wireless SoC for Bluetooth® LE 6.0. This chip supports industrial alliance standards including Bluetooth® LE and 2.4GHz proprietary standard.

This development board supports testing of various functions, such as RF conduction test, current test, CAN and LIN input and output test, audio input and output test, combination of lights and buttons, and so on.

This document provides a detailed description of the TL3225B development board's interfaces, power supply, debugging methods, audio sockets, buttons, lights, jumpers, and others to make it easy for users to familiarize with this board and use it for subsequent development and debugging.

1.1 Block Diagram

The top and bottom view of the TL3225B development board are shown as below.

Figure 1-1 Top View of TL3225B Development Board

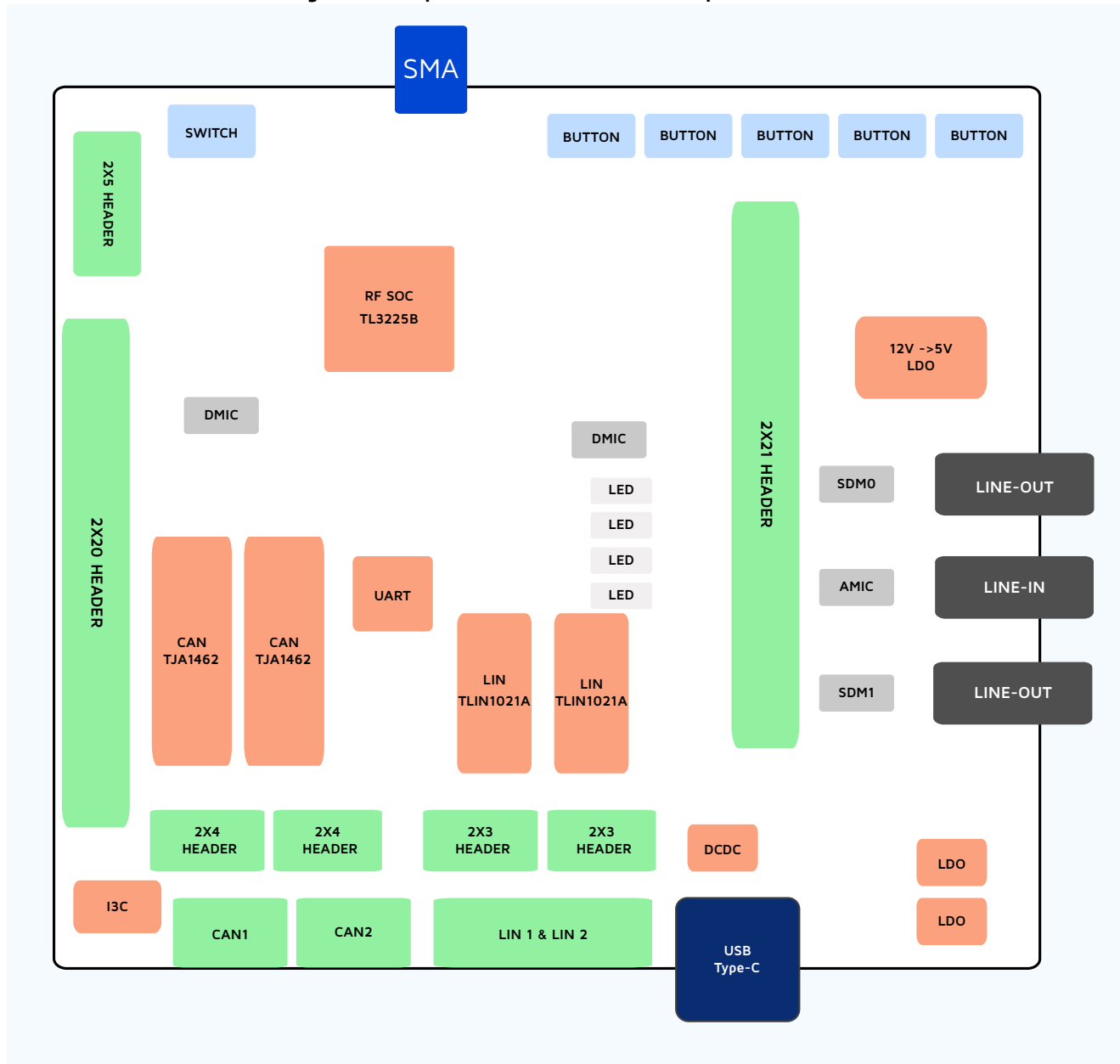
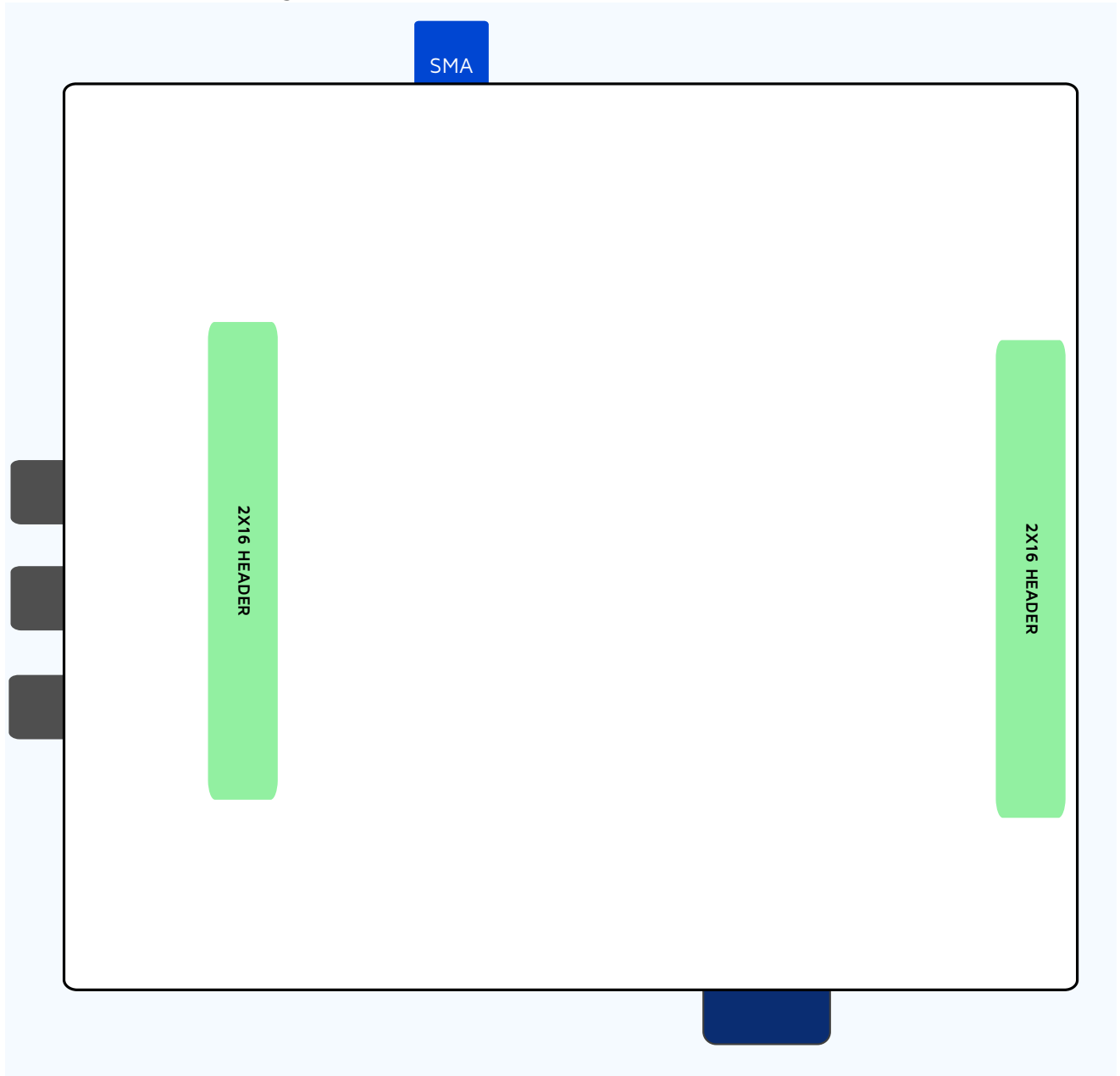


Figure 1-2 Bottom View of TL3225B Development Board



1.2 Board Features

The following table lists the features of the TL3225B development board.

Table 1-1 Board Features

No.	Name	Description	Reference section
1	Current test interface	Total current test and each branch current test via jumper combinations	2.3 Current Measurement
2	RF interface	RF conduction test via SMA connector	2.4 RF Test
3	Debug interface	Supports 2-wire SDP and 4-wire JTAG interface Supports single wire interface	2.2 Debug Interface
4	GPIO interface	Supports flexible connection of all GPIOs	2.5 GPIO Interface
5	Peripheral interface	Supports peripherals such as buttons, LEDs, DMIC, AMIC, USB-to-UART, CAN, LIN, etc.	2.6 Peripheral Interface - USB-To-UART 2.7 Peripheral Interface - CAN 2.8 Peripheral Interface - LIN 2.9 Peripheral Interface - 32.768KHz Crystal 2.10 Peripheral Interface - DMIC 2.11 Peripheral Interface - I3C
6	Uplink interface	Supports differential uplink testing	2.12 Uplink Interface
7	Downlink interface	Supports SDM differential downlink testing	2.13 Downlink Interface

1.3 Kit List

The following table lists the main materials in this development kit.

Table 1-2 Kit List

No.	Name	Quantity
1	TL3225B development board	1
2	Whip antenna	1
3	USB 2.0 Type-A to Type-C cable	1

The following picture shows the default state of the board for user verification.

This image shows the custom PCB for the Raspberry Pi 4 Model B. The board is populated with various components, including the Raspberry Pi 4 SoC, 8GB LPDDR4-3200 memory, and a 5V USB Type-C connector. The board also features a 3.5mm audio jack, a 4-pin I2C header, and a 10-pin UART header. The PCB is populated with various components, including the Raspberry Pi 4 SoC, 8GB LPDDR4-3200 memory, and a 5V USB Type-C connector. The board also features a 3.5mm audio jack, a 4-pin I2C header, and a 10-pin UART header.

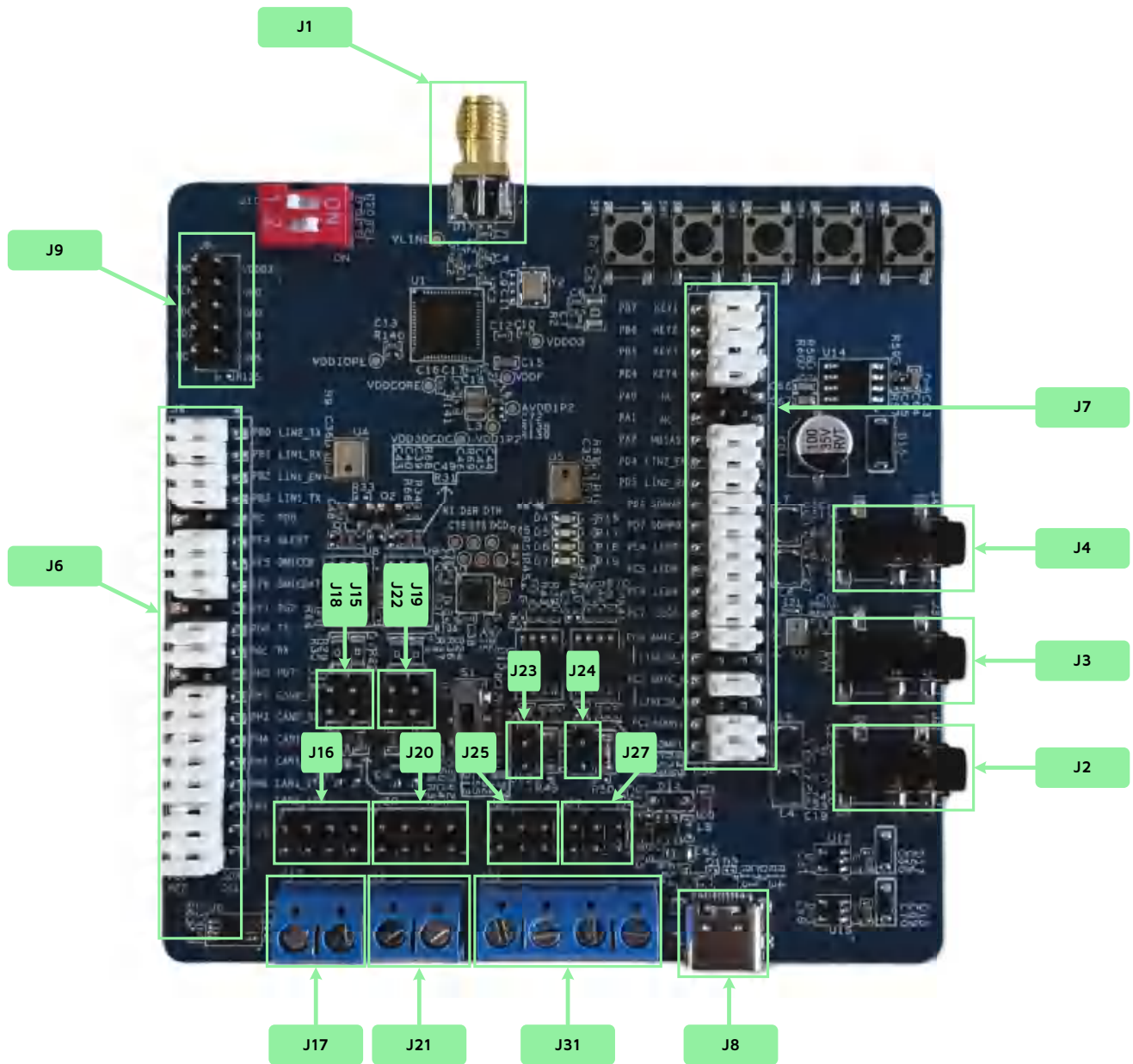
Figure 1-4 Bottom View of the Real Board



1.5 Connectors

The following figure identifies the connectors such as jumpers and sockets on the top of the development board.

Figure 1-5 Board Top Connectors



The following table lists the connectors on the top of the development board.

Table 1-3 Board Top Connectors List

No.	Ref. Des.	Connector type	Description	Reference section
1	J9	2x5-pin header	JTAG and single wire connector	2.2 Debug Interface
2	J6	2x20-pin header	GPIO connector	2.5 GPIO Interface
3	J7	2x21-pin header	GPIO connector	2.5 GPIO Interface
4	J18/J15/ J22/J19	1x2-pin header	CAN Term_R connector	2.7 Peripheral Interface - CAN
5	J23/J24	1x2-pin header	LIN master connector	2.8 Peripheral Interface - LIN
6	J16/J20	2x4-pin header	CAN connector	2.7 Peripheral Interface - CAN
7	J17/J21	1x2-pin header	CAN connector	2.7 Peripheral Interface - CAN
8	J25/J27	2x3-pin header	LIN connector	2.8 Peripheral Interface - LIN
9	J31	1x4-pin header	LIN connector	2.8 Peripheral Interface - LIN
10	J8	USB Type-C	USB-to-UART interface	2.6 Peripheral Interface - USB-To-UART
11	J1	SMA female connector	RF connector	2.4 RF Test
12	J3	3.5mm jack	Uplink connector	2.12 Uplink Interface
13	J2/J4	3.5mm jack	Downlink connector	2.13 Downlink Interface

The following figure identifies the connectors such as jumpers and sockets on the bottom of the development board.

Figure 1-6 Board Bottom Connectors



The following table lists the connectors on the bottom of the development board.

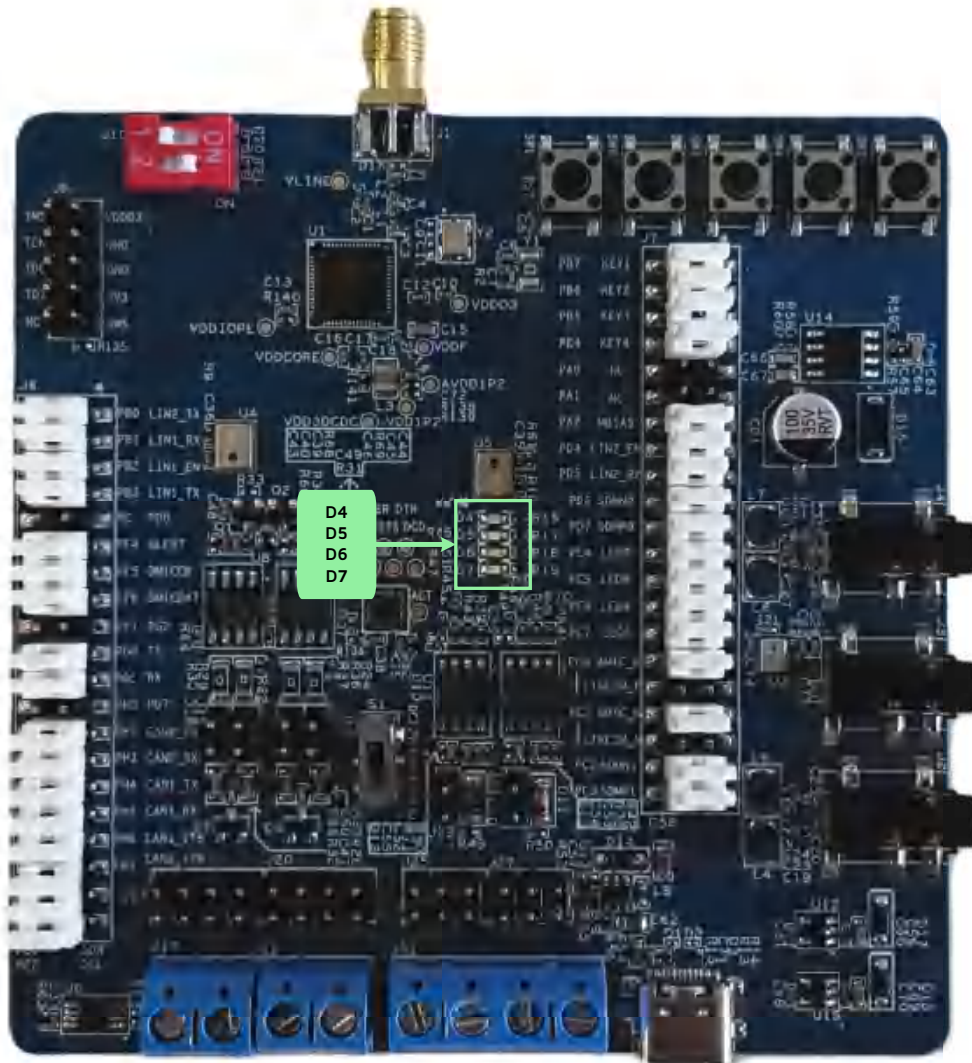
Table 1-4 Board Bottom Connectors List

No.	Ref. Des.	Connector type	Description	Reference section
1	J30	2x16-pin header	Connector for current test	2.3 Current Measurement
2	J29	2x16-pin header	Connector for current test	2.3 Current Measurement

1.6 LED

The following figure identifies the LEDs on the top of the development board.

Figure 1-7 Board Top LEDs



The following table lists the LEDs on the top of the board.

Table 1-5 Board Top LEDs

No.	Ref. Des.	LED color	Description
1	D4	Red	(1) PC4 of TL3225B connects to PIN24 of J7 (2) The LED anode is connected to PIN23 of J7 through a 1 kΩ series resistor (3) PIN24 of J7 connects to PIN23 via a jumper by default (4) PC4 directly drives the on/off state and brightness of D4 (5) If you want to use another GPIO of the TL3225B to control D4, remove this jumper and connect PIN23 of J7 to the other GPIO you want to use.
2	D5	Blue	(1) PC5 of TL3225B connects to PIN26 of J7 (2) The LED anode is connected to PIN 25 of J7 through a 1 kΩ series resistor (3) PIN26 of J7 connects to PIN25 via a jumper by default (4) PC5 directly drives the on/off state and brightness of D5 (5) If you want to use another GPIO of the TL3225B to control D5, remove this jumper and connect PIN25 of J7 to the other GPIO you want to use.
3	D6	White	(1) PC6 of TL3225B connects to PIN28 of J7 (2) The LED anode is connected to PIN27 of J7 through a 1 kΩ series resistor (3) PIN28 of J7 connects to PIN27 via a jumper by default (4) PC6 directly drives the on/off state and brightness of D6 (5) If you want to use another GPIO of the TL3225B to control D6, remove this jumper and connect PIN27 of J7 to the other GPIO you want to use.
4	D7	Green	(1) PC7 of TL3225B connects to PIN30 of J7 (2) The LED anode is connected to PIN29 of J7 through a 1 kΩ series resistor (3) PIN30 of J7 connects to PIN29 via a jumper by default (4) PC7 directly drives the on/off state and brightness of D7 (5) If you want to use another GPIO of the TL3225B to control D7, remove this jumper and connect PIN29 of J7 to the other GPIO you want to use.

1.7 Button

The following figure identifies the Buttons on the top of the development board.

Figure 1-8 Board Top Buttons



The following table lists the buttons on the top of the board.

Table 1-6 Board Top Buttons List

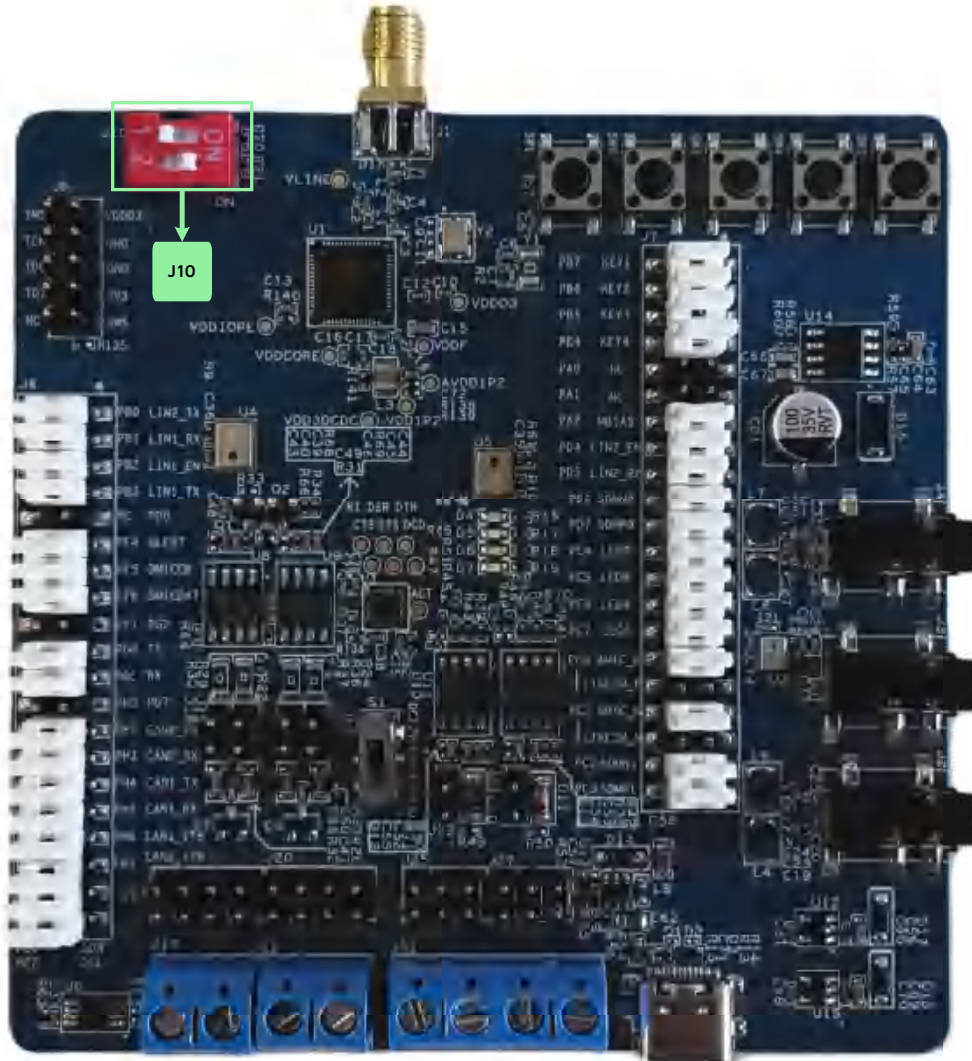
No.	Ref. Des.	Function	Description
1	SW1	Chip reset	Press SW1 to reset the main chip

No.	Ref. Des.	Function	Description
2	SW3	—	(1) SW3, SW4, SW5 and SW6 form a 2x2 key matrix.
3	SW4		(2) SW3's two end networks are TL_Key1 and TL_Key3 respectively.
4	SW5		(3) SW4's two end networks are TL_Key1 and TL_Key4 respectively.
5	SW6		(4) SW5's two end networks are TL_Key2 and TL_Key3 respectively. (5) SW6's two end networks are TL_Key2 and TL_Key4 respectively. (6) TL_Key1 is sourced as follows: a) PB7 of TL3225B connects to PIN2 of J7. b) PIN2 of J7 is shorted to PIN1 via a jumper by default. c) PIN1 of J7 is connected to one end of SW3 and SW4 with the network name TL_Key1. (7) TL_Key2 is sourced as follows: a) PB6 of TL3225B connects to PIN4 of J7. b) PIN4 of J7 is shorted to PIN3 via a jumper by default. c) PIN3 of J7 is connected to one end of SW5 and SW6 with the network name TL_Key2. (8) TL_Key3 is sourced as follows: a) PB5 of TL3225B connects to PIN6 of J7. b) PIN6 of J7 is shorted to PIN5 via a jumper by default. c) PIN5 of J7 is connected to one end of SW3 and SW5 with the network name TL_Key3. (9) TL_Key4 is sourced as follows: a) PB4 of TL3225B connects to PIN8 of J7. b) PIN8 of J7 is shorted to PIN7 via a jumper by default. c) PIN7 of J7 is connected to one end of SW4 and SW6 with the network name TL_Key4. (10) If you want to use another GPIO of the TL3225B to control the keys, remove the corresponding jumper and connect PIN 1/3/5/7 of J7 to the other GPIO you want to use.

1.8 Switch

The following figure identifies the switches on the top of the development board.

Figure 1-9 Board Top Switches



The following table lists the switch functions on the top of the board.

List of switches on board top

No.	Ref. Des.	Function	Description
1	J10	JTAG mode selection	(1) PBO of the TL3225B determines the SDP/JTAG work mode. a) When PBO is high, JTAG supports 2-wire SDP mode. b) When PBO is low, JTAG supports 4-wire JTAG mode. (2) Default setting: Move Switch 2 to the right to ON, Switch 1 to the left for JTAG mode. Conversely, move Switch 1 to the right to ON, and Switch 2 to the left for SDP mode.

2 Function Description

2.1 Power Supply

The TL3225B development board can be powered by the following ways:

- 5 V via the USB Type-C port and regulated to 3.3 V by LDO U15 to provide a dedicated regulated power supply for the chip;
- 12 V via J31 PIN4/J25 PIN1&PIN2/J27 PIN1&PIN2/J16 PIN1&PIN2/J20 PIN1&PIN2 to power the LIN module. The 12 V input is also regulated to 5 V by LDO U14 to power the CAN module. The 5 V output is further regulated to 3.3 V by LDO U15 to provide a regulated supply for the chip, and to 3.3 V by LDO U12 to provide regulated power for the CAN, LIN, and I3C peripheral modules;
- Access 1.9 V ~ 3.6 V through J9 PIN7 interface, J29 PIN5 and PIN6 are shorted through a jumper, J29 PIN5 provides voltage to U1 PIN28 VBAT pin.

The following table lists the power path of the chip.

Table 2-1 Power Supply

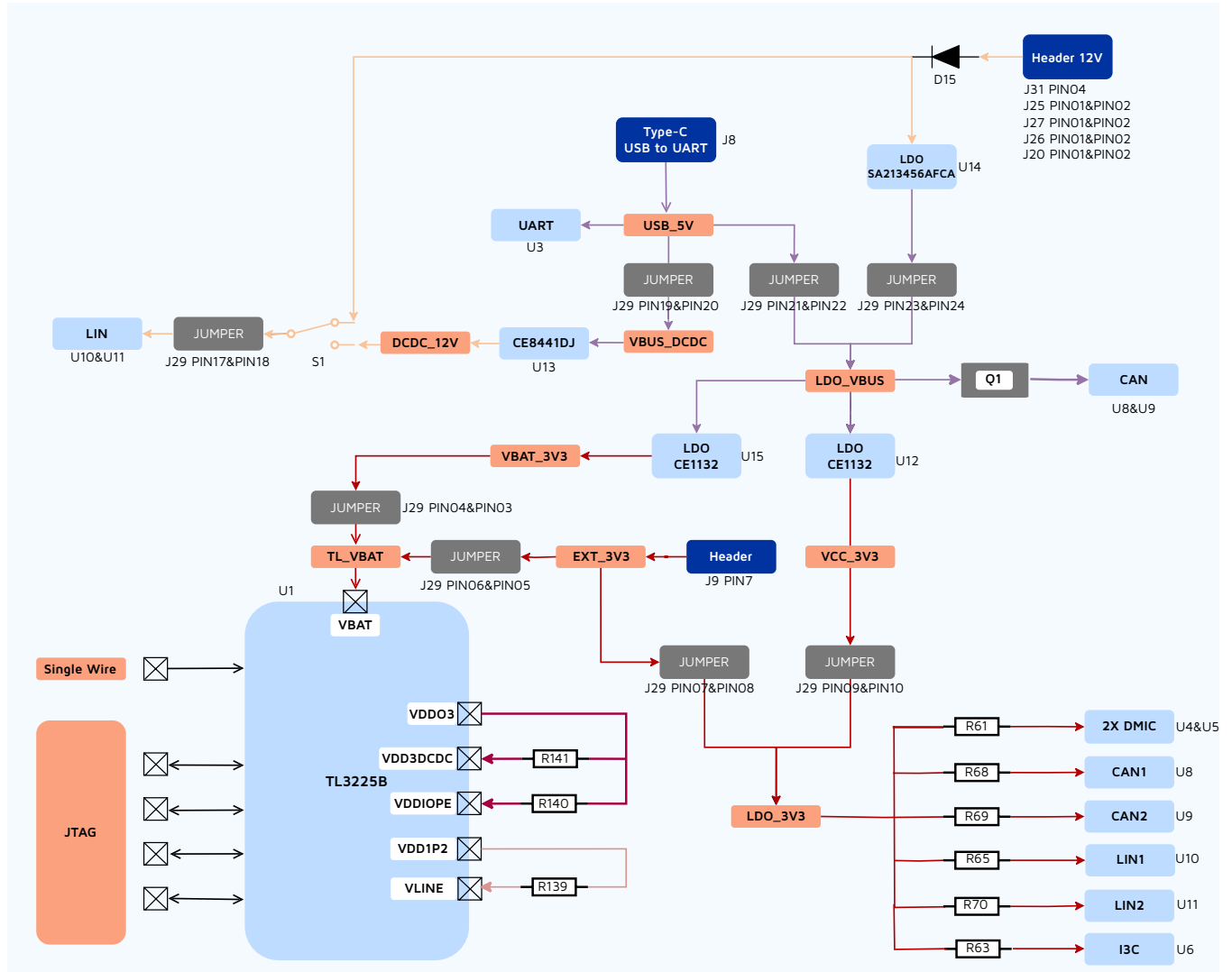
No.	Power source	Power supply	Description
1	External power via USB Type-C J8	VBUS to VBAT	(1) Apply 5 V to J29 PIN22 (net name: USB_5V). The voltage is routed to J29 PIN21 through a jumper (net name: LDO_VBUS). J29 PIN21 is connected to U15, which regulates the input to 3.3 V (net name: VBAT_3V3) and outputs it to J29 PIN4. J29 PIN4 is shorted to J29 PIN3, providing TL_VBAT to PIN28 of U1, which is the chip's power supply input pin. Note: This power supply configuration powers all peripherals on the development board simultaneously. When measuring the chip power consumption, disconnect the resistors for the peripheral modules. (2) Apply 5 V to J29 PIN20 (net name: USB_5V). The voltage is routed to J29 PIN19 through a jumper (net name: VBUS_DCDC). J29 PIN19 is connected to U13, which converts the input to 12 V (net name: DCDC_12V). The 12V net is selected through switch S1 and connected to J29 PIN17. It is then shorted to J29 PIN18 through a jumper to supply power to the LIN transceivers U10 and U11. (3) Apply 5 V to PIN9 of U3 (net name: USB_5V).



No.	Power source	Power supply	Description
2	12 V via J31 PIN4/ J25 PIN1&PIN2/J27 PIN1&PIN2/J16 PIN1&PIN2/J20 PIN1&PIN2	12 V to 5 V, then to 3.3V	(1) Apply 12 V to J31 PIN4, J25 PIN1 and PIN2, J27 PIN1 and PIN2, J16 PIN1 and PIN2, or J20 PIN1 and PIN2 (net name: EXT_12V). The input passes through the reverse-polarity protection diode D15 and is regulated to 5 V by U14 (net name: LDO_5V). LDO_5V is connected to J29 PIN24, which is shorted to J29 PIN23 through a jumper to supply 5 V to the LDO_VBUS net. a. LDO_VBUS is connected to U15, which regulates the input to 3.3 V (net name: VBAT_3V3) and outputs it to J29 PIN4. J29 PIN4 is shorted to J29 PIN3, providing TL_VBAT to PIN28 of U1, which is the chip's power supply input pin. b. LDO_VBUS is also connected to U12, which regulates the input to 3.3 V (net name: VCC_3V3) and outputs it to J29 PIN10. J29 PIN10 can be shorted to J29 PIN9 through a jumper (net name: LDO_3V3). LDO_3V3 supplies power to the peripheral modules or serves as the pull-up supply. It powers the DMIC devices U4 and U5 and the I3C device U6, and provides the VIO pull-up supply for the CAN devices U8 and U9 and the LIN devices U10 and U11. c. LDO_VBUS is also routed through the Q1 and Q2 MOSFET circuit, which is controlled by LDO_3V3, to provide a switched 5 V output (net name: CAN_5V) for the CAN devices. (2) Apply 12 V to J31 PIN4, J25 PIN1 and PIN2, J27 PIN1 and PIN2, J16 PIN1 and PIN2, or J20 PIN1 and PIN2 (net name: EXT_12V). The input passes through the reverse-polarity protection diode D15 (net name: VCC_12V). The 12V net is then selected by switch S1 and connected to J29 PIN17, which can be shorted to J29 PIN18 through a jumper to supply power to the LIN devices U10 and U11. Note: Some peripheral modules, including the LIN devices, require a 12 V supply for normal operation.
3	External power via connector J9	TL_VBAT	(1) Apply an external voltage between 1.9 V and 3.6 V to J9 PIN7. With J29 PIN5 and PIN6 shorted by a jumper, the voltage is supplied as TL_VBAT to PIN28 of U1. (2) Apply an external voltage between 1.9 V and 3.6 V to J29 PIN1, PIN3, or PIN5. The voltage is supplied directly as TL_VBAT to PIN28 of U1.

The following figure shows the power supply path of the main power sources.

Figure 2-1 Power Supply Path



2.2 Debug Interface

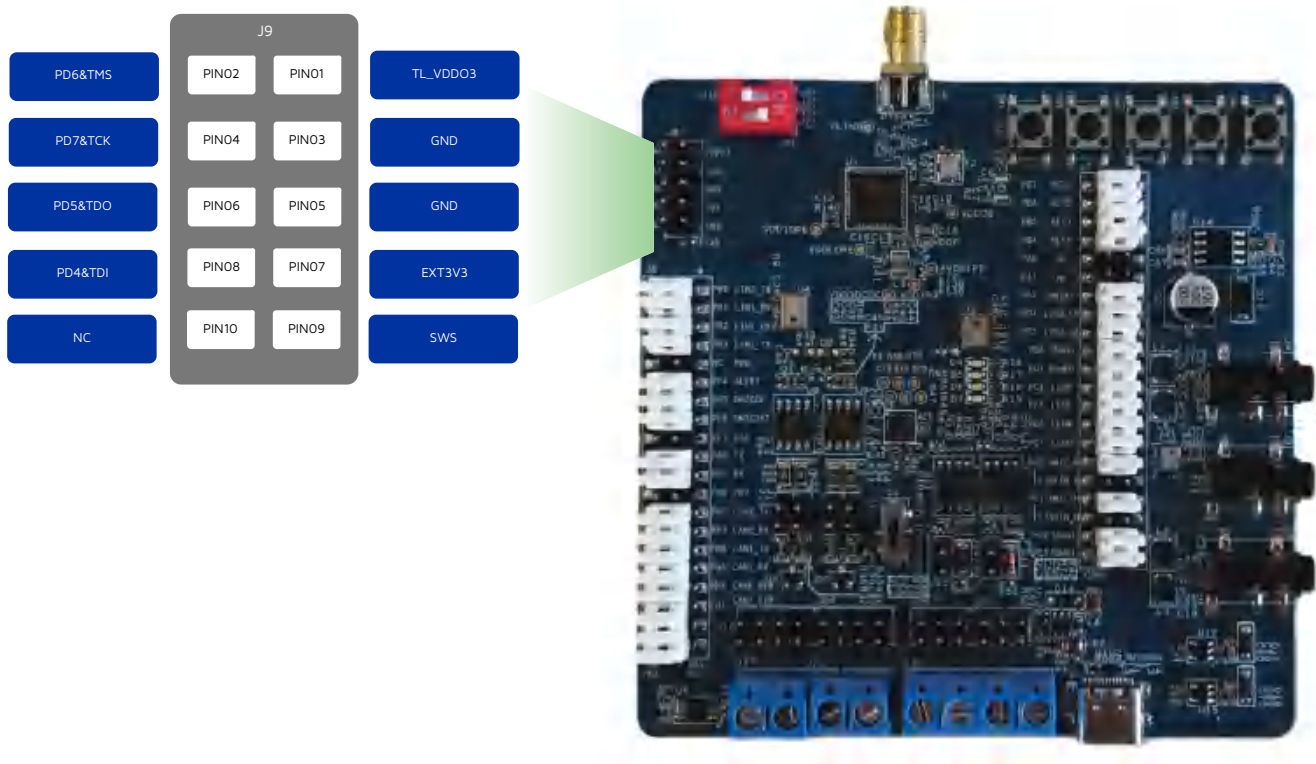
The TL3225B development board supports the following two debug methods.

Table 2-2 Debug Methods

No.	Debug method	Connector	Description
1	JTAG	J9	(1) Power up the TL3225B development board. (2) J9 supports 4-wire JTAG function - U1.PIN12.PD4 to J9.PIN08 - TDI - U1.PIN11.PD5 to J9.PIN06 - TDO - U1.PIN9.PD7 to J9.PIN04 - TCK - U1.PIN10.PD6 to J9.PIN02 - TMS
2	Single Wire	J9	(1) Power up the TL3225B development board. (2) J9 supports Telink proprietary debug protocol, single wire. U1.PIN19.PA7 to J9.PIN09 - SWS

The following figure shows the details of each J9 pins.

Figure 2-2 Debug Interfaces



2.3 Current Measurement

The methods to measure the current of each pin of TL3225B development board are provided as follows.

Table 2-3 Current measurement method of the board

No.	Test item	Power supply	Description
1	Total current of the chip	TL_VBAT	(1) The main power supply of the chip is U1 PIN28. (2) Power supply method 3 described above is recommended for measuring the chip power consumption. (3) When using power supply method 3, remove the jumper between VBAT_3V3 and TL_VBAT first, then connect an ammeter in series between the external power supply and J9 PIN7. The total current consumption of the chip can then be measured. (4) Make sure that there is no external power consumption and no GPIO external current (including JTAG and SWS), so as to avoid high chip current. (5) Details refer to Figure 2-1.

2.4 RF Test

The methods for conducting and radiating tests on RF of TL3225B development board are provided.

The following table lists the methods of RF test.

Table 2-4 RF test method

No.	Test item	Connector	Description
1	RF test	J1	(1) Power up the TL3225B development board normally. (2) RF conduction test: connect the J1 SMA connector to the test instrument to perform RF conduction test. (3) RF radiation test: connect the whip antenna in the kit to the J1 SMA connector to perform RF radiation test.

2.5 GPIO Interface

On the TL3225B development board, all GPIOs are connected to the connectors for easy access.

The following table lists the connections of all GPIO.

Table 2-5 GPIO Connections

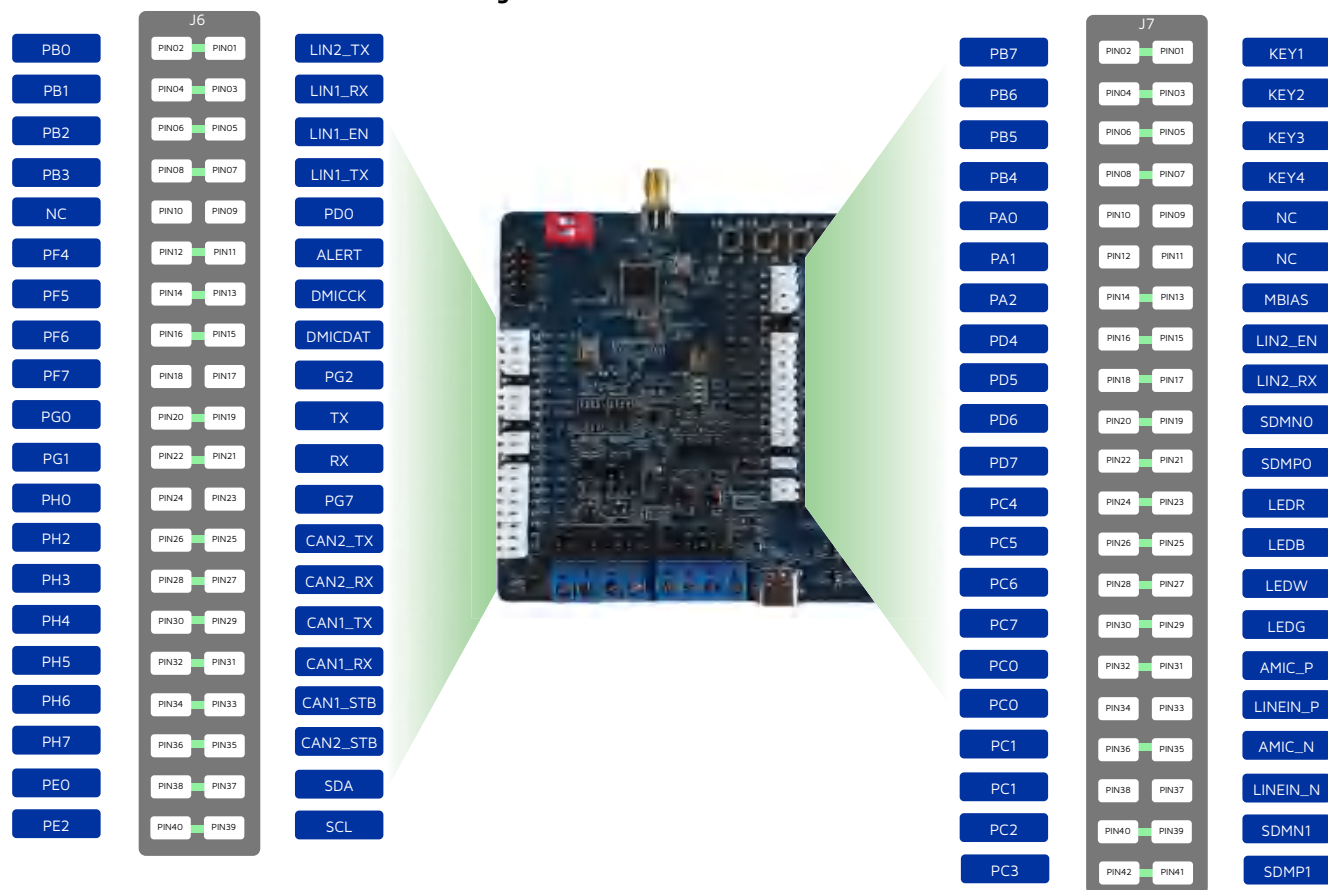
No.	Chip pins	IO name	Connector pins
1	U1.PIN01	PG7	J6 PIN23

No.	Chip pins	IO name	Connector pins
2	U1.PIN02	PH0	J6 PIN24
3	U1.PIN03	PH2	J6 PIN26
4	U1.PIN04	PH3	J6 PIN28
5	U1.PIN05	PH4	J6 PIN30
6	U1.PIN06	PH5	J6 PIN32
7	U1.PIN07	PH6	J6 PIN34
8	U1.PIN08	PH7	J6 PIN36
9	U1.PIN09	PD7	J7 PIN22
10	U1.PIN10	PD6	J7 PIN20
11	U1.PIN11	PD5	J7 PIN18
12	U1.PIN12	PD4	J7 PIN16
13	U1.PIN14	PE0	J6 PIN38
14	U1.PIN15	PE2	J6 PIN40
15	U1.PIN16	PA0	J7 PIN10
16	U1.PIN17	PA1	J7 PIN12
17	U1.PIN18	PA2	J7 PIN14
18	U1.PIN21	PC5	J7 PIN26
19	U1.PIN22	PC6	J7 PIN28
20	U1.PIN23	PC7	J7 PIN30
21	U1.PIN29	PB4	J7 PIN08
22	U1.PIN30	PB5	J7 PIN06
23	U1.PIN31	PB6	J7 PIN04
24	U1.PIN32	PB7	J7 PIN02
25	U1.PIN35	PC0	J7 PIN32 & PIN34
26	U1.PIN36	PC1	J7 PIN36 & PIN38
27	U1.PIN37	PC2	J7 PIN40
28	U1.PIN38	PC3	J7.PIN42
29	U1.PIN39	PC4	J7.PIN24

No.	Chip pins	IO name	Connector pins
30	U1.PIN45	PB0	J6.PIN02
31	U1.PIN46	PB1	J6.PIN04
32	U1.PIN47	PB2	J6.PIN06
33	U1.PIN48	PB3	J6.PIN08
34	U1.PIN49	PD0	J6.PIN10
35	U1.PIN50	PF4	J6.PIN12
36	U1.PIN51	PF5	J6.PIN14
37	U1.PIN52	PF6	J6.PIN16
38	U1.PIN53	PF7	J6.PIN18
39	U1.PIN54	PG0	J6.PIN20
40	U1.PIN55	PG1	J6.PIN22
41	U1.PIN56	PG2	J6.PIN17

The following figure shows the net names of all the pins of J6 and J7 for reference.

Figure 2-3 All Pins of J6 and J7



2.6 Peripheral Interface - USB-To-UART

The TL3225B development board is designed with a USB-To-UART connector for UART communication.

The following table lists the USB-To-UART configuration.

Table 2-6 USB-to-UART

No.	Chip pins	Description
1	USB-to-UART	(1) The J8 USB connector is connected to J6 PIN19 and PIN21 through the U3 USB-to-UART bridge. Through jumpers, the signals are routed to J6 PIN20 and PIN22, which are connected to PIN54 (PG0) and PIN55 (PG1) of the U1 TL3225B device, respectively. (2) When using this function, configure PG0 of U1 as UART_RX and PG1 as UART_TX by default.

2.7 Peripheral Interface - CAN

The TL3225B development board integrates two CAN FD channels to facilitate CAN communication validation and testing.

The following table lists the connections between the two CAN transceivers and their corresponding interfaces.

Table 2-7 CAN Transceiver Pin Connections

No.	Chip pins	IO name	Connector pins	Description
1	U1.PIN5	PH4	J6.PIN30	(1) Connected to J6 PIN30 and routed to J6 PIN29 through a jumper (net name: TL_CAN_TXD). (2) Connected to PIN1 of the CAN transceiver U8.
2	U1.PIN6	PH5	J6.PIN32	(1) Connected to J6 PIN32 and routed to J6 PIN31 through a jumper (net name: TL_CAN_RXD). (2) Connected to PIN4 of the CAN transceiver U8.
3	U1.PIN7	PH6	J6.PIN34	(1) Connected to J6 PIN34 and routed to J6 PIN33 through a jumper (net name: TL_CAN_STB). (2) Connected to PIN8 of the CAN transceiver U8.
4	U1.PIN3	PH2	J6.PIN26	(1) Connected to J6 PIN26 and routed to J6 PIN25 through a jumper (net name: TL_CAN_TXD2). (2) Connected to PIN1 of the CAN transceiver U9.
5	U1.PIN4	PH3	J6.PIN28	(1) Connected to J6 PIN28 and routed to J6 PIN27 through a jumper (net name: TL_CAN_RXD2). (2) Connected to PIN4 of the CAN transceiver U9.

No.	Chip pins	IO name	Connector pins	Description
6	U1.PIN8	PH7	J6.PIN36	(1) Connected to J6 PIN36 and routed to J6 PIN35 through a jumper (net name: TL_CAN_STB2). (2) Connected to PIN8 of the CAN transceiver U9.

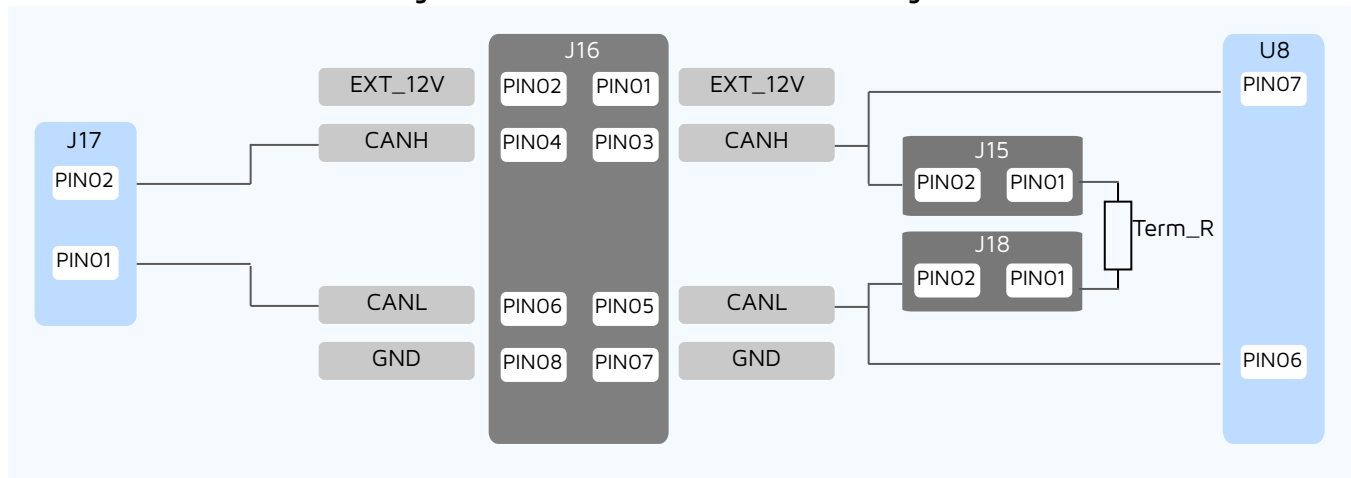
CAN1 Channel

J15 and J18 are used to configure the termination resistors for the CAN1 channel. When the board is used as part of a CAN network, the nodes located at both ends of the CAN bus should have J15 and J18 shorted with jumpers to enable the termination resistors.

Configure the jumpers according to the application requirements to ensure that the CAN transceiver enable signal is connected correctly. Also ensure that the CAN bus termination resistors are installed only at the two ends of the bus to maintain signal integrity and communication reliability.

J16 and J17 serve as the external interfaces for the CAN1 channel. J16 provides two sets of CANH/CANL/12V/GND signals for convenient debugging and connection, while J17 provides CANH and CANL interfaces.

Figure 2-4 CAN1 Channel Connection Diagram

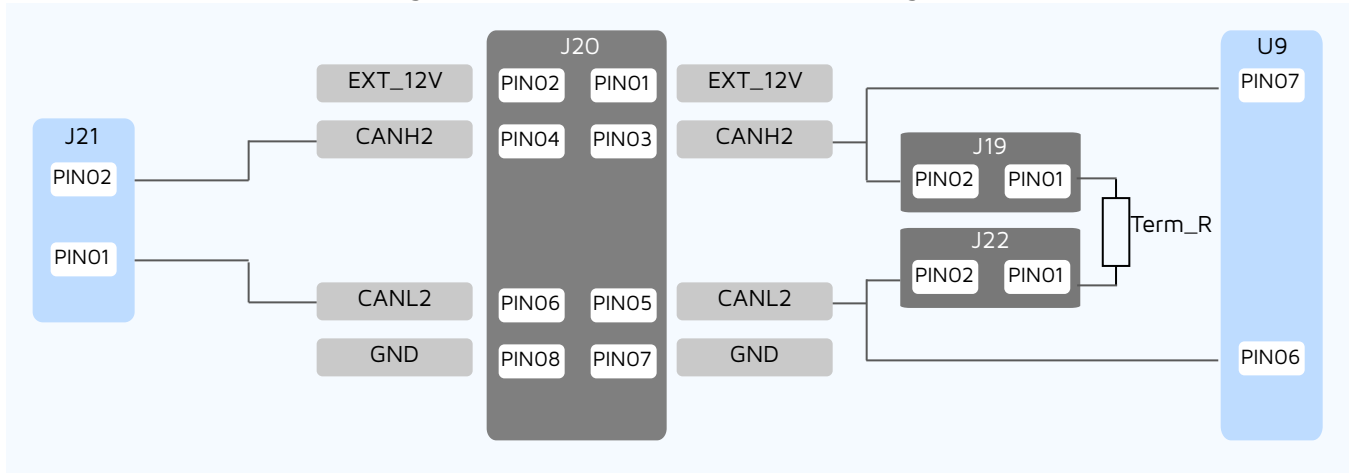


CAN2 Channel

J19 and J22 are used to configure the termination resistors for the CAN2 channel. When the board is used as part of a CAN network, the nodes located at both ends of the CAN bus should have J19 and J22 shorted with jumpers to enable the termination resistors.

Configure the jumpers according to the application requirements to ensure that the CAN transceiver enable signal is connected correctly. Also ensure that the CAN bus termination resistors are installed only at the two ends of the bus to maintain signal integrity and communication reliability.

J20 and J21 serve as the external interfaces for the CAN1 channel. J20 provides two sets of CANH2/CANL2/12V/GND signals for convenient debugging and connection, while J21 provides CANH2 and CANL2 interfaces.

Figure 2-5 CAN2 Channel Connection Diagram


2.8 Peripheral Interface - LIN

The TL3225B development board integrates two LIN channels to facilitate LIN communication validation and testing.

The following table lists the connections between the two LIN transceivers and their corresponding interfaces.

Table 2-8 LIN Transceiver Pin Connections

No.	Chip pins	IO name	Connector pins	Description
1	U1.PIN46	PB1	J6.PIN04	(1) Connected to J6 PIN04 and routed to J6 PIN03 through a jumper (net name: LIN_RXD1). (2) Connected to PIN1 of the LIN transceiver U10.
2	U1.PIN47	PB2	J6.PIN06	(1) Connected to J6 PIN06 and routed to J6 PIN05 through a jumper (net name: LIN_EN1). (2) Connected to PIN2 of the LIN transceiver U10.
3	U1.PIN48	PB3	J6.PIN08	(1) Connected to J6 PIN08 and routed to J6 PIN07 through a jumper (net name: LIN_TXD1). (2) Connected to PIN4 of the LIN transceiver U10.
4	U1.PIN11	PD5	J7.PIN18	(1) Connected to J6 PIN18 and routed to J6 PIN17 through a jumper (net name: LIN_RXD2). (2) Connected to PIN1 of the LIN transceiver U11.
5	U1.PIN12	PD4	J7.PIN16	(1) Connected to J6 PIN16 and routed to J6 PIN15 through a jumper (net name: LIN_EN2). (2) Connected to PIN2 of the LIN transceiver U11.
6	U1.PIN45	PB0	J7.PIN02	(1) Connected to J6 PIN02 and routed to J6 PIN01 through a jumper (net name: LIN_TXD2). (2) Connected to PIN4 of the LIN transceiver U11.

LIN1 Channel

J23 is used to configure the LIN1 channel as either a master or a slave node. To operate as a LIN master, short J23 with a jumper. To operate as a LIN slave, leave J23 unconnected (NC).

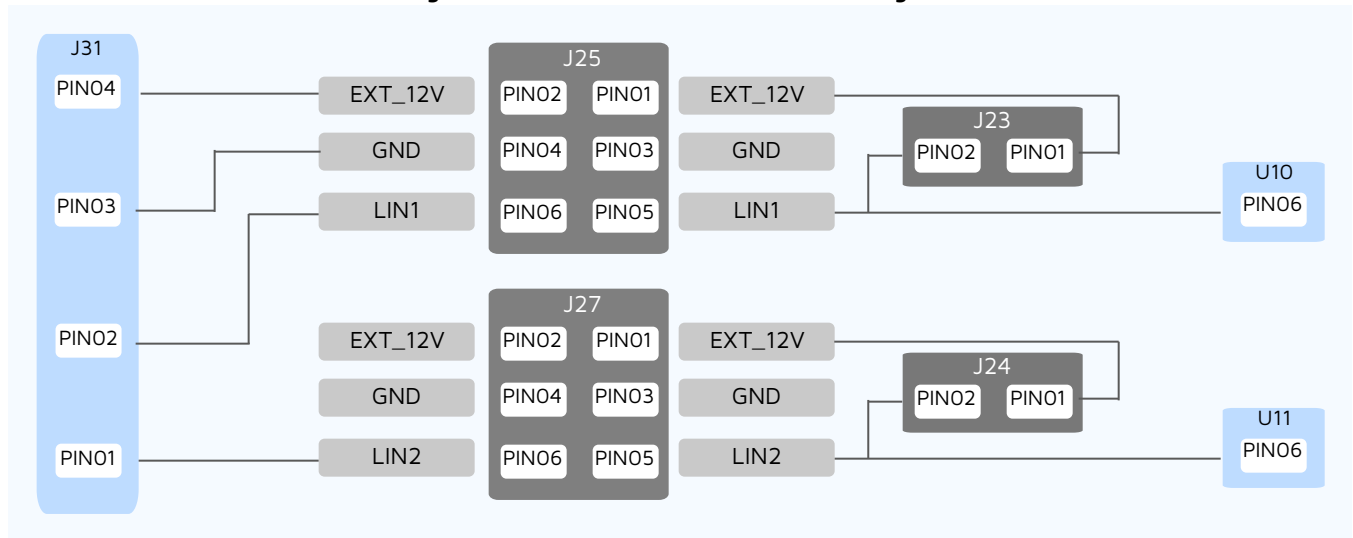
J25 and J31 serve as the external interfaces for the LIN1 channel. J25 provides two sets of LIN1/12V/GND signals for convenient debugging and connection, while J31 is a shared external interface for both the LIN1 and LIN2 channels.

LIN2 Channel

J24 is used to configure the LIN2 channel as either a master or a slave node. To operate as a LIN master, short J24 with a jumper. To operate as a LIN slave, leave J24 unconnected (NC).

J27 and J31 serve as the external interfaces for the LIN2 channel. J27 provides two sets of LIN2/12V/GND signals for convenient debugging and connection, while J31 is a shared external interface for both the LIN1 and LIN2 channels.

Figure 2-6 LIN Channel Connection Diagram



2.9 Peripheral Interface - 32.768KHz Crystal

The TL3225B development board embeds a 32 kHz RC circuit and also supports an external 32.768 kHz crystal.

The following table lists the pin connections of the 32.768 kHz crystal.

Table 2-9 Connection of 32.768 kHz Crystal

No.	Chip pins	IO name	Connector pins	Description
1	U1.PIN37	PC2	J7.PIN40	(1) Supports configuration as GPIO and external 32.768 kHz crystal function. By default, it is configured as GPIO. The 32.768 kHz crystal is not populated by default and may be populated as needed. (2) The pin location refers Figure 2-3 .
2	U1.PIN38	PC3	J7.PIN42	(1) Supports configuration as GPIO and external 32.768 kHz crystal function. By default, it is configured as GPIO. The 32.768 kHz crystal is not populated by default and may be populated as needed. (2) The pin location refers Figure 2-3 .

2.10 Peripheral Interface - DMIC

The TL3225B development board is designed with two DMICs, the part number of microphone is WMM7047DTFN0 for demonstration.

The following table lists the connections of DMIC pin.

Table 2-10 Connection of DMIC Pin

No.	Chip pins	IO name	Connector pins	Description
1	U1.PIN52	PF6	J6.PIN16	(1) Connect to J6 PIN16 and then to J6 PIN15 via the jumper. (2) Connect to the data pins of DMIC U4 and U5. (3) The pin location refers Figure 2-3 .
2	U1.PIN51	PF5	J6.PIN14	(1) Connect to J6 PIN14 and then to J6 PIN13 via the jumper. (2) Connect to the clock pins of DMIC U4 and U5. (3) The pin location refers Figure 2-3 .

2.11 Peripheral Interface - I3C

The TL3225B development board is designed with I3C debugging circuit. U6 is a digital temperature sensor with an I3C interface and can be used for I3C function validation and debugging.

The following table lists the connections of the I3C pins.

Table 2-11 Connections of I3C Pins

No.	Chip pins	IO name	Connector pins	I3C pins
1	U1.PIN14	PE0	J6 PIN37 & PIN38	U6.PIN01
2	U1.PIN15	PE2	J6 PIN39 & PIN40	U6.PIN02
3	U1.PIN50	PE4	J6 PIN11 & PIN12	U6.PIN03

2.12 Uplink Interface

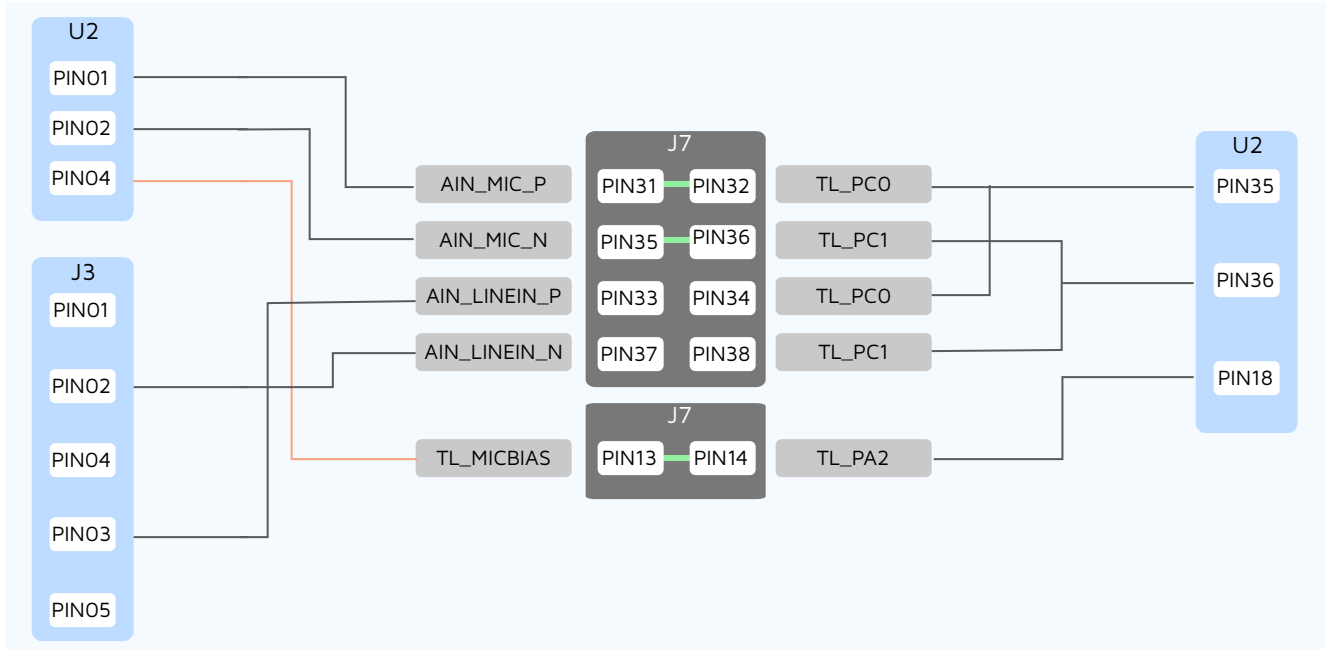
The uplink of the TL3225B development board supports one AMIC, one differential LINE-IN path configuration. Both can be configured via wires.

The following table lists the configuration methods for the uplink path.

Table 2-12 Configuration of Uplink Path

No.	Chip pins	Description
1	One differential AMIC configuration	(1) The default connection of the development board is one differential AMIC configuration. (2) The jumper on PIN32-PIN31 of J7 and the jumper on PIN36-PIN35 of J7 are plugged by default. (3) The pin location refers Figure 2-7.
2	One single-end LINE-IN configuration	(1) Unplug the connector on PIN32-PIN31 of J7 and the jumper on PIN36-PIN35 of J7. (2) Plug the jumper on PIN34-PIN33 of J7 and the jumper on PIN38-PIN37 of J7. (3) At this point, connect to the audio test instrument through the 3.5mm socket of the J3 for uplink performance testing using the differential connection method. (4) The pin location refers Figure 2-7.

The following figure shows the relationship of differential AMIC and LINE-IN uplink path.

Figure 2-7 Relationship of Differential AMIC and LINE-IN Uplink


2.13 Downlink Interface

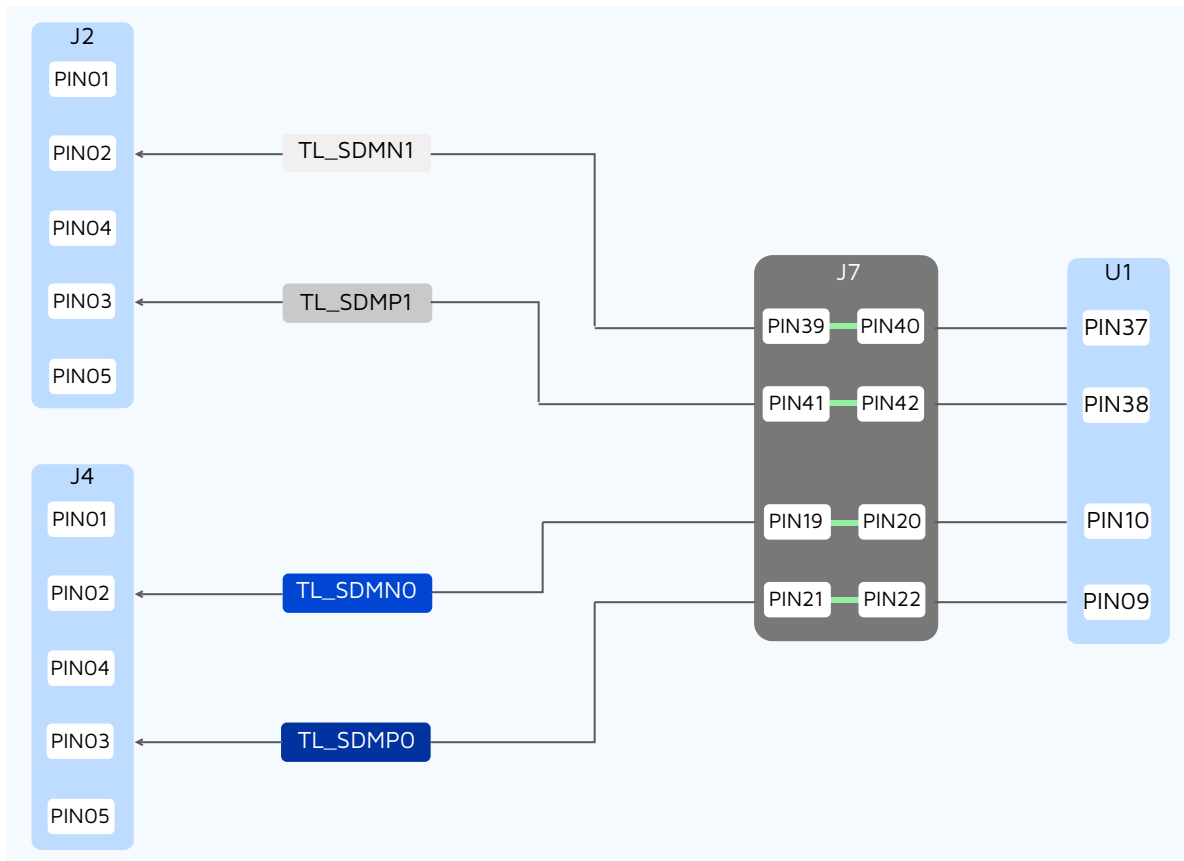
The downlink of the TL3225B development board supports two SDM differential outputs. Note that single-ended configuration is not supported.

The following table lists the downlink configuration methods.

Table 2-13 Configuration of Downlink Path

No.	Chip pins	IO name	Connector pins	Description
1	U1.PIN37	PC2	J7.PIN40	(1) Connect to J7 PIN40 and then to J7 PIN39 via the jumper. (2) Connect to J2 PIN02 after passing through the relevant circuit of SDM. (3) The pin location refers Figure 2-8 .
2	U1.PIN38	PC3	J7.PIN42	(1) Connect to J7 PIN42 and then to J7 PIN41 via the jumper. (2) Connect to J2 PIN03 after passing through the relevant circuit of SDM. (3) The pin location refers Figure 2-8 .
3	U1.PIN10	PD6	J7.PIN20	(1) Connect to J7 PIN20 and then to J7 PIN19 via the jumper. (2) Connect to J4 PIN02 after passing through the relevant circuit of SDM. (3) The pin location refers Figure 2-8 .

No.	Chip pins	IO name	Connector pins	Description
4	U1.PIN09	PD7	J7.PIN22	(1) Connect to J7 PIN22 and then to J7 PIN21 via the jumper. (2) Connect to J4 PIN03 after passing through the relevant circuit of SDM. (3) The pin location refers Figure 2-8.

Figure 2-8 Connections of Downlink Path


3 Related Documents

The following table lists other documents and resources that you can refer to for more information. Some of these documents are only available under a Non-Disclosure Agreement (NDA). To access such documents, please contact your local Telink Field Application Engineer (FAE) or sales representative.

Table 3-1 Related Documents

No.	Name	Description	Link / Obtain method
1	TL3225B Datasheet	Provides information on the electrical characteristics, hardware description, and ordering options for the TL3225B chip.	TL3225 datasheet
2	TL322x/TL382x Hardware Guideline	Provides hardware design guide for the TL322x/TL382x chip.	TL322x_Hardware_Design_Guideline
3	TL3225B board files	Provides design files of schematic, PCB layout and gerber file for the TL3225B development board.	TL3225B board files

4 Certification Statement

4.1 FCC Statement

1. This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:
 - (1) This device may not cause harmful interference, and
 - (2) This device must accept any interference received, including interference that may cause undesired operation.
2. Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.

This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

4.2 FCC Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.