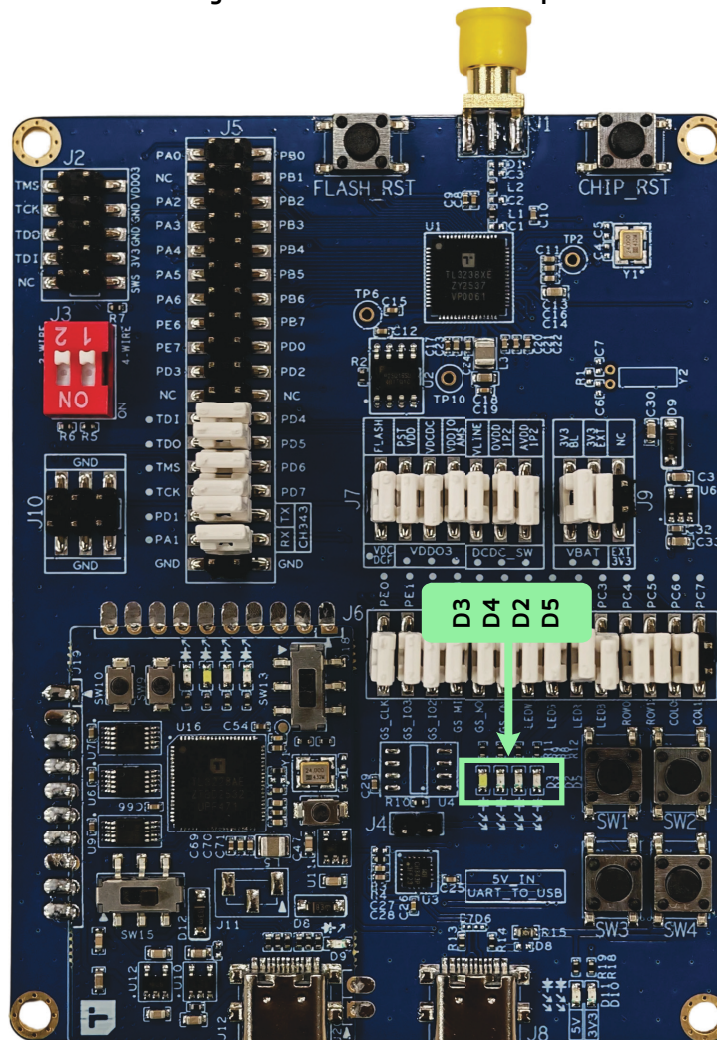




1.6 LED

The following figure identifies the LEDs on the top of the development board.

Figure 1-5 LEDs on Board Top



The following table lists the LEDs on the top of the board.

Table 1-4 LEDs on Board Top

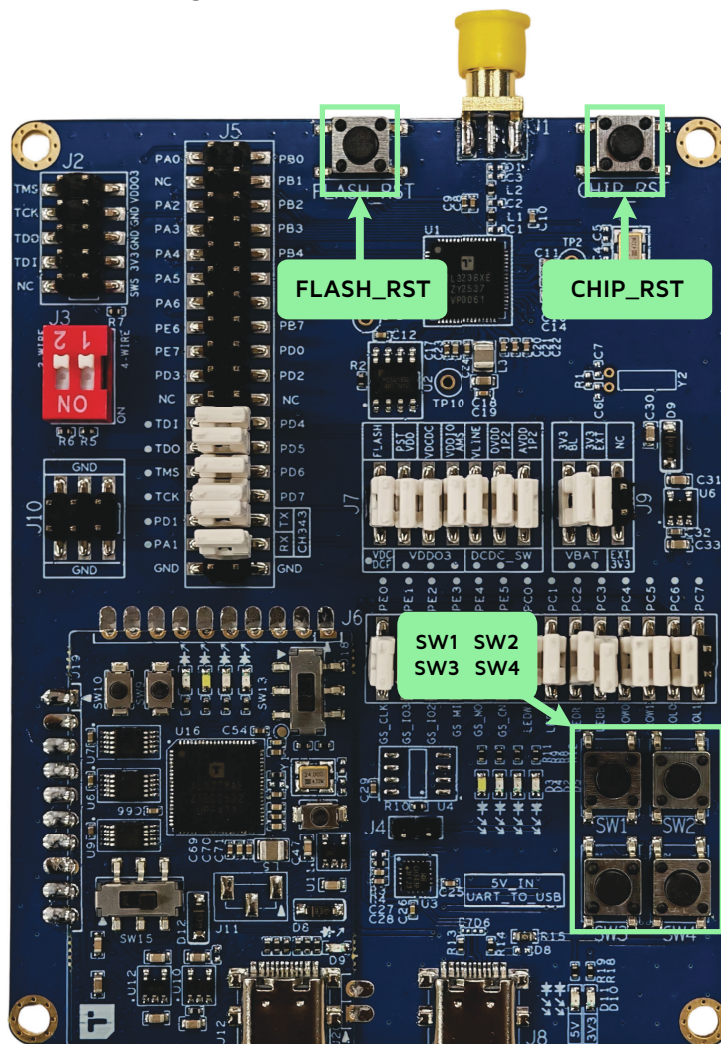
No.	Ref. Des.	LED color	Description
1	D3	White	(1) D3 is connected to PC0 of the chip TL3238X through a jumper on J6. The exact jumper position is indicated by the silkscreen markings on both sides of the pin header. (2) If PC0 needs to be used for another purpose, remove the jumper, then connect the circuit as required through the pin header.

No.	Ref. Des.	LED color	Description
2	D4	Green	(1) D4 is connected to PC1 of the chip TL3238X through a jumper on J6. The exact jumper position is indicated by the silkscreen markings on both sides of the pin header. (2) If PC1 needs to be used for another purpose, remove the jumper, then connect the circuit as required through the pin header.
3	D2	Red	(1) D2 is connected to PC2 of the chip TL3238X through a jumper on J6. The exact jumper position is indicated by the silkscreen markings on both sides of the pin header. (2) If PC2 needs to be used for another purpose, remove the jumper, then connect the circuit as required through the pin header.
4	D5	Blue	(1) D5 is connected to PC3 of the chip TL3238X through a jumper on J6. The exact jumper position is indicated by the silkscreen markings on both sides of the pin header. (2) If PC3 needs to be used for another purpose, remove the jumper, then connect the circuit as required through the pin header.

1.7 Button

The following figure identifies the Buttons on the top of the development board.

Figure 1-6 Buttons on Board Top



The following table lists the buttons on the top of the board.

Table 1-5 List of Buttons on Board Top

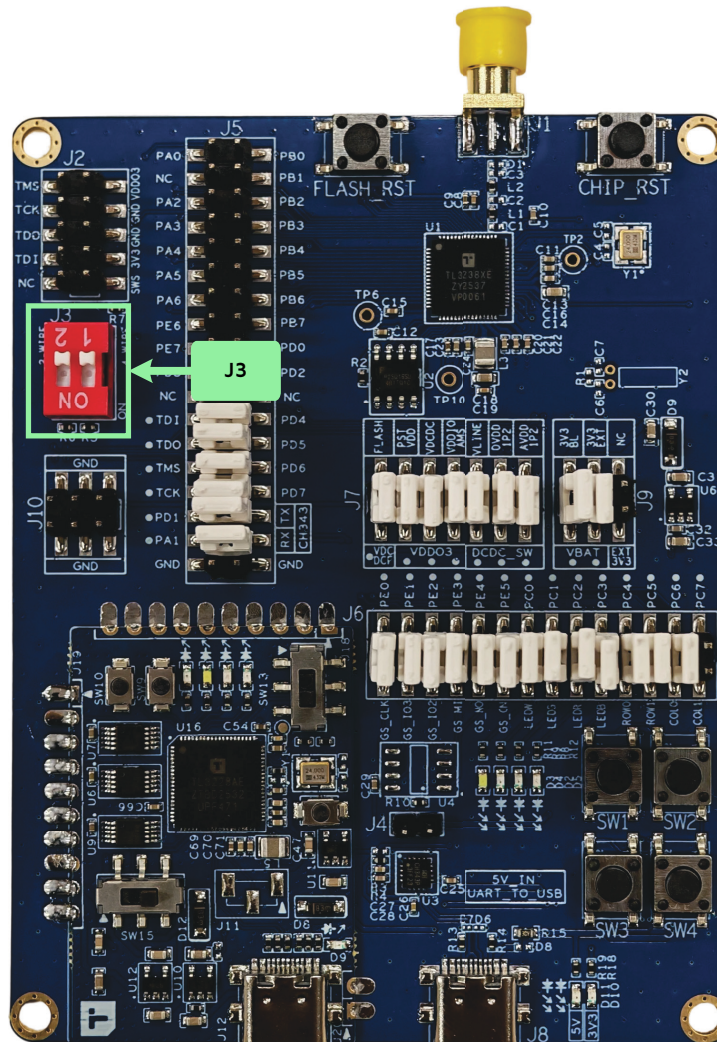
No.	Ref. Des.	Function	Description
1	CHIP_RST	Chip reset	Press CHIP_RST to reset the main chip
2	FLASH_RST	Flash reset	Press FLASH_RST to reset the flash

No.	Ref. Des.	Function	Description
3	SW1	Key Matrix	(1) SW1, SW2, SW3 and SW4 form a 2x2 key matrix. In the circuit topology, they are located at Row 1 Column 1, Row 1 Column 2, Row 2 Column 1, and Row 2 Column 2, respectively. (2) Row 1 is connected to PC4 of the chip TL3238X through a jumper on J6. (3) Row 2 is connected to PC5 of the chip TL3238X through a jumper on J6. (4) Column 1 is connected to PC6 of the chip TL3238X through a jumper on J6. (5) Column 2 is connected to PC7 of the chip TL3238X through a jumper on J6. (6) The exact jumper positions are indicated by the silkscreen markings on both sides of the J6 header. (7) If these four pins are required for other purposes, remove the corresponding jumpers and connect the circuit as needed through the pin header.
4	SW2		
5	SW3		
6	SW4		

1.8 Switch

The following figure identifies the switches on the top of the development board.

Figure 1-7 Switches on Board Top



The following table lists the switch functions on the top of the board.

Table 1-6 List of Switches on Board Top

No.	Ref. Des.	Function	Description
1	J3	JTAG/SDP mode selection	(1) PBO of the TL3238X determines the JTAG/SDP work mode. a) When PBO is high, supports 2-wire SDP mode. b) When PBO is low, supports 4-wire JTAG mode. (2) By default, with switch 2 toggled down to ON and switch 1 up, the interface operates in JTAG mode; conversely, with switch 1 toggled down to ON and switch 2 up, it operates in SDP mode.

2 Function Description

2.1 Power Supply

The TL3238X development board can be powered by the following ways:

- 5V via the USB Type-C port and converted to 3.3V through LDO U6 for regulated power supply. The 3.3V is then fed to U1's VBAT pin through the jumper between J9 PIN1 and PIN2.
- U1's VBAT pin can be powered via J9 PIN6. In this case, a jumper must be placed between J9 PIN3 and PIN4.

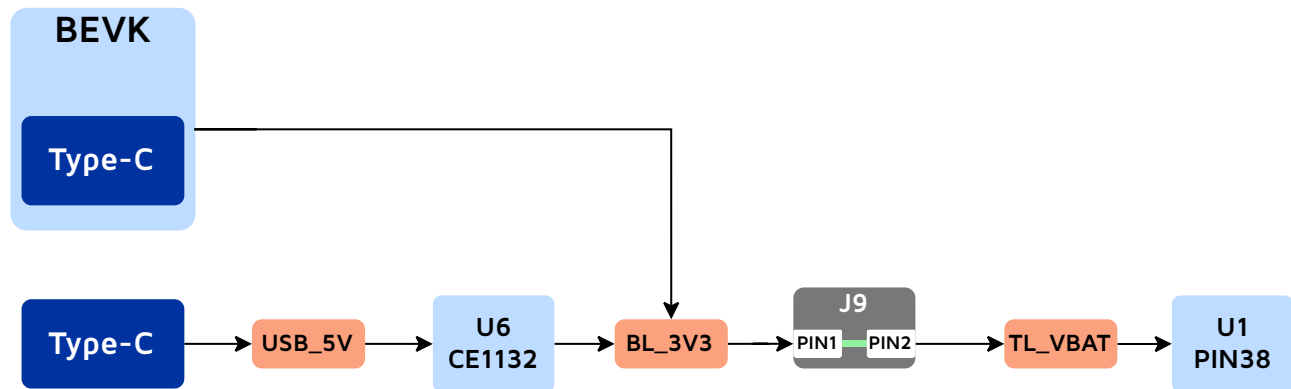
The following table lists the power path of the chip.

Table 2-1 Power Supply of the Chip

No.	Power source	Power supply	Description
1	External power via USB Type-C J8	VBUS to VBAT	The external power provides 5V to U6, which outputs 3.3 V. The 3.3V is then fed to U1's VBAT pin through the jumper between J9 PIN1 and PIN2.
2	External power via connector J9	VBAT	U1's VBAT pin can be powered via J9 PIN6. In this case, a jumper must be placed between J9 PIN3 and PIN4.

The following figure shows the power supply path of the main power sources.

Figure 2-1 Power Supply Path





2.2 Debug Interface

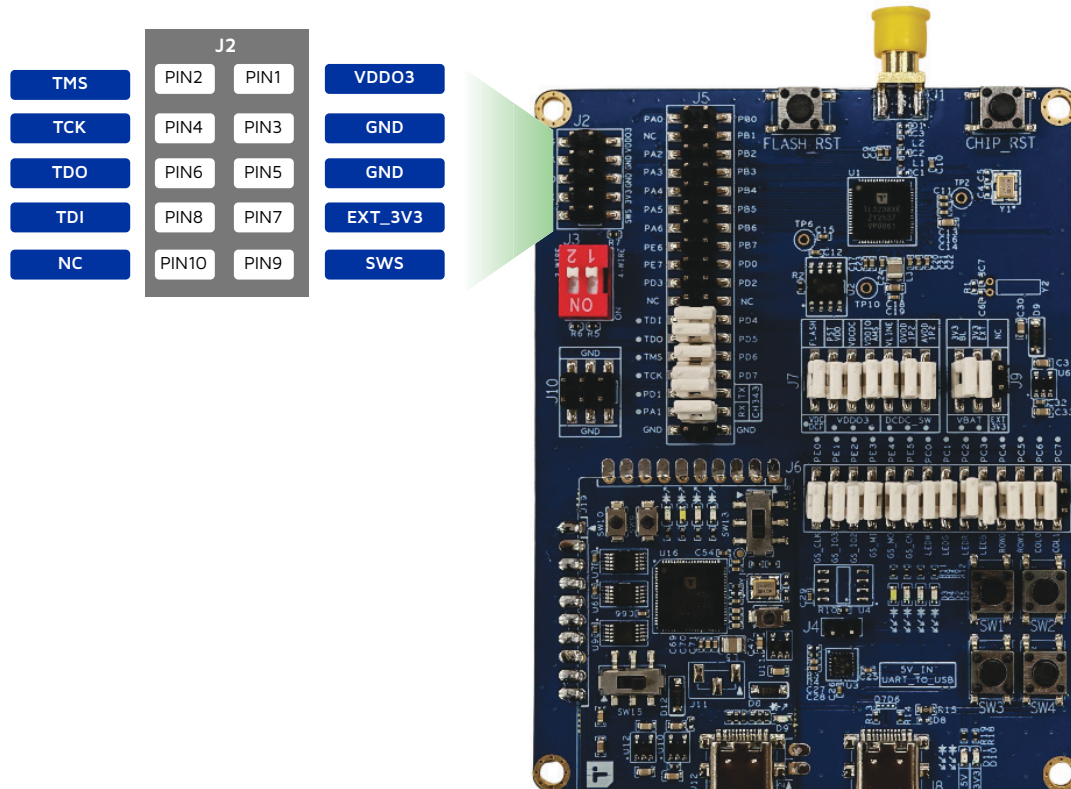
The TL3238X development board supports the following three debug methods.

Table 2-2 Debug Methods

No.	Debug method	Connector	Description
1	JTAG	J4	(1) Power up the TL3238X development board. (2) J2 supports 4-wire JTAG function - U1.PIN7.PD4 to J2.PIN8 - TDI - U1.PIN62.PD5 to J2.PIN6 - TDO - U1.PIN8.PD7 to J2.PIN4 - TCK - U1.PIN9.PD6 to J2.PIN2 - TMS
2	Single Wire		(1) Power up the TL3238X development board. (2) J2 supports Telink proprietary debug protocol, single wire. U1.PIN60.PA7 to J2.PIN9 - SWS
3	BEVK module		(1) Connect the USB Type-C port of the J12 BEVK module to a PC, and use BDT version 5.9.0 or later. (2) For usage instructions, refer to 2.6 Peripheral Interface - BEVK Module

The following figure shows the details of each J2 pins.

Figure 2-2 Debug Interfaces on the Board





2.3 Current Measurement

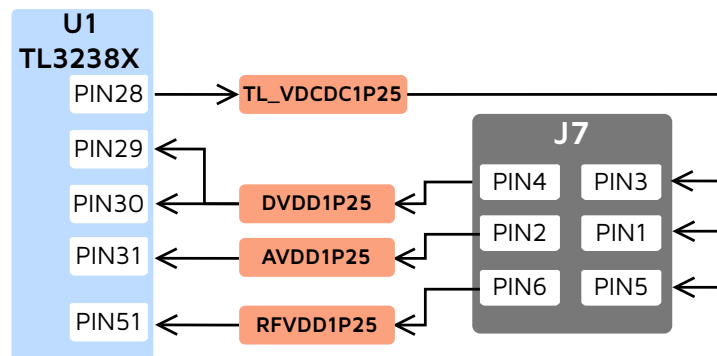
The methods to measure the current of each pin of TL3238X development board are provided as follows.

Table 2-3 Current Measurement Method of the Board

No.	Test item	Power supply	Description
1	Total current of the chip	TL_VBAT	(1) The main power supply of the chip is TL_VBAT. (2) When using the above method 1 power supply, pull out the jumpers between J9 PIN1 and PIN2. Connect in series an ammeter, at this time the total chip current can be measured. (3) When using the above method 2 power supply, pull out the jumpers between J9 PIN1 and PIN2. Then pull out the jumpers between J9 PIN3 and PIN4, connect in series an ammeter, at this time the total chip current can be measured. (4) Make sure that there is no external power consumption and no GPIO external current (including JTAG and SWS), so as to avoid high chip current. (5) Details refer to Figure 2-1.
2	1V25 branch current of the chip	TL_VDCDC1P25 TL_RFVDD1P25 TL_DVDD1P25 TL_AVDD1P25	(1) The PIN28 generates 1.25V branch voltage when the chip U1 is connected to 3.3V. (2) The U1 PIN28 is the 1.25V branch voltage output source. (3) The U1 PIN28 and U1 PIN29/PIN30, PIN31, PIN51 are shorted together through three jumpers, respectively, and supply power to the DVDD, AVDD and RF.

The following figures shows the connection of 1V25 branch of the chip.

Figure 2-3 The 1V25 Branch of the Chip



2.4 RF Test

The methods for conducting and radiating tests on RF of TL3238X development board are provided.

The following table lists the methods of RF test.

Table 2-4 RF Test Method

No.	Test item	Connector	Description
1	RF test	J1	(1) Power up the TL3238X development board normally. (2) RF conduction test: connect the J1 SMA connector to the test instrument to perform RF conduction test. (3) RF radiation test: connect the whip antenna in the kit to the J1 SMA connector to perform RF radiation test.

2.5 GPIO Interface

On the TL3238X development board, all GPIOs are connected to the connectors for easy access.

The following table lists the connections of all GPIO.

Table 2-5 GPIO Connections

No.	Chip pins	IO name	Connector pins
1	U1.PIN01	PB1	J5.PIN03
2	U1.PIN02	PB0	J5.PIN01
3	U1.PIN03	PD0	J5.PIN17
4	U1.PIN04	PD1	-
5	U1.PIN05	PD2	J5.PIN19
6	U1.PIN06	PD3	J5.PIN20
7	U1.PIN07	PD4	J5.PIN23
8	U1.PIN08	PD7	J5.PIN29
9	U1.PIN09	PD6	J5.PIN27
10	U1.PIN10	PA6	J5.PIN14
11	U1.PIN11	PA5	J5.PIN12
12	U1.PIN12	PA1	J5.PIN34
13	U1.PIN13	PA2	J5.PIN06
14	U1.PIN14	PA4	J5.PIN10
15	U1.PIN15	PA3	J5.PIN08

No.	Chip pins	IO name	Connector pins
16	U1.PIN23	PC5	J6.PIN23
17	U1.PIN24	PC6	J6.PIN25
18	U1.PIN33	PB7	J5.PIN15
19	U1.PIN34	PB6	J5.PIN13
20	U1.PIN35	PB5	J5.PIN11
21	U1.PIN36	PB4	J5.PIN09
22	U1.PIN37	PC7	J6.PIN27
23	U1.PIN42	PC0	J6.PIN13
24	U1.PIN43	PC1	J6.PIN15
25	U1.PIN44	PC2	J6.PIN17
26	U1.PIN45	PC3	J6.PIN19
27	U1.PIN46	PC4	J6.PIN21
28	U1.PIN52	PE0	J6.PIN01
29	U1.PIN53	PE1	J6.PIN03
30	U1.PIN54	PE5	J6.PIN11
31	U1.PIN55	PE4	J6.PIN09
32	U1.PIN56	PE3	J6.PIN07
33	U1.PIN57	PE2	J6.PIN05
34	U1.PIN58	PE7	J5.PIN18
35	U1.PIN59	PE6	J6.PIN16
36	U1.PIN60	PA7_SWS	-
37	U1.PIN61	PA0	J5.PIN02
38	U1.PIN62	PD5	J5.PIN25
39	U1.PIN63	PB3	J5.PIN07
40	U1.PIN64	PB2	J5.PIN05

The following figure shows the net names of all the pins of J5 and J6 for reference.

Figure 2-4 All Pins of J5

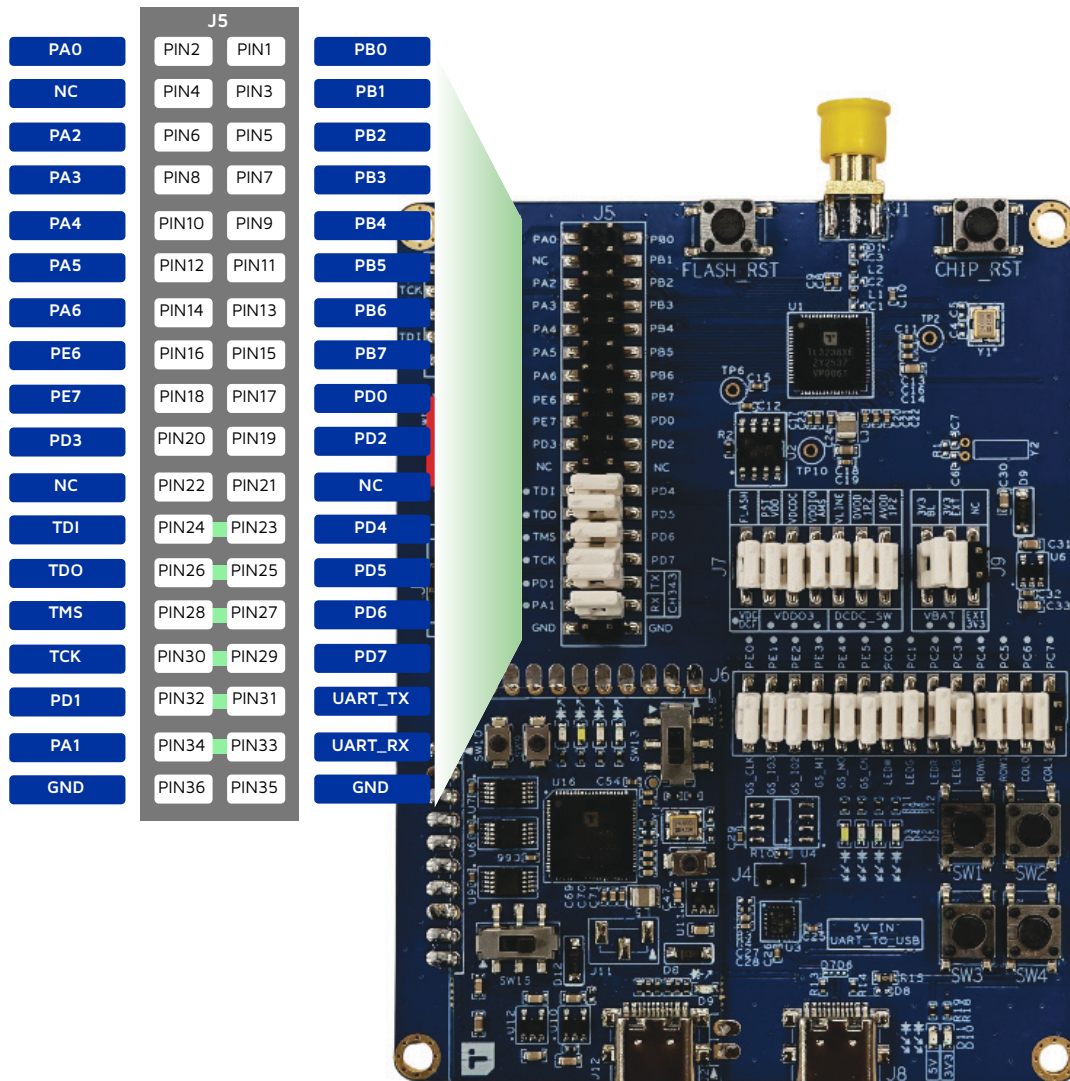
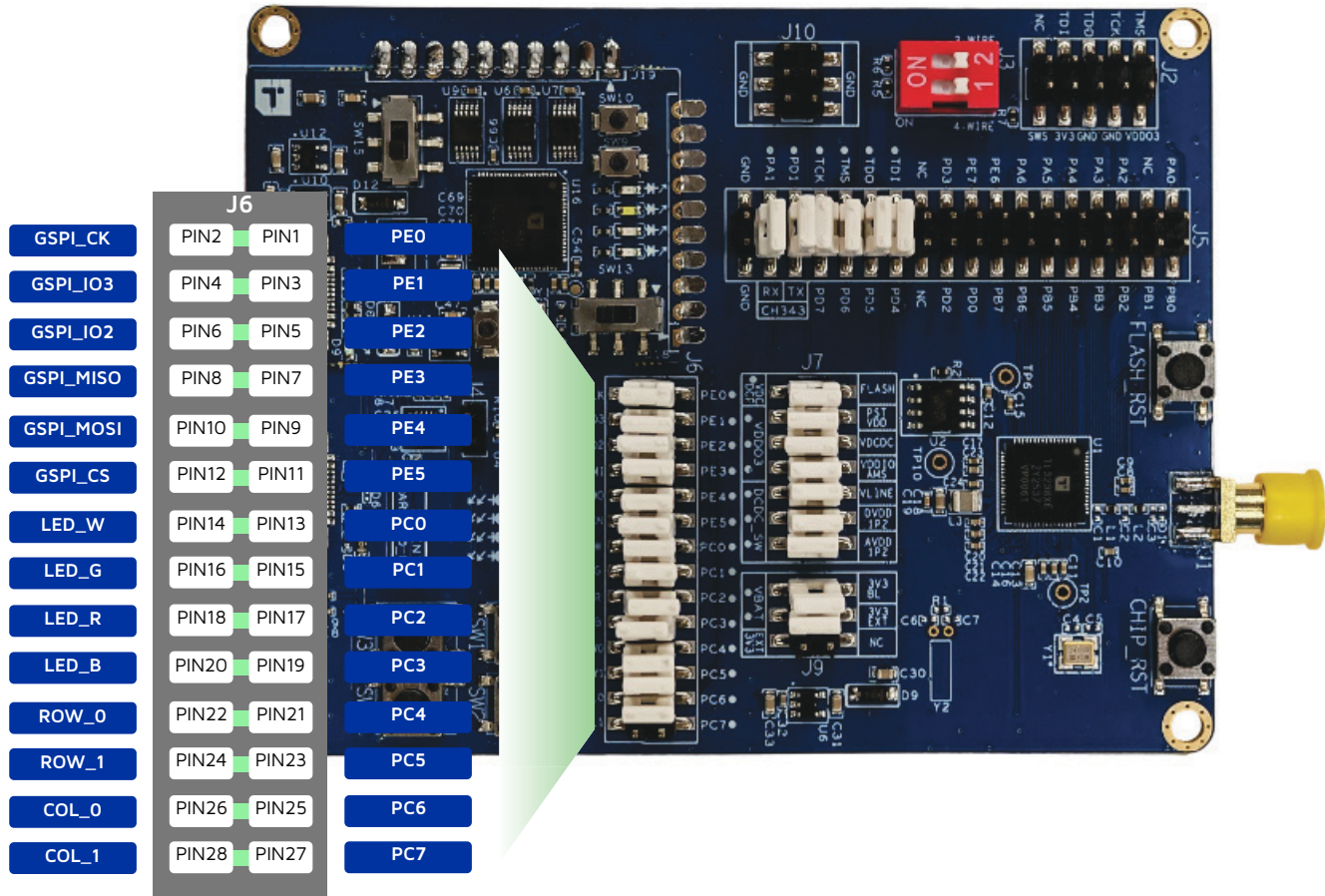


Figure 2-5 All Pins of J6


2.6 Peripheral Interface - BEVK Module

The TL3238X development board is designed with an on-board BEVK module for debugging support.

The following table lists the configuration methods for debugging with the on-board BEVK module.

Table 2-6 BEVK Module Debugging

No.	Item	Description
1	On-board BEVK module debugging	(1) The BEVK module used in the current version supports BDT version 5.9.0 or later. (2) After connecting the USB cable, use jumpers to connect J9 BL3V3, EXT3V3, and VBAT. Set SW15 on the BEVK module to the right position (left position disconnects the BEVK SWS or JTAG from U1), and set SW13 to the down position (up position selects JTAG mode). Debugging can then proceed normally. (3) On the BEVK module, the green LED indicates SWS mode, and the blue LED indicates JTAG mode.

BEVK Module Usage Instructions

Step 1 Connect the J12 USB Type-C port to a PC. The red LED indicates normal power supply.

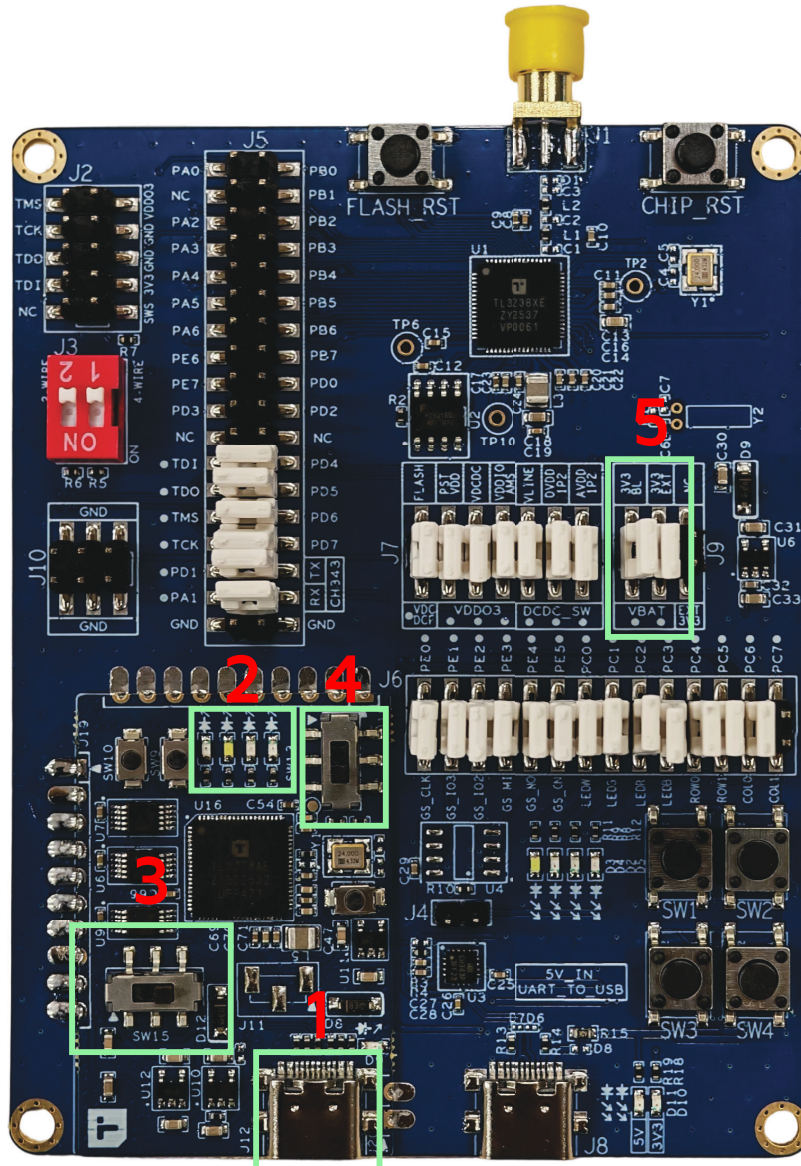
Step 2 A blinking green LED indicates that the BEVK module is operating normally.

Step 3 Set switch SW15 to the right position.

Step 4 Set switch SW13 to the down position.

Step 5 Verify that the jumpers are correctly installed.

Figure 2-6 BEVK Module



Step 6 When using Telink BDT tool, version 5.9.0 or later is required, and select V4.



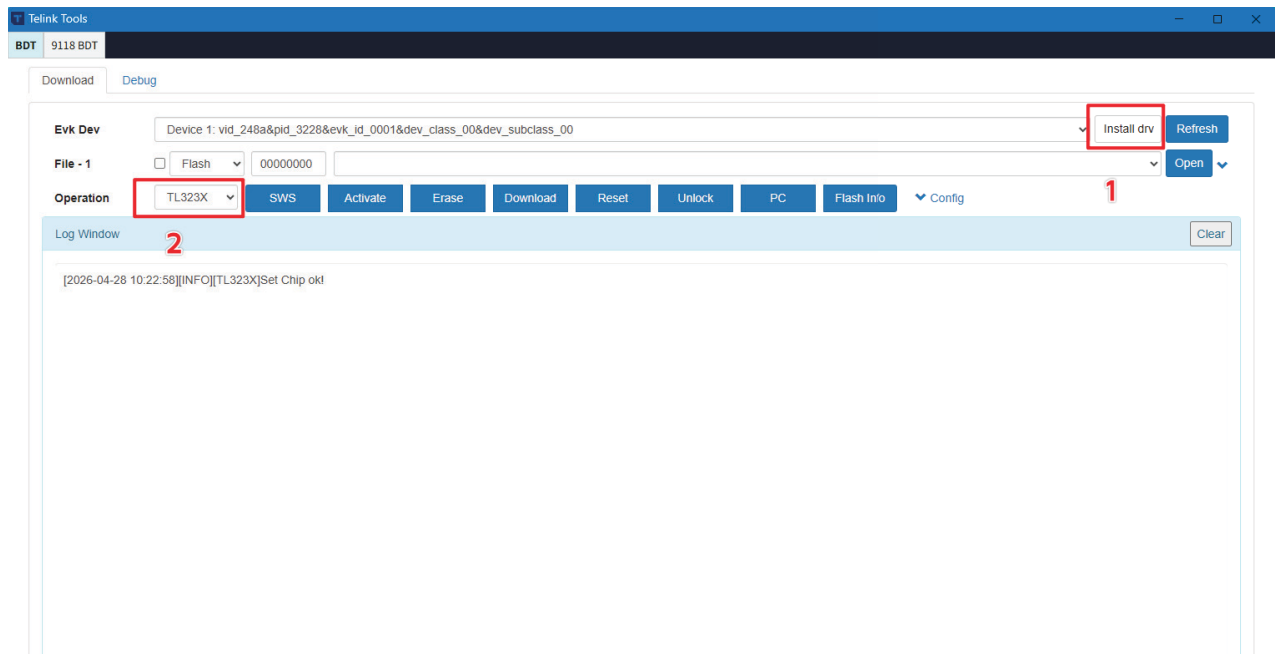
Figure 2-7 EVK Selection



Step 7 For first-time use, click "Install drv" to install the driver.

Step 8 Select the corresponding chip to begin operation.

Figure 2-8 Driver Installation and Chip Selection



2.7 Peripheral Interface - Flash

The TL3238X development board is equipped with an external flash, the part number is P25Q16SU, which is convenient for customers to extend the use or verify the new flash.

The following table lists the connections of the flash pins.

Table 2-7 Connections of Flash Pins

No.	Chip pins	IO name	Flash
1	U1.PIN19	PF0	U2.PIN05
2	U1.PIN18	PF1	U2.PIN06
3	U1.PIN17	PF2	U2.PIN07
4	U1.PIN22	PF3	U2.PIN01
5	U1.PIN21	PF4	U2.PIN02
6	U1.PIN20	PF5	U2.PIN03

3 Related Documents

The following table lists other documents and resources that you can refer to for more information. Some of these documents are only available under a Non-Disclosure Agreement (NDA). To access such documents, please contact your local Telink Field Application Engineer (FAE) or sales representative.

Table 3-1 Related Documents

No.	Name	Description	Link / Obtain method
1	TL323x datasheet	Provides information on the electrical characteristics, hardware description, and ordering options for the TL323x chips.	Contact a Telink FAE / Sales representative.
2	TL323x hardware design guideline	Provides hardware design guide for the TL323x chips.	Contact a Telink FAE / Sales representative.
3	TL3238X board files	Provides design files of schematic, PCB layout and gerber file for the TL3238X development board.	Contact a Telink FAE / Sales representative.

FCC STATEMENT

1. This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- (1) This device may not cause harmful interference, and
- (2) This device must accept any interference received, including interference that may cause undesired operation.

2. Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.

This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

Reorient or relocate the receiving antenna.

Increase the separation between the equipment and receiver.

Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

Consult the dealer or an experienced radio/TV technician for help.

RF warning statement:

The device has been evaluated to meet general RF exposure requirement.

The device can be used in portable exposure condition without restriction.