

Telink

User Manual for TL7519H Development Board

UM-TL7519H-E3

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Keyword

TL7519H, Bluetooth[®] Basic Rate (BR), Enhanced Data Rate (EDR), Low Energy (LE), Indoor Positioning, BLE Mesh, Zigbee, HomeKit, Thread, Matter, 2.4 GHz

Brief

This document is the development board user manual of Telink multi-standard wireless SoC TL7519H. It mainly introduces the development board block diagram, development board features, various peripheral interfaces and detailed function descriptions.

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Revision History

Version	Change Description
1.0.0	Initial release.
1.0.1	• Section 1.5 Connectors: Updated the pin descriptions for J3 and J65.
1.0.2	• Section 1.6 LED: Updated the descriptions for D10 and D6. • Section 1.5 Connectors: Updated the pin descriptions for J3 and J4. • Section 1.8 Switch: Updated the description for SW17. • Chapter 5 Certification Statement: Added FCC statement.

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1 Overview

The TL7519H development board is designed based on TL7519H chip and is used for application development and debugging for TL751x series chips. It is suitable for all chips in the TL751x series, including but not limited to the following:

- TL7519H
- TL7514H

The TL7519H chips support multiple protocols including Bluetooth[®] Basic Rate (BR), Enhanced Data Rate (EDR), Low Energy (LE), Indoor Positioning, BLE Mesh, Zigbee, HomeKit, Thread, Matter and 2.4 GHz proprietary protocol.

This development board supports testing of various functions, such as RF conducted test, current test, audio input and output, combination of lights and buttons, and so on.

This document provides a detailed description of the TL7519H development board's interfaces, power supply, debugging methods, audio socket, buttons, lights, jumpers, and others to make it easy for users to familiarize with this board and use it for subsequent development and debugging.

1.1 Block Diagram

The top and bottom view of the TL7519H development board are shown as below.

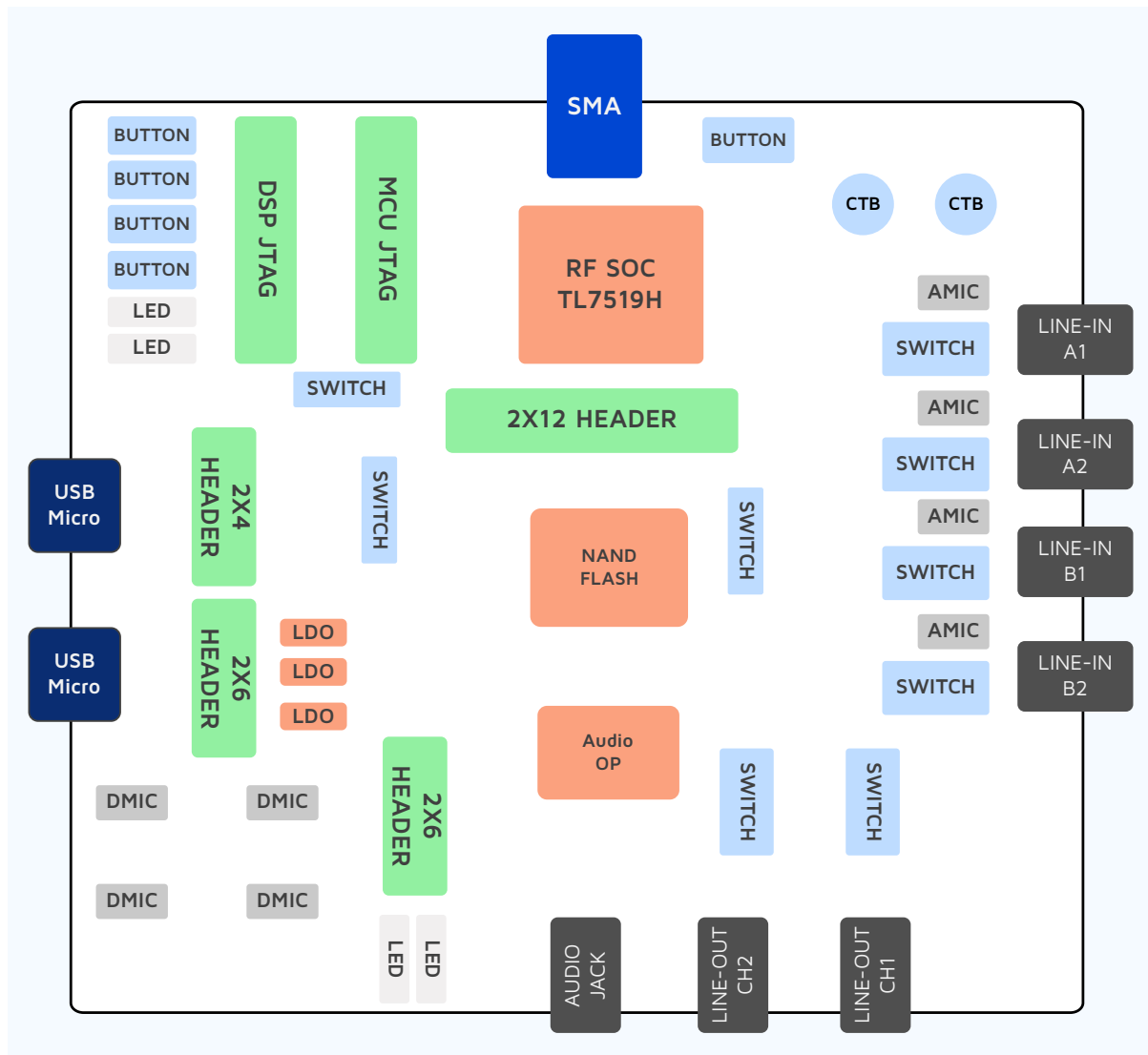
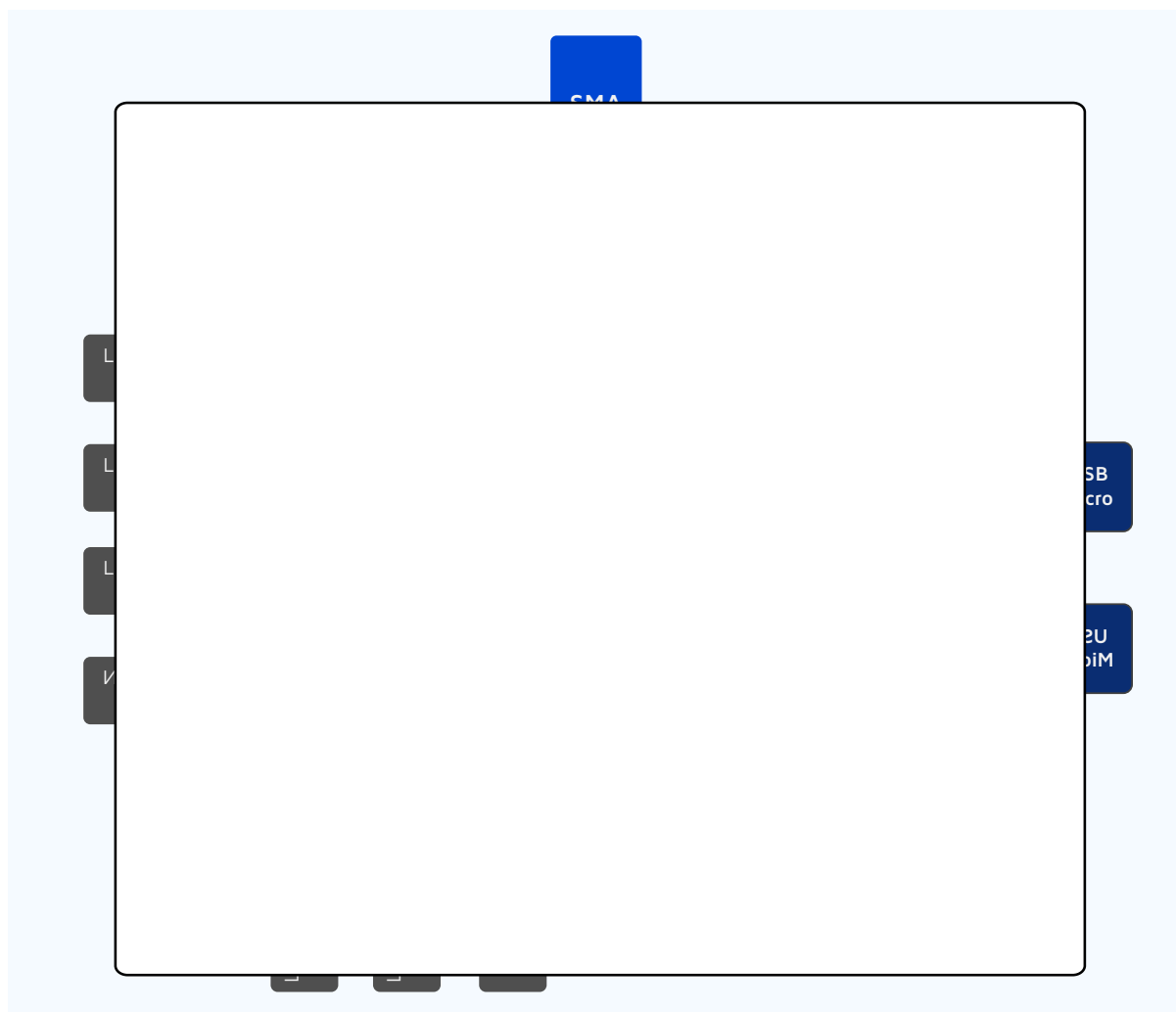
Figure 1-1 Top view of the development board


Figure 1-2 Bottom view of development board



1.2 Board Features

The following table lists the features of the TL7519H development board.

Table 1-1 Board Features

No.	Name	Description	Reference section
1	Current test interface	Total current test and each branch current test via jumper combinations	2.3 Current Measurement
2	RF interface	RF conducted test via SMA connector	2.4 RF Test
3	Debug interface	Supports JTAG, SDP, Swire interfaces; Supports Full-speed USB interface	2.2 Debug Interface
4	Peripheral interface	Supports peripherals such as Mini USB, DMIC, Nand flash, CTB, etc.	2.5 Peripheral Interface - Mini USB 2.6 Peripheral Interface - DMIC 2.7 Peripheral Interface - Nand Flash 2.8 Peripheral Interface - Capacity Touch Button (CTB)
5	Uplink interface	Supports single-ended or differential uplink testing	2.9 Uplink Interface
6	Downlink interface	Supports differential downlink testing	2.10 Downlink Interface

1.3 Kit List

The following table lists the main materials in this development kit.

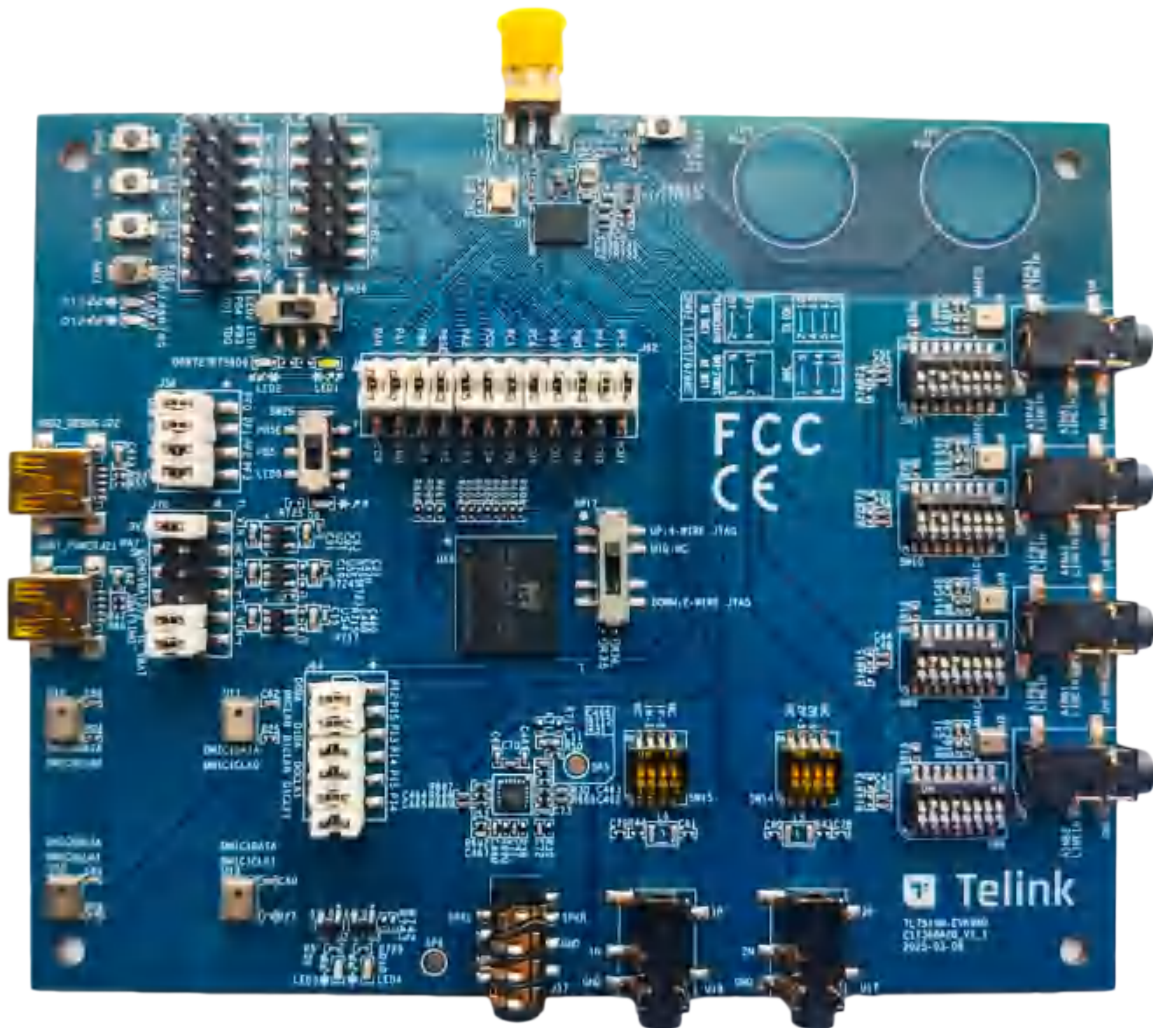
Table 1-2 Kit List

No.	Name	Quantity
1	TL7519H development board	1
2	Whip antenna	1
3	USB 2.0 Type-A to Mini USB cable	2

1.4 Board Pictures

The following picture shows the default state of the board for user verification.

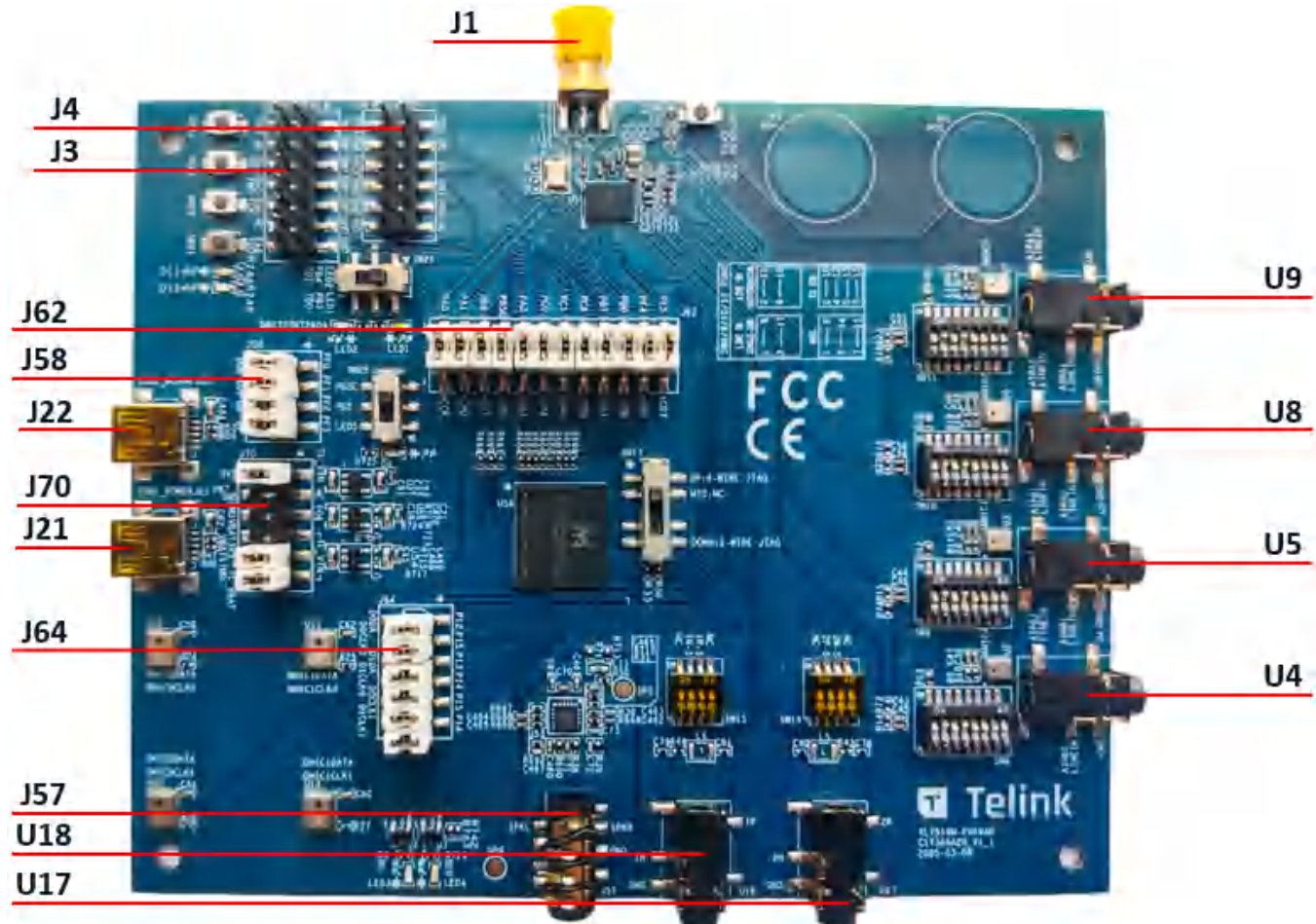
Figure 1-3 Top view of the real board



1.5 Connectors

The following figure identifies the connectors such as jumpers and sockets on the top of the development board.

Figure 1-5 Connectors on top of the board



The following table lists the connectors on the top of the development board.

Table 1-3 List of Connectors on board top

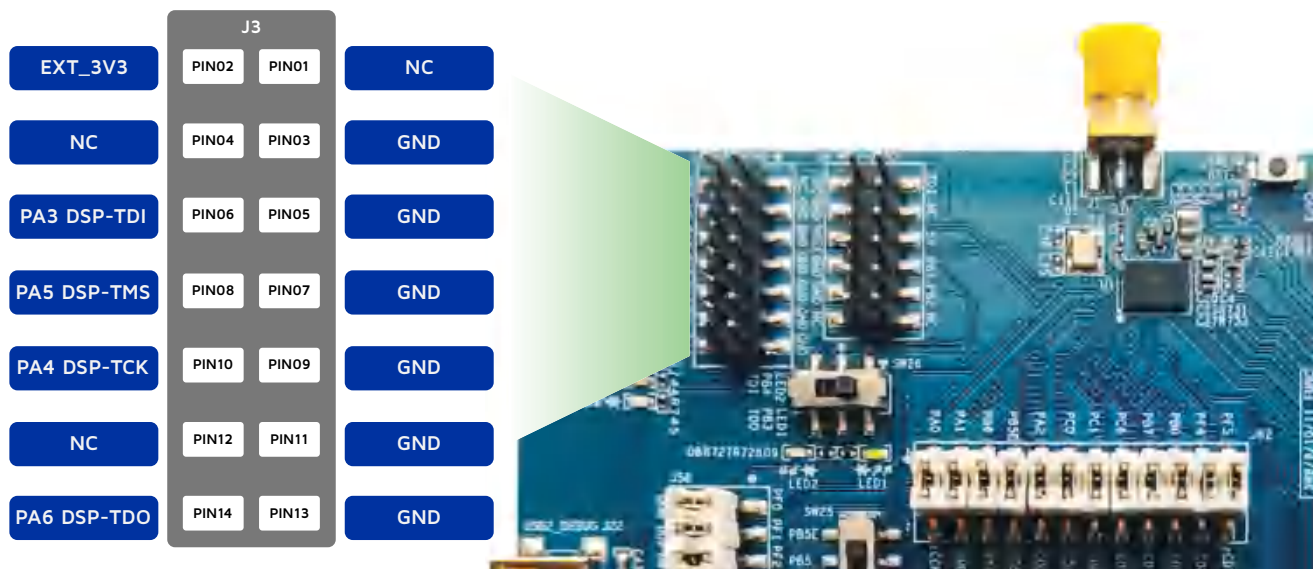
No.	Ref. Des.	Connector type	Description	Reference section
1	J1	SMA female connector	RF connector	2.4 RF Test
2	J3	2x7-pin header	DSP JTAG ^a connector	2.2 Debug Interface
3	J4	2x6-pin header	MCU JTAG ^b connector	
4	J21	Mini USB	Full-speed USB connector	2.5 Peripheral Interface - Mini USB
5	J22	Mini USB	Debug USB connector	
6	J58	2x4-pin header	USB connector	

No.	Ref. Des.	Connector type	Description	Reference section
7	J62	2x12-pin header	Nand flash connector	2.7 Peripheral Interface - Nand Flash
8	J64	2x6-pin header	DMIC connector	2.6 Peripheral Interface - DMIC
9	J70	2x6-pin header	Power and single-wire connector	2.3 Current Measurement
10	J57	Audio jack	Differential to single-ended output audio jack	2.10 Downlink Interface
11	U17	Audio jack	Differential output audio jack	
12	U18	Audio jack	Differential output audio jack	
13	U4	Audio jack	Differential input audio jack	2.9 Uplink Interface
14	U5	Audio jack	Differential input audio jack	
15	U8	Audio jack	Differential input audio jack	
16	U9	Audio jack	Differential input audio jack	

- In this document, DSP (Digital Signal Processing) JTAG supports two modes: JTAG and SDP. For details, refer to the JTAG mode selection section in [Table 1-6](#).
- MCU (Micro-controller Unit) JTAG applies in the same way as above.

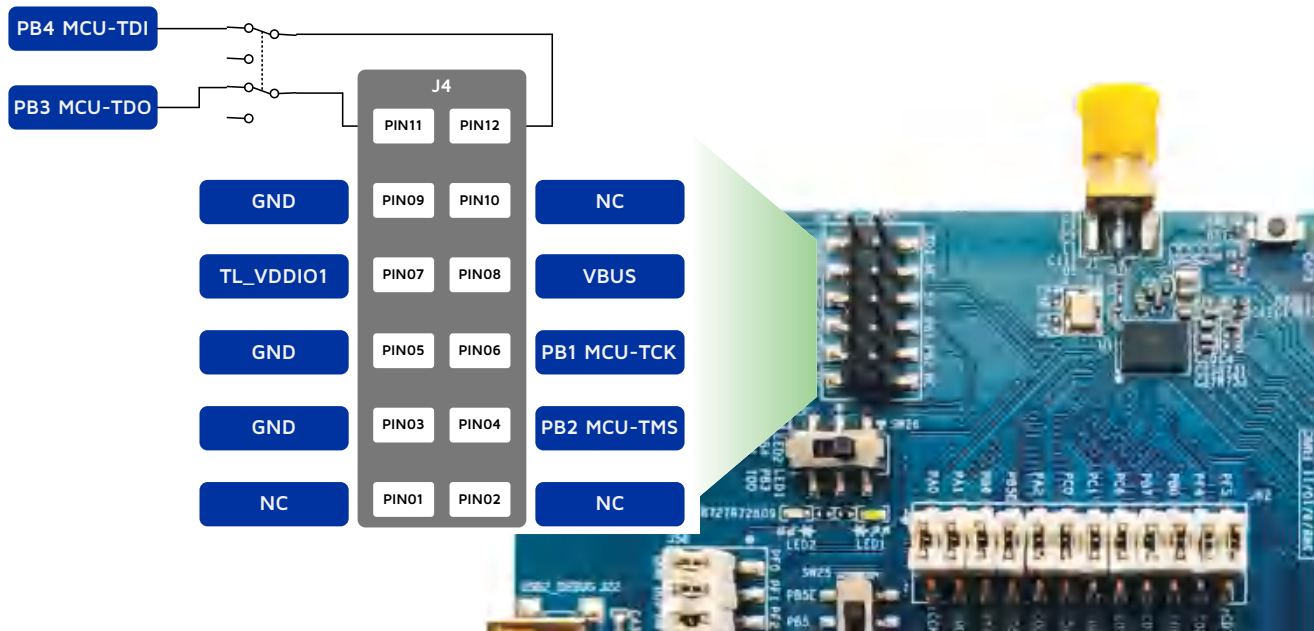
The following figure shows the description of each J3 pin.

Figure 1-6 J3 Pin Description



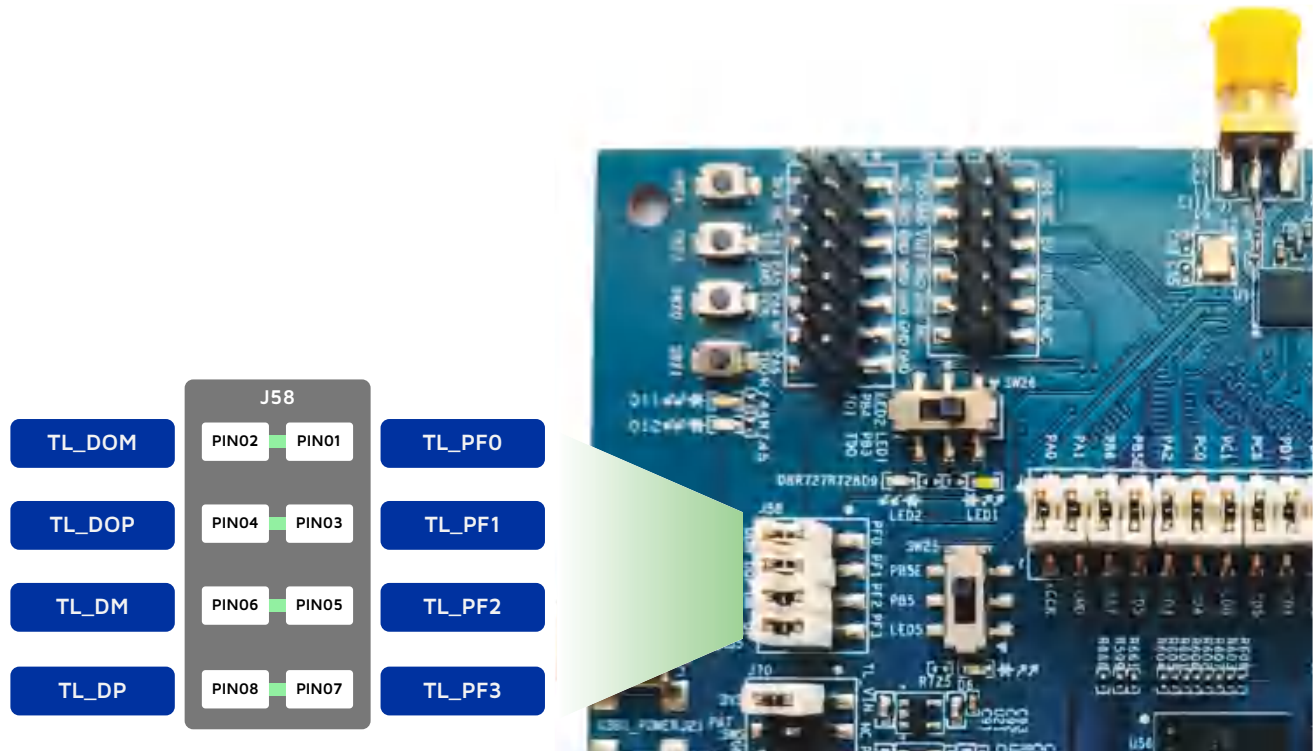
The following figure shows the description of each J4 pin.

Figure 1-7 J4 Pin Description



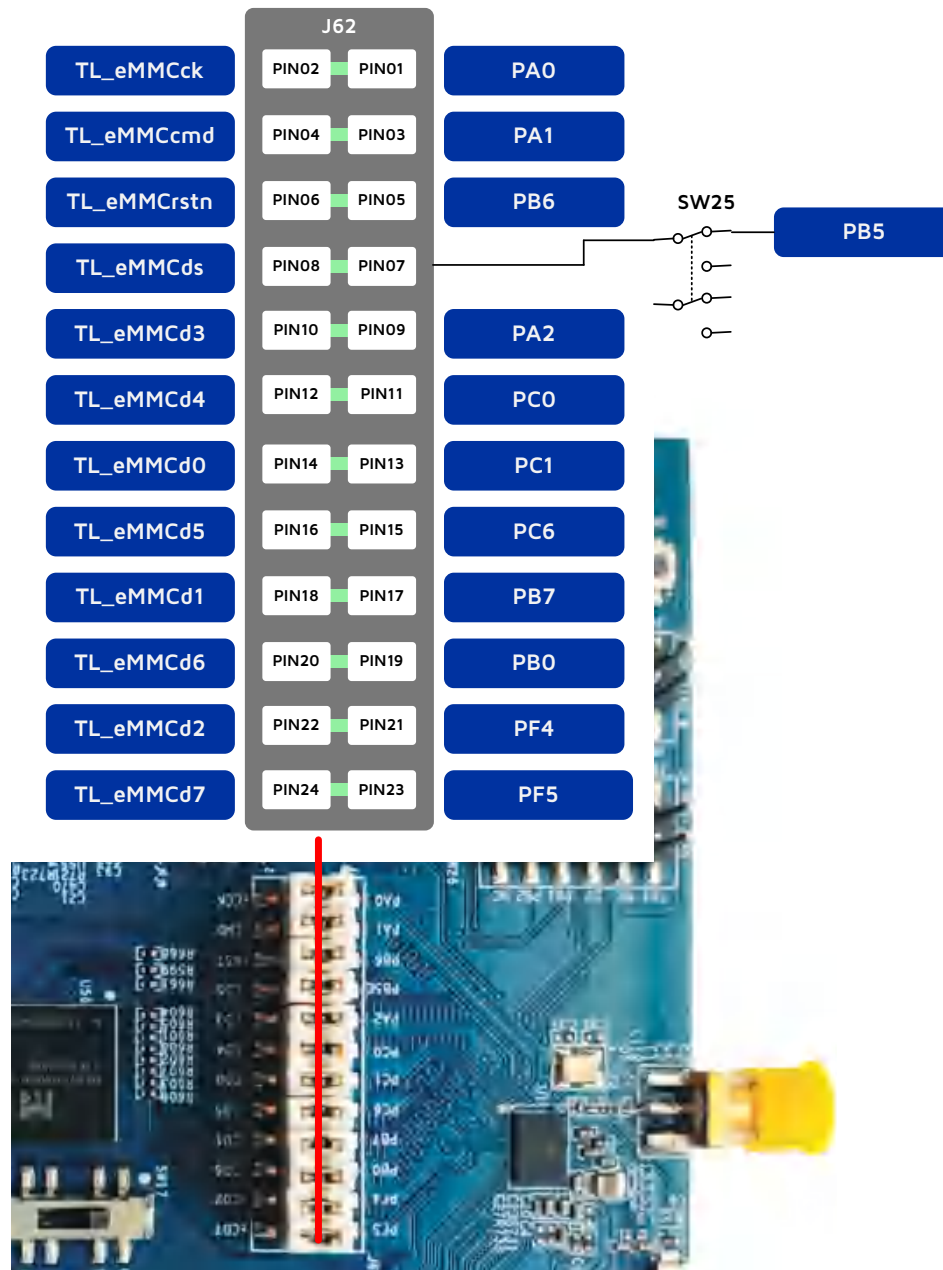
The following figure shows the description of each J58 pin.

Figure 1-8 J58 Pin Description



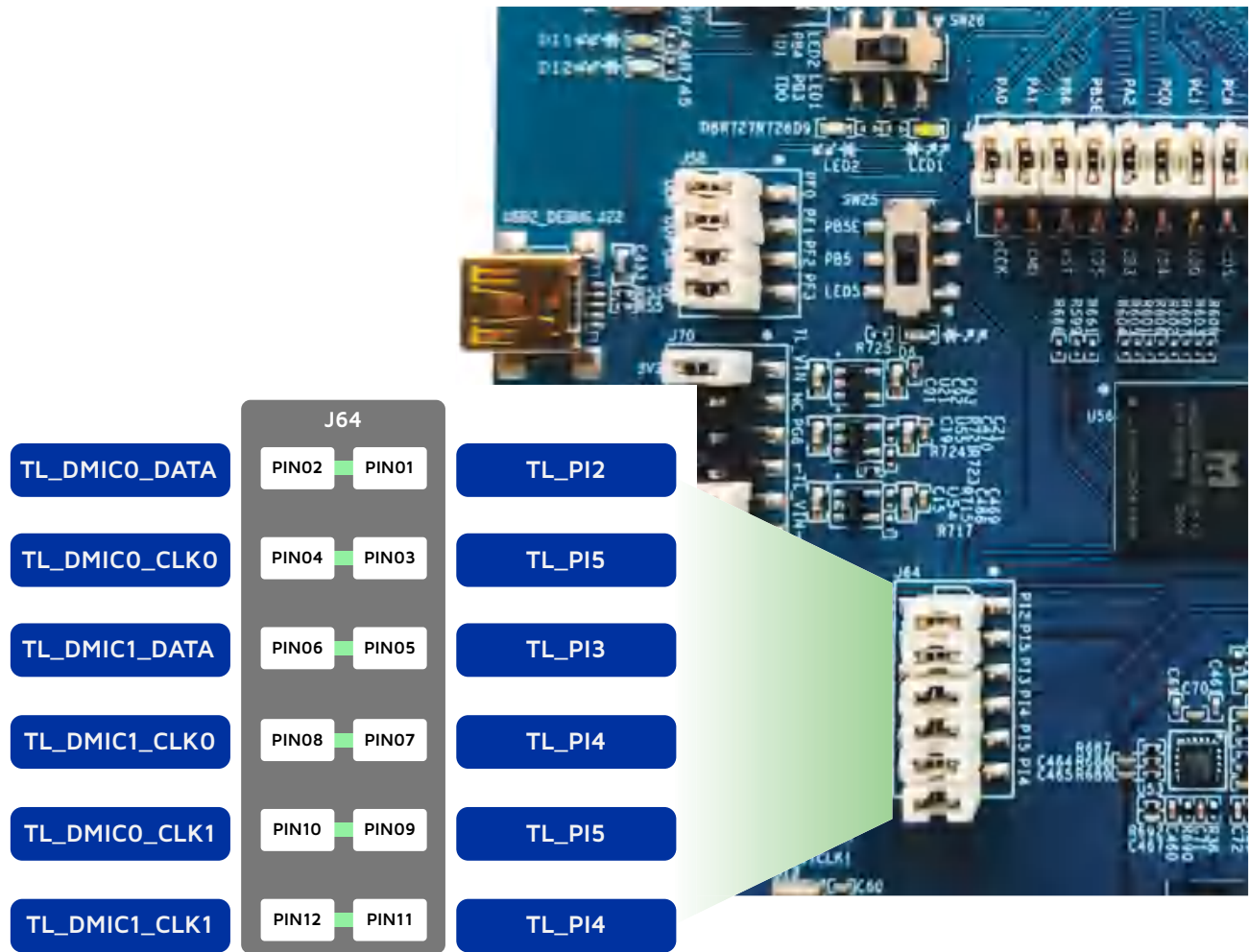
The following figure shows the description of each J62 pin.

Figure 1-9 J62 Pin Description



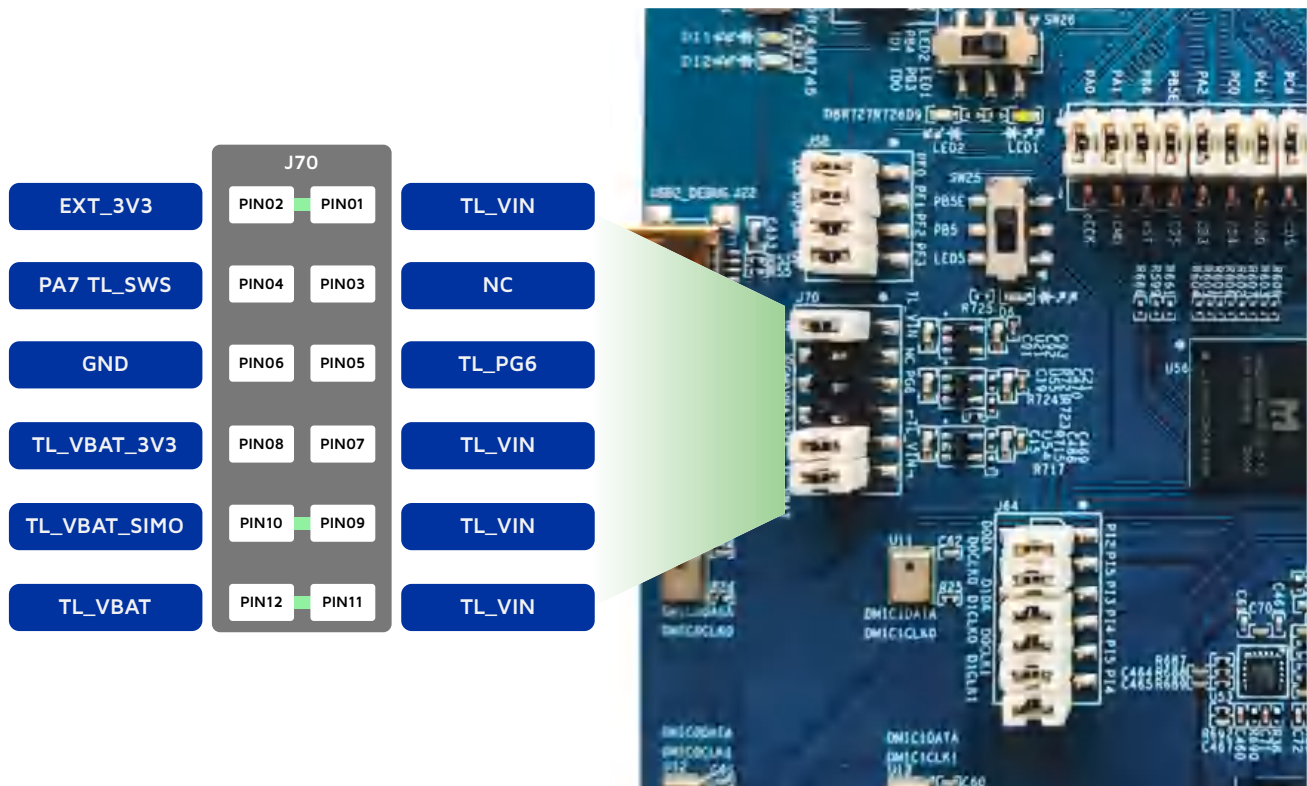
The following figure shows the description of each J64 pin.

Figure 1-10 J64 Pin Description



The following figure shows the description of each J70 pin.

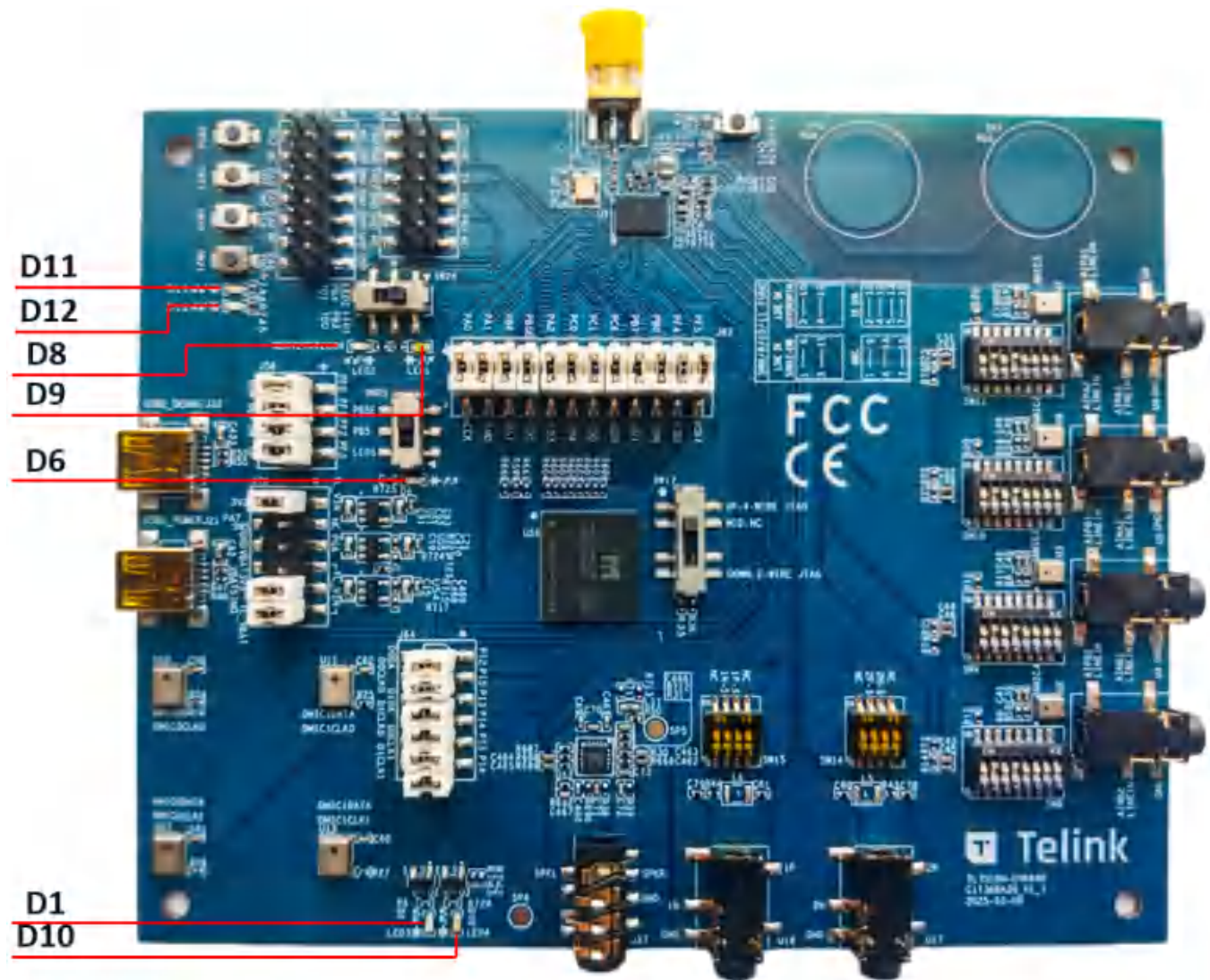
Figure 1-11 J70 Pin Description



1.6 LED

The following figure identifies the LEDs on the top of the development board.

Figure 1-12 LEDs on top of the board



The following table lists the LEDs on the top of the board.

Table 1-4 LEDs on board top

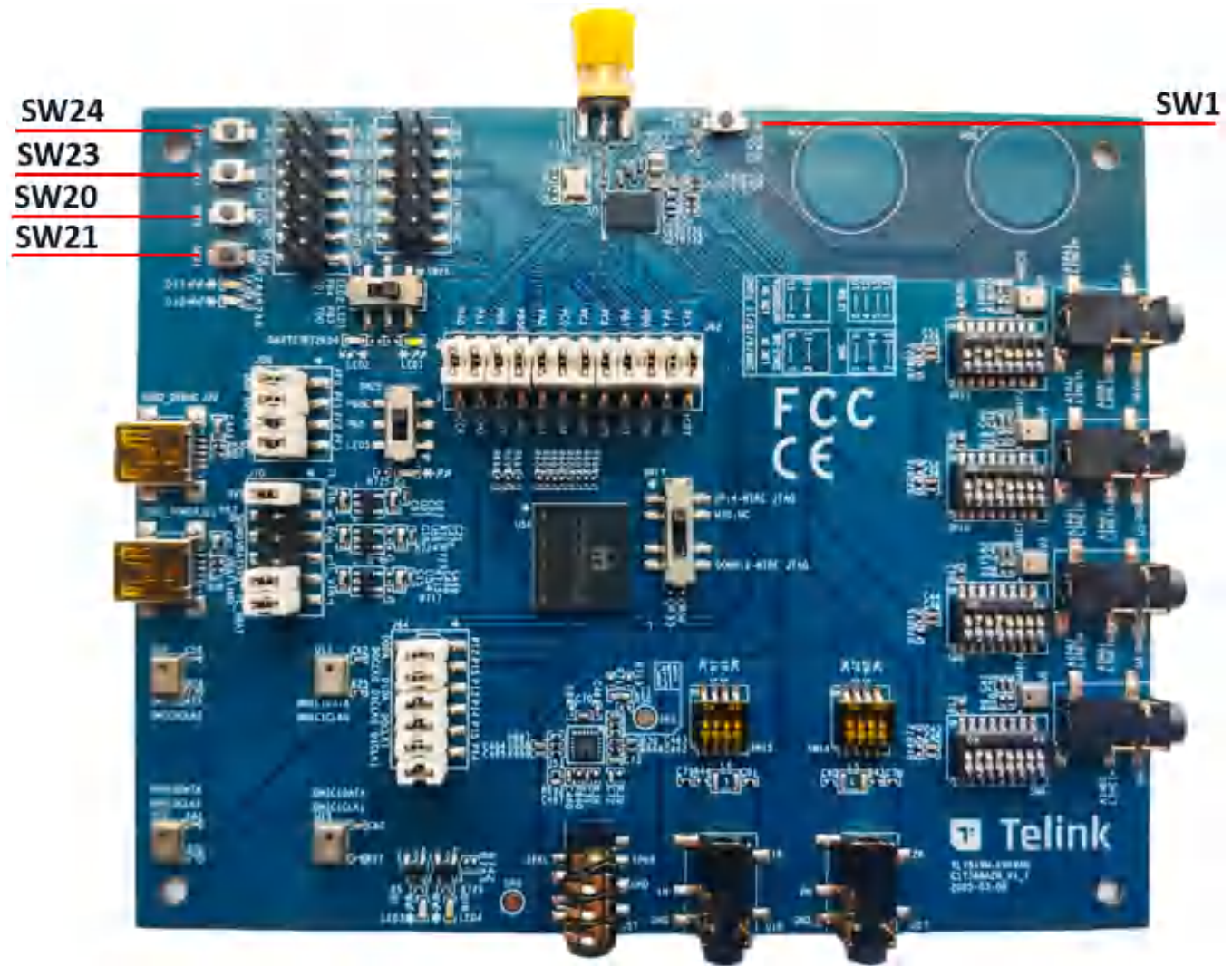
No.	Ref. Des.	LED color	Description
1	D12	Blue	- PA3 of TL7519H controls D12 - PA3 is a DSP JTAG signal, multiplexed as an LED control signal - D12 turns on when PA3 outputs high voltage level; D12 turns off when PA3 outputs low voltage level

No.	Ref. Des.	LED color	Description
2	D11	Green	- PA4 of TL7519H controls D11 - PA4 is a DSP JTAG signal, multiplexed as an LED control signal - D11 turns on when PA4 outputs high voltage level; D11 turns off when PA4 outputs low voltage level
3	D8	Red	- Set SW26 to the right position, PB4 of TL7519H controls D8 - PB4 is an MCU JTAG signal, multiplexed as an LED control signal - D8 turns on when PB4 outputs high voltage level; D8 turns off when PB4 outputs low voltage level
4	D9	White	- Set SW26 to the right position, PB3 of TL7519H controls D9 - PB3 is an MCU JTAG signal, multiplexed as an LED control signal - D9 turns on when PB3 outputs high voltage level; D9 turns off when PB3 outputs low voltage level
5	D10	Green	- PI1 of TL7519H controls D10 - PI1 belongs to the 1.8V voltage domain - D10 turns on when PI1 outputs high voltage level; D10 turns off when PI1 outputs low voltage level
6	D1	Blue	- PIO of TL7519H controls D1 - PIO belongs to the 1.8V voltage domain - D1 turns on when PIO outputs high voltage level; D1 turns off when PIO outputs low voltage level
7	D6	Yellow	- Set SW25 to the down position, PB5 of TL7519H controls D6 - PB5 is a Nand flash signal, multiplexed as an LED control signal - D6 turns on when PB5 outputs high voltage level; D6 turns off when PB5 outputs low voltage level

1.7 Button

The following figure identifies the buttons on the top of the development board.

Figure 1-13 Buttons on top of the board



The following table lists the buttons on the top of the board.

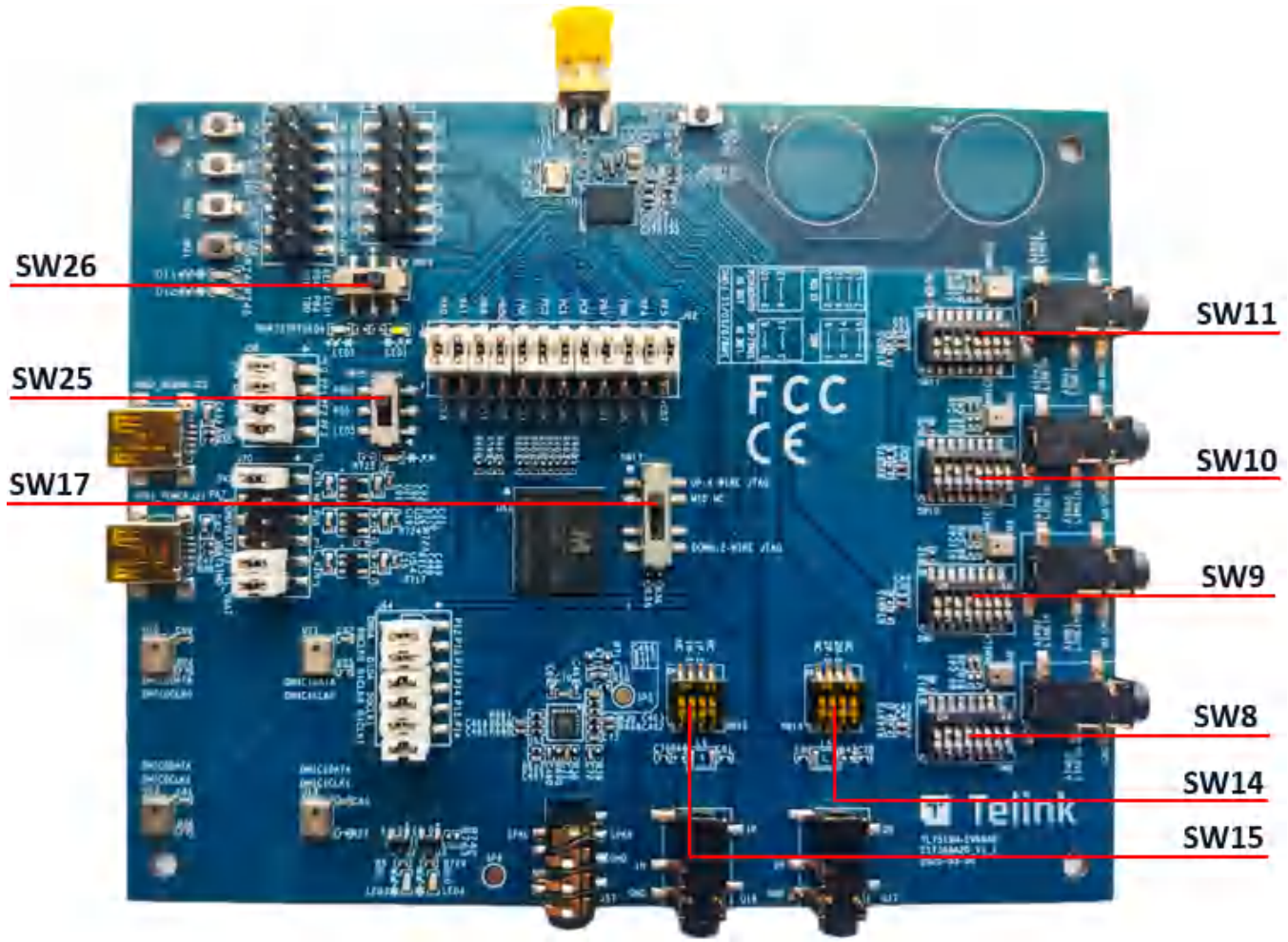
Table 1-5 List of buttons on the board top

No.	Ref. Des.	Function	Description
1	SW1	Chip reset	Press SW1 to reset the main chip
2	SW23	-	PA5 is a DSP JTAG signal, multiplexed as a key control signal
3	SW24	-	PA6 is a DSP JTAG signal, multiplexed as a key control signal
4	SW20	-	PB1 is an MCU JTAG signal, multiplexed as a key control signal
5	SW21	-	PB2 is an MCU JTAG signal, multiplexed as a key control signal

1.8 Switch

The following figure identifies the switches on the top of the development board.

Figure 1-14 Switches on top of the board



The following table lists the switch functions on the top of the board.

Table 1-6 List of switches on board top

No.	Ref. Des.	Function	Description
1	SW26	LED and MCU JTAG selection	- When SW26 is set to the left position, PB3/4 are used as MCU JTAG signals. - When SW26 is set to the right position, PB3/4 are used as LED control signals (default).
2	SW25	LED and Nand flash selection	- When SW25 is set to the up position, PB5 is connected to the Nand flash (default). - When SW25 is set to the down position, PB5 is used as an LED control signal.

No.	Ref. Des.	Function	Description
3	SW17	JTAG mode selection	- PB6 is the MCU JTAG mode selection pin. - By default, set SW17 to the up position before EVB power-up, the MCU operates in JTAG (four-wire: TDI, TDO, TMS, TCK) mode. - Before EVB power-up, when SW17 is set to the down position, the MCU operates in SDP (two-wire: TMS, TCK) mode. - When SW17 is set to the middle position, PB6 is connected to the Nand flash via J62.
4	SW15	Audio output selection	- SW15 is used for mode switching between differential and single-ended outputs for Audio output channel1. - When all SW15 DIP switches are set to the down position, Audio output channel1 is connected to U18 and operates in differential output mode(default). - When all SW15 DIP switches are set to the up position, Audio output channel1 is connected to J57 and operates in single-ended output mode.
5	SW14	Audio output selection	- SW14 is used for mode switching between differential and single-ended outputs for Audio output channel2. - When all SW14 DIP switches are set to the down position, Audio output channel2 is connected to U17 and operates in differential output mode(default). - When all SW14 DIP switches are set to the up position, Audio output channel2 is connected to J57 and operates in single-ended output mode.
6	SW8	Audio input selection	- SW8 is a multi-mode switch for audio input B2. - SW8 supports four external connection modes via four DIP switch settings: (1) Differential input connection: set SW8.CH2 and SW8.CH4 to the up position (default) (2) Single-ended input connection: set SW8.CH1 and SW8.CH3 to the up position (3) On-board AMIC connection: set SW8.CH1, SW8.CH6 and SW8.CH7 to the up position (4) External ECM(Electret Condenser Microphone) connection: set SW8.CH2, SW8.CH4, SW8.CH5 and SW8.CH7 to the up position

No.	Ref. Des.	Function	Description
7	SW9	Audio input selection	- SW9 is a multi-mode switch for audio input B1. - SW9 supports four external connection modes via four DIP switch settings. For details, refer to the DIP switch settings for SW8.
8	SW10	Audio input selection	- SW10 is a multi-mode switch for audio input A2. - SW10 supports four external connection modes via four DIP switch settings. For details, refer to the DIP switch settings for SW8.
9	SW11	Audio input selection	- SW11 is a multi-mode switch for audio input A1. - SW11 supports four external connection modes via four DIP switch settings. For details, refer to the DIP switch settings for SW8.

2 Function Description

2.1 Power Supply

The TL7519H development board can be powered by the following ways:

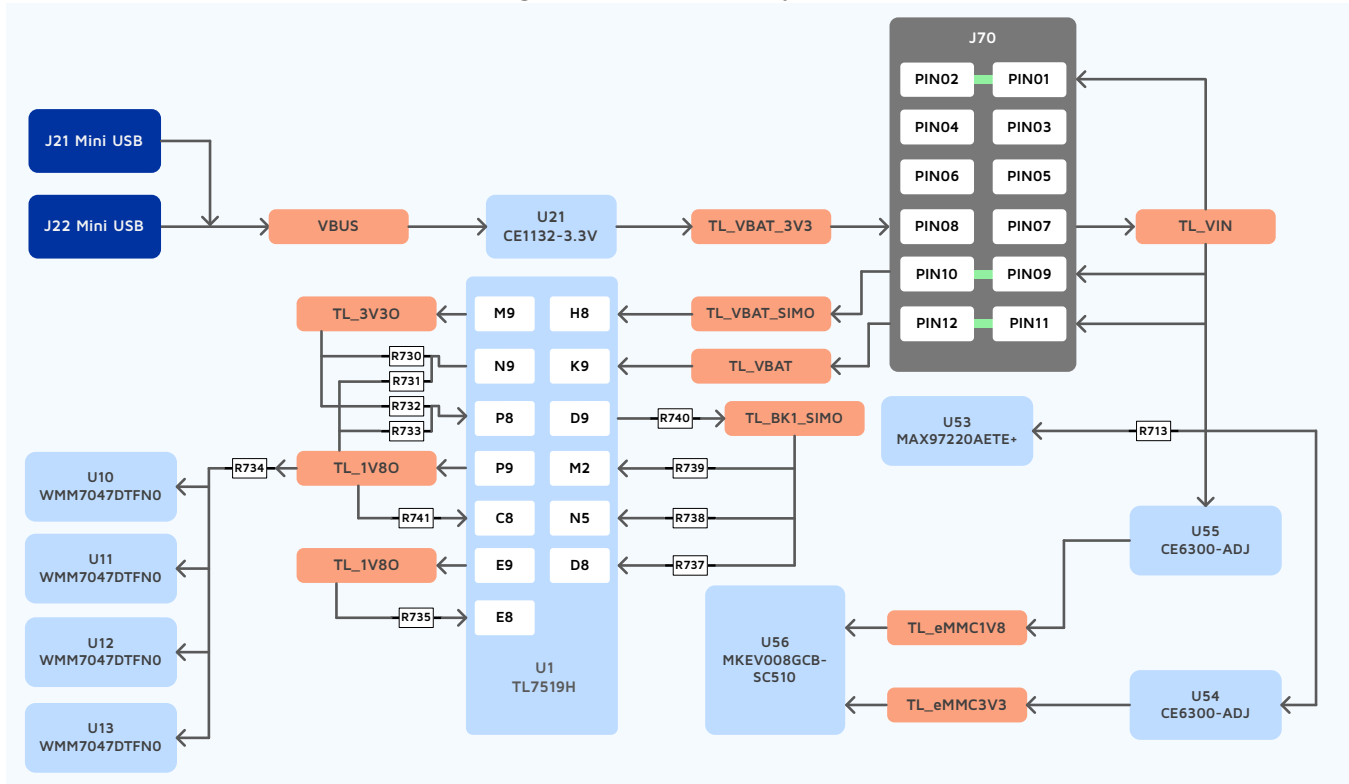
- 5V via the Mini USB port;
- 1.8V ~ 4.2V is supplied to the U1.PIN42 (VBAT) via J51.PIN12.

The following table lists the power path of the chip.

Table 2-1 Power supply of the chip

No.	Power source	Power supply	Description
1	External power via connector J70.PIN7	TL_VIN	Apply an external voltage of 1.8V ~ 4.2V to J70.PIN7. Ensure the jumpers (J70.PIN10–PIN9 and PIN12–PIN11) are installed to directly supply TL_VBAT to pins K9 and H8 of U1. Both K9 and H8 pins should be powered simultaneously to supply the chip; either one missing results in failure.
2	External power via Mini USB (J21 or J22)	VBUS	1. Connect a Type-A to Mini USB cable to either J21 or J22 to power the system. 2. When a Type-A to Mini USB cable is connected to J21 or J22, 5V is supplied to U21, which then generates TL_VBAT_3V3 to J70.PIN8. Install a jumper between PIN8 and PIN7 of J70, and ensure that the jumpers between PIN10–PIN9 and PIN12–PIN11 of J70 are also installed.

The following figure shows the power supply path of the main power sources.

Figure 2-1 Power supply path


2.2 Debug Interface

The TL7519H development board supports the following two debug methods.

Table 2-2 Debug method

No.	Debug method	Connector	Description
1	Single Wire	J70	Power up the TL7519H development board. (1) J70 supports Telink proprietary debug protocol, single wire. • U1.PINA4.PA7 to J70.PIN4 - SWS (2) Connect the SWM of the burner with this SWS.
2	MCU JTAG	J4	Power up the TL7519H development board. J4 supports the MCU JTAG interface.
3	DSP JTAG	J3	Power up the TL7519H development board. J3 supports the DSP JTAG interface.

2.3 Current Measurement

The methods to measure the current of TL7519H development board are provided as follows.

Table 2-3 Current measurement method of the board

No.	Test item	Power supply	Description
1	Total current of the chip	TL_VBAT TL_VBAT_SIMO	1. The chip requires simultaneous power supply to pins K9 and H8 of U1; either one missing results in failure. 2. When powering via Method 1 above, remove the jumpers between J70.PIN10–PIN9 and PIN12–PIN11. Then connect ammeters in series at these positions. The sum of the two measured currents is the total chip current. 3. When powering via Method 2 above, install a jumper between PIN8 and PIN7 of J70. Then remove the jumpers between J70.PIN10–PIN9 and PIN12–PIN11, and connect ammeters in series at these positions. The sum of the two measured currents is the total chip current. 4. Make sure that there is no external power consumption and no GPIO external current (including JTAG and SWS), so as to avoid high chip current. 5. For details, refer to Figure 2-1.

2.4 RF Test

The methods for conducted and radiated tests on RF of TL7519H development board are provided.

The following table lists the methods of RF test.

Table 2-4 RF test method

No.	Test item	Connector	Description
1	RF test	J1	Power up the TL7519H development board normally. (1) RF conducted test: connect the J1 SMA connector to the test instrument to perform RF conducted test. (2) RF radiated test: connect the whip antenna in the kit to the J1 SMA connector to perform RF radiated test.

2.5 Peripheral Interface - Mini USB

The TL7519H development board is designed with a Mini USB connector for power supply, debugging and full-speed communication.

The following table lists the connections of DM and DP.

Table 2-5 DM and DP of USB

No.	Chip pins	IO name	Connector pins	Description
1	U1.F1	PF0	J22.PIN02	- J22 is used for system power supply and debug information output. - J21 is used for system power supply and supporting the Full-speed USB protocol. - The corresponding pins of J21 and J22 of U1 are connected via J58. - The pin location refers Figure 1-5.
2	U1.F2	PF1	J22.PIN03	
3	U1.G1	PF2	J21.PIN02	
4	U1.H1	PF3	J21.PIN03	

2.6 Peripheral Interface - DMIC

The TL7519H development board is designed with four DMICs.

The following table lists the connections of DMIC pin.

Table 2-6 Connection of DMIC pin

No.	Chip pins	IO name	Connector pins	Description
1	U1.G4	PI2	J64.PIN01	- The corresponding pins of U1, U2, U3, U6, and U7 are connected via J64. - The pin location refers Figure 1-5.
2	U1.H6	PI3	J64.PIN05	
3	U1.J6	PI4	J64.PIN07 J64.PIN11	
4	U1.K6	PI5	J64.PIN03 J64.PIN09	

2.7 Peripheral Interface - Nand Flash

The TL7519H development board is designed with a Nand flash.

The following table lists the connections of the flash pins.

Table 2-7 Connections of flash pins

No.	Chip pins	IO name	Net name	Nand Flash
1	U1.B7	PA0	TL_eMMCck	U56.M6
2	U1.B6	PA1	TL_eMMCcmd	U5.M5
3	U1.B2	PB6	TL_eMMCstn	U5.K5
4	U1.C1	PB5 ^a	TL_eMMCDs	U5.H5
5	U1.A6	PA2	TL_eMMCD3	U5.B2
6	U1.A3	PC0	TL_eMMCD4	U5.B3
7	U1.A2	PC1	TL_eMMCD0	U5.A3
8	U1.A1	PC6	TL_eMMCD5	U5.B4
9	U1.B1	PB7	TL_eMMCD1	U5.A4
10	U1.E2	PB0	TL_eMMCD6	U5.B5
11	U1.G2	PF4	TL_eMMCD2	U5.A5
12	U1.H2	PF5	TL_eMMCD7	U5.B6

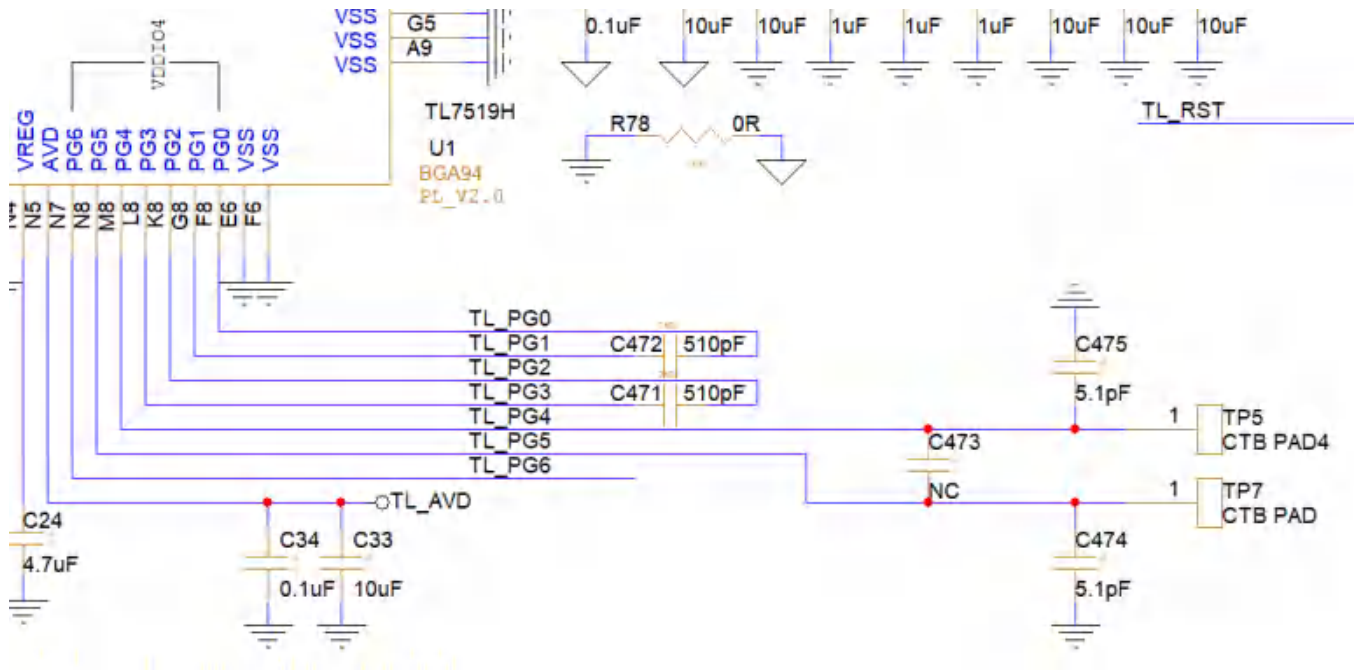
- a. Note: When connecting PB5 to the Nand flash via J62, set SW25 to the up position.

2.8 Peripheral Interface - Capacity Touch Button (CTB)

The TL7519H supports two channels of Capacity Touch Button (CTB). In actual applications, a capacitor (e.g., C472) must be connected in parallel between PG0 and PG1, and another capacitor (e.g., C471) between PG2 and PG3. One or two detection channels can be selected from PG4, PG5, and PG6. Typically, a pF-level capacitor is connected in parallel on each selected channel (e.g., C474, C475). Note: The capacitor values in the figure are for reference only; actual values on the development board prevail.

The reference circuit is shown in the figure below.

Figure 2-2 CTB Reference Circuit



2.9 Uplink Interface

The TL7519H development board supports four uplink channels: A1, A2, B1, and B2. The uplink supports four AMICs and four single-ended or differential LINE-IN paths. All configurations above can be set via jumpers.

The following example demonstrates configuring the A1 uplink channel; the configuration for the other three channels is identical.

The following table lists the configuration methods for the A1 uplink path.

Table 2-8 Configuration of A1 uplink path

No.	Chip pins	Description
1	Differential LINE-IN configuration	- The default connection of the development board is two-channel differential connection, with SW11.CH2 and SW11.CH4 set to the up position. - At this point, connect the 3.5mm socket U9 to the audio test instrument for uplink performance testing. - To achieve better performance, differential connections are generally used in practical applications.
2	Single-ended LINE-IN configuration	- When SW11.CH1 and SW11.CH3 are set to the up position, the configuration is set to single-ended connection mode. - To achieve better performance and avoid noise interference, differential connections are recommended in practical applications rather than single-ended connections.
3	Onboard AMIC configuration	Set SW11.CH1, SW11.CH6, and SW11.CH7 to the up position to enable the onboard AMIC U7.
4	External ECM configuration	- Set SW11.CH2, SW11.CH4, SW11.CH5, and SW11.CH7 to the up position. - At this point, the 3.5-mm audio jack U9 can be used to connect to an external ECM. - In this case, U9.PIN02 (silkscreened as AINA1) is connected to the negative (N) terminal of the external ECM, and U9.PIN03 (silkscreened as AIPA1) is connected to the positive (P) terminal of the external ECM.

2.10 Downlink Interface

The downlink of the TL7519H development board supports two-channel differential output, and single-ended configuration is not supported. Additionally, to facilitate demonstration of the solution, a differential to single-ended conversion circuit is designed on the development board.

The following table lists the downlink configuration methods.

Table 2-9 Configuration of downlink path

No.	Configuration	Description
1	Differential LINE-OUT configuration	- The default connection of the development board is a two-channel differential connection, where all four channels of both SW14 and SW15 are set to the down position. - At this point, connect the two 3.5mm sockets U17 and U18 to the audio test instrument for downlink performance testing.
2	Differential to Single-ended LINE-OUT configuration	- Set all four channels of both SW14 and SW15 to the down position. - At this point, connect a standard stereo headphone cable to the 3.5mm socket J57 for the solution demonstration.

3 Development Board Design and Layout

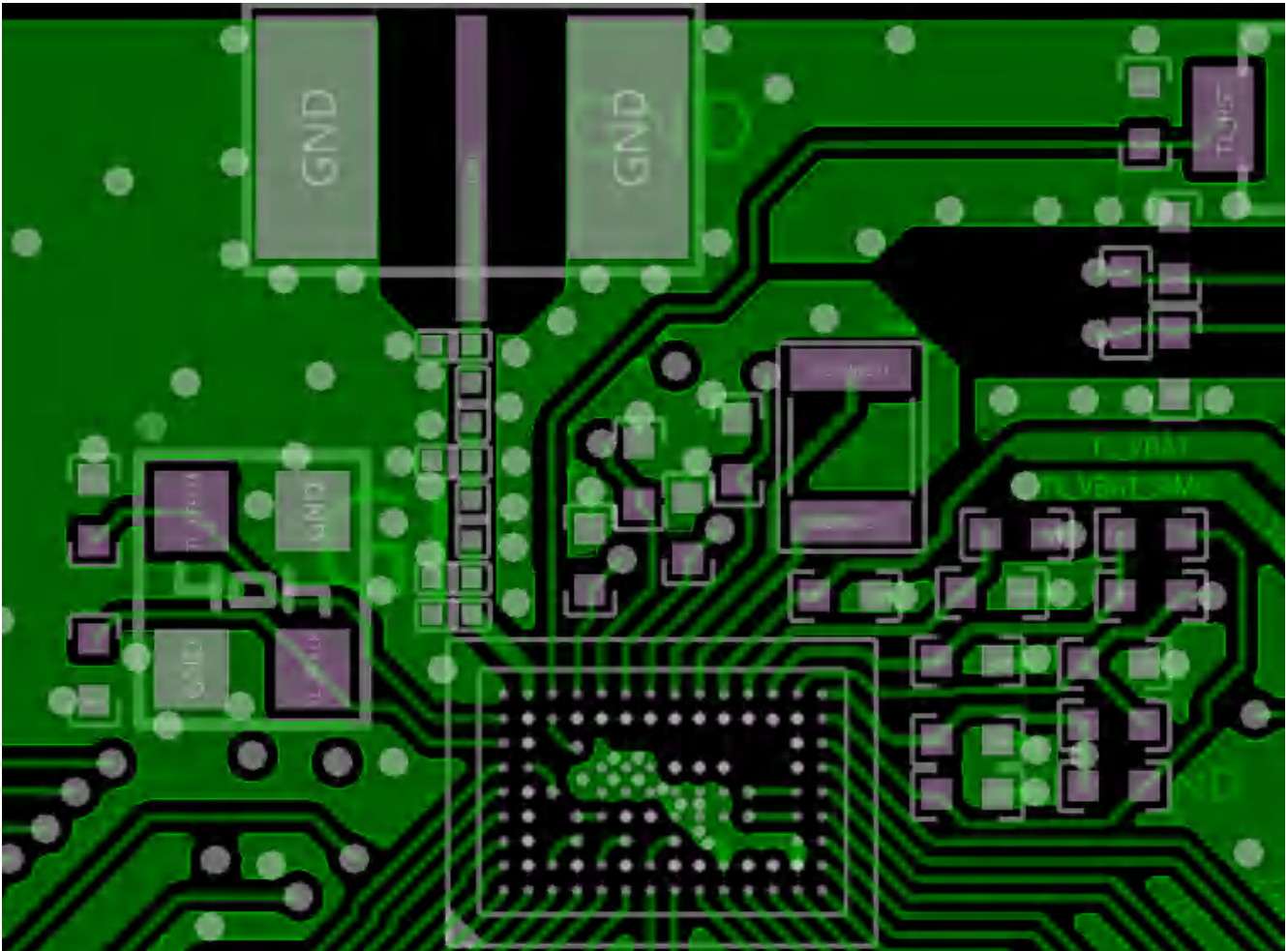
To achieve a successful wireless hardware design, particular attention must be paid to component packaging, RF layout, circuit matching, antenna design, and RF measurement capabilities. The RF circuit design, layout, and antenna design require specialized knowledge, experience, and dedicated tools.

Based on the hardware reference designs and RF design guidelines provided by Telink, as well as the recommendations in this document, hardware engineers can design RF circuit boards with excellent performance.

The PCB layout is a critical factor that directly impacts RF performance. Therefore, to achieve optimal RF performance, we recommend using Telink's reference design optimized for RF performance.

The figure below shows an example of PCB layout for the key RF regions.

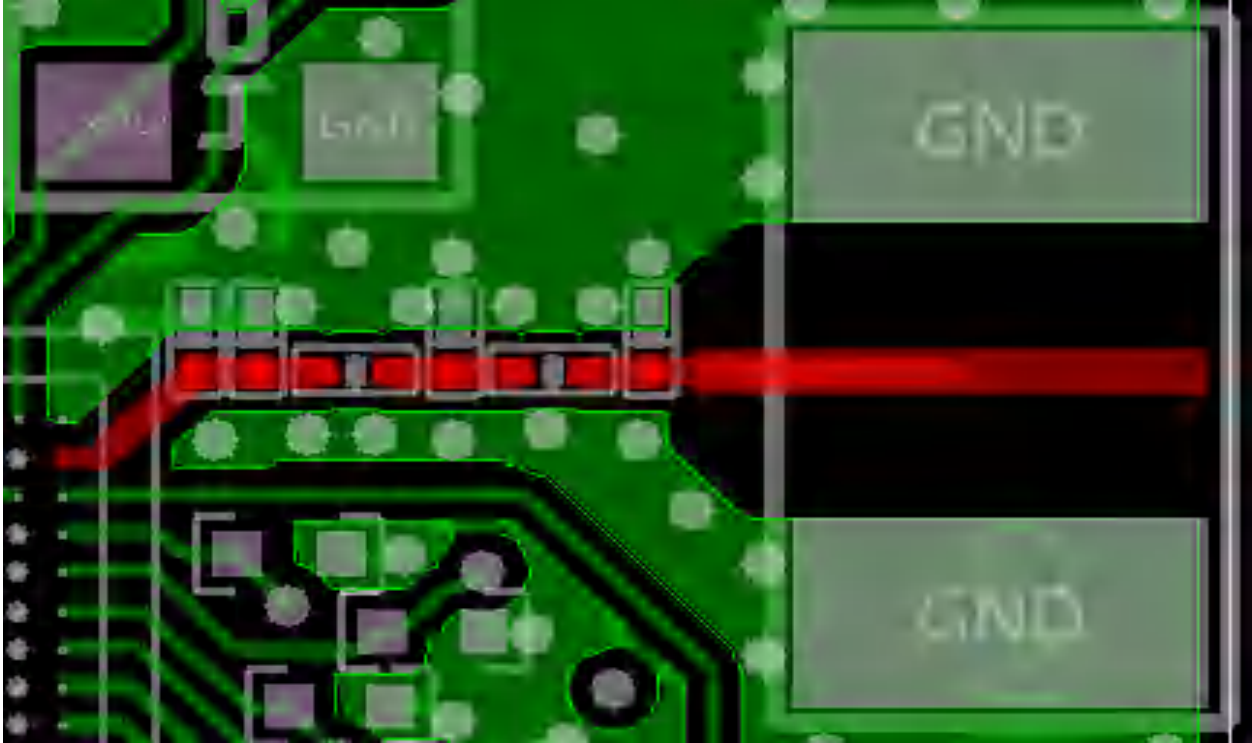
Figure 3-1 Example Layout of Key RF Regions



3.1 RF Routing Recommendations

The figure below shows the RF port routing (highlighted in red).

Figure 3-2 RF Port Routing

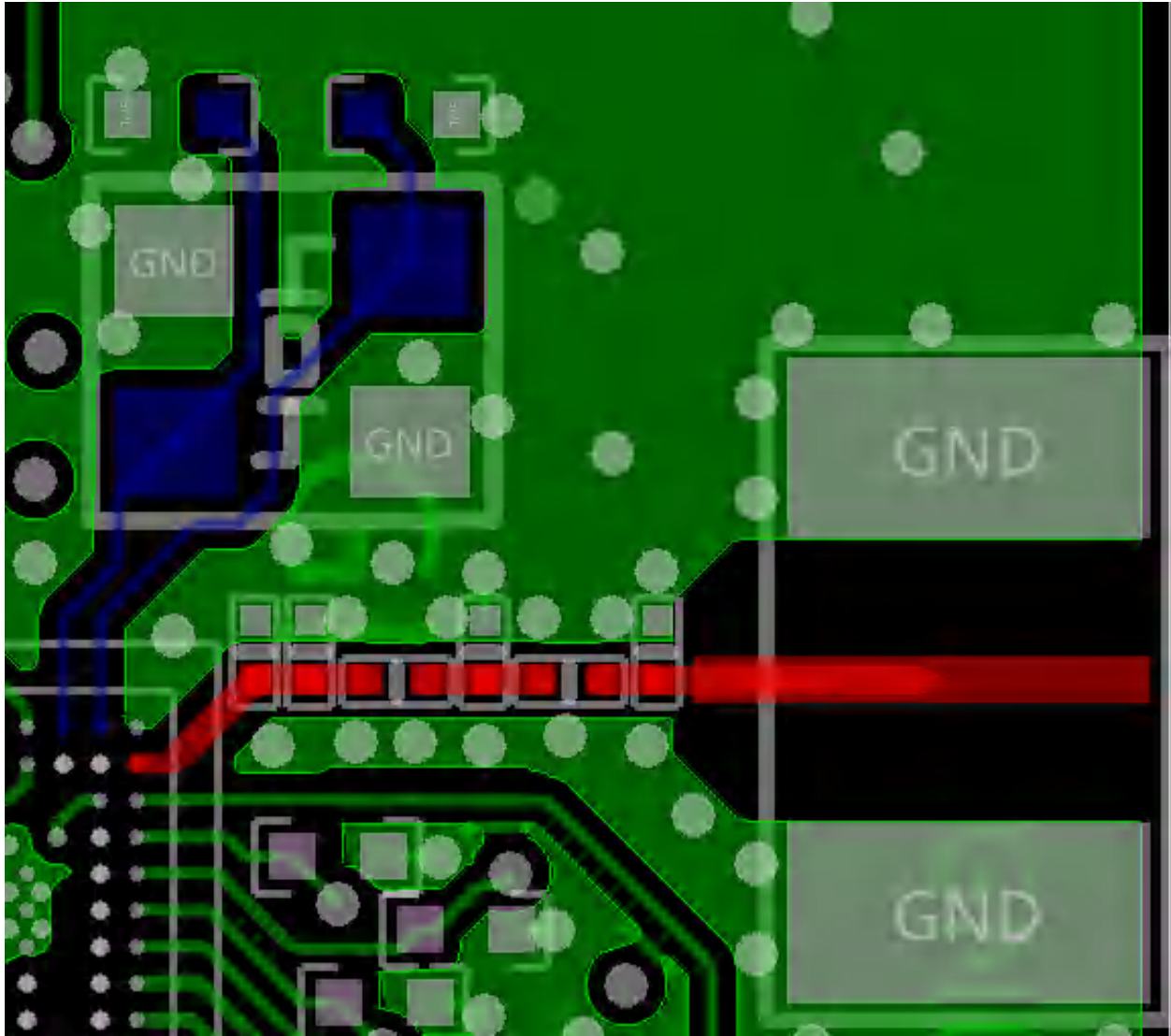


These red-highlighted traces represent the RF signal paths. Users should coordinate with the PCB manufacturer to design these traces as 50-ohm transmission lines. Factors such as trace width, spacing between the traces and surrounding shapes, and PCB stack-up design are critical to achieving a robust RF design. It is recommended to place multiple via holes along the RF routing to provide effective shielding. For RF impedance matching, Murata GRM series capacitors and LQP series inductors are recommended.

3.2 Crystal Layout Recommendations

The figure below shows the crystal routing (highlighted in blue).

Figure 3-3 Crystal Routing



Below are some recommendations for crystal layout:

- The crystal must be placed perpendicular to RF traces; parallel routing is not permitted.
- Keep the crystal traces as symmetrical as possible.
- Ensure adequate isolation and shielding between the crystal circuit components and other components.

The crystal selected for the TL7519H development board is the E3SB48E001D01E. Considering variations in parasitic capacitance across customer-designed boards, it is recommended to consult the crystal manufacturer to select a crystal with an appropriate load capacitance (CL).

The table below lists the parameters of the E3SB48E001D01E crystal.

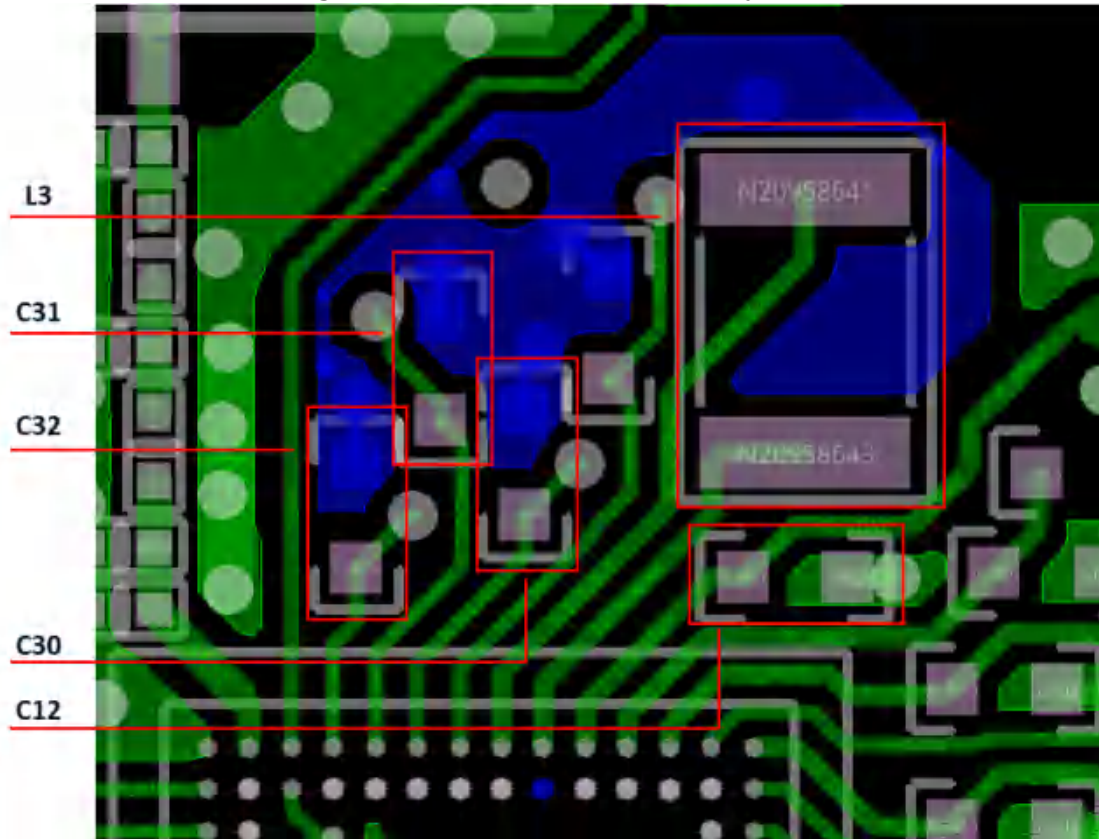
Table 3-1 E3SB48E001D01E Parameters

No.	Item	Symb.	Electrical Specification				Remark
			Min.	Typ.	Max.	Units	
1	Nominal Frequency	F0	48.000000			MHz	
2	Mode of Vibration		Fundamental				
3	Frequency Tolerance	$\Delta F/F0$	-10	-	10	ppm	At 25°C±3°C
4	Operating Temperature Range	T _{OPR}	-40	-	85	°C	
5	Frequency Stability Ref. to 25°C	TC	-10	-	10	ppm	-30~85°C
			-20	-	20	ppm	-40~85°C
6	Storage Temperature	T _{STG}	-55	-	125	°C	
7	Load capacitance	CL	-	6	-	pF	
8	Equivalent Series Resistance	ESR	-	-	50	Ω	
9	Drive Level	DL	-	100	200	μW	
10	Insulation Resistance	IR	500	-	-	MΩ	At 100V _{DC}
11	Shunt Capacitance	C0	-	-	3	pF	
12	Aging Per Year	Fa	-2	-	2	ppm	First Year
13	Package type	E3SB					

3.3 DCDC Power Layout Recommendations

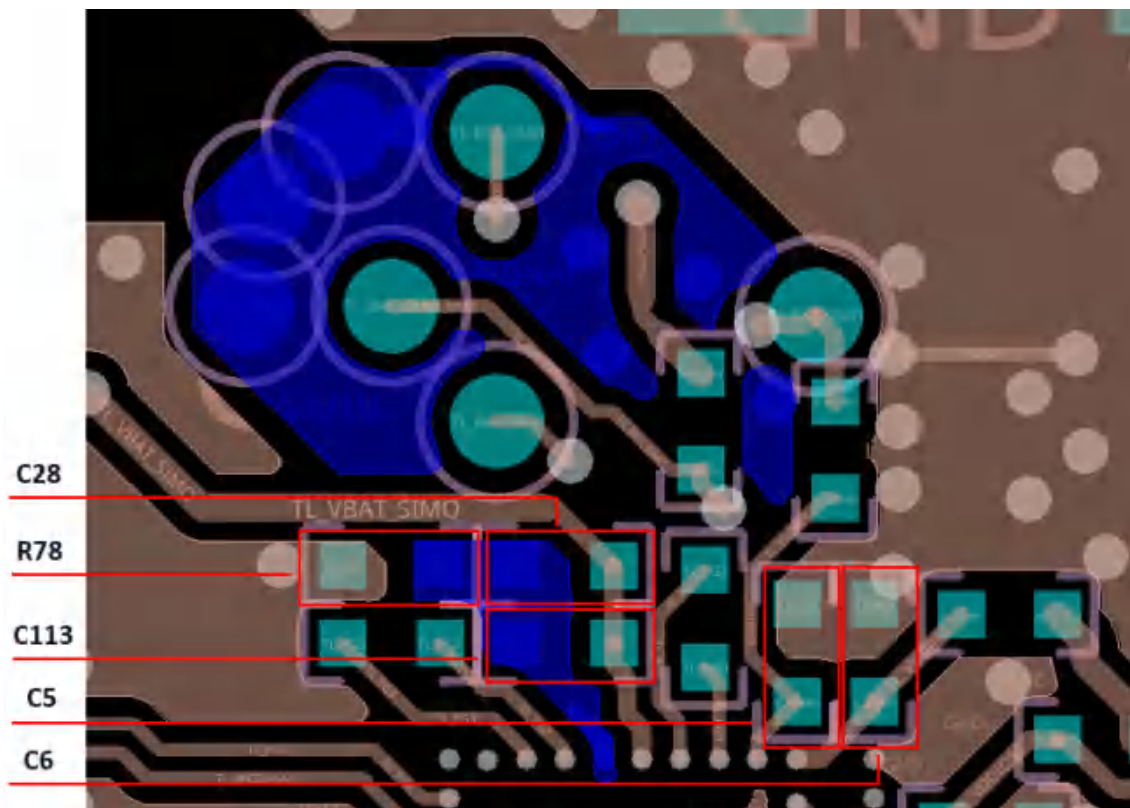
The figure below shows the top view of key components in the DCDC power layout.

Figure 3-4 Top view of the DCDC Layout



The figure below shows the bottom view of key components in the DCDC power layout.

Figure 3-5 Bottom view of the DCDC Layout



The following are key design considerations for the DCDC power layout:

- Place capacitors C113 and C28 as close as possible to the VBAT_SIMO pin.
- Place capacitor C12 closer to the VBAT pin than inductor L1.
- Place capacitors C32, C31, and C30 as close as possible to the BK1_SIMO / BK2_SIMO / BK3_SIMO pins.
- Place capacitors C6 and C5 as close as possible to the VDDRF1 and VDDRF2 pins.
- R78 is used to isolate the DCDC ground from system ground. Please place it according to the figure. The blue-marked area in the figure indicates the DCDC ground.
- In addition to the capacitors listed above, all other capacitors should also be placed as close as possible to their respective pins. However, if placement conflicts with the capacitors or inductors mentioned above, the placement of the above capacitors takes priority.

The inductor used on the TL7519H development board is EFE201612E-1R0M, with key parameters as follows:

- Inductance value: 1uH
- Package size (inch/mm): 0806(2016)
- Isat: 2.4A
- DC resistance: 0.116ohm

If customer independently selects the power inductor, note the following requirements:

- Inductor type: Wire-wound inductor
- Inductance value: 1uH
- Isat>1.6A
- DC resistance: <0.3ohm

3.4 CTB Layout Recommendations

The TL7519H development board is a four-layer board. The CTB design requires consideration of isolation from other signals; therefore, it is recommended that CTB detection channel traces be kept away from other signals. Refer to the layout design below.

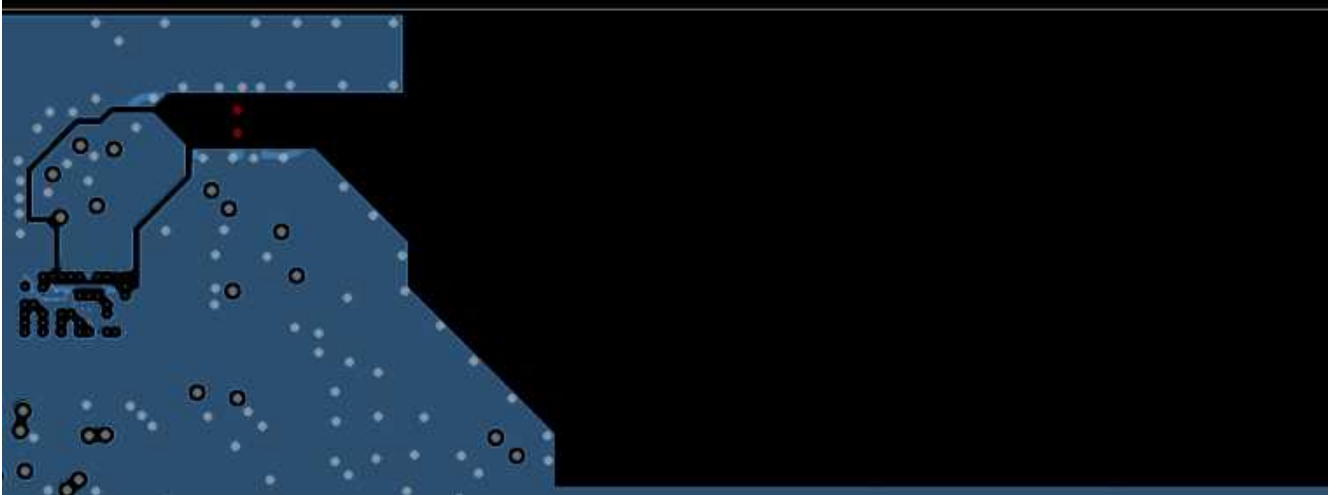
The figure below shows the CTB layout on the top layer.

Figure 3-6 CTB Top Layer



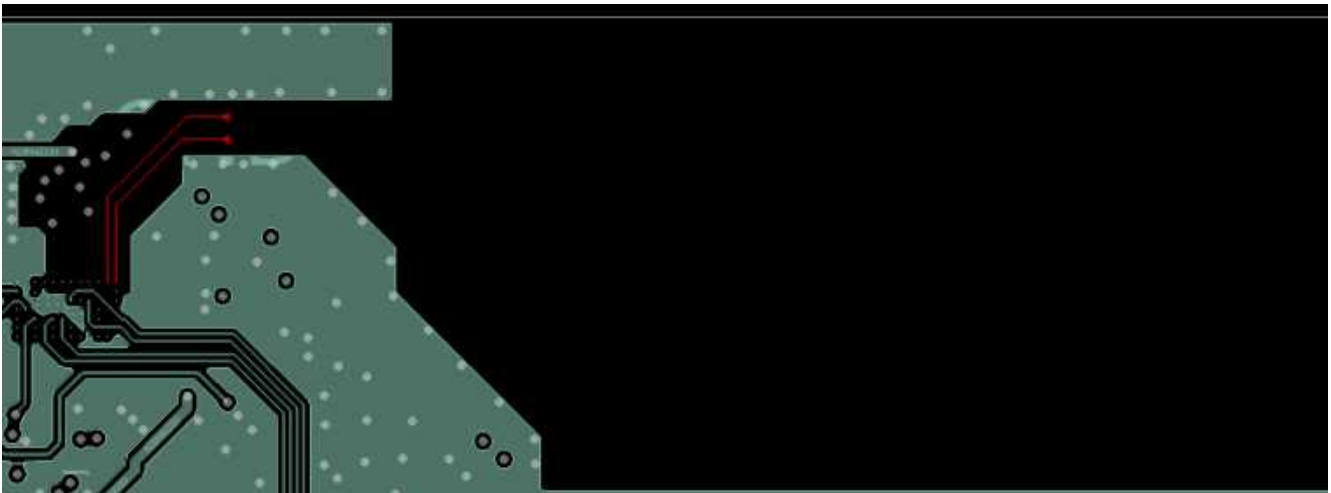
The figure below shows the CTB layout on the GND layer.

Figure 3-7 CTB GND Layer



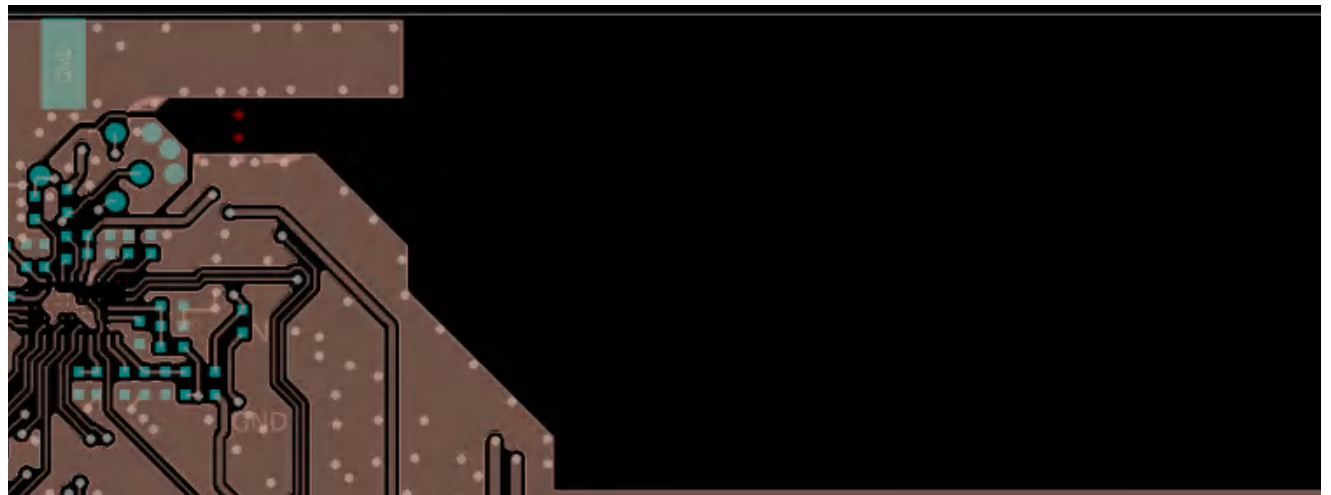
The figure below shows the CTB layout on the power layer.

Figure 3-8 CTB Power Layer



The figure below shows the CTB layout on the bottom layer.

Figure 3-9 CTB Bottom Layer



4 Related Documents

The following table lists other documents and resources that you can refer to for more information. Some of these documents are only available under a Non-Disclosure Agreement (NDA). To access such documents, please contact your local Telink Field Application Engineer (FAE) or sales representative.

Table 4-1 Related documents

No.	Name	Description	Link / Obtain method
1	TL751x datasheet	Provides information on the electrical characteristics, hardware description, and ordering options for the TL751x series chip.	TL751x datasheet
2	TL751x board files	Provides design files of schematic, PCB layout and gerber file for the TL751x development board.	TL751x board files

5 Certification Statement

5.1 FCC Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- (1) This device may not cause harmful interference, and
- (2) This device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.

This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.