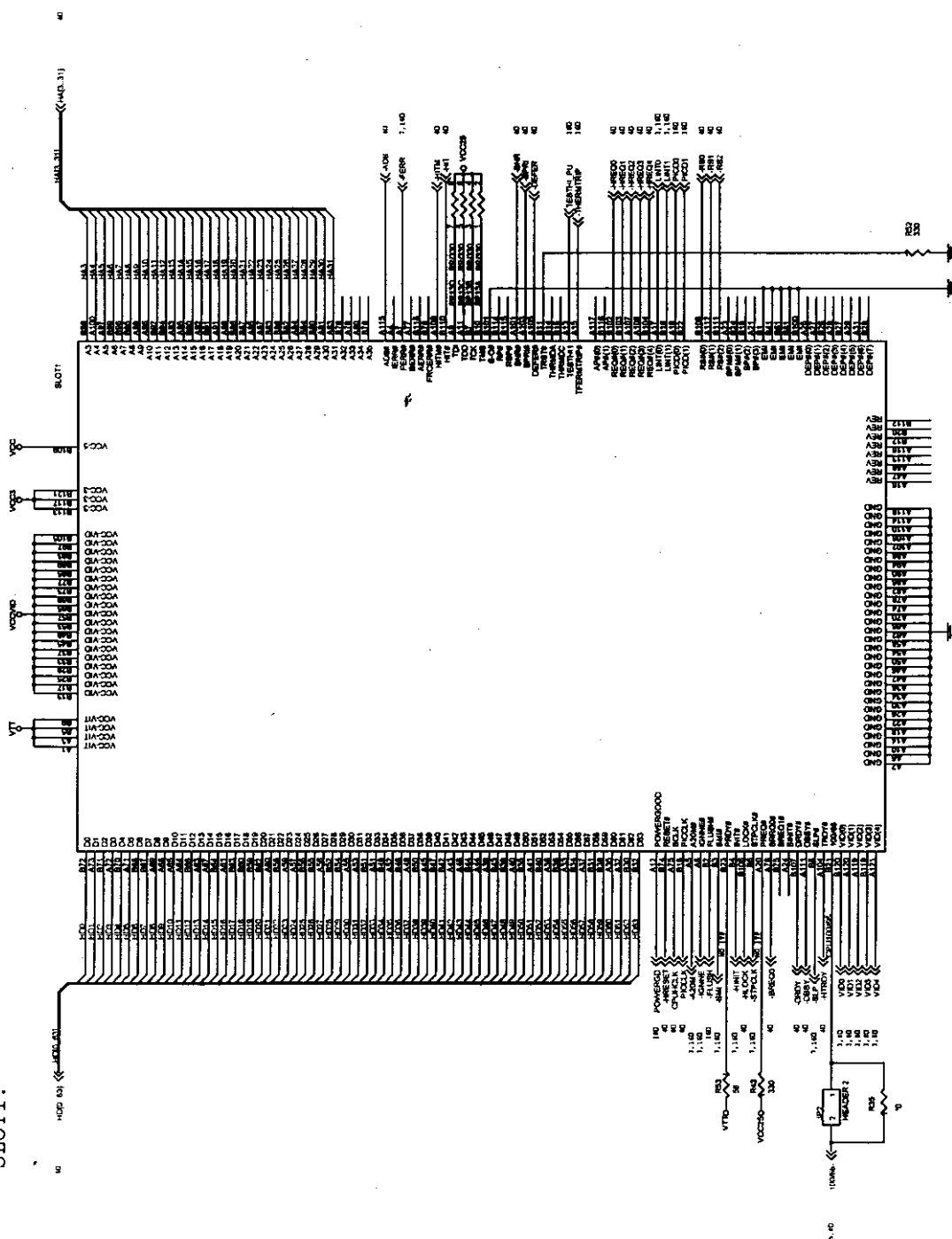
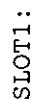
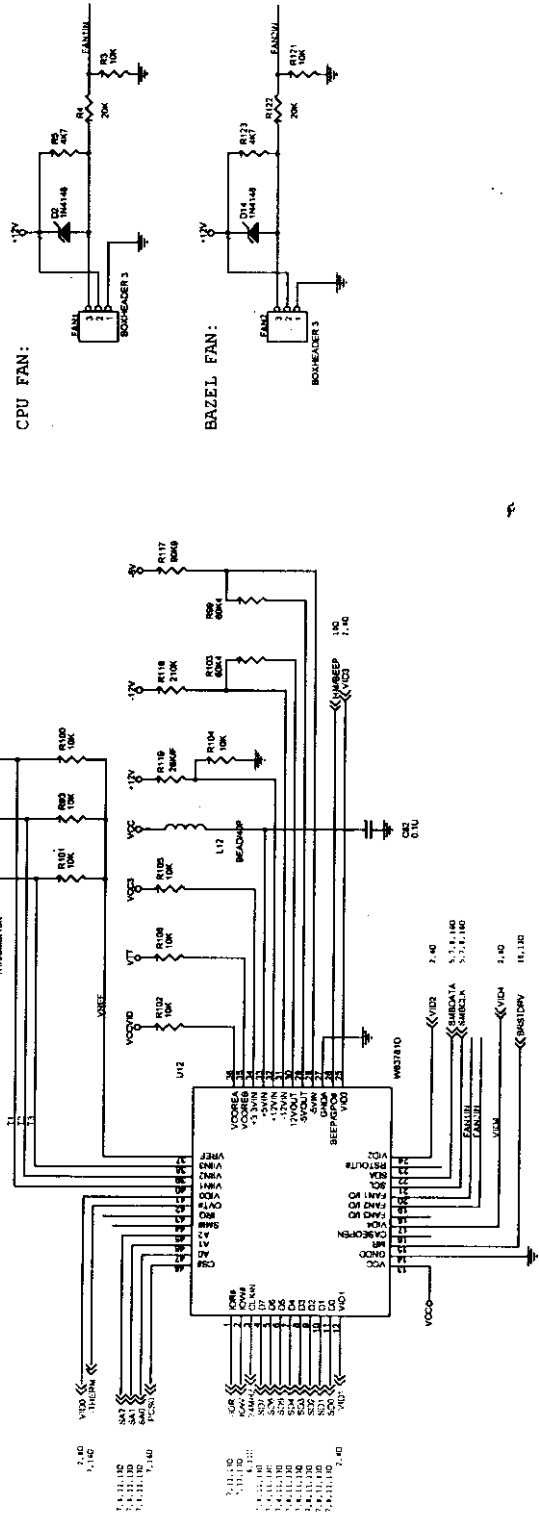
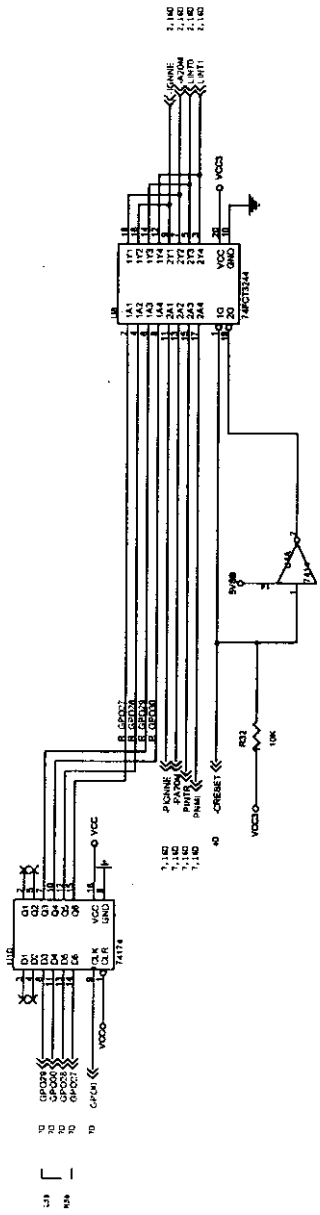




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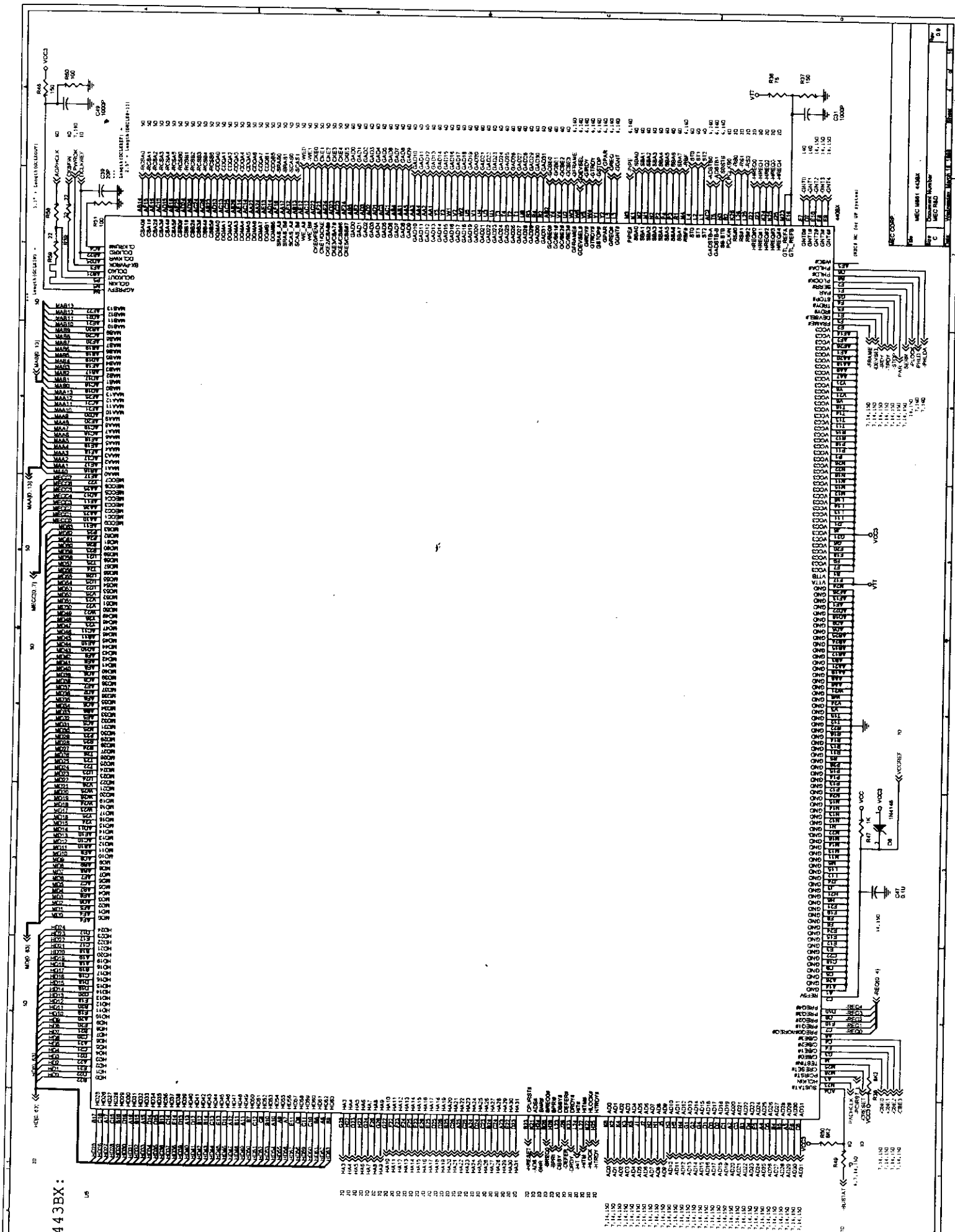


CLOCK SELECTOR:

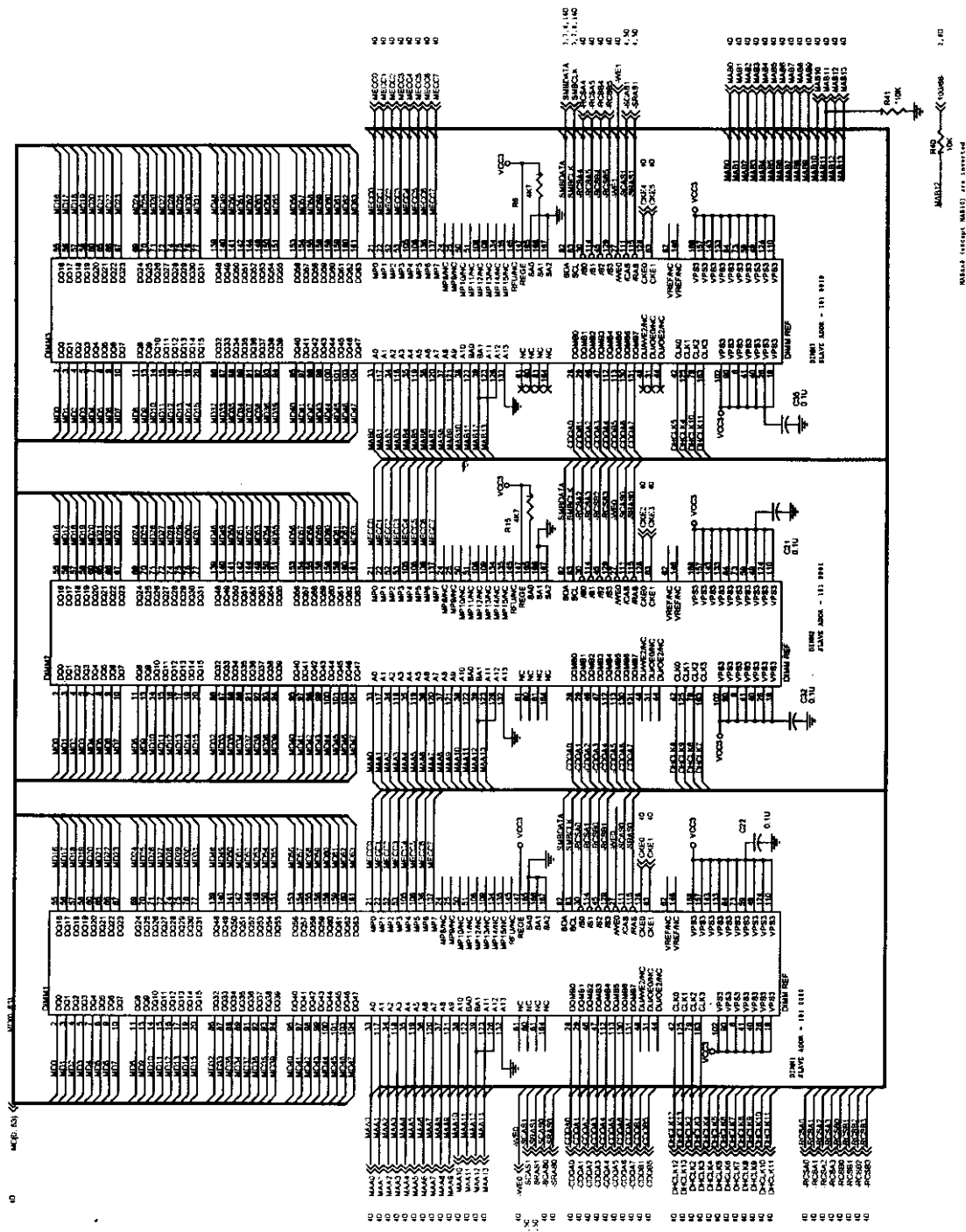


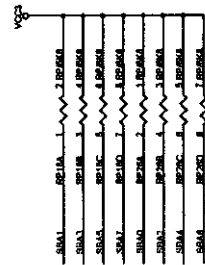
CPU FAN:

BAZEL FAN:

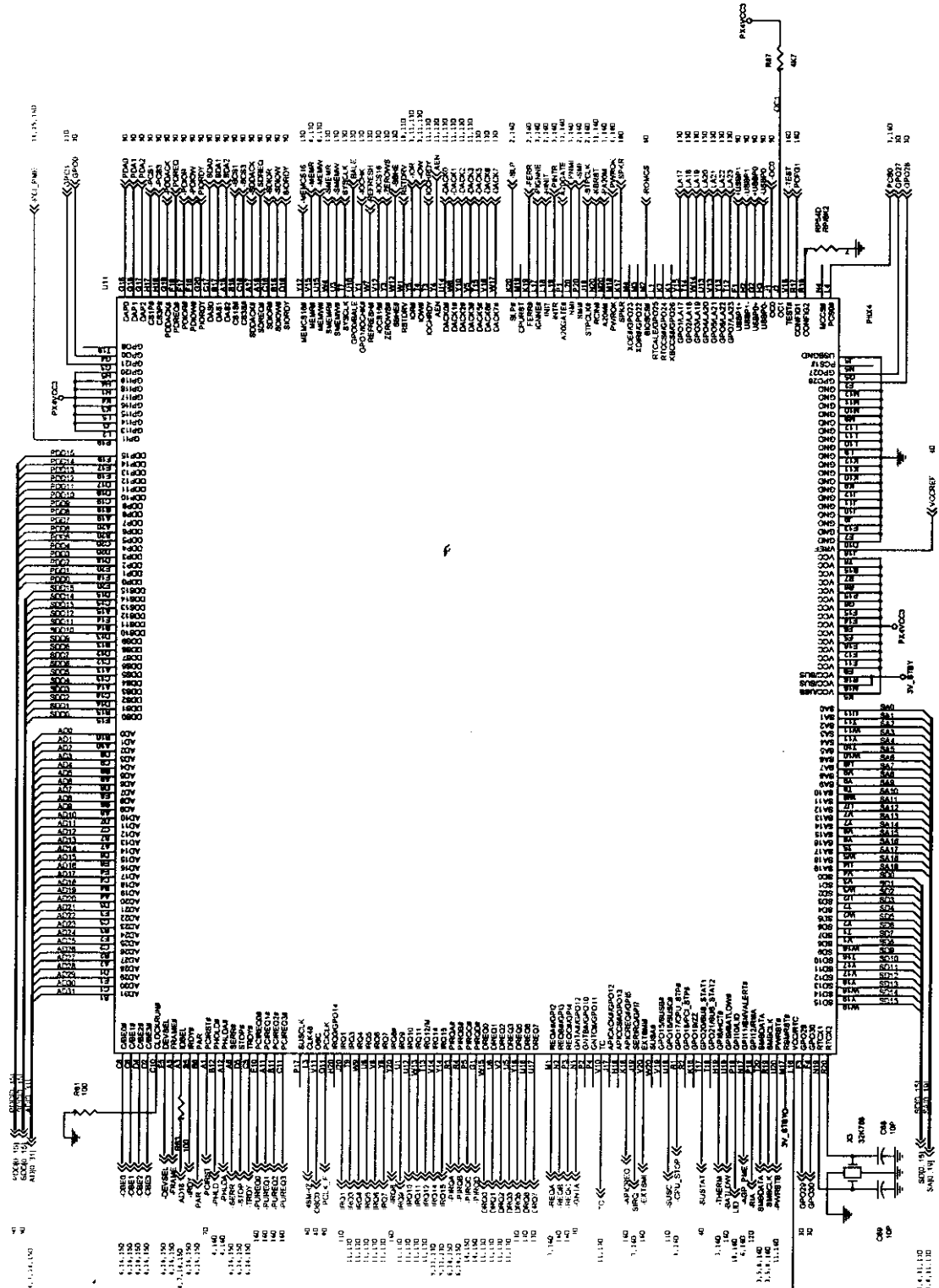


DIMM 1,2,3:

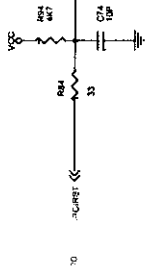


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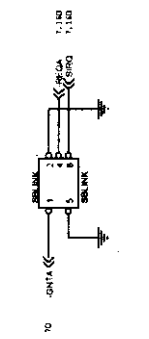
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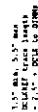
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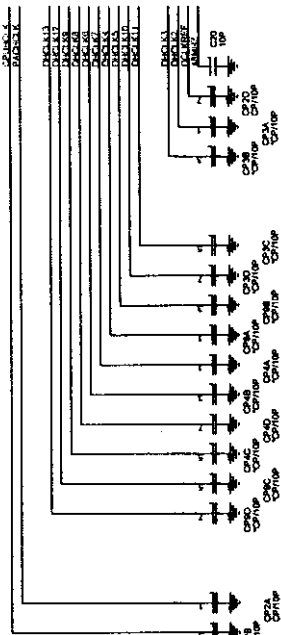
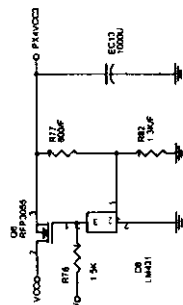
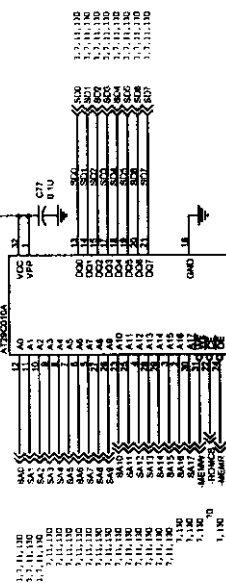
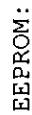
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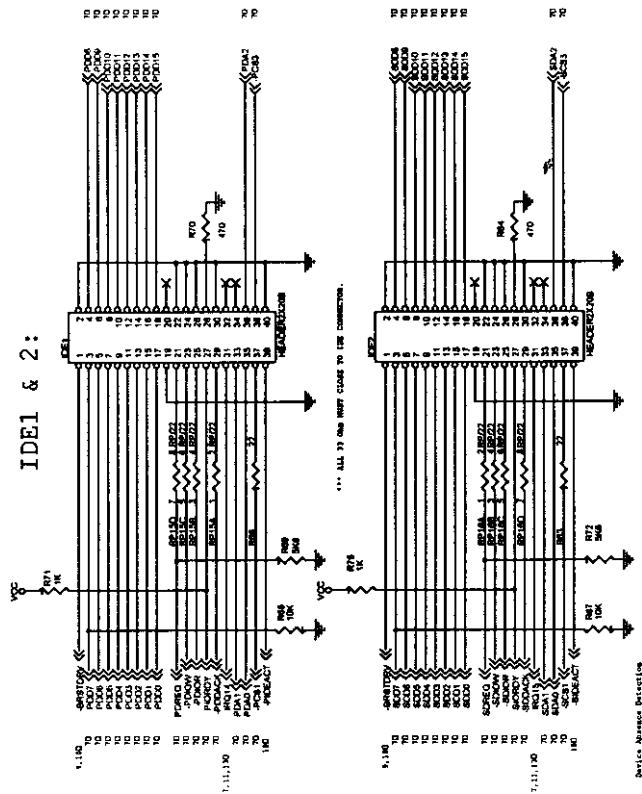
UNCLASSIFIED
DATE 10/10/11 BY 60322 JAV/ST



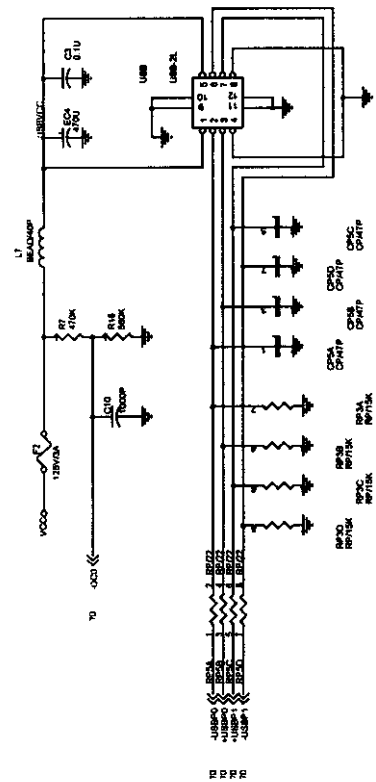
L14: D.C.M. 1/8 Obs 12th Dec. 1
 78 Obs (58 Dec. 1)



IDE1 & 2:

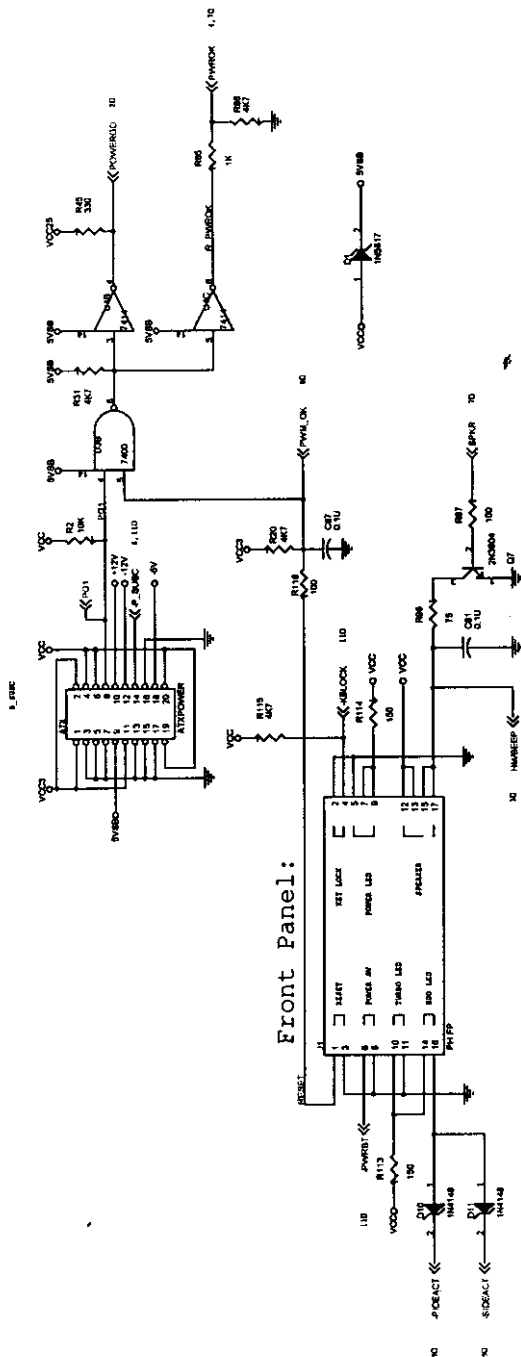


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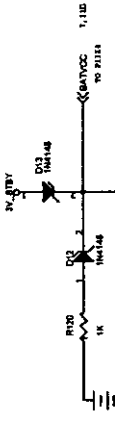
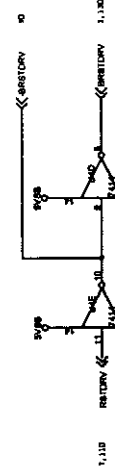
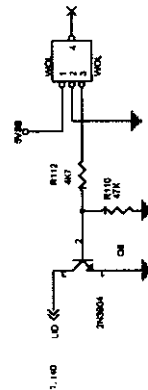


POWER CONNECTOR & FRONT PANEL CONNECTOR:

Power Conn:



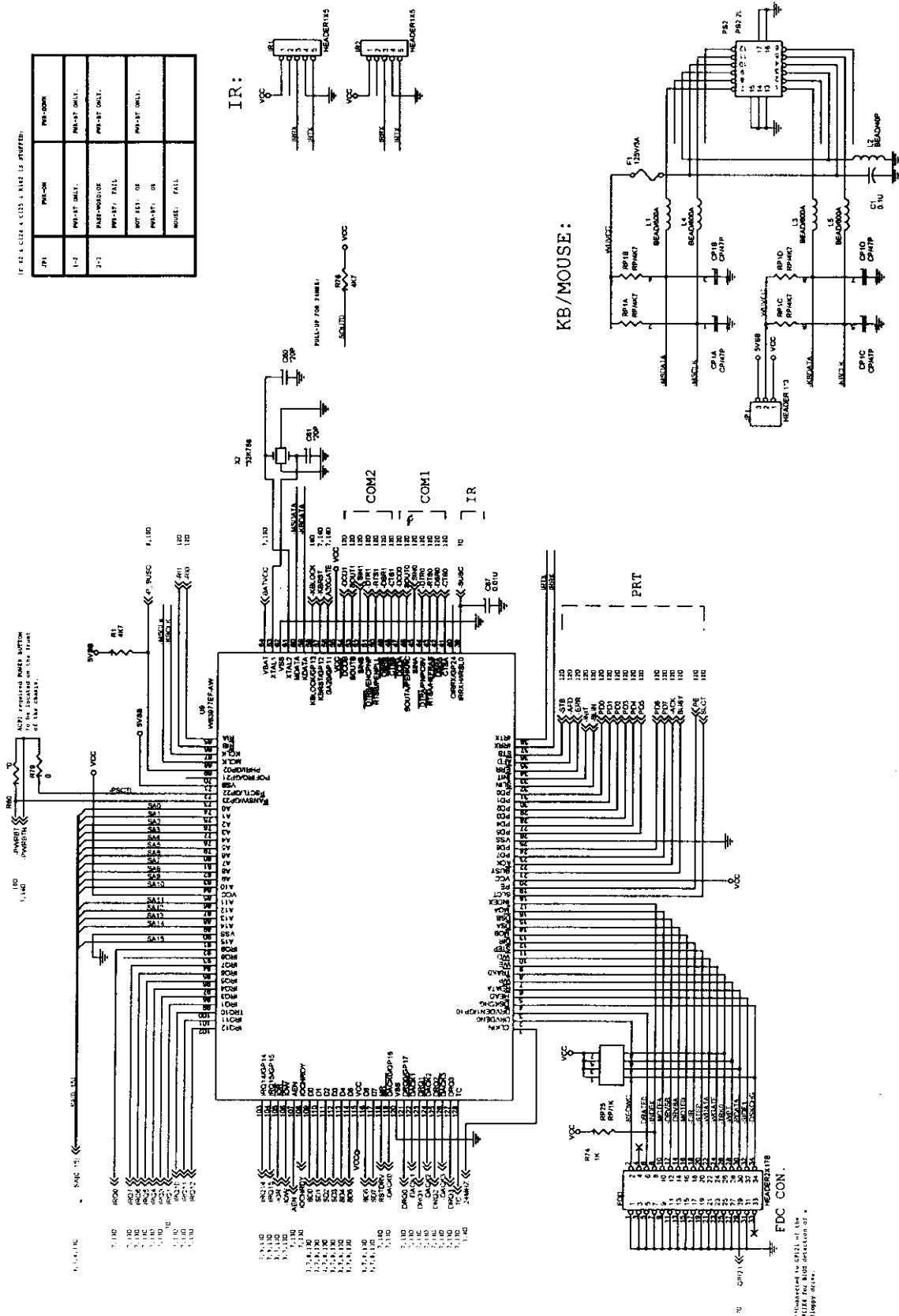
WOL CONNECTOR:



REV	1	DATE	10/10/88
BY	MEC	CHKD	MEC
APP	MEC	APP	MEC
DES	MEC	DES	MEC
PROJ	MEC	PROJ	MEC
FILE	MEC	FILE	MEC
REV	1	DATE	10/10/88
BY	MEC	CHKD	MEC
APP	MEC	APP	MEC
DES	MEC	DES	MEC
PROJ	MEC	PROJ	MEC
FILE	MEC	FILE	MEC

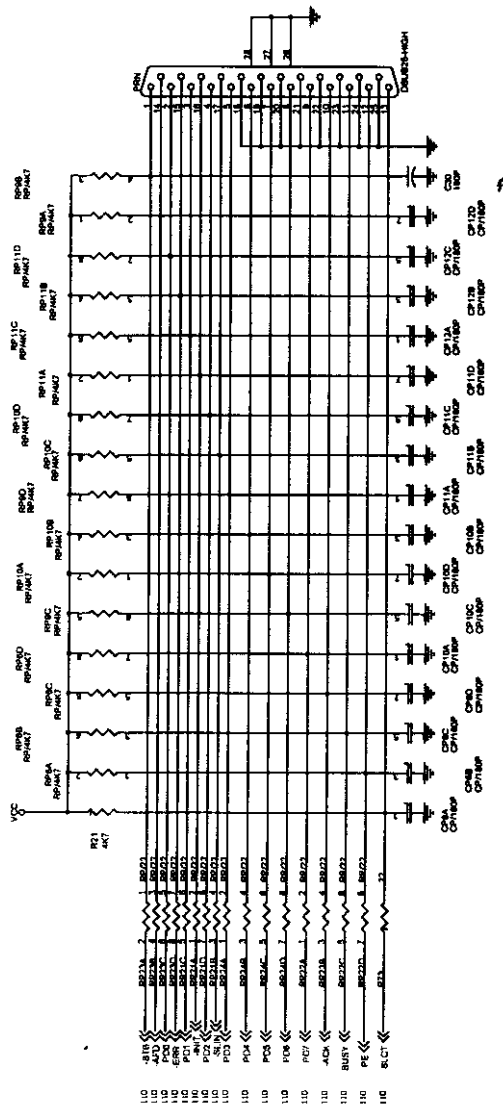
```
IF K2 < C124 + C125 + K102 LS STUFFED;
```

29)	PM-06	PM-0006
1-2	PM-17 MAIL	PM-17 MAIL
2-3	PM-0010 DE PM-17 MAIL	PM-17 MAIL
	NOT LIST DE	PM-17 MAIL
	PM-17 DE	
	MODEL MAIL	

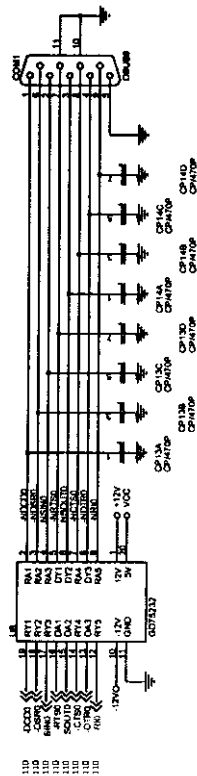


connected to GPI2 of the
ISA for BIOS detection of a

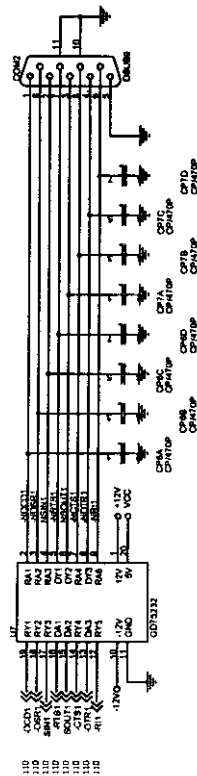
LPT:



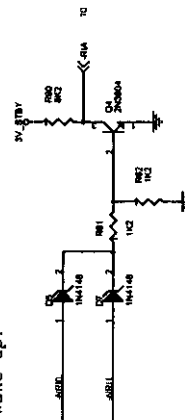
COM1:



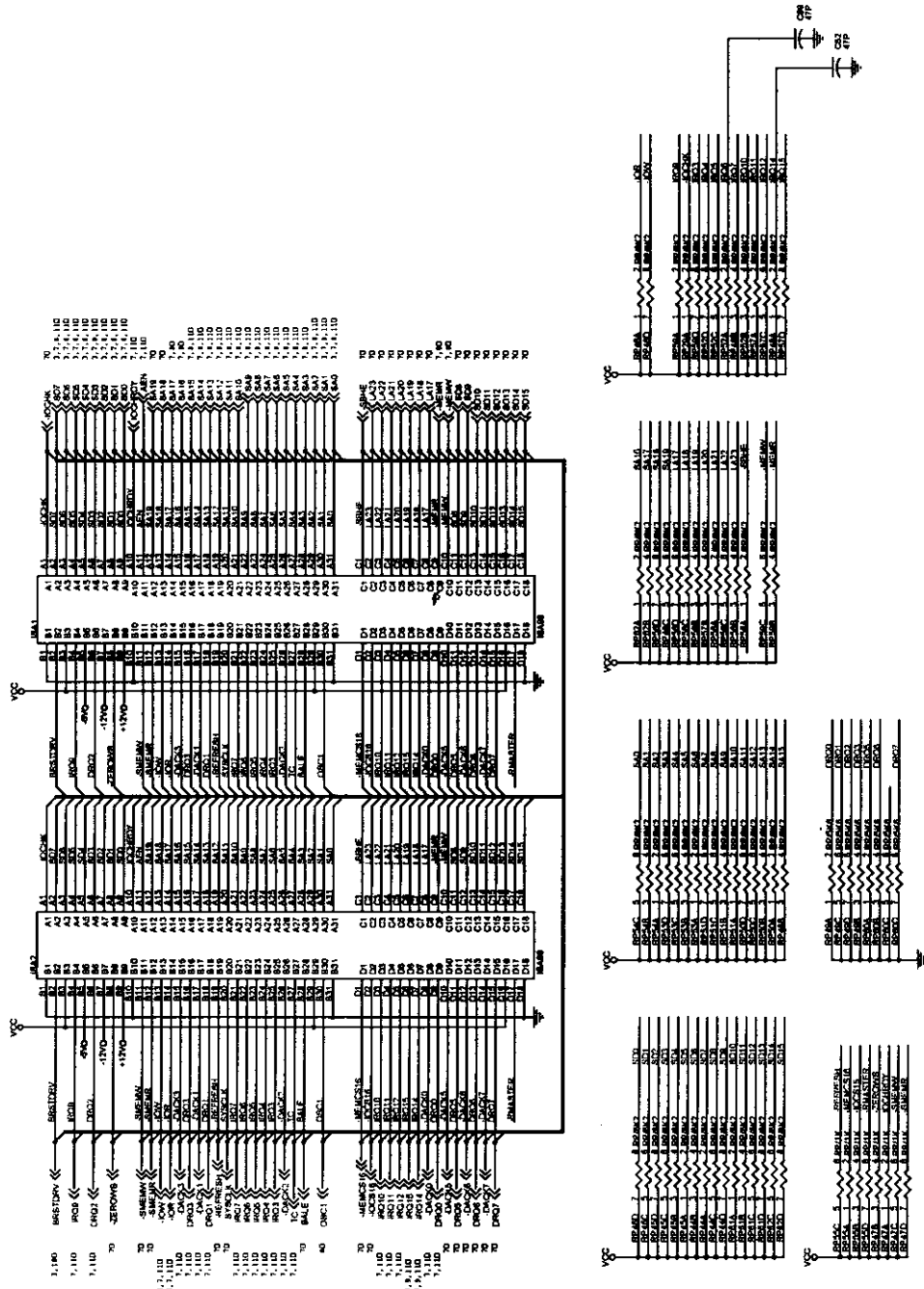
COM2:



Ring wake up:



ISA1/2/3:



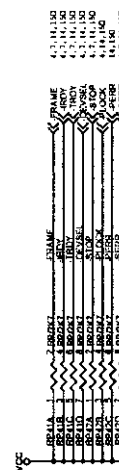


Figure 10 is a detailed schematic diagram of the digital logic circuitry for the P-10, showing the internal structure of the P-10 and its connection to the P-10A. The diagram is organized into four main sections, each representing a different functional block: P-10, P-10A, P-10B, and P-10C. Each section contains a complex network of logic gates, flip-flops, and other digital components, with signals labeled with names like P-10, P-10A, P-10B, and P-10C. The diagram is a high-level representation of the hardware, showing the interconnections between various components and the flow of data and control signals. The P-10 section is on the left, followed by P-10A, P-10B, and P-10C on the right. The diagram is a detailed representation of the hardware, showing the interconnections between various components and the flow of data and control signals.

