



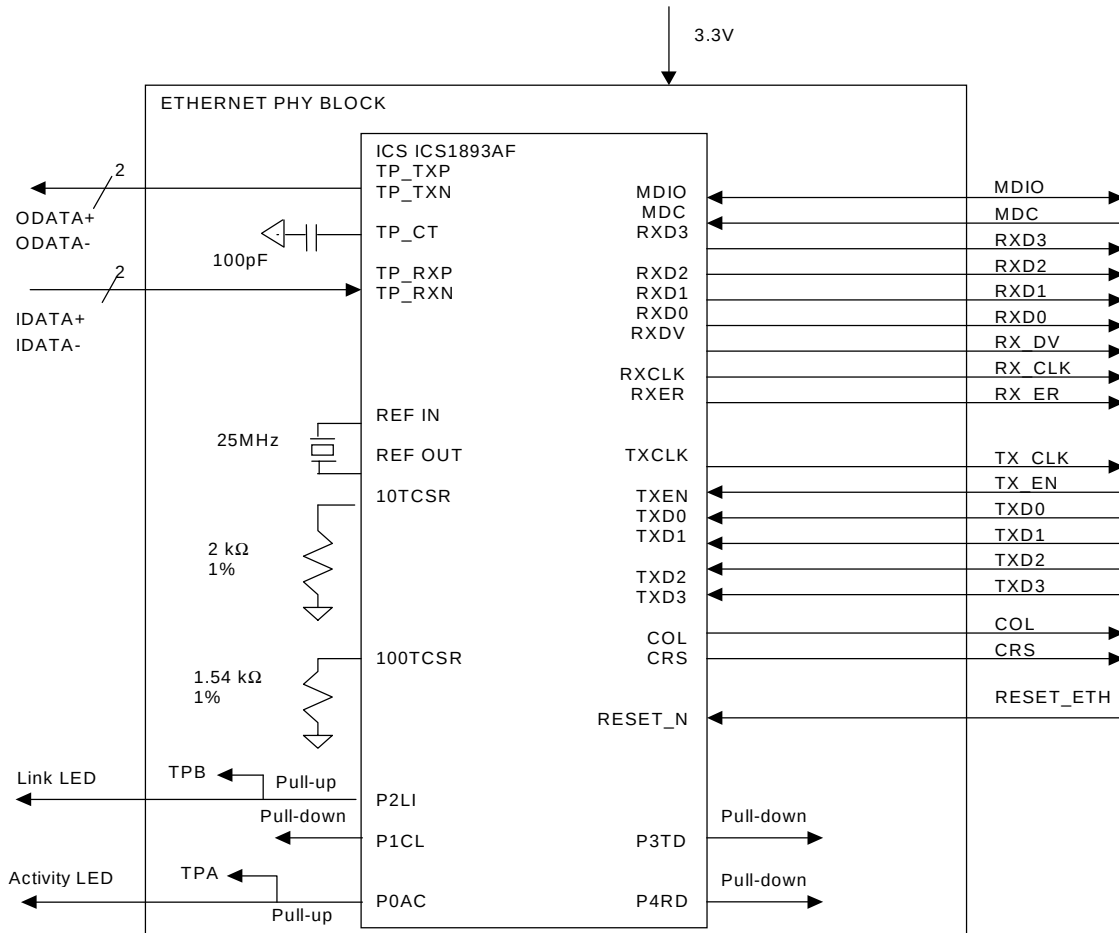
The diagram illustrates the RF front end of the CC2538 SoC, showing the internal components and their connections to external components. The main components include:

- Power Supply:** 4.2V supply connected to a 3.3V LO Regulator and a 3.3V Regulator. The 3.3V LO Regulator outputs 3.3V LO, and the 3.3V Regulator outputs 3.3V RF.
- Logic and Control:** Logic + 2.85V reg, 4.2V DC, and 3.3V RF are connected to the Logic block.
- TX Path:**
 - TX IF Amp:** Receives TXIF+ and TXIF- signals from the I/Q MOD/DE-MODULATOR.
 - TX Mixer:** Receives TXIF+ and TXIF- signals and is driven by 3.3V LO.
 - TX RF Image Filter:** Filters the TX Mixer output.
 - PA (Power Amplifier):** Driven by 4.2V DC and 3.3V RF, it drives the TX RX Switch.
 - TX RX Switch:** Connects the PA output to the Front End Filter.
 - Front End Filter:** Filters the TX signal before it reaches the Antenna.
- RX Path:**
 - RX LNA (Low Noise Amplifier):** Receives the signal from the Front End Filter and is driven by 3.3V RF.
 - RX RF Image Filter:** Filters the RX LNA output.
 - RX Mixer:** Receives the RX RF Image Filter output and is driven by 3.3V LO.
 - RX IF Amp:** Receives the RX Mixer output and drives the RXIF+ and RXIF- signals to the I/Q MOD/DE-MODULATOR.
- Internal Components:**
 - Buffer and SYN (Synthesizer):** Receives 3.3V LO and 44MHz synth signals.
 - RF LO (975-995 MHz):** Provides the RF LO signal to the TX Mixer and RX Mixer.
 - 44MHz synth:** Provides the 44MHz synth signal to the SYN and the 44MHz REF OSC.
 - 44MHz REF OSC:** Provides the 44MHz reference signal to the 44MHz synth.
 - 140 MHz IFLO:** Provides the 140 MHz IFLO signal to the I/Q MOD/DE-MODULATOR.
- External Connections:**
 - To MICRO/MAC:** Receives M_LE_RF, PAPE, PE1, PE2, CAL_EN, RFSW, M_SD_IF_RF, M_SCLK_IF_RF, and M_LE_IF signals.
 - To Antenna:** Receives the TX signal from the Front End Filter.
 - To BBP:** Receives RXIFAGC and RXIFAGC signals.

Figure 1.2 – RF Section Block Diagram

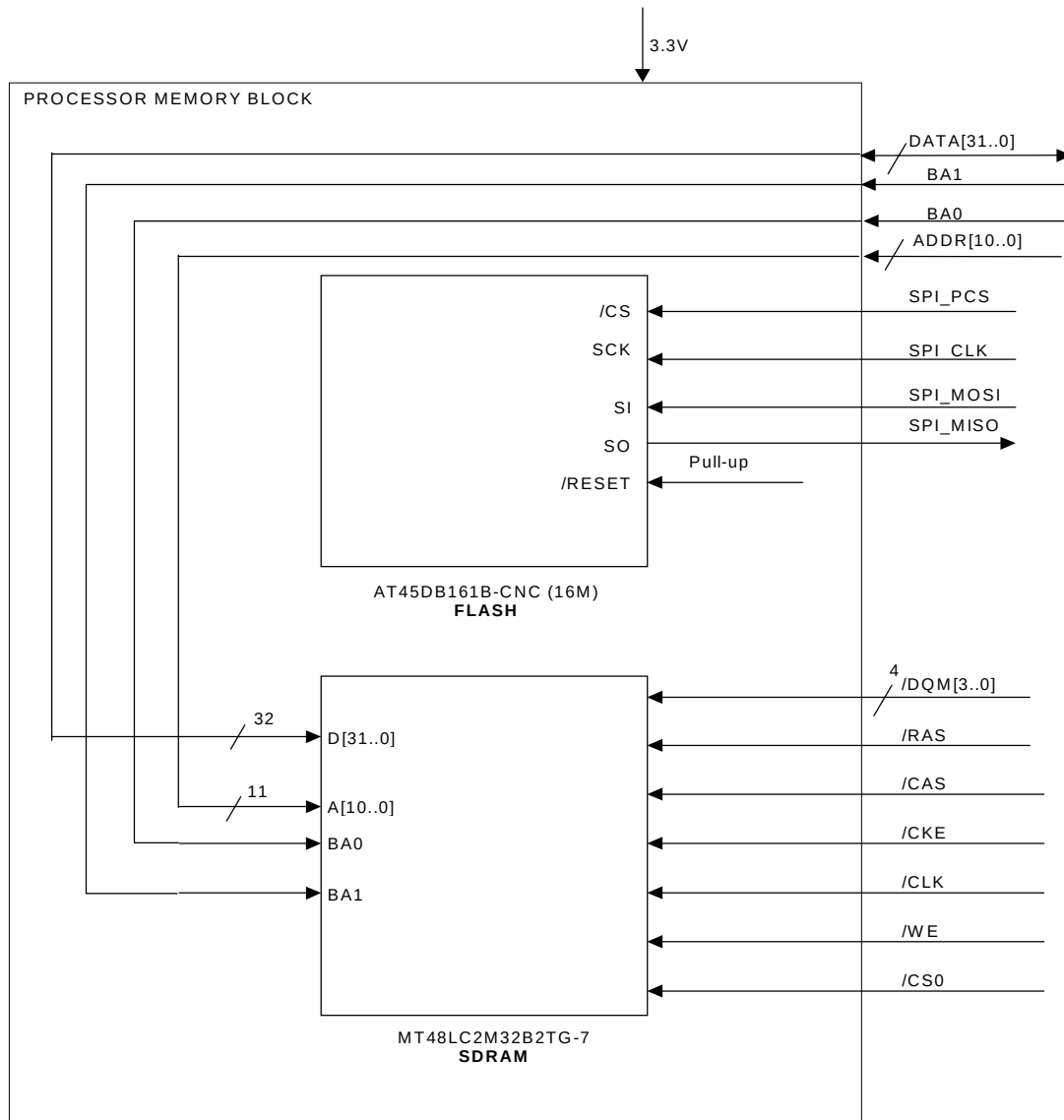
1.3 Digital Section

1.3.1 Ethernet PHY



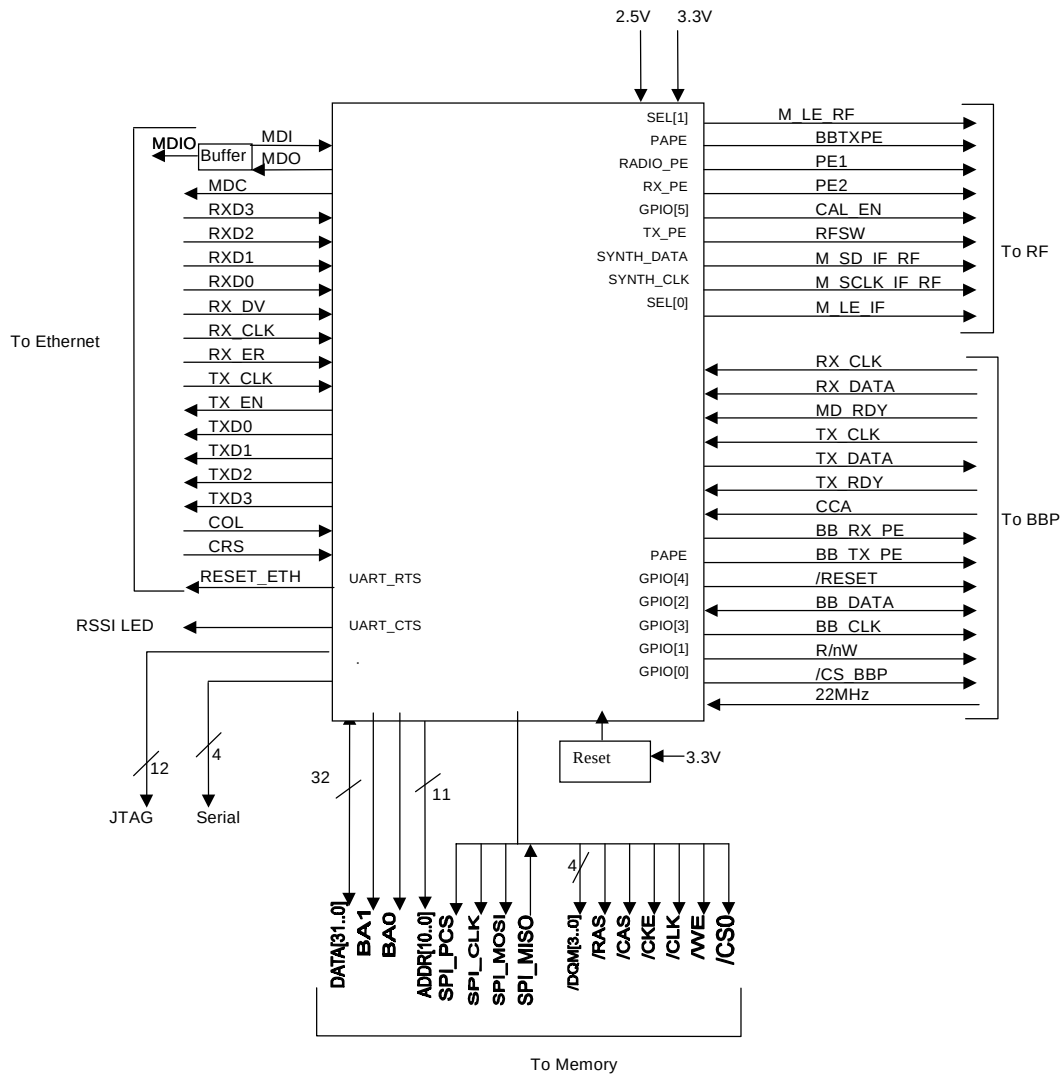
5.3.1 Ethernet PHY Block Diagram

1.3.2 Microprocessor/MAC Memory (FLASH,SDRAM)



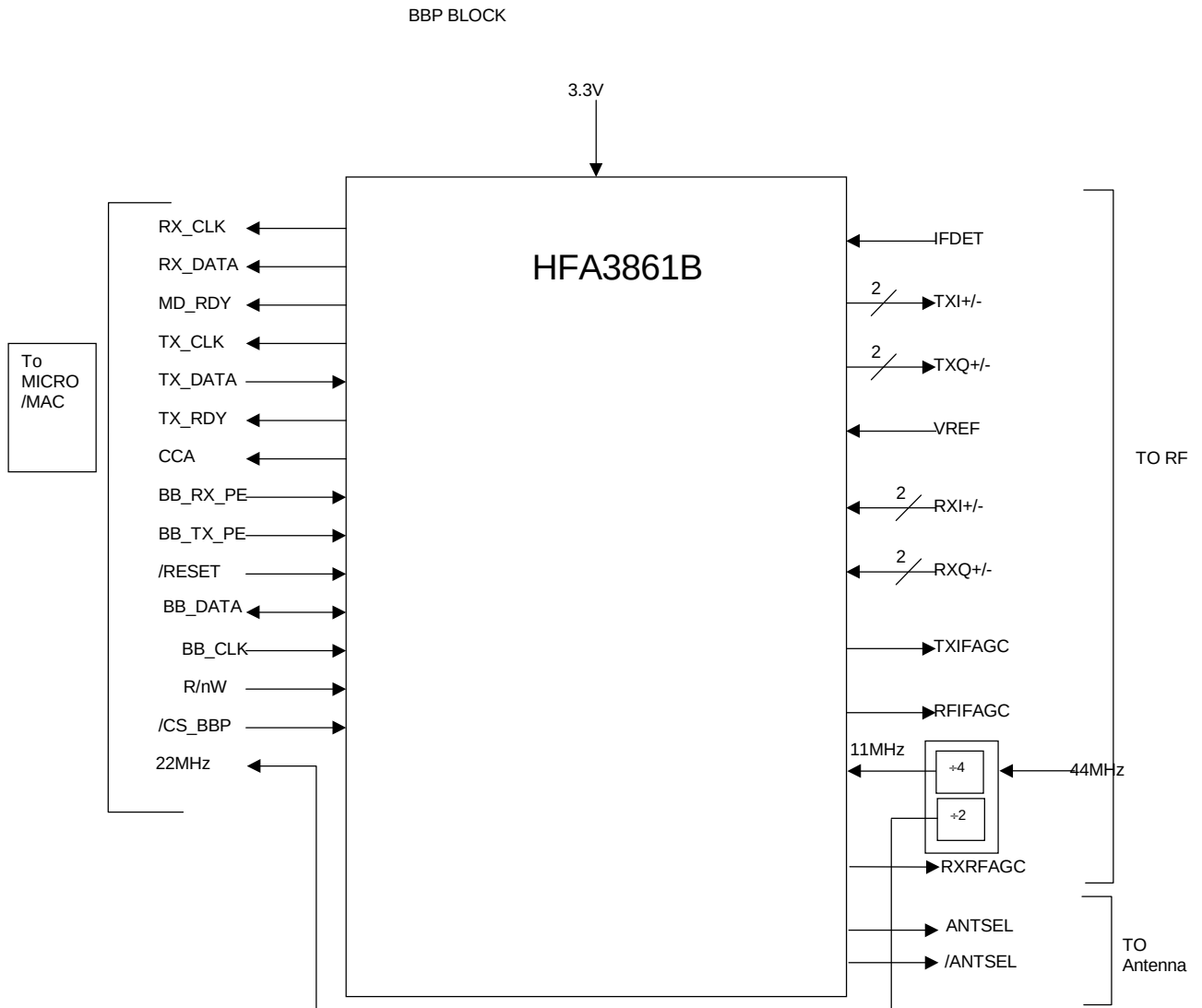
5.3.2 Microprocessor/MAC Memory Block Diagram

1.3.3 Microprocessor/MAC



5.3.3 Microprocessor/MAC Interface Block Diagram

1.3.4 BBP Interface



5.3.4 BBP Interface Block Diagram