

intersil

The block diagram illustrates the system architecture for the ISL3874 MAC/BBP. It shows the integration of several key components:

- External Antenna:** Connected to the system via an optional diversity switch.
- ISL3984 RFPA:** A radio frequency power amplifier that receives signals from the antenna and provides a 44 MHz clock to the ISL3685IR.
- ISL3685IR RF/IF CONV:** A radio frequency to intermediate frequency converter that includes a PLL, SAW filter, and RF VCO. It receives a 44 MHz clock and provides a 32KHz sleep signal to the ISL3874.
- HFA3783 QUAD IF:** A quad intermediate frequency block that receives signals from the ISL3685IR and provides a 32KHz sleep signal to the ISL3874.
- ISL3183 IF VCO:** An intermediate frequency voltage-controlled oscillator that receives a 44 MHz clock and provides a 32KHz sleep signal to the ISL3874.
- ISL3874 MAC/BBP:** The main MAC/BBP block, which includes a CONTROL PROCESSOR, MEMORY, WEP ENGINE, and optional parallel flash and serial EEPROM. It is connected to a miniPCI HOST interface via PHY, RADIO, and HOST T/I/O lines.

The diagram also shows various control and data buses, including a 32KHz sleep signal, a 44 MHz clock, and a miniPCI HOST interface. The ISL3874 MAC/BBP is shown in a dashed box, indicating its internal components and connections.

