

CIRCUIT DESCRIPTION

Circuit Composition and Operation Theory

The basic explanation for the circuit composition

FR531-2 consists mainly of the two parts controlling the RF circuit parts and the digital circuit parts.

Receiver

FR531-2 receive parts are composed in the double conversion system, which has the 1st IF Frequency of 10.7MHz and the 2nd IF frequency of 450KHz, with the front-end circuit which has an excellent band characteristic and skirt characteristic, the 1 pole MCF used in the 1st IF, and the 4 pole ceramic filter in the 2nd IF, the reception interrupting factors such as the image and the sensitivity repression are reduced for the more stable reception.

RF Front-end

The signal received by the antenna will be transmitted to the front-end through the antenna switching circuit consisted of C88, L13 and D11. The front-end consists of the RF amplifier transistor Q21 and the high pass filter block. High pass filter primarily diminishes the other signal rather than the 1st IF image and other signal within the reception band and amplifies only the necessary signal within the RF.

1st Mixer

The receiver signal, which has been amplified in the RF front-end, is provided to the base of the 1st mixer Q22. The 1st L/O signal provided from the VCO circuit (Q14, Q23) is supplied to the emitter of Q22 and converted to the 1st IF 10.7MHz.

1st IF Filter and 1st IF Amplifier

The signal converted by Q22 to 10.7MHz, the 1st frequency, changes its impedance through L17 and then is infused to the fundamental MCF which has the center frequency of 10.7MHz and the band width of $\pm 12.5\text{KHz}$.

Here, the signal reduces the image and other unwanted signal for the 2nd IF. Then the signal is infused to the Q25, the 1st IF amplifier. The signal infused to the Q25 is amplified approximately by 20dB in order to acquire the required reception sensitivity, and infused to the U2 which function as the 2nd mixer, the 2nd IF amplifier, and the FM detector.

2nd Mixer, 2nd IF, FM Detector(U2)

The receiver IF signal of 21.7MHz, which has been infused to U2 is mixed with the 2nd L/O signal of 10.250MHz, and converted to 450KHz, the 2nd IF frequency. The receiver signal converted to the 2nd IF frequency passed through the CF13, the ceramic filter of 450KHz again. After the limiting inside the U2 and the FM demodulating by the quarter detector inside the U2, the signal offers the output through the 9th pin of the U2.

The 2nd L/O signal of 10.250MHz, which infused to detect the noises from the received signal, demodulates in the 9th pin of the U2. For this purpose, the noise filter is using the OP. Amplifier inside the U2.

De-Emphasis

The audio signal, which has been FM demodulating in the U2, supplies to R33, C81, which function as the De-emphasis.

Audio Power Amplifier (IC6)

The received audio signal, which has been adjusted to RV101, 102, 103 is supplied to the IC6 and amplified approximately by 20dB. Then, it turns up the speaker with the maximum output of 0.5Watts.

The 6th pin of the IC6 is the VDD.

Transmitter

The transmission part of the FR531-2 is designed to amplify the RF signal oscillated and modulated by the synthesizer to approximated below 300mW(ERP) by the power transistor of Q12, 17, 18, 20.

Pre-emphasis (IC5)

The voice signal input from the microphone is pre-emphasized at the IC5. The signal, which comes out of the IC5, is limited to certain amplitude for the voice signal not to exceed the allowable bandwidth assigned for transmission.

TX Power (Q12, 17, 18, 20)

The transmitted signal amplified to 0.3Watts here passes the TX LPF of the 6th characteristic of the L100, C89, L14, C19, L9 and C73. And RX / TX switching takes place by the D7, D11.

Frequency Synthesizer

Voltage Control Oscillator (VCO)

The VCO of oscillates 462.5625MHz under the transmission condition and 451.8625MHz under the reception condition. The VCO consists of the colpitts oscillator of the Q14, and contains the oscillator frequency difference of approximately 10.7MHz during the transmission / reception conversion. That is since the VCO should oscillate relatively low frequency during reception compared to transmission.

Therefore as a result, the C96, 80 is added in parallel to the resonance circuit of the VCO to oscillate a low frequency. During reception, a relatively low frequency should be oscillated compared to transmission.

The IC1 PLL IC controls the VCO in order to oscillate the accurate frequency. The output frequency of the VCO is supplied to the IC1 PLL IC immediately. At the IC1, 10.250MHz by the X2 are compared to the output frequency of the VCO. The VCO is controlled through the loop filter consisted of the R73, C120, C113, R74 and the C20 in order to oscillate the stable frequency wanted for the radio.

The VCO controlled voltage which has passed the loop filter supplies to the D9 variator diode, and oscillate the PLL programmed frequency by the capacity variation in the D9. In addition, the L12 on the VCO circuit functions as frequency for the VCO to be properly controlled by the IC1 PLL IC.

RX/TX Buffer Amplifier (Q23)

The RF signal oscillated at the VCO is provided to the Q19 power driver amplifier through the Q23 during the transmission.

PLL Frequency Synthesizer (IC1)

The PLL synthesizer of the signal loop PLL circuit with the reference of 12.5KHz.

The IC1 PLL IC includes all the functions such as the reference oscillator, the driver, the phase detector, the lock detector, and the programmable divider.

At the reference oscillator, the 10.250MHz are connected to the pin 10, 11 of the IC1 to oscillate the frequency of 10.250MHz.

The phase detector sends out the output power to the loop filter through 3rd pin of the IC1.

If the oscillation frequency of the VCO is low compared to the referenced frequency, the phase detector sends out the output power in positive pulse. If the oscillation frequency of the VCO is high, phase detector sends out the output power in negative pulse. Therefore, the VCO can maintain the frequency set.

The programmable divider maintains the desired frequency with the control from the CPU. The dividing ratio, "N" to oscillate the desired frequency is as below:

$$N = \text{VCO oscillation frequency} / \text{reference frequency}$$

If the desired frequency is 462.5625MHz

$$N = 462.5625\text{MHz} / 0.00625\text{MHz} = 37005$$

CPU and Memory

The IC4 CPU controls most of the control functions.