

## 6 CIRCUIT ANALYSIS

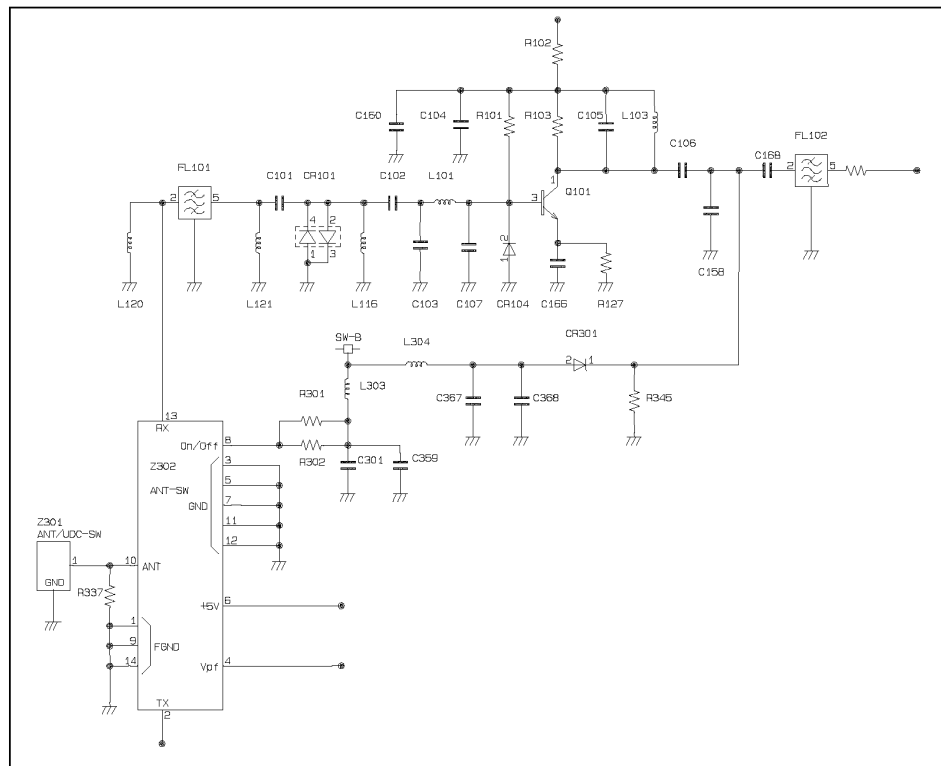
The JAGUAR 700P is a dual-conversion super heterodyne FM transceiver (see Table 1 for model number and frequency band information).

### 6.1 RECEIVER CIRCUITS

The 800 MHz JAGUAR 700P receiver is designed for operation in the 851-869 MHz frequency range. (865-870 MHz for Australia). The receiver has intermediate frequencies (IF) of 115.65 MHz and 450 kHz. Adjacent channel selectivity is obtained by using band pass filters- a 115.65 MHz crystal filter and two 450 kHz ceramic filters. The receive detector is the phase digitizer located within Hillary.

#### 6.1.1 Receiver Front End

A RF signal from the antenna is coupled through the low pass filter/antenna switch, and the bandpass filter (FL101) to the input of low noise amplifier Q101. The output of Q101 is coupled through another bandpass filter (FL102) to the input of first Mixer Z101. Front End selectivity is provided by the bandpass filters.

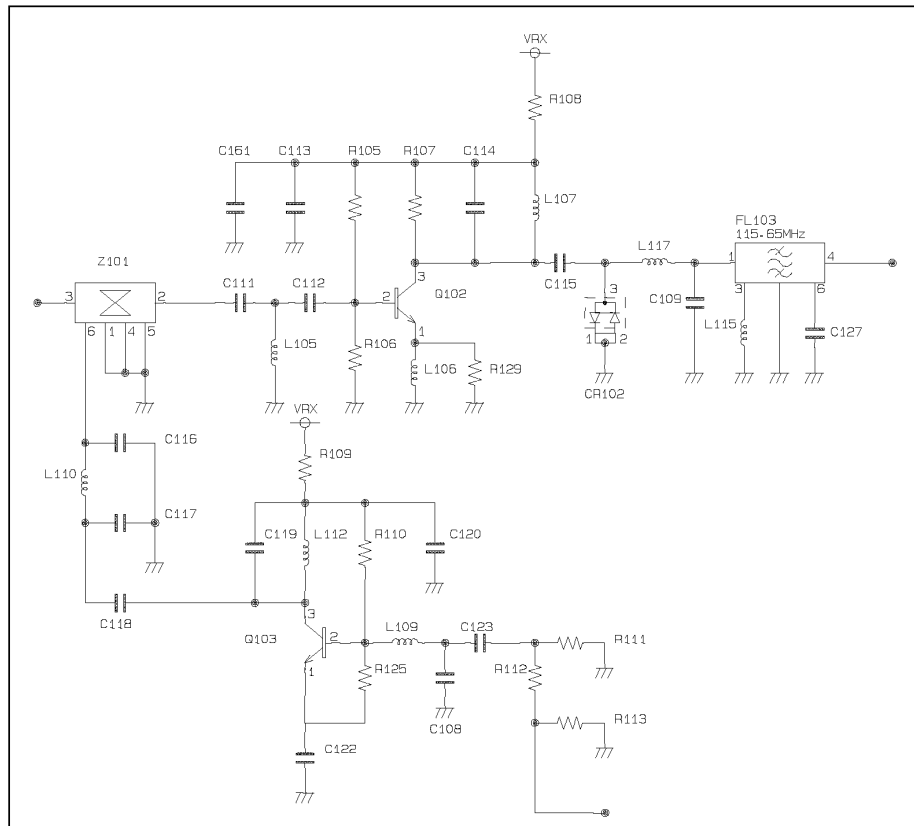


### 6.1.2 First Mixer Circuit

The first mixer is a Double-Balanced-Mixer (Z101) that converts a RF signal in the 851-869 MHz range to the 115.65 MHz first IF frequency. The Rx L.O. signal is derived from the Rx VCO, amplified by Q103, and input into Z101, pin 6. The signal on the output of Z101 is provided to the input of the first IF amplifier, Q102.

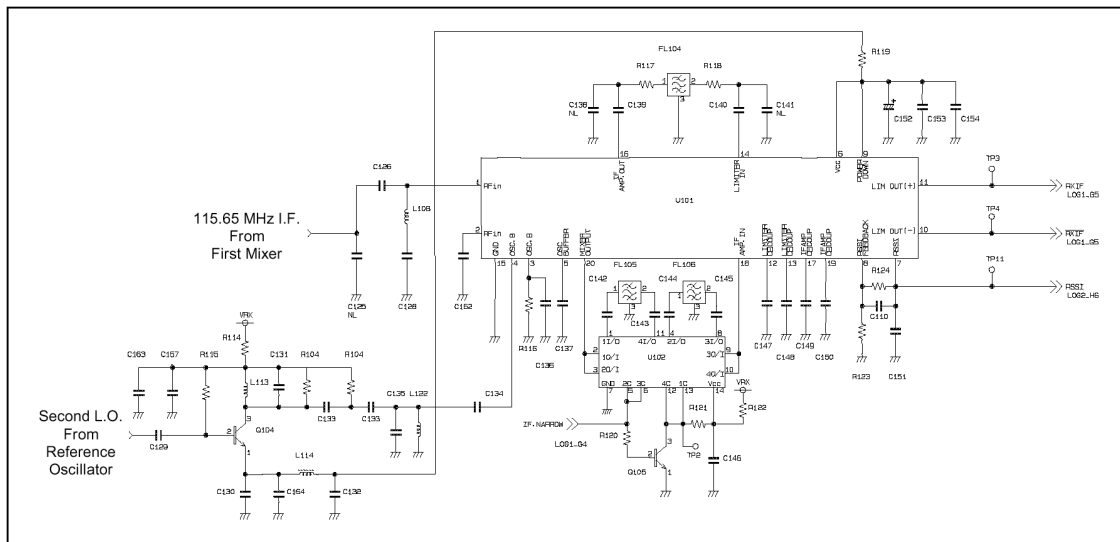
### 6.1.3 First IF Circuit

The first IF signal from the output of the first Mixer is coupled through first IF amplifier Q102 to crystal filter FL103. The highly selective crystal filter provides the first portion of the receiver IF selectivity. The output of the filter is coupled through an impedance-matching network to the Rx back end IC (U101).



### 6.1.4 Second Mixer, Second IF Filters and Second IF Amplifier

The receiver back end IC (U101) is a single chip digital communication systems IC. It includes the second Mixer, second IF amplifier and the limiter amplifier. Within the internal circuits of U101, the first IF signal is amplified and applied to the input of the second mixer. The second local injection frequency, 115.2 MHz, is applied from the second L.O. amplifier (Q106) to another input to the second mixer. [Note that the 115.2 MHz second L.O. signal is the 6th harmonic of the 19.2 MHz reference oscillator.] The second mixer converts the first IF signal (115.65 MHz) down to the second IF frequency 450 kHz. The second IF signal is applied to Ceramic Filter FL105 (wideband mode) or FL106 (Project 25 mode), which provide the first part of the 450 kHz selectivity. Selection of FL105 or FL106 filters are controlled by the IF.NARROW signal from the microcomputer ("Hillary":U700). The output of the second IF filter is amplified through the second IF amplifier and back to ceramic filter FL104 (wideband mode) or FL107 (Project 25 mode), which provide the second part of the 450 kHz selectivity. Selection of FL104 or FL107 filters are controlled by the C4FM.DATA signal from the microcomputer ("Hillary":U700). The output is then run to a limiter amplifier where the IF signal is amplified/limited, balanced and output at RXIF and RXIF (bar). These outputs are then sent to Hillary. These two lines, one positive and the other negative, are used to cancel out any noise that might be on the line. These balanced outputs are applied to the phase digitizer in Hillary and detected.



## **6.2 TRANSMITTER CIRCUIT**

The 800 MHz Jaguar 700P transmitter circuit consists of modulator IC U203, a notch filter, variable attenuator CR201, buffer/driver amplifier U202, a low pass filter, RF switches U204 & U205, SAW filter FL201, PA module U201, automatic power control and antenna switch module Z302.

### **6.2.1 Modulator IC and Notch Filter**

The main VCO in the synthesizer circuit is programmed to generate the transmitter carrier frequencies 806 to 824 MHz (repeater input band) and 851 to 869 MHz (repeater talkaround band). [Australian Tx frequency ranges are 820-825 MHz & 865-870 MHz.] The notch filter consists of C222, C224, C226, and L221. The output of modulator IC U203 is applied to the notch filter attenuator pad R221-R223.

### **6.2.2 Variable Attenuator**

The output of the notch filter is applied to variable attenuator circuit R224, R225, and CR201. The transmitter power level is controlled by voltage feedback from the automatic power control circuit (APC). This control voltage is applied through resistor R224 to the anode of variable capacitor CR201 and to R225.

### **6.2.3 Buffer Amplifier and Low Pass/Bandpass Filter**

The output of the variable attenuator circuit is applied to buffer amplifier U202 and is amplified to +6 dBm. The collector voltage for U202 is provided by a switch circuit controlled by DPTT.

In the repeater input band, the output of U202 is applied to the input to SAW filter FL201. The drive signal is bandpass filtered and then applied to the PA module input. In the repeater talk-around band, the output of U202 is applied to a low pass filter consisting of C232, C233, C234, and L223. The output of the low pass filter is then applied to the PA module input.

### **6.2.4 PA Module**

The output of the PA Module is amplified to about 4.5 watts. B+ (7.5 VDC) is connected to U201 through RF choke L251. The PA Module is a two stage RF amplifier. The first stage power supply voltage is supplied by a power control circuit. The second RF amplifier operates in Class C. This output is regulated by the automatic power control circuit.

### **6.2.5 Automatic Power Control**

The automatic power control circuit samples the output power to the antenna to maintain a constant power level across the band. The automatic power control circuit controls the voltage "Vcont" to PA Module U201, pin 2.

A directional coupler is included in the antenna switch module. This directional coupler provides a sample of transmitted forward power for diode detection. The diode produces a positive DC voltage proportional to the transmitter output power level. This DC voltage (U302, pin 4) is compared at comparator U404 to the “TX POWER CONT” signal from the control unit. The output of U404 is applied to DC driver amplifier Q421, and over to DC amplifier Q422. The output voltage of Q422 is applied to the Vcont input of PA Module U201, pin 2 to provide a constant output power level.

### **6.2.6 Antenna Switch Module**

The Antenna Switch Module also consists of a transmit/receive switch circuit IC and a low pass filter. During transmit, the DPTT signal from Hillary is high. Transistor Q402 turns on “SW-5V” supply to antenna switch module Z302, pin 6. When transmitting, the antenna switch diode is low impedance.

The losses through the power control circuitry and the antenna switch module reduce the PA output power for 4.5 W down to around 3.25 W at the antenna connector. This provides the rated 3 Watts output power.

### **6.2.7 Frequency Synthesizer Circuit**

The frequency synthesizer circuit consists of the reference oscillator, PLL frequency synthesizer chip U305 (CX72301), loop filter, RX VCO Z303, and TX VCO Z304.

The PLL frequency synthesizer chip receives PLL data, clock, and control information from the microcomputer and from this generates the Tx carrier or Rx L.O. frequencies. It also provides frequency lock status back to the microcomputer.

The Rx VCO and the Tx VCO are locked to the reference oscillator by a single direct-divide synthesis loop consisting of the feedback buffer, prescaler, and PLL frequency synthesizer chip.

The TX VCO operates over a frequency range of 806-824 MHz & 851-869 MHz. The RX VCO operates over a frequency range of 735.35-753.35 MHz. [Upper limits at 825, 870 MHz for Tx; & 754.35 MHz for Rx L.O. exist for Australia.]

### **6.2.8 Reference Oscillator**

The 19.2 MHz reference oscillator consists of a 1.5 PPM TCXO (Temperature Compensated Crystal Oscillator). The TCXO is enclosed in a RF shielded can. The TCXO is internally temperature compensated for both low and high temperatures. The nominal temperature is +25 °C (+77 °F). With no additional compensation the oscillator will provide 1.5 PPM stability from –30 °C to +60 °C (-22 °F to 140 °F).

### 6.2.9 PLL Frequency Synthesizer

Fractional-N PLL frequency synthesizer chip U305 (CX72301) provides fractionality through the use of its main modulators. The output from the modulators are combined with the main and auxiliary divider ratios through their respective Fractional Units.

The 19.2 MHz reference frequency from the reference oscillator is divided by a ratio from 1 to 32 to create reference frequencies for the phase detectors. The divide ratios can be programmed through the Reference Frequency Dividers Register.

The dividend is the Desired VCO division ratio in fractional-N applications. This number is a real number and can be interpreted as the reference frequency (Fref) multiplying factor such that the resulting frequency is equal to the desired VCO frequency.

When in 18 bit mode, the 18 bit signed input value to the modulator, ranging from -131,072 to +131,071 provides 262,144 steps, each of  $F_{div\_ref}/2^{18}$  (Hz). The divider is 262,144 when the modulator is in 18 bit mode. With the modulator in 18 bit mode, the value to be programmed in the Main Dividend register is programmed by the microprocessor.

This results in an error voltage when the phases differ and a constant output voltage when phase-detector input compare in frequency and phase. If a phase error is detected, an error voltage is developed and applied to the VCO DC offset and loop filter to reset the VCO frequency. The dividend is controlled by the frequency data received on the SC.CLK, SC.DATA, and SC.SYN1LE line from the microprocessor.

When a different channel is selected or when changing to the transmit or receive mode, an error voltage is generated and appears at the phase detector output, causing the Phase Locked Loop to acquire the new frequency.

### 6.2.10 Loop Filter

The loop filter consists of R322, R323, R325-R327, R341, R343, and C335 through C341. This filter controls the bandwidth and stability of the synthesizer loop. The loop filter's bandwidth is switched via audio gate U304 which is controlled by "SC.SYN1LE" from the microcontroller. The output of the loop filter is applied to the varicaps in the transmit and receive VCO's to adjust and maintain the VCO frequency. The use of two VCO's allows rapid, independent selection of transmit and receive frequencies across the frequency band.

### **6.2.11 Rx VCO and Tx VCO**

The VCO's consist of low-noise silicon transistor oscillators followed by high-gain buffers. When changing to a different channel or changing from transmit or receive mode, signal "VCO.Rx/Tx" is used to control analog switches U304 & U306. These switches are used to either turn on the Rx VCO or the Tx VCO.

When the "VCO.RX/TX" signal is low, the U307 inverter and analog switch U304 turn on transistor Q301, which turns on Rx VCO Z303. When the "VCO.RX/TX" signal is high, analog switch U306 turns on transistor Q302, which turns on Tx VCO Z303. Both pass transistors Q301 and Q302 provide a low noise bias voltage to the VCO's via the "VSYN" bias line to provide optimized low phase noise performance.

The VCO's output powers are typically 0 dBm. The output is applied back to the PLL IC (U305, pin 7) for VCO frequency control via C367. The Rx VCO output is used as the local oscillator frequency by the receiver first mixer through the first local oscillator buffer amplifier (Q103). The Tx VCO output is applied to the modulator IC as the "LoIn" input.

The VCO voltages need only be set once at any frequency within the band and split. After that they will operate correctly over the entire split with no additional tuning.

### 6.2.12 Integrated Circuit Overview

The RF circuitry is dominated by three (3) integrated circuits. These IC's are described as follows:

- U101 (SA647) – This Rx back end IC contains the second mixer and the second IF (450 kHz) amplifier and limiter chain. The L.O. for the second mixer is the sixth harmonic of the 19.2 MHz reference oscillator. External ports are provided between the second mixer output and the I.F. amplifier input, and between the I.F. amplifier output and the limiter input to provide appropriate second I.F. selectivity. The limiter circuit provides a balanced output to HILLARY. The IC also provides the **Receiver Signal Strength Indicator (RSSI)** signal.
- U203 ( $\mu$ PC8110GR) – This Quadrature Phase Shift Keying modulator uses the baseband I & Q signals provided by the microprocessor to modulate the Local Oscillator drive signal provided by the Tx VCO.
- U305 (CX72301) – This PLL IC provides the main and auxiliary frequency synthesizer for the Rx VCO to provide the L.O. for the first mixer and for the Tx VCO to provide the L.O. drive to the QPSK modulator.

The digital circuitry is dominated by three (3) integrated circuits. These IC's are described as follows:

- U500 (“Patti”) – Provides the CODEC that digitizes Tx analog baseband signals. It also provides the CODEC to convert digitized Rx signals back to analog signals for driving the audio amplifier. Digitized Tx/Rx signals are interfaced with Hillary. This IC also contains D/A converters for setting the Tx frequency on channel and setting the Tx RF power to the proper level. This IC contains an A/D converter for an RSSI input from the Rx backend IC. This IC also handles the Rx volume control function.
- U600 (TMS320VC5416) – The DSP performs Digital Signal Processing on Tx/Rx analog and/or digital signals. Specifically, it provides the pre-emphasis filter, limiter, and post-limiter filter for Tx analog signals. It provides the digital data filter for Tx data. It provides de-emphasis for Rx analog signals. The DSP also provides all sub-audible baseband filtering.
- U700 (“Hillary”) – Contains the microprocessor, phase digitizer, timing & logic control, frequency discriminator and sigma/delta modulator to provide digital modulation.