REVISIONS	SYM	DATE	POSITION	DESCRIPTION	REVISED	CHECKED	APPROVED
	1 X 0	'01.07.09		Rev.up	H.Wakaizumi	Y.Ikeda	H.Kawaguchi
	2 X 1	'01.10.01		Signal addition	M.Sato	K.Sugimoto	N.Kimura
	3 X 0	'01.10.15		Rev.up	M.Sato	K.Sugimoto	N.Kimura
	4 X 0	'01.12.22		Rev.up	M.Sato	K.Sugimoto	N.Kimura
	5 X						

J1 AXN340038P

PTT	21	20	INT.MIC.HI
AGND	22	19	AGND (INT.MIC.LO)
N.C	23	18	Rx.DATA.OUT
B+	24	17	EMER.UDC
B+	25	16	N.C
N.C	26	15	EXT.MIC.IN
PWR.SW	27	14	MUTE.OUT
KPCOL0	28	13	UDC.TX
KPROW0	29	12	SWA+.OUT
KPROW1	30	11	UDC.SENSE.IN
KPROW2	31	10	UDC.AUDIO.OUT
KPROW3	32	9	AGND
KPCOL1	33	8	TX.DATA.IN
KPROW4	34	7	PTT.UDC
KPCOL3	35	6	SDA
KPCOL2	36	5	VLCD
AGND	37	4	+5VA
N.C	38	3	SCL
SPKR.HI	39	2	N.C
SPKR.LO	40	1	BACKLITE

U700
Hillary

D3	109	108	UPDATA6
A11	110	107	UPADDR15
A16	111	106	BINIO.PT1
MUTE.OUT	112	105	UPADDR14
A10	113	104	UPDATA4
GND	114	103	VSSO
A7	115	102	BINIO.PT0
RX.VOL.ATTN	116	101	UPADDR13
A6	117	100	UPDATA5
D7	118	99	UPEECS
BAT.ID	119	98	DAR1
WRITE	120	97	UPADDR19
A5	121	96	UPDATA0
A4	122	95	UPDATA2
A9	123	94	UPDATA1
A8	124	93	UPADCS0
A3	125	92	UPADDR18
+5VD	126	91	VSSO
GND	127	90	VDDO
AUDIO.PA>UNMUTE	128	89	UPADDR17
A2	129	88	SCL
A12	130	87	UPRAMCS
A1	131	86	SDA
A0	132	85	RXSIF.CONV
+5VD	133	84	UPPHI
CH.KEY.SEL	134	83	UPWAIT
KPCOL0	135	82	RXSIF.CLK
READ	136	81	RXSIF.DATA
LCD.BIAS3	137	80	TXSIF.DSPSYNC
PWR.LATCH	138	79	TXSIF.DSPCLK
GND	139	78	VSSO.3V
RX.DATA.OUT	140	77	TXSIF.DSPDATA
TX.DATA.IN	141	76	DSPCLK1
UDC.SWA+	142	75	DSPRST
INT.MIC.ON/OFF	143	74	RXSIF.DSPSYNC
HDATA.IN	144	73	RXSIF.DSPCLK

RESPOW	1	2	VCO.BAND.SEL
BINIO.PT11	3	4	MCLK
INPCLK	5	6	TG.SYNC
TG.SYNC	7	8	BAND/REV
BINIO.PT7	9	10	+5VD
AVDDI	11	12	RX.IF
IF.IN	13	14	RX>IF
IF.IN	15	16	RX.ON
RX.ON	17	18	PWR.SW.SENSE
BINIO.PT8	19	20	SC.DATA
SC.DO	21	22	SC.CLK
SC.SYNCLK	23	24	GND
VSSO	25	26	MODI
MODI	27	28	MODI
MODI	29	30	MODQ
MODQ	31	32	MODQ
MODQ	33	34	VDDO
VDDO	35	36	VSSO
VSSO	37	38	TX.GATE
TX.GATE	39	40	BINIO.PT2
BINIO.PT2	41	42	SC.SYN1LE
SC.SYN1LE	43	44	AVSSI
AVSSI	45	46	TEST300H
TEST300H	47	48	KPROW3
KPROW3	49	50	TX.ON
TX.ON	51	52	BINIO.PT4
BINIO.PT4	53	54	KPROW2
KPROW2	55	56	KPROW4
KPROW4	57	58	VSSI
VSSI	59	60	UPMOD
UPMOD	61	62	KPROW1
KPROW1	63	64	KPROW0
KPROW0	65	66	KPCOL3
KPCOL3	67	68	BINIO.PT5
BINIO.PT5	69	70	KPCOL4
KPCOL4	71	72	LCD/BIAS0
LCD/BIAS0	73	74	N.C

PCM.DSPCLK	72	71	PCM.DSPCLK
DSPC.TXSYNC	70	69	DSPC.TXSYNC
RXDSP.INT	68	67	DSP.INT
RXSIF.DSPDATA	66	65	RXSIF.DSPDATA
PCM.DSPMIC	64	63	PCM.DSPMIC
VDDO.3V	62	61	+3.3V
DSPC.RXSYNC	60	59	DSPC.RXSYNC
PCM.DSPSYNC	58	57	LCD.BIAS2
PCM.DSPEAR	56	55	PCM.DSPMIC
DSPC.CLK	54	53	LCD.BIAS1
DSPC.RXDATA1	52	51	TX.BAND.SEL
VSSO	50	49	GND
TXDSP.INT	48	47	DPTT
RES.RXDSP	46	45	LOW.BATT.PWR.OFF
DSPC.RXDATA2	44	43	UDC.TX
DSPCLK2	42	41	DSPCLK2
DSPC.TXDATA	40	39	C4FM.DATA
VSSI	38	37	GND
VDDI	36	35	+5VD
SC.STRB	34	33	SC.STRB
BINIO.PT3	32	31	EMER.UDC
DARO	30	29	DARO
RES.A	28	27	RES.A
SC.ACLK	26	25	SC.ACLK
VDDO	24	23	+5VD
PERIPH	22	21	EMULMODE
BINIO.PT6	20	19	BACKLITE
CON3	18	17	CON3
KPCOL1	16	15	KPCOL1
PCM.CDCSYNC	14	13	PCM.CDCSYNC
VSSO	12	11	GND
PCM.CDCMIC	10	9	PCM.CDCMIC
PCM.CDCEAR	8	7	PCM.CDCEAR
SC.SYN2LE	6	5	N.C
PCM.CDCCLK	4	3	PCM.CDCCLK
KPCOL2	2	1	KPCOL2

DRAWN H.Wakaizumi	DATE '01.05.30	CHECKED O.Baba	DATE '01.05.30	DATE '01.05.30		UNIT mm	MODEL H/H	EQPT.NAME J700P(C5416) 800MHz
DSGN OR ENGR Y.Ikeda	DATE '01.05.30	APROVED H.Kawaguchi	DATE '01.05.30	STORED	SCALE		TITLE MAIN LOGIC SCHEMATIC	6/6
KOKUSAIDENKI ENGINEERING CO., LTD					PARTS CODE		DWG. No. G3UD06903	Rev. 4