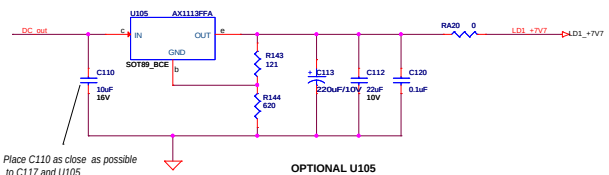
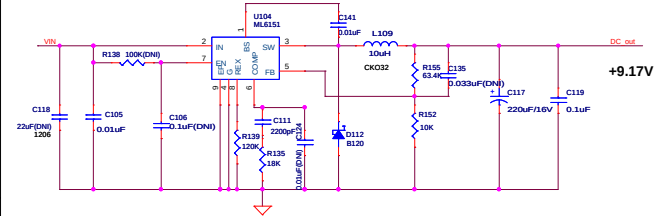
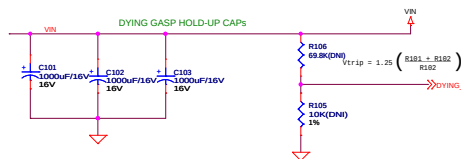
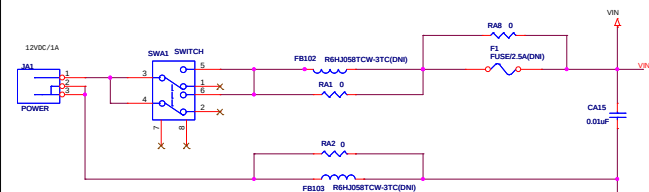
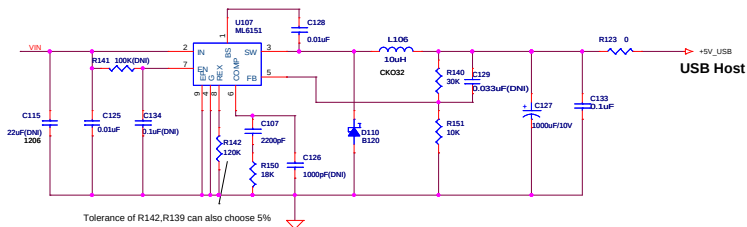
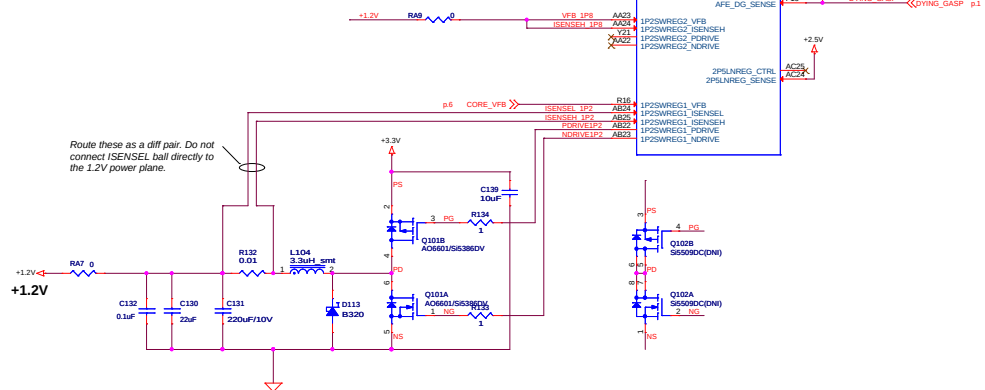


+12VDC Regulated Input

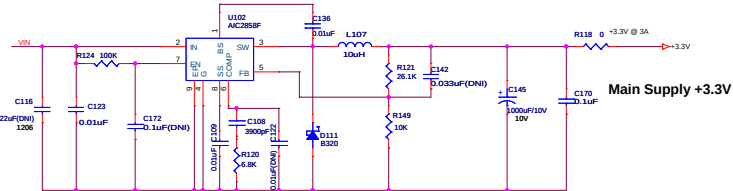


	U104	U105	R155	R152	R143	R144
U104	7.7V	DNI	52.3K	10K	DNI	DNI
U104+U105	9V	7.7V	62K	10K	121	620

Place C110 as close as possible to C117 and U105



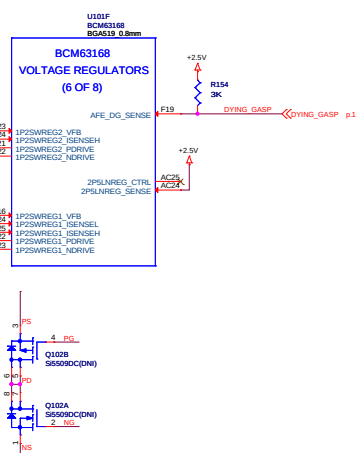
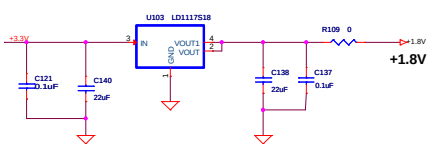
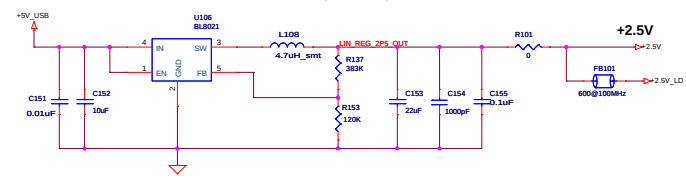
Tolerance of R142,R139 can also choose 5%



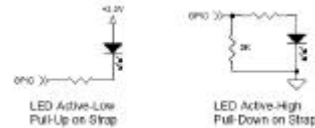
OPTIONAL ML6151 on U102 to output 3.3V

Output	U102	R120	C108	C109	R121
3.3V	AIC2858F	6.8K	3900pF	0.01uF	26.1K
3.3V	ML6151	18K	2200pF	120K	16.5K

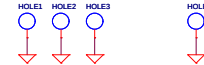
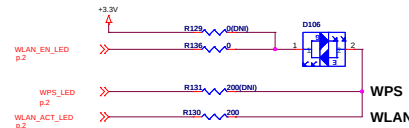
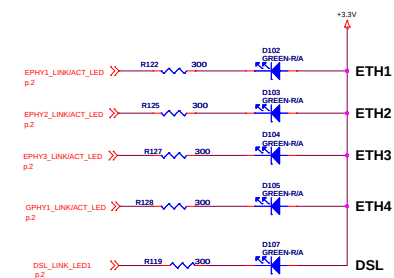
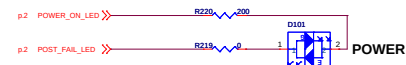
Other components stay the same



If a pull-down resistor is added to a strap pin which drives an LED, the LED driver will automatically invert from active low to active high. In this case, connect the LED to be driven as active high. Note this inversion is true even when the LED is driven from the shift register.



FRONT PANEL LEDs



DDR SDRAM layout rules:

All timing is relative to the CLK/CLKB that arrive at the destination DDR SDRAM chip.

- 1) X = CLK/CLKB should be a matched differential pair with a length < 4"
- 2) Address and control should be X +/- 20mm
- 3) DQS and DQM should be X +/- 20mm
- 4) All DQs should match corresponding byte lane DQS/DQMs within +/- 10mm
- 5) Trace impedances should be 50 ohms +/- 10% (45-55 ohms)
- 6) Route VREF with 30-mil trace and at least 1 high quality ceramic bypass capacitor for each connection to a device.
- 7) All traces should have a >= 3 to 1 spacing ratio from the reference GND/PWR layer. (e.g. 15 mil line-to-line spacing for a 5 mil dielectric thickness)

16b DDR2 SDRAM
32Mx16
NC = A2.E2

MAIN MEMORY
DDR2 SDRAM
32-256 MBYTES

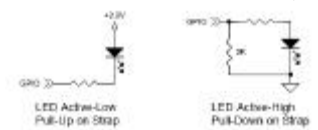
BCM63168 Strap Options

Strap settings change for B0 and C0 or later silicon

NAND SPARE 16B	NAND ENABLE ECC	NAND ECC SEL[2:0]
SPARE RES[0] 1 0 0	ENABLE 0 0	SPARE RES[0] 1 0 0
SPARE RES[1] 1 0 0	ENABLE 0 1	SPARE RES[1] 1 0 0
SPARE RES[2] 1 0 0	ENABLE 1 0	SPARE RES[2] 1 0 0
SPARE RES[3] 1 0 0	ENABLE 1 1	SPARE RES[3] 1 0 0

* All other values = No ECC

If a pull-down resistor is added to a strap pin which drives an LED, the LED driver will automatically invert from active low to active high. In this case, connect the LED to be driven as active high. Note this inversion is true even when the LED is driven from the shift register.



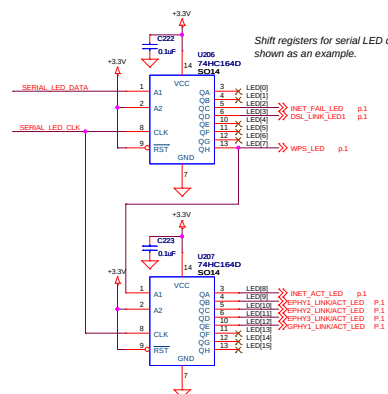
LED USAGE:

- a) LED connections only supported on LED[23:0]
- b) USB_DEVICE_LED always use LED[3]
- c) INET_LED always use LED[8]
- d) EPHY[3:1]_ACT_LED always use LED[11:9]
- e) EPHY[3:1]_SPD_LED always use LED[15:13]
- f) GPHY_SPD_LED[0] always use LED[0]
- g) WLAN_LED only supported through GPIO[38:36]
- h) Applications using NAND flash must access LED[7:2] through GPIO[7:2], and may shift out LED[7:0] through SERIAL_LED_CLK and SERIAL_LED_DATA.

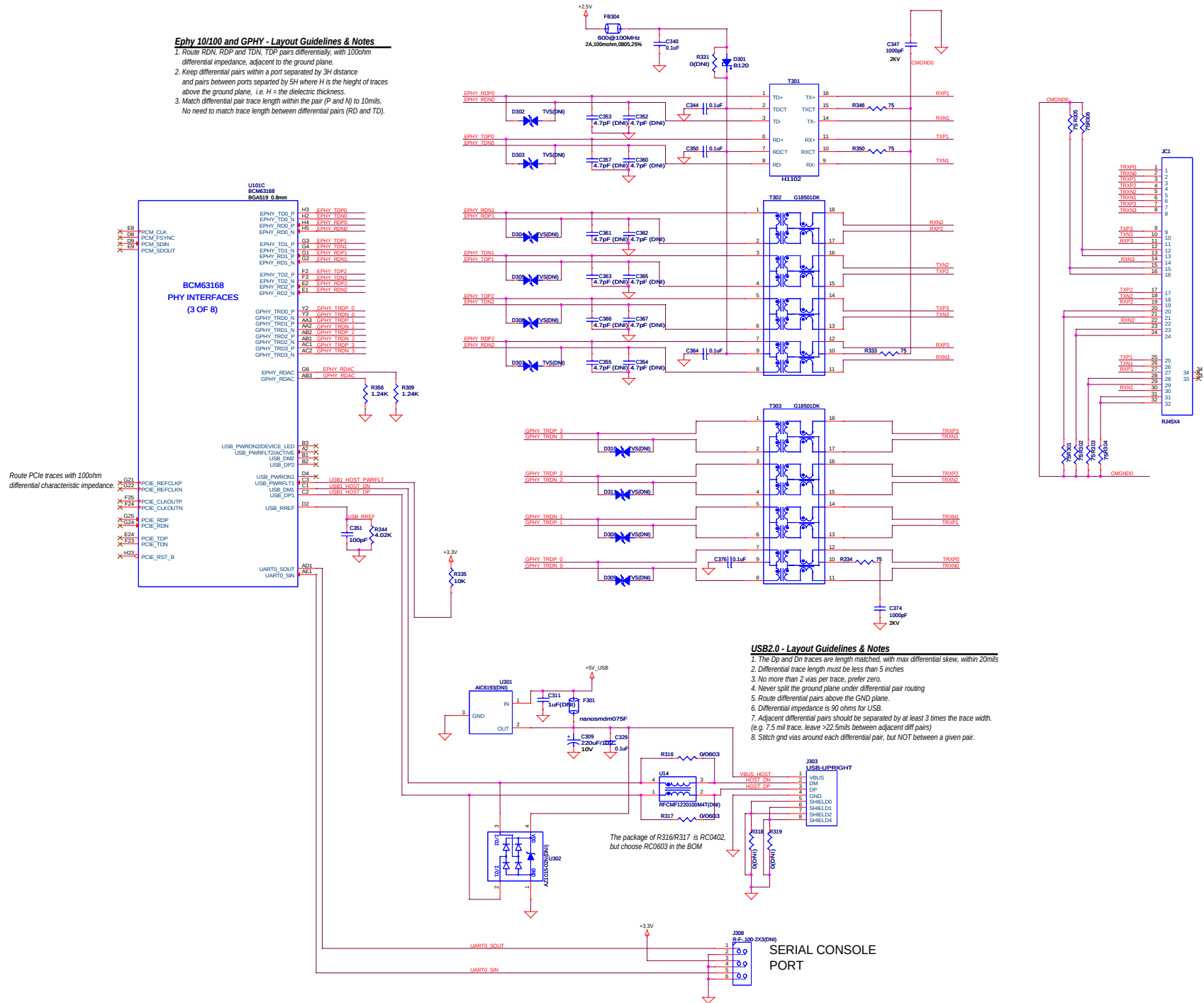
Bootstrap inputs are muxed onto GPIO[31:24,21,19,17,15,13,11,7,5,3,1:0]. Be aware that placing a pull-down resistor on any of these gpio will change the default bootstrap configuration.

GPIO[51:40] are not accessible on a 4-layer PCB. I/O voltage of GPIO[51:40] is provided by M12_VDDO. Connect to 3.3V if any of GPIO[51:40] are used. GPIO[51:36] do not have internal pull ups.

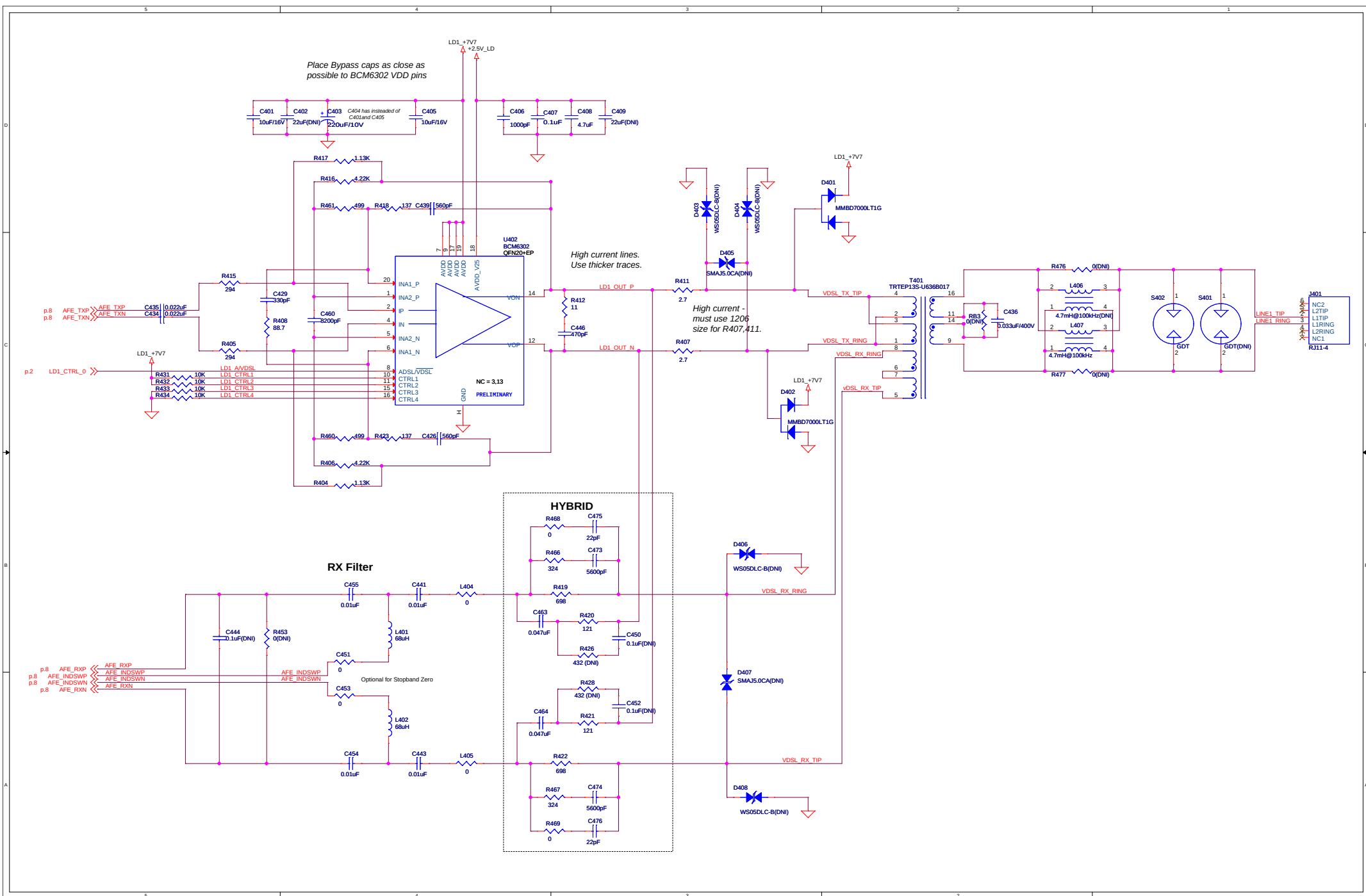
Shift registers for serial LED driver are shown as an example.



1. Route RDN, RDP and TDN, TDP pairs differentially, with 100ohm differential impedance, adjacent to the ground plane.
2. Keep differential pairs within a port separated by 3H distance and pairs between ports separated by 5H where H is the height of traces above the ground plane, i.e. $H = \frac{1}{\epsilon}$ is the dielectric thickness.
3. Match differential pair trace length within the pair (P and N) to 10mils. No need to match trace length between differential pairs (RD and TD).

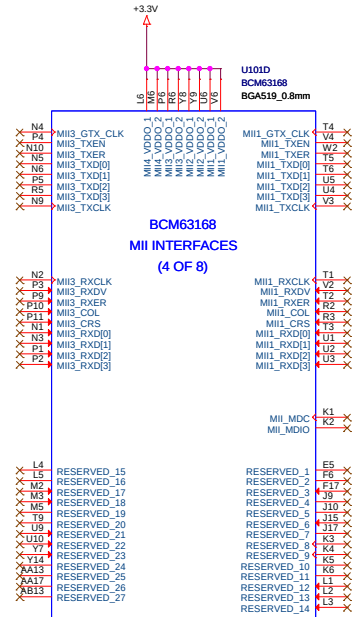


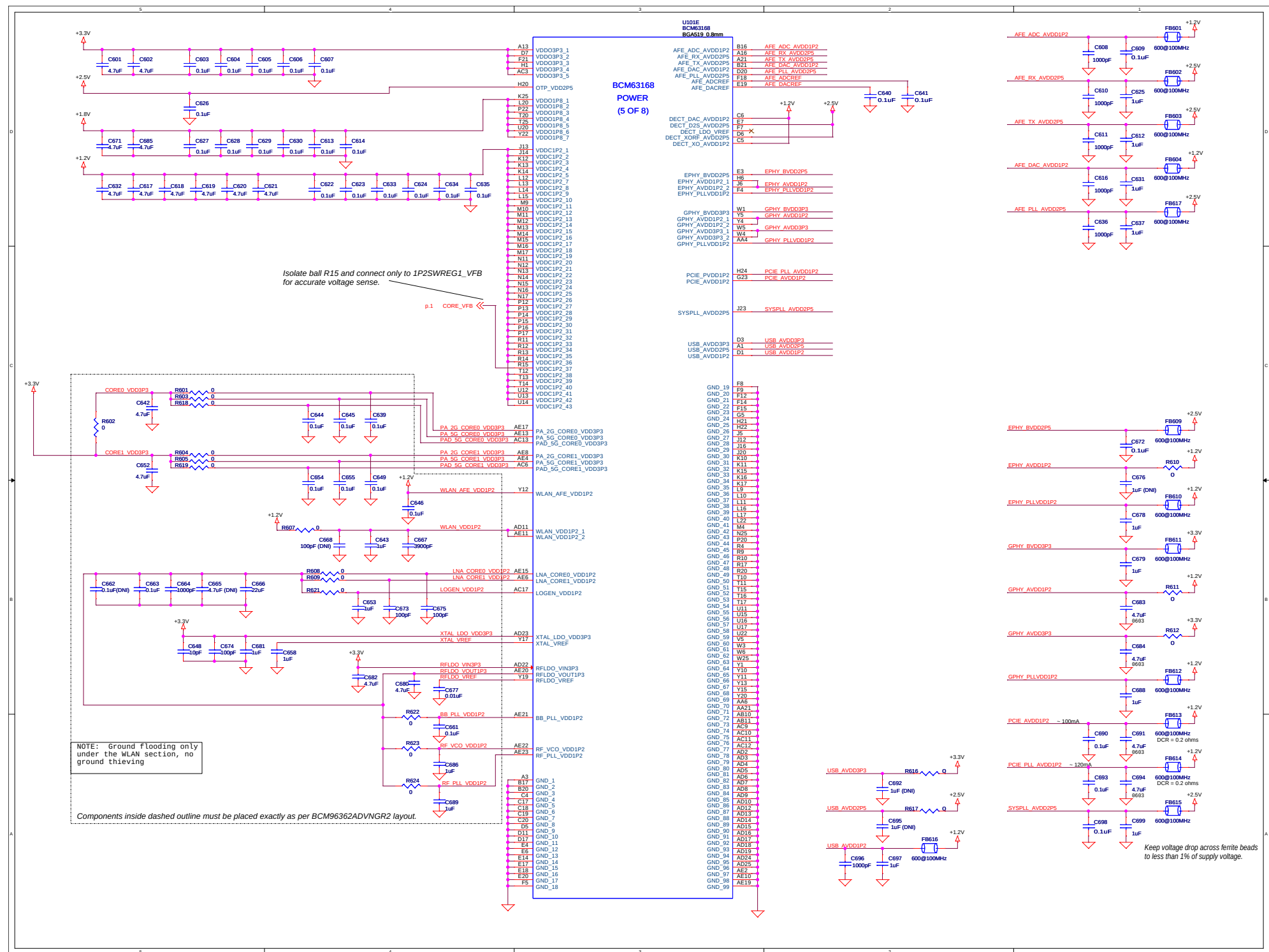
1. The Dp and Dn traces are length matched, with max differential skew, within 20mils
2. Differential trace length must be less than 5 inches
3. No more than 2 vias per trace, prefer zero.
4. Never split the ground plane under differential pair routing
5. Route differential pairs above the GND plane.
6. Differential impedance is 90 ohms for USB.
7. Adjacent differential pairs should be separated by at least 3 times the trace width. (e.g. 7.5 mil trace, leave >22.5mils between adjacent diff pairs)
8. Stitch gnd via along each differential pair, but NOT between a given pair.



CONNECT MI1X_VDDO_1 & _2 TO 3.3V WHEN USED IN MI1, R/MII, TMII MODE, OR WHEN NOT USED
CONNECT MI1X_VDDO_1 & _2 TO 2.5V WHEN USED IN RGMII MODE, OR WHEN NOT USED

! MI12_VDDO_1 & _2 PROVIDE THE I/O VOLTAGE FOR GPIO[51:40]. THEREFORE,
MI12_VDDO_1 & _2 MUST BE CONNECTED TO 3.3V WHEN ANY OF GPIO[51:40] ARE USED.





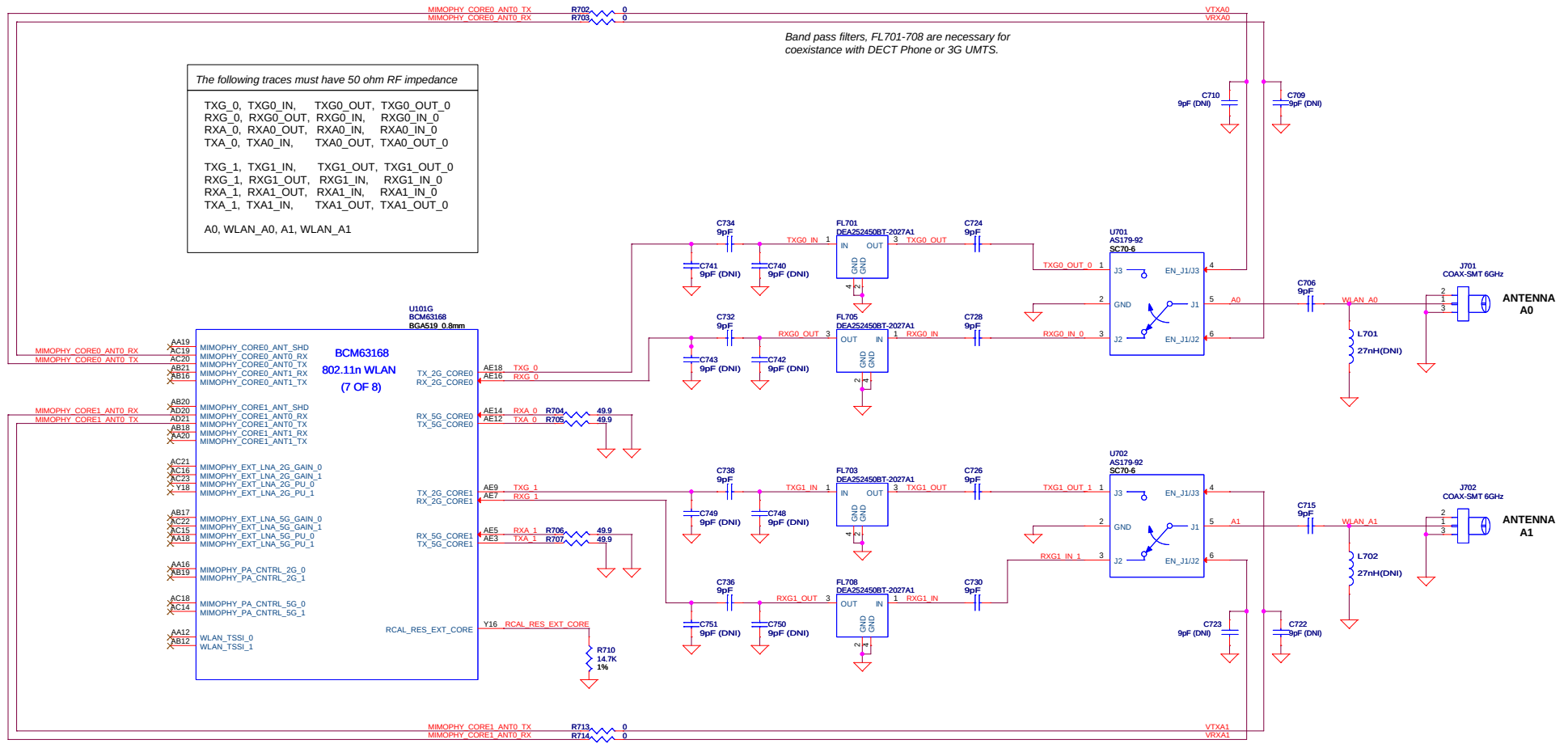
The following traces must have 50 ohm RF impedance

TXG_0, TXG0_IN, TXG0_OUT, TXG0_OUT_0
RXG_0, RXG0_OUT, RXG0_IN, RXG0_IN_0
RXA_0, RXA0_OUT, RXA0_IN, RXA0_IN_0
TXA_0, TXA0_IN, TXA0_OUT, TXA0_OUT_0

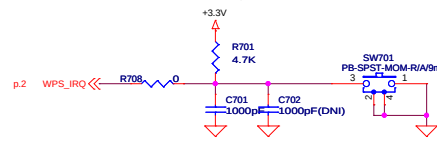
TXG_1, TXG1_IN, TXG1_OUT, TXG1_OUT_0
RXG_1, RXG1_OUT, RXG1_IN, RXG1_IN_0
RXA_1, RXA1_OUT, RXA1_IN, RXA1_IN_0
TXA_1, TXA1_IN, TXA1_OUT, TXA1_OUT_0

A0, WLAN_A0, A1, WLAN_A1

Band pass filters, FL701-708 are necessary for coexistence with DECT Phone or 3G UMTS.



Wi-Fi Protected Setup Push-Button



Wi-Fi

