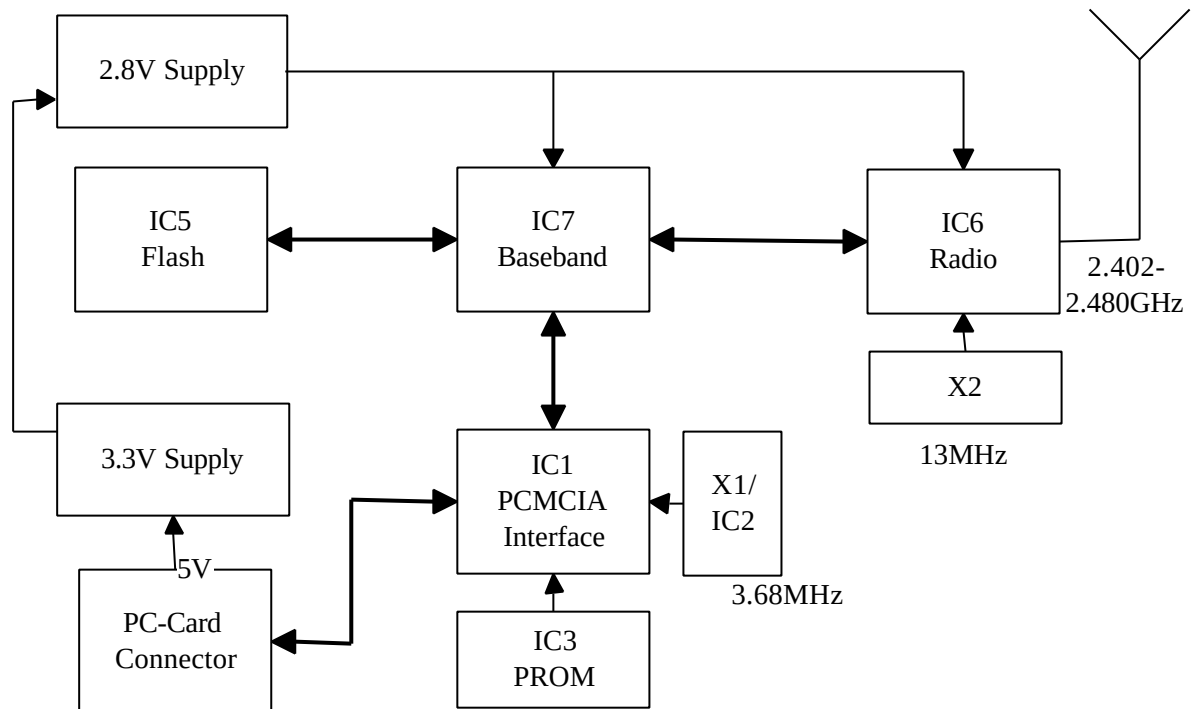


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1 Block Diagram



2 Circuit Description

There is a 3.68 MHz clock generated by IC2 and X1 used by IC1.

The radio IC6 is using the 13MHZ reference X2.

Power to the card is supplied via P1 pin 17 and 51 at 5.0 volt.

Supply voltage is regulated in IC4 to 3.3 volts for IC1, IC2 and IC3.

IC8 regulates from 3.3 to 2.8 volts for the BT-radio parts IC5, IC6 and IC7.

All control logic, PC Card interface and BT interface (UART) is placed in IC1 a Xilinx FPGA. IC1 automatically loads its configuration from IC3 during the first 200 ms after power is applied.

The UART has signals RxD and TxD for receive and transmit data, signals RTS and CTS for “hardware” flow control.

The signal “BTON” controls the BT power on/off from IC1.

The antenna is a quarter wave type PCB antenna with 0dBi gain.

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