

scott

From: scott [scott@celectronics.com]
Sent: Wednesday, August 04, 2004 1:58 PM
To: Mike Christensen
Subject: FCC ID: P2E3TPMW2

Mr. Christensen,

In order for processing of this application (FCC ID: P2E3TPMW2) to continue, the following issue(s) will have to be addressed:

- 1) The schematic diagram states that the RF is at 447.725 MHz, which disagrees with the rest of the application. Please clarify.
- 2) The schematic diagram does not show the oscillators shown in the Block Diagram. Please indicate the reason.
- 3) Please indicate how the device complies with section 15.231 (a)(2) of the FCC rules.

FYI: Although it is not a compliance issue in this case, it appears as if the duty cycle was derived by averaging over more than one pulse train. When calculating duty cycle, if the pulse train is less than 100 ms, it is determined over one pulse train, not 100 ms.

The item(s) indicated above must be submitted before processing can continue on the above referenced application. Failure to provide the requested information within 60 days of the original e-mail date may result in application dismissal and forfeiture of the filing fee. Also, please note that partial responses increase processing time and should not be submitted. Please upload responses and/or exhibits to the electronic filing website. Your correspondence number is P2E3TPMW2-1.

If you have any questions, feel free to contact me.

Best Regards,

Scott McCutchan
Operations Manager
Compatible Electronics TCB
114 Olinda Drive
Brea, California 92823
Main (714) 579-0500
Direct (714) 579-1489
Fax (714) 579-1850
scott@celectronics.com
www.celectronics.com

10/5/2004

Correspondence by Project

Project Number:

-511601430

Correspondence Number	Memo
P2E3TPMW2-1	Here are the responses to the following questions you had: 1) The schematic diagram states that the RF is at 447.725 MHz, which disagrees with the rest of the application. Please clarify. The schematic diagram was mistakenly stated that the RF is at 447.725 MHz. Please see the corrected schematic diagram that I will upload. 2) The schematic diagram does not show the oscillators shown in the Block Diagram. Please indicate the reason. The transmitter has a self OSC by Q1 and Y1; the CPU clock is built-in. 3) Please indicate how the device complies with section 15.231 (a)(2) of the FCC rules. I will upload a statement about stopping the transmission in 5 seconds. FYI: Although it is not a compliance issue in this case, it appears as if the duty cycle was derived by averaging over more than one pulse train. When calculating duty cycle, if the pulse train is less than 100 ms, it is determined over one pulse train, not 100 ms. Regarding the duty cycle calculation, our sample transmitter is hardwired to transmit signals all the time for facilitating the tests and that's the reason you would see continuous pulse trains. In real application the transmission is event driven and would only transmit a few packets each time.