# GARFIELD PEAK 2 1216 RL03C
## HW FREEZE SCH

## IPN'S FOR RL03

| No# | Standard BOM Structure IPNs | Check Box if NEW IPN needed. (Check by Requestor) | | New IPNs (Filled out by Product Config) |
|---|---|---|---|---|
| 1 | TA# | X | | M14671-001 |
| 2 | Optional on 1216 - Assy Module # | X | | M14672-001 |
| 3 | PBA# | X | | M14674-001 |
| 4 | PBMP - # up | X | | M14675-001 |
| 5 | PBMP PANEL | X | | M1467501 |
| 6 | PBMP - VDCR | X | | M1467601 |
| 7 | PB | X | | M14677-001 |
| 8 | PB FAB | X | | M1467701 |
| 9 | AM | X | | M1467801 |
| 10 | Assy Dwg/Mrkt Dwg | X | | M1467401 |
| 11 | Schematic | X | | M1467901 |
| 12 | IPC | X | | M1468001 |
| 13 | XY | X | | M1468101 |
| 14 | CAD | X | | M1468201 |
| 15 | Fabmaster | X | | M1468301 |

## GFP/TYP 1216-2230 ADP'S

USE THIS

| 1216 Adapter Board | |
|---|---|
| Discrete (new): (TyP2) | MP: K62881-001 / PCB: K62884-001 |
| CNVi (GfP2) | MP: J26338-001 / PCB: J26401-001 |

## IPN'S FOR C-STEP

| | | |
|---|---|---|
| 1 | TA# | M14671-003 |
| 2 | Optional on 1216 - Assy Module # | M14672-003 |
| 3 | PBA# | M27109-001 |
| 4 | Schematic | M1467903 |

| | | | |
|---|---|---|---|
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| SCH: M1467903 | | PBA: M27109-001 | |
| | ENGINEER: Moshe Stern | LOCAL PAGE: 1 OF 13 | GLOBAL PAGE: 1 OF 13 |
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# STACKUP

| Layer Name | Layer Type | Option 1D (POR) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Materials (um) | Finished (um) | Tolerance of the Individual measuremnet (%) | Tolerance of the Individual measuremnet +/- (um) | Min L/S (um) | M-Via (um) Prefer(ALT) | M-Via Pad (um) | R/C (%) | Dk/2G | Supplier |
| S/M | SolderMask | | 15 | 65.0% | 10 | | | | | | PSR-4000 |
| FRONT | Copper(1/3 umBase+Plating) | 12 | 25 | 28.0% | 7 | see DR | | | | | |
| | Prepreg/1-1078( 65%) | 76.2 | 65 | 20.0% | 13 | | 100( 90) | 240 | 65% | 4.03 | EM37B(Z) Prepreg (Tg 180C) |
| L2 | Copper(1/3 umBase+Plating) | 12 | 25 | 28.0% | 7 | see DR | | | | | |
| | Core (1-1086)( 61%) | 76 | 76 | 17.0% | 13 | | 100 ( 110) | 240 | 61% | 4.11 | EM370(Z) (Tg 180C) Laminate |
| L3 | Copper(1/3 umBase+Plating) | 12 | 25 | 28.0% | 7 | see DR | | | | | |
| | Prepreg/1-1078(65%) | 76.2 | 65 | 20.0% | 13 | | 100( 90) | 240 | 65% | 4.03 | EM37B(Z) Prepreg (Tg 180C) |
| BACK | Copper(1/3 umBase+Plating) | 12 | 25 | 28.0% | 7 | see DR | | | | | |
| S/M | SolderMask | | 15 | 65.0% | 10 | | | | | | PSR-4000 |
| | Finished Board Thickness (L1-L4) | | 306 | | | | | | | | |
| | Finished Board Thickness with SM | | 336 | 15% | 50 | | | | | | |

| | | | |
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# CHANGES & COMMENTS

BOARD IS BASED ON GFP2 1216 RL03A (TY BOM) AND RL03B (WALSIN BOM)

UPDATES FROM 18-OCT-2020

BASE SCH IS BASED ON RL03A, 2ND SOURCE WAL IS BASED ON RL03B

UPDATES FROM 28-OCT-2020

SCH CLEAN-UP:

- GFP SI STEP: K66335-001 (A0) --> K66335-006 (A4)
- RF SHIELD: K63118-001 --> K63118-003
- 60MHZ XTAL: G22404-054 (HOSONIC OLD) --> G22404-062 (HOSONIC NEW)

UPDATES FROM 30-NOV-2020

STACKUP UPDATED TO ITS FINAL VERSION

| | | | |
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| | | | | | |
|---|---|---|---|---|---|
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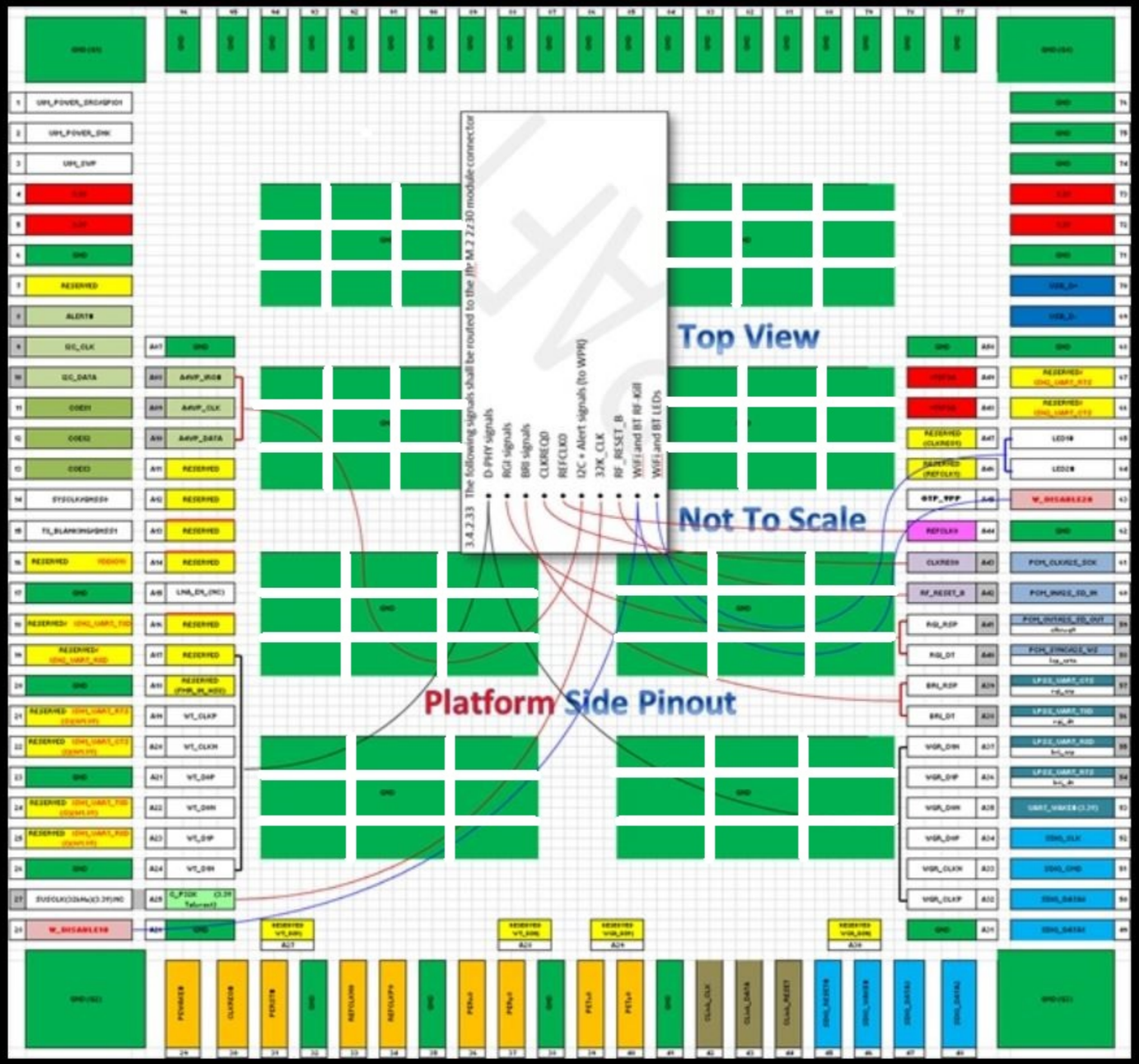
# PIN MAPPING




BASELINE IS HRP SOLDERDOWN STRUCTURE,
WITH 8 CENTRAL GND PADS
DIVDED TO 72 EQUAL-SIZED PADS
FOR BETTER-HANDLING WARPAGE ISSUES

| | | | |
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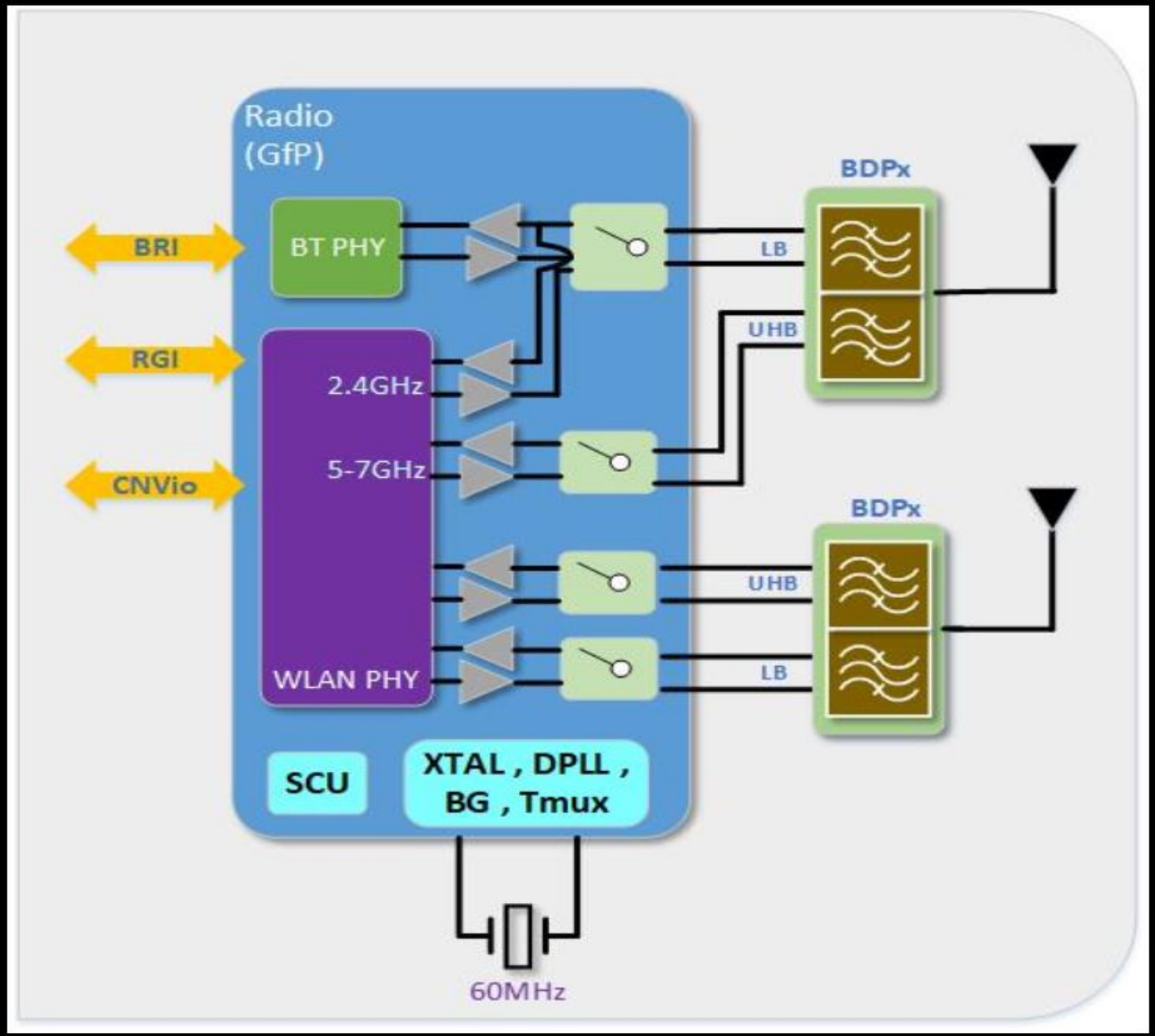
# BLOCK DIAGRAM




| | | | |
|---|---|---|---|
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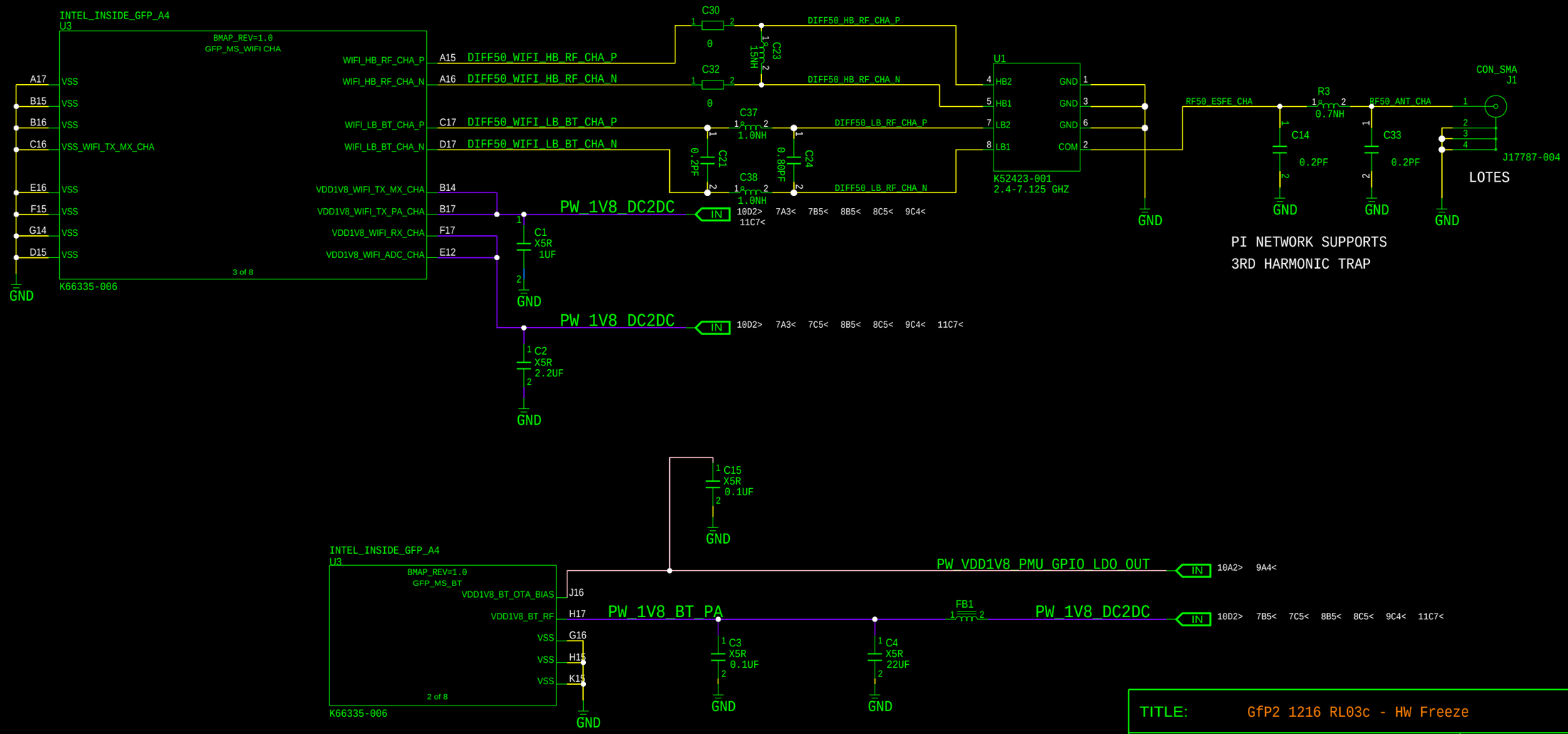
# CHAIN A

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|---|---|---|---|
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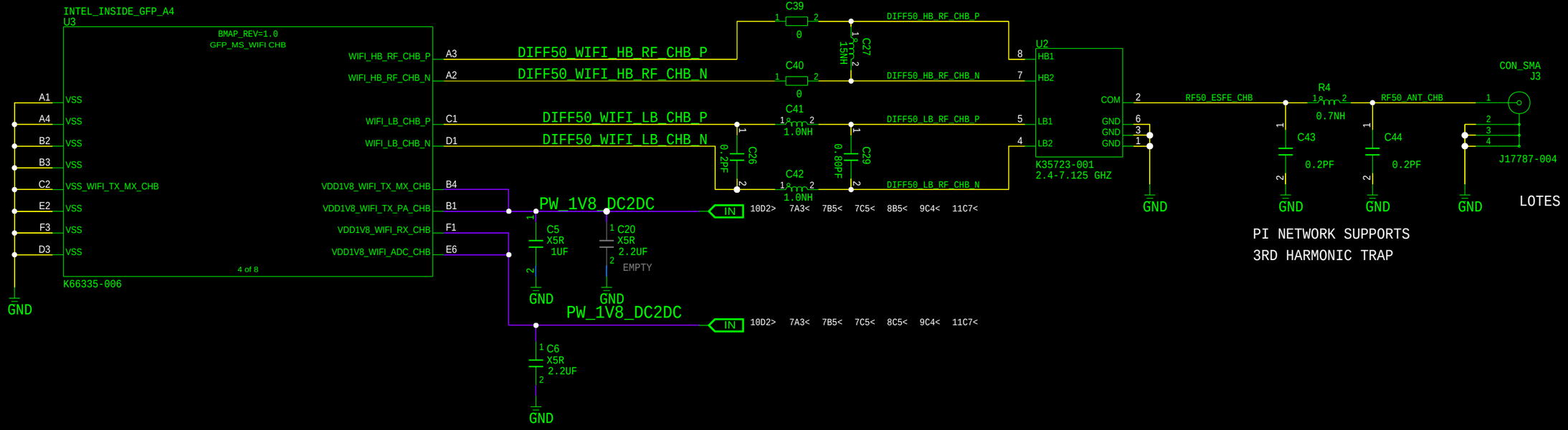
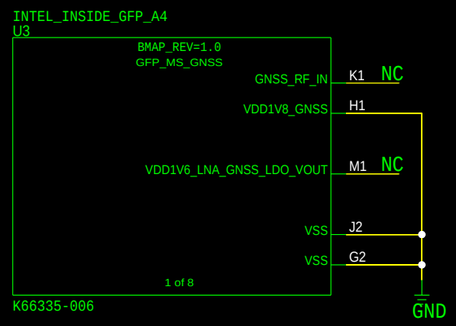
# CHAIN B




BALLS K1 & M1 ARE NC FOR GFP SI

BALL H1 IS NC IN PKG - GND

| | | | |
|---|---|---|---|
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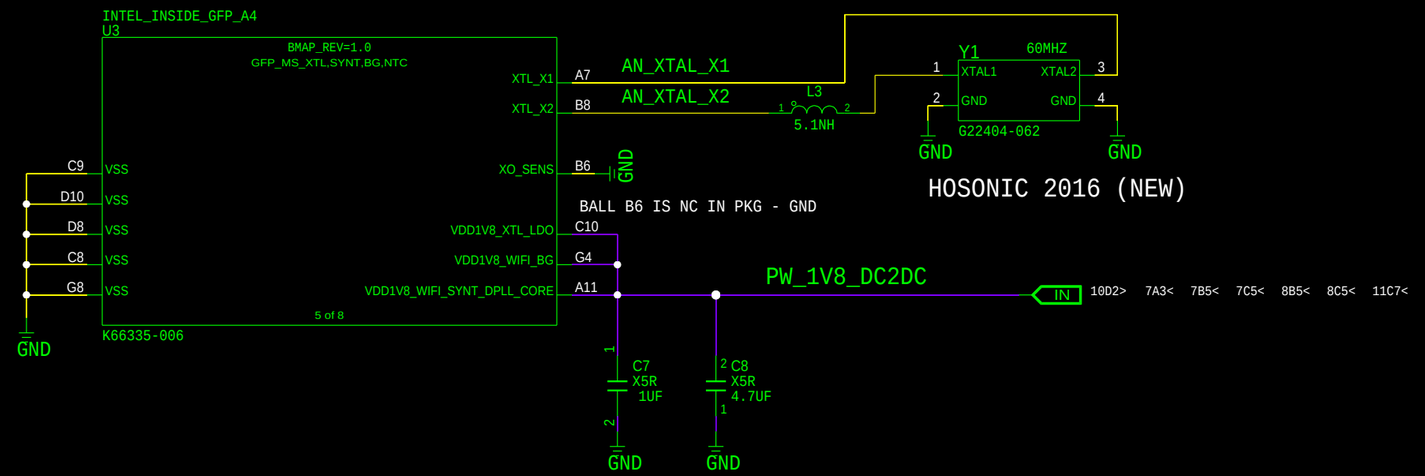
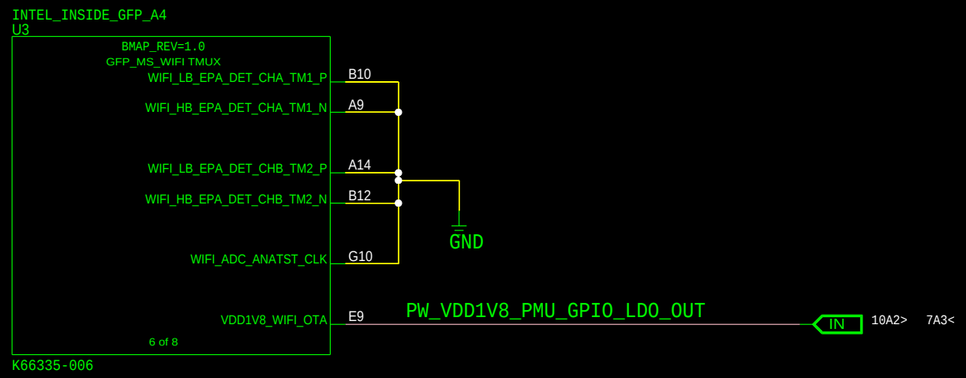
# XTAL & SYNT

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|---|---|---|---|
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# PMU

PW_VBAT_3V3

IN 13C5<>

C10 X5R 10UF

MURATA
0402 SIZE

GND

L1 1UH

CHILISIN

PW_1V8_DC2DC

OUT 7A3< 7B5< 7C5< 8B5< 8C5< 9C4< 11C7<

C11 X5R 22UF

C19 X5R 4.7UF

GND

GND

INTEL_INSIDE_GFP_A4
U3

BMAP_REV=1.0
GFP_MS_PMU

| | |
|---|---|
| VDD_VBAT_1V8_PMU | P17 |
| VDD_VBAT_PMU_SD1V8 | U16 |
| PMU_SD1V8_LX1_1 | V17 |
| PMU_SD1V8_LX1_2 | Y17 |
| PMU_SD1V8_FB | R16 |
| VDD_VBAT_SD1V1 | U2 |
| SD1V1_LX1_1 | V1 |
| SD1V1_LX1_2 | Y1 |
| SD1V1_FB | R2 |
| VDD1V8_PMU_GPIO_LDO_OUT | V16 |
| PMU_CLK_32K_IO | T12 |
| VDD3V2_PMU_FEM_CLDO | P14 |

| | |
|---|---|
| T17 | VSS_PMU_SD1V8 |
| T15 | VSS_PMU_SD1V8_ISO |
| T1 | VSS_SD1V1 |
| T3 | VSS_SD1V1_ISO |

GND

7 of 8

K66335-006

GND

PW_VBAT_3V3_DIG

IN 13C8<>

C12 X5R 10UF

MURATA
0402 SIZE

GND

L2 1UH

PW_1V1_DC2DC

OUT 11B7<

CHILISIN

C13 X5R 22UF

GND

BALL P14 IS CONNECTED TO GND
(FINAL PRODUCT)

PW_VDD1V8_PMU_GPIO_LDO_OUT

OUT 7A3< 9A4<

C9 X5R 1UF

GND

DG_CLK_IN_32KHZ

IN 13C4>

32KHZ FROM SOC

| | | | |
|---|---|---|---|
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# DIGITAL

INTEL_INSIDE_GFP_A4
U3
BMAP_REV=1.0
GFP_MS_JFP DIGITAL

NC — P3 — POWER_GOOD
NC — M15 — DIG_VPP_OTP
NC — L2 — DIG_SPI_DI
NC — M3 — DIG_SPI_CLK
NC — H3 — DIG_SPI_DO
NC — T6 — DIG_SPI_CS_B
K3 — DIG_GPIO0
GND

9C4< 8C5< 8B5< 7C5< 7B5< 7A3< 10D2> IN — PW_1V8_DC2DC — M9 — VDD1V8_PLL_REFCLK

13C5<> IN — BT_RFKILLN — K17 — BT_RFKILLN
13B8<> IN — WIFI_RFKILLN — J9 — WIFI_RFKILLN

13C5<> OUT — DIG_BT_LED — L16 — DIG_BT_LED
13C5<> OUT — WIFI_LED — J12 — WIFI_LED

BALL M17 IS CONNECTED TO GND
REFCLK1 USED AS A TEST POINT

GND — M17 — DIG_REFCLK0
REFCLK1 — N16 — DIG_REFCLK1

10B2> IN — PW_1V1_DC2DC — P4 — VDD1V0_DIG_1
P8 — VDD1V0_DIG_2

U9 — VSS
J6 — VSS
P15 — VSS
U11 — VSS
U13 — VSS
U15 — VSS
U3 — VSS
U5 — VSS
V2 — VSS
Y15 — VSS
U7 — VSS
GND

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K66335-006

DIG_BRI_DT — T9 — DIG_BRI_DT — IN — 13C1<>
DIG_BRI_RSP — P10 — DIG_BRI_RSP — OUT — 13C1<>

DIG_RGI_DT — N2 — DIG_RGI_DT — IN — 13C1<>
DIG_RGI_RSP — P1 — DIG_RGI_RSP — OUT — 13C1<>

DIG_CLKREQ0 — M12 — DIG_CLKREQ0 — IN — 13C1<>
DIG_CLKREQ1 — K14 — NC
DIG_RF_RESET_B — K10 — DIG_RF_RESET_B — IN — 13C1<>

DIG_I2C_ALERT_B — M6 — NC
DIG_I2C_SCL — K4 — NC
DIG_I2C_SDA — K8 — GND

BALL K4 BS XTAL_SEL - NC
BALL K8 IS CONNECTED TO GND

(FINAL PRODUCT)

DPHY_WGR_CLK_P — Y9 — DPHY_WGR_CLK_P — OUT — 13C1<>
DPHY_WGR_CLK_N — V10 — DPHY_WGR_CLK_N — OUT — 13C1<>
DPHY_WGR_D0_P — Y11 — DPHY_WGR_D0_P — OUT — 13C1<>
DPHY_WGR_D0_N — V12 — DPHY_WGR_D0_N — OUT — 13C1<>
DPHY_WGR_D1_P — Y13 — DPHY_WGR_D1_P — OUT — 13C1<>
DPHY_WGR_D1_N — V14 — DPHY_WGR_D1_N — OUT — 13C1<>
DPHY_WT_CLK_P — Y3 — DPHY_WT_CLK_P — IN — 13C4<>
DPHY_WT_CLK_N — V4 — DPHY_WT_CLK_N — IN — 13C4<>
DPHY_WT_D0_P — Y5 — DPHY_WT_D0_P — IN — 13C4<>
DPHY_WT_D0_N — V6 — DPHY_WT_D0_N — IN — 13C4<>
DPHY_WT_D1_P — Y7 — DPHY_WT_D1_P — IN — 13C4<>
DPHY_WT_D1_N — V8 — DPHY_WT_D1_N — IN — 13C4<>

| | | | |
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# SHIELD

MISC_SHLD_PSEUDO_LID
PSEUDO_LID1
1PIECE
LID
K63118-003

MISC_SHLD_FEN
SD1
SHIELD

| | | | |
|---|---|---|---|
| 1 | GND | GND | 8 |
| 2 | GND | GND | 9 |
| 3 | GND | GND | 10 |
| 4 | GND | GND | 11 |
| 5 | GND | GND | 12 |
| 6 | GND | GND | 13 |
| 7 | GND | GND | 14 |

K63118-003

GND GND

NEW SHIELD TARGETED FOR GFP2 SD1216

| | | | |
|---|---|---|---|
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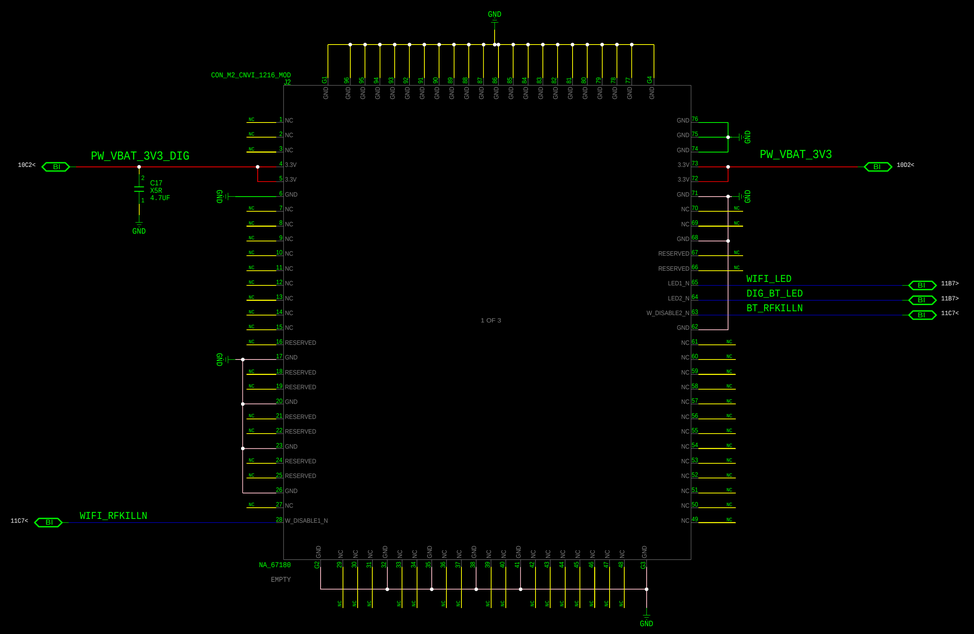
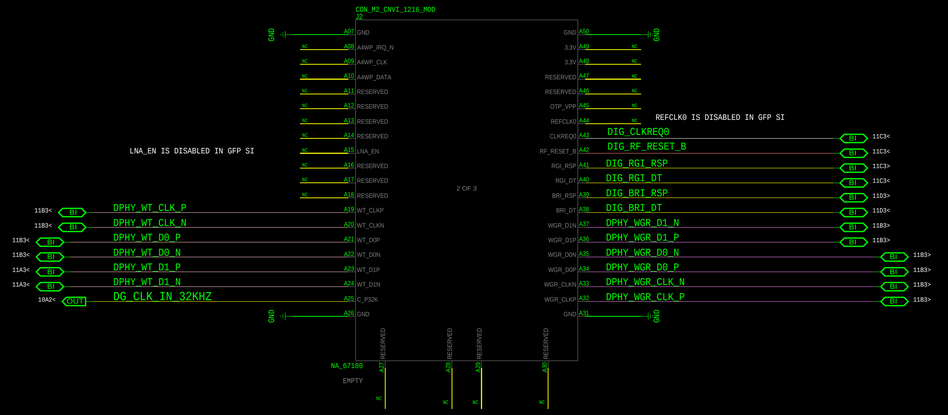
# 1216 SOLDER DOWN

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | LTR | DESCRIPTION | DATE | APPROVED |
| | | | | |





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| | | SHEET 13 OF 13 |