Unlicensed 5G mmWave (57 - 71 GHz) 16T16R beamforming RF module

General description

The Sivers Semiconductors 16+16 IEEE 802.11ad Beamforming RF Module is optimized for high performance WiGig applications. It is compliant with the IEEE 802.11ad standard and is designed to interface with market leading baseband modems.

The RF Module architecture is using direct conversion in both transmit and receive mode, with a signal path optimized for the on-board 57-71 GHz patch antenna and seamless IQ connection with the baseband modem. It includes analog channel filtering for suppression out of band interferers, making the RF Module robust in a noisy radio environment. It includes a fully autonomous AGC, optimizing the receive gain based on both wanted as well as out of band signal levels. It also includes autonomous ALC, limiting and optimizing the transmit power. The RFM to modem electrical interface is a high speed 100-pin board-to-board connector.

Applications

- Fixed wireless access (FWA)
- Backhaul (point-to-point)
- WiGig (802.11ad)

Features

- Wide band receive and transmit antenna array.
- 16 receive and 16 transmit beamforming channels.
- Compliant with the IEEE 802.11ad standard, MCS0-MCS12 modulation.
- Support for 64-QAM modulation.
- Support for half and quarter band channels.
- Excellent RF performance providing best in class EVM performance.
- Fixed cut-off analog Receive/Transmit IQ baseband filters.
- DC connection to the baseband modem.
- Easy to use with autonomous calibration routines and seamless baseband interface.
- Auxiliary ADC for temperature measurements.
- Small highly integrated form factor.

Key specifications

- Supported frequencies: 57-71GHz bandwidth
- Beam steering in azimuth 90°
- Antenna gain 11dBi supporting a combined output power of +42dBm (EIRP)
- 2dB margin to 802.11ad receive sensitivity specifications
- Power dissipation <5W, 50/50 duty cycle
- High performance solution with 10 RF layers

Revision History

Revision	Date	Change description
1.0	2019-01-15	Initial Version
2.0	2019-09-18	Revised version
3.0	2019-10-28	Updated with clk ref details section 3.4 added. Added EEPROM section 3.5 Updated figure in section 4.1
4.0	2021-04-23	New template added. Section 3, General Specification. TX/EIRP Min/Max values added. RX Sensitivity MCS5 min value added. Section 3.1/3.2 updated figures.
4.1	2021-05-10	Update duplicates in Features section. Added revision history.
4.2	2021-05-28	Updated template, first page re-arrangement and some table data and section re-arrangement. Updated receiver specification, common mode voltage. Updated transmitter specification, common mode voltage. Updated EEPROM section with updated contents of the programming. Added antenna 3D plot

Document information

Document number:	SIVDOC-410959866-142551
Document title:	BFM06010 Preliminary Datasheet
Revision:	4.2
Author:	Sivers Wireless
Document type:	
Approved by:	
Date:	
Confidentiality class:	Confidential

Table of Contents

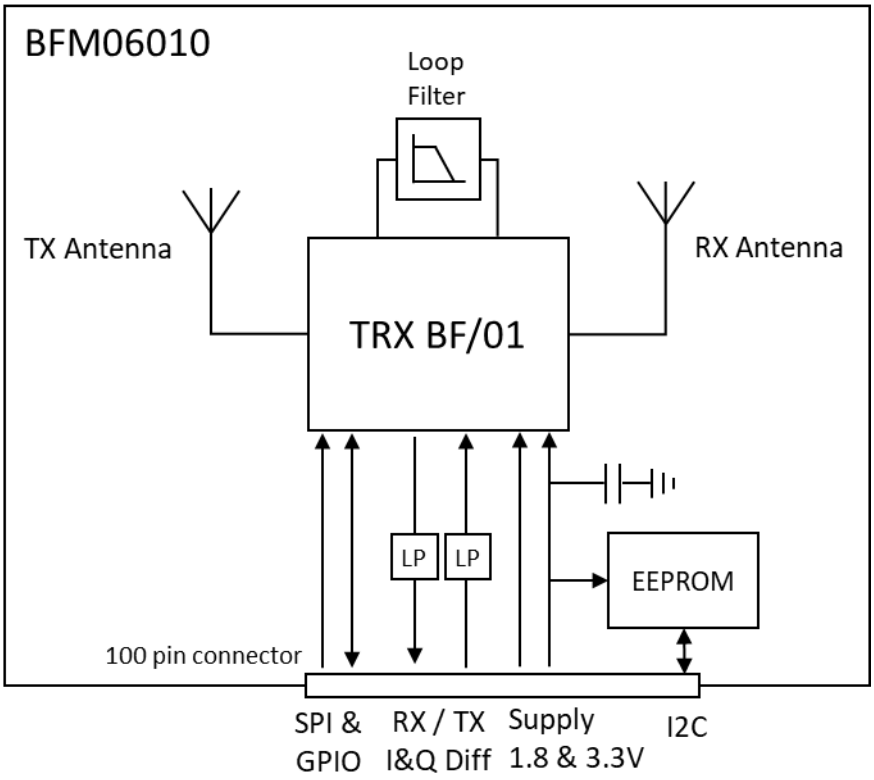
List of Figures

List of Tables

1 Overview

The BFM06010 Beamforming RF Module (RFM) is optimized for high performance unlicensed 5G mmWave applications operating in the 57 to 71GHz frequency band. The module integrates Sivers Semiconductors high performance TRX BF/01 mm-wave beamforming transceiver IC, an antenna array, loop filter, decoupling capacitors, baseband filtering and a EEPROM storing device and calibration data.

Figure 1 Block diagram BFM06010



2 Electrical Characteristics

2.1 Absolute maximum rating

Stressing the device beyond the conditions shown in Table 1 may cause permanent damage to the device.

Table 1: Absolute maximum ratings

Parameter	Condition	Minimum	Maximum	Unit
Supply voltage	vdd1v8 and dvdd1v8 pins		3.6	V
Maximum voltage on non-supply pins	Analog pins	-0.50	3.6	V
Maximum RF input	Peak power, per pin		5	dBm
Storage temperature		-40	+150	°C
Maximum junction temperature			+105	°C
Max ESD voltage, HBM Class 1B	JEDEC JESD22-A114-B, all ports	1000		V
Max ESD voltage, CDM Class 4	JEDEC JS-002-2018	500		V

2.2 Recommended operating conditions

Recommended operating conditions include parameters under user control, such as power supply voltage and case temperature.

Table 2: Operating conditions

Parameter	Condition	Min	Typ	Max	Unit
Case temperature, exposed die		-40	65	+85	°C
Analog supply voltage	VCC pins	3.1	3.3	3.5	V
Digital I/O supply voltage	VDDIO pins	1.65	1.8	3.5	V
Maximum Base Band output swing at RX	Driving Z_L=100 ohms differential			0.8	Vp-p
Maximum Base Band input swing at TX	Driving Z_L=100 ohms differential			2.5	mAp
Power Dissipation			5		W
Junction to case thermal resistance	Backside of case (exposed die)		1		°C/W

2.3 Power supply characteristics

The power supply noise requirements are provided in Table 3. Exceeding these values may lead to degraded performance.

Table 3: Power supply characteristics

Parameter	Condition	Min	Typ	Max	Unit
Analog supply ripple, low frequency	1 kHz ≤ f_{ripple} ≤ 4 MHz Single tone Total ripple			 5 7	 mVp mVp
Analog supply ripple, high frequency	10 GHz ≤ f_{ripple}≤ 70 GHz Single tone			 2.5	 Vpp
Analog supply noise	1 kHz ≤ f_{noise} ≤ 30 kHz			2000	nV/√Hz

Parameter	Condition	Min	Typ	Max	Unit
Analog supply noise	30 kHz ≤ f_{noise} ≤ 100 kHz			400	nV/√Hz
	100 kHz ≤ f_{noise} ≤ 1 MHz			40	nV/√Hz
	1 MHz ≤ f_{noise} ≤ 4 MHz			10	nV/√Hz
	4 MHz ≤ f_{noise} ≤ 10 MHz			4	nV/√Hz
	10 MHz ≤f_{noise} ≤ 40 MHz			1	nV/√Hz
	10 GHz ≤ f_{noise} ≤ 70 GHz			1	nV/√Hz

2.4 Frequency reference and distribution

An external reference clock is used for generating all radio frequencies and normal operation clocking.

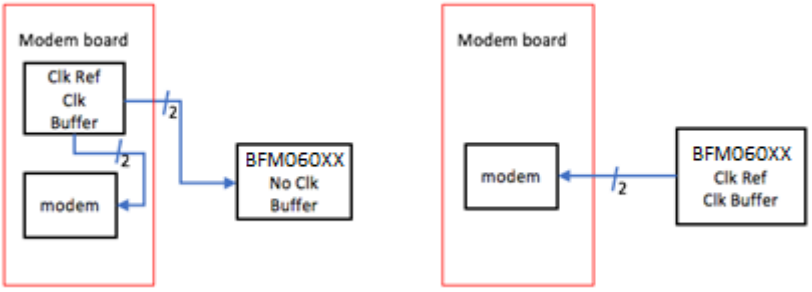
Table 4: External reference clock requirements

Parameter	Condition	Min	Typ	Max	Unit
Reference clock frequency	External clock		45[1]		MHz
Reference clock input level	Clipped sinusoidal	0.3	0.5	1	Vpp
	Differential LVDS levels		0.35		Vpp
	CMOS logic levels	1.2		2.5	Vpp
Reference clock accuracy		-10		10	ppm

[1] 40 MHz reference clock frequency is supported upon customer request.

There are two different mounting options on the BFM06010 for the 45MHz clock reference distribution as shown in Figure 2. Refer to Table 4 for detailed requirements of the external reference.

Figure 2: Differential clock from modem (left) and differential clock to modem (right)



3 RF Specifications

This section describes the RF characteristics of the mmWave transceiver.

Unless otherwise, all RF signal levels are referred to the input of an ideal matching network and typical operating conditions.

3.1 General RF specifications

Table 5: Effective isotropic radiated power and sensitivity

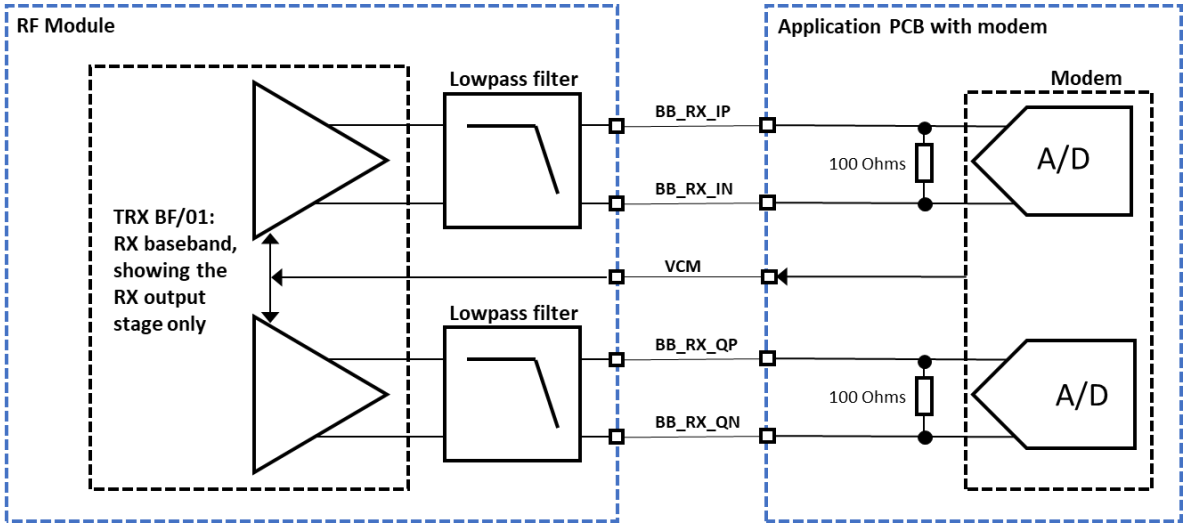
Parameter	Condition	Min	Typ	Max	Unit
TX EIRP boresight[2]	MCS0	38	39	40	dBm
	MCS5	37	39	40	dBm
	MCS9	37	39	40	dBm
	MCS12	36	38	40	dBm
RX sensitivity	MCS0	-81			dBm
	MCS5	-65			dBm
	MCS9	-62			dBm
	MCS12	-56			dBm

3.2 Receiver specifications

The receiver consists of 16 identical array antenna sections which are individually controlled in phase and amplitude to perform beamforming and beam steering. The received RF signal is then converted to zero IF, I/Q signals. The receive data path is DC coupled to avoid settling issues during Rx/Tx switching.

For I/Q signal output levels and CM levels refer to Table 6.

Figure 3: RX interface schematics



2 Performance correlation in Sivers Wireless antenna chamber reference test setup.

Table 6: Receiver specifications

Parameter	Condition	Min	Typ	Max	Unit
Frequency range		57		71	GHz
Frequency step size	With 45MHz reference clock		270		MHz
Maximum Base Band output swing	Driving ZL=100 ohms differential			0.8	Vp-p
Common mode voltage range	VCM, defined by the modem	0.55		1.0	V
Output Impedance	Differential.		100		Ω
Base band Bandwidth (-1dB)	DC coupling must be used to avoid DC shifts with long time constants at turn on/off		1		GHz
Amplitude imbalance			0.25		dB
Phase imbalance			1		°
DC offset at ADC input after calibration	Maximum gain	-25		25	mV
Single ended load impedance	From any output pin to ground	2			kΩ
Differential source impedance		85	100	115	Ω

3.3 Transmitter specification

The IQ connection with the digital modem is DC coupled, where a 3rd-order filter with fixed cutoff frequency removes anti-aliasing products. The I/Q signal input levels and CM levels are shown in Table 7.

The IQ signal is directly up-converted to 16 identical 4-patch array antenna sections which are individually controlled in phase and amplitude to perform beamforming and beam steering.

Figure 4: TX interface schematics (current sourcing DAC)

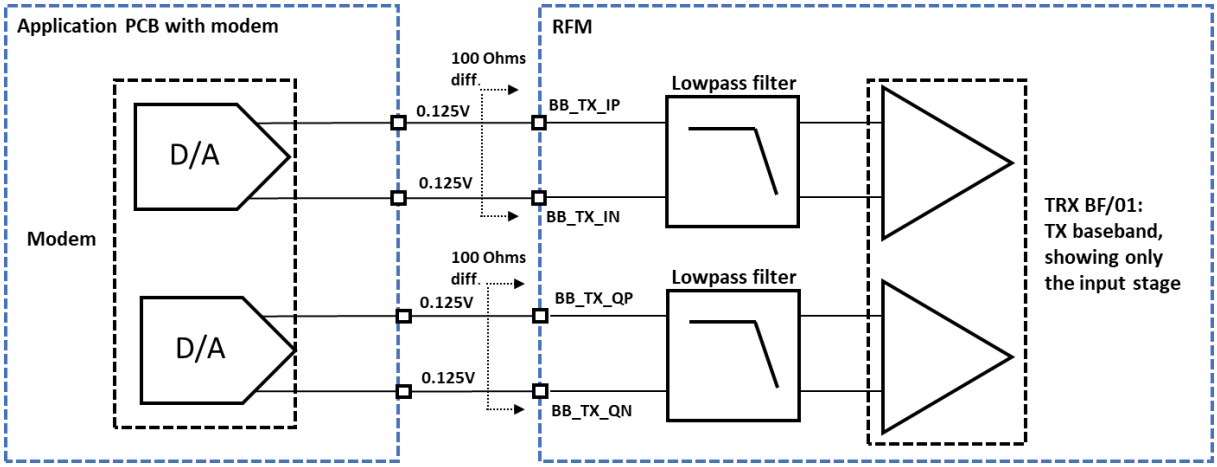


Table 7: Transmitter specifications

Parameter	Condition	Min	Typ	Max	Unit
Frequency range		57		71	GHz
Frequency step size	With 45MHz reference clock		270		MHz
Maximum Base Band input swing at TX	Driving Z_L=100 ohms differential			2.5	mAp
Common mode voltage		0.150	0.200	0.250	V
Input Impedance	Differential		100		Ω
Base band Bandwidth (-1 dB)	DC coupling must be used to avoid DC shifts with long time constants at turn on/off.		1		GHz
Amplitude imbalance	After calibration			0.5	dB
Phase imbalance	After calibration			1	°

3.4 Antenna specifications

The antenna consists of 4-patches per channel for both receive and transmit mode. The beam steering is performed in one dimension (azimuth).

Table 8: Antenna specifications

Parameter	Condition	Min	Typ	Max	Unit
Operating frequency		57		71	GHz
Antenna Gain	Boresight			11	dBi
Antenna Gain	At any scan angle (azimuth)	17			dBi

Parameter	Condition	Min	Typ	Max	Unit
Sidelobe suppression	Elevation	-10			dB
Grating Lobe Level	Azimuth	-8			dB
3dB lobe width	Azimuth (pencil beam)		±3		°
	Elevation		±9		°
Beam steering	Azimuth		90		°
	Elevation (Fixed)		18		°
Azimuth resolution			1.4		°
Beam book size	Number of vectors		64		
Pencil Beam to Omni Level	Boresight beam to omni beam	-15			dB
Omni Beam Variation	Over beam direction		±1		dB
Aperture Polarization			Vertical		

3.5 EEPROM and temperature sensor

The RFM has an on board EEPROM containing a temperature sensor. The EEPROM is accessible via and I2C interface defined in the pin list in 6.3. The current EEPROM / Temp sensor used is SE97BTP, see component datasheet for function and parametrical performance.

Address setting for the EEPROM/Temp sensor is defined by application (A0 – A1). The A2 is set by the BFM to low (A2 = 0). Addressing the device will then be done by "set address" through the I2C protocol.

EEPROM is partitioned as follows:

- 128 upper bytes address 80h to FFh is currently undefined and can be used freely by the application.
- 128 lower bytes address 00h to 7Fh is restricted for future use storing product information and potential parametrical data.

- 80 bytes Product information
- 3 bytes Temperature offset
- 21 bytes TX PWR calibration used by ALC
- 16 bytes Revision ID of product
- 8 bytes MODS

Data entry to the EEPROM is done in products production flow, however the calibration data can be updated by customer tailoring system TX PWR performance.

4 Interfaces

4.1 SPI interface

The BFM06010 includes registers to control the operating states and configuration parameters. The control registers are written or read through the serial SPI interface.

A typical timing diagram for the SPI write access is shown in Error! Reference source not found.. The SPI i nterface characteristics is shown in Table 9.

Figure 5: SPI timing diagram

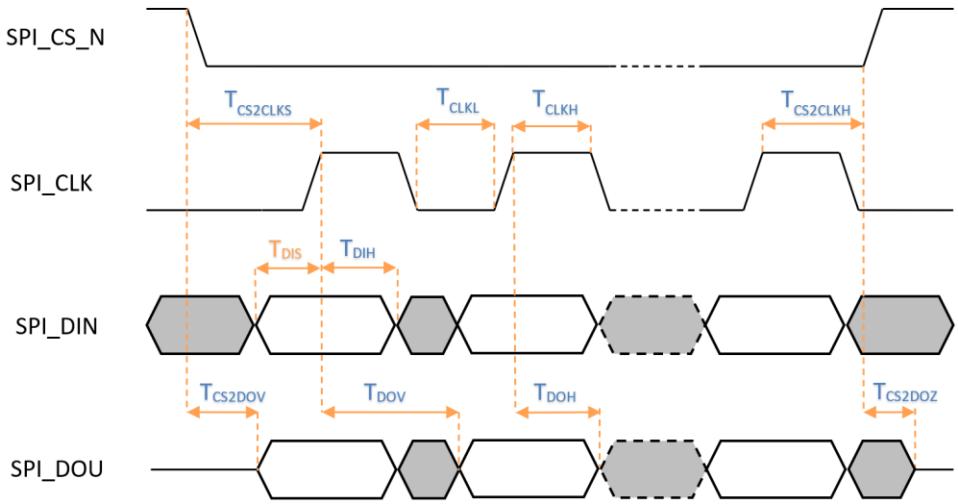


Table 9: SPI control interface characteristics

Parameter	Conditions	Min	Typ	Max	Unit
IO Voltage		0.9xVDDIO	VDDIO	1.1xVDDIO	V
IO High output voltage	@VDDIO Typ	0.95xVDDIO		1.05xVDDIO	V
IO Low output voltage	@VDDIO Typ	-0.2		0.2	V
IO High Input voltage	@VDDIO Typ	0.9xVDDIO		1.1xVDDIO	V
IO Low Input voltage	@VDDIO Typ	-0.3		0.6	V
Input capacitance				2	pF
Drive current		5			mA
SPI_CLK frequency				100	MHz
SPI_CLK high time (T_{CLKH})		5			ns
SPI_CLK low time (T_{CLKL})		5			ns
SPI_CS_N to SPI_CLK setup time ($T_{CS2CLKS}$)		10			ns
SPI_CS_N to SPI_CLK hold time ($T_{CS2CLKH}$)		10			ns
SPI_DIN setup time (T_{DIS})		3.5			ns
SPI_DIN hold time (T_{DIH})		1			ns
SPI_DOU valid time (T_{DOV})				5	ns

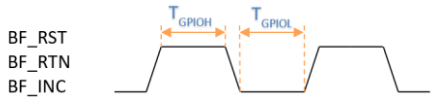
Parameter	Conditions	Min	Typ	Max	Unit
SPI_DOU hold time (T_{DOH})		1			ns
SPI_CS_N to SPI_DOU valid time (T_{CS2DOV})				3.5	ns
SPI_CS_N to SPI_DOU tri-state time (T_{CS2DOZ})				3.5	ns

4.2 GPIO interface

In addition to the SPI interface, the BFM06010 includes a GPIO interface for timing critical control signals.

Beamforming

Figure 6: Beamforming GPIO timing diagram



AGC

Figure 7: AGC GPIO timing diagram

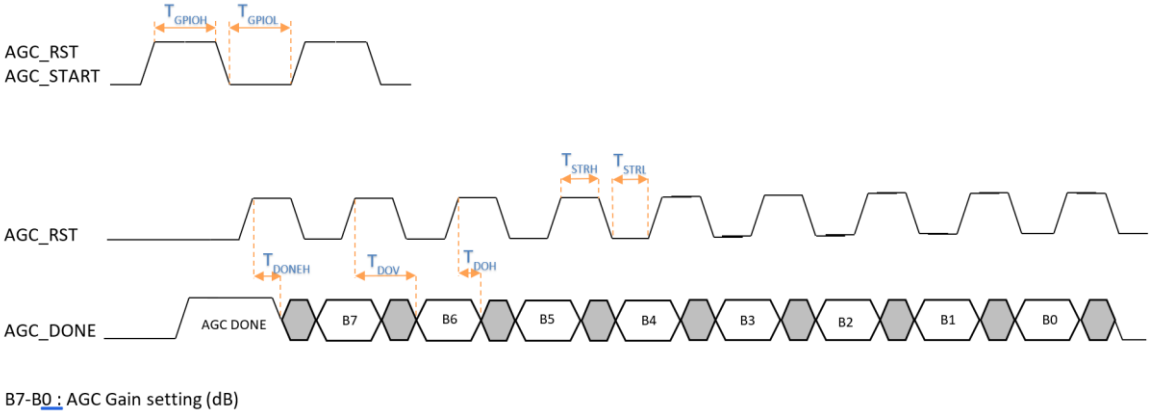


Table 10: GPIO control interface specification

Parameter	Condition	Min	Typ	Max	Unit
DC characteristics					
IO Voltage		0.9xVDDIO	VDDIO	1.1xVDDIO	V
IO High output voltage	@VDDIO Typ	0.95xVDDIO		1.05xVDDIO	V
IO Low output voltage	@VDDIO Typ	-0.2		0.2	V
IO High Input voltage	@VDDIO Typ	0.9xVDDIO		1.1xVDDIO	V
IO Low Input voltage	@VDDIO Typ	-0.3		0.6	V
Input capacitance				TBD	pF
Drive current		TBD			mA

Parameter	Condition	Min	Typ	Max	Unit
AC characteristics					
GPIO high time (T_{GPIOH})		5			ns
GPIO low time (T_{GPIOL})		5			ns
GPIO high time (T_{GPIOH})		5			ns
GPIO low time (T_{GPIOL})		5			ns

5 Calibrations

The required calibrations are performed at power-up, where limited interaction with the digital modem is required. The calibration maintains the Transceiver in a defined state also when the temperature changes. If required by the user, calibration can be requested by writing into device registers. The following calibrations are performed at power-up.

- RF Synthesizer calibration, to ensure that the synthesizer is running within its optimal operating conditions. Carried out without support from the digital modem.
- Receiver DC offset calibration, to ensure that the DC offset seen on the I/Q outputs are within its specified values. Carried out without support from the digital modem.
- Transmitter IQ error and LO leakage calibration. Support from the baseband is required.

The Receiver IQ error is by design sufficiently good for an IEEE 802.11ad system and is not required to calibrate. The Receiver is therefore used in loop-back mode during calibration of the transmitter IQ error and LO leakage, where a continuous wave is generated in the digital modem and up-converted by the transmitter. The transmitted signal is looped back over the air into the Receiver, which down-converts the transmitted spectrum and feeds it back into the digital modem. The digital modem determines the LO-leakage and image rejection and provides appropriate calibration parameters for the Transceiver to minimize IQ error and LO leakage.

6 Module, pin map and signal descriptions

6.1 Interface

Table 11: Module interface connector specification

Connector	Function	P/N	MFR	Notes
J101	Power, control, baseband	ASP-204840-01	Samtec Inc.	ERM5-050-02.0-L-DV without guide pins, identical interface.

6.2 Thermal characteristics

The module features an exposed die on the back of the TRX BF/01 package intended for thermal contact. This first interface is crucial for the system thermal performance. It is recommended that a contact material is chosen that yields a thermal resistance as per below requirements for the exposed die to cooling mechanics' interface. The contact area is 4.3 mm x 4.8 mm and it is recommended to use Laird coolzorb500 to also support RF LO leakage reduction as well as thermal cooling.

6.3 Pin list of J101 connector

Table 12: J101 connector Pin list

Signal Name (RWM6050 Denomination)	Pin	Group	Direction	Function	Signal Name (BFM Denomination)
5V_RFM	1	Power		Not used	Not used
Ground	2	Power		Ground	Ground
Ground	3	Power		Ground	Ground
MSFE_TX_IP	4	ADIFF	Input	TX baseband I signal, diff plus	BB_TX_I_P
Ground	5	Power		Ground	Ground
MSFE_TX_IN	6	ADIFF	Input	TX baseband I signal, diff minus	BB_TX_I_N
5V_RFM	7	Power		Not used	Not used
Ground	8	Power		Ground	Ground
Ground	9	Power		Ground	Ground
MSFE_TX_QP	10	ADIFF	Input	TX baseband Q signal, diff plus	BB_TX_Q_P
Ground	11	Power	Input/Output	GPIO	Ground
MSFE_TX_QN	12	ADIFF	Input	TX baseband Q signal, diff minus	BB_TX_Q_N
5V_RFM	13	Power		Not used	Not used
Ground	14	Power		Ground	Ground
Ground	15	Power	Output	GPIO	Ground
MSFE_REFCLKS	16	CMOS1V8		Not used	Not used
5V_RFM	17	Power		Not used	Not used
Ground	18	Power		Ground	Ground
Ground	19	Power	Output	GPIO	Ground

Signal Name (RWM6050 Denomination)	Pin	Group	Direction	Function	Signal Name (BFM Denomination)
MSFE_REFCLKP	20	LVDS	Input/Output	Differential clock pair from ref_clk buffer or in to TRX BF01	REF_P
Ground	21	Power	Input/Output	GPIO	Ground
MSFE_REFCLKN	22	LVDS	Input/Output	Differential clock pair from ref_clk buffer or in to TRX BF01	REF_N
Ground	23	Power	Output	GPIO	Ground
Ground	24	Power		Ground	Ground
Ground	25	Power	Output	GPIO	Ground
MSFE_CLKOUTS	26	CMOS1V8	Input	Single ended reference clock to TRX BF01	REF_TMP_SE
Ground	27	Power	Output	GPIO	Ground
Ground	28	Power		Ground	Ground
Ground	29	Power	Output	GPIO	Ground
MSFE_RX_QN	30	ADIFF	Output	RX baseband Q signal, diff plus	BB_RX_Q_N
MSFE_ADC_VCM	31	Power	Input	RX baseband common-mode voltage input	BB_RX_VCM
MSFE_RX_QP	32	ADIFF	Output	RX baseband Q signal, diff minus	BB_RX_Q_P
Ground	33	Power		Ground	Ground
Ground	34	Power		Ground	Ground
Ground	35	Power		Ground	Ground
MSFE_RX_IP	36	ADIFF	Output	RX baseband I signal, diff plus	BB_RX_I_P
Ground	37	Power		Ground	Ground
MSFE_RX_IN	38	ADIFF	Output	RX baseband I signal, diff minus	BB_RX_I_N
3.3V_RFM	39	Power	Input	Power to TRX BF01	3.3V_RFM
Ground	40	Power		Ground	Ground
3.3V_RFM	41	Power	Input	Power to TRX BF01	3.3V_RFM
3.3V_RFM	42	Power	Input	Power to TRX BF01	3.3V_RFM
Ground	43	Power		Ground	Ground
3.3V_RFM	44	Power	Input	Power to TRX BF01	3.3V_RFM
RCI_CSN1_S	45	CMOS1V8		Not used	Not used
Ground	46	Power		Ground	Ground
RCI_MOSI3_S	47	CMOS1V8		Not used	Not used
RCI_CSN1_P	48	LVDS		Not used	Not used
RCI_MOSI2_S	49	CMOS1V8		Not used	Not used
RCI_CSN1_N	50	LVDS		Not used	Not used
RCI_MOSI1_S	51	CMOS1V8		Not used	Not used
Ground	52	Power		Ground	Ground

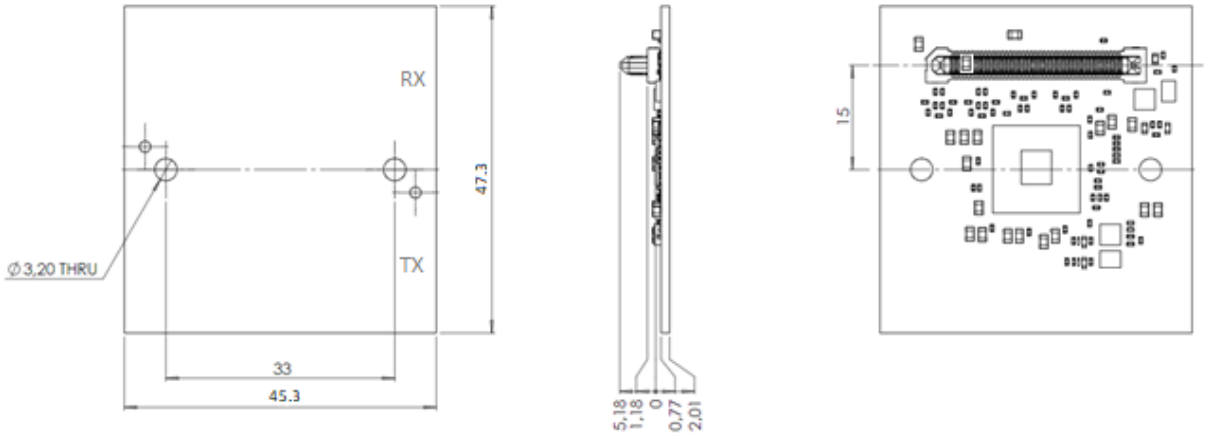
Signal Name (RWM6050 Denomination)	Pin	Group	Direction	Function	Signal Name (BFM Denomination)
RCI_MOSI0_S	53	CMOS1V8	Input/Output	SPI MOSI	SPI_MOSI
RCI_MOSI3_P	54	LVDS		Not used	Not used
RCI_MSIO1_S	55	CMOS1V8		Not used	Not used
RCI_MOSI3_N	56	LVDS		Not used	Not used
RCI_MSIO0_S	57	CMOS1V8	Input/Output	SPI MISO	SPI_MISO
Ground	58	Power		Ground	Ground
RCI_CSN0_S	59	CMOS1V8	Input/Output	SPI chip select	SPI_CS_N
RCI_MOSI2_P	60	LVDS		Not used	Not used
RCI_VDDIO(reference)	61	CMOS1V8		Not used	Not used
RCI_MOSI2_N	62	LVDS		Not used	Not used
RCI_SCLK_S	63	CMOS1V8	Input/Output	SPI Clock	SPI_CLK
Ground	64	Power		Ground	Ground
Ground	65	Power		Ground	Ground
RCI_MOSI1_P	66	LVDS		Not used	Not used
RCI_GPIO9	67	CMOS1V8	Input/Output	GPIO	BF_RTN
RCI_MOSI1_N	68	LVDS		Not used	Not used
RCI_GPIO8	69	CMOS1V8	Input/Output	GPIO	BF_INC
Ground	70	Power		Ground	Ground
RCI_GPIO7	71	CMOS1V8	Input/Output	GPIO	BF_RST
RCI_MOSI0_P	72	LVDS		Not used	Not used
RCI_PPIO6	73	CMOS1V8	Input/Output	GPIO	AGC_GAIN_0
RCI_MOSI0_N	74	LVDS		Not used	Not used
RCI_GPIO5	75	CMOS1V8	Input/Output	GPIO	AGC_GAIN_1
Ground	76	Power		Ground	Ground
RCI_GPIO4	77	CMOS1V8	Input/Output	GPIO	AGC_GAIN_2
RCI_SCLK_P	78	LVDS		Not used	Not used
RCI_GPIO3	79	CMOS1V8	Input/Output	GPIO	AGC_START
RCI_SCLK_N	80	LVDS		Not used	Not used
RCI_GPIO2	81	CMOS1V8	Input/Output	GPIO	AGC_GAIN_3
Ground	82	Power		Ground	Ground
RCI_GPIO1	83	CMOS1V8	Input/Output	GPIO	AGC_RST
RCI_CSN0_P	84	LVDS		Not used	Not used
RCI_GPIO0	85	CMOS1V8	Input	GPIO	TX_RX_SW
RCI_CSN0_N	86	LVDS		Not used	Not used
notRESET_1V8	87	CMOS1V8	Input	TRX BF01 reset signal	RST_N
RCI_VDDIO_SEL	88	CMOS1V8	Output	Requesting to set the RCIO pins to 1.8V	VCC_3V3_EEPROM
Ground	89	Power		Ground	Ground
3V3_PWREN	90	3V3		3V3 voltage supply control enable signal	shorted to pin 94 via 0ohm

Signal Name (RWM6050 Denomination)	Pin	Group	Direction	Function	Signal Name (BFM Denomination)
VDDIO (reference)	91	1V8	Input	Logic supply to TRX-BF01	VCC1V8
5V_PWREN	92	5V		Not used	Not used
I2C_SDA	93	OD3V3	Input/Output	I2C data	I2C_SDA
PWREN	94	1V8	Output	3V3 voltage supply control enable signal	shorted to pin 90 via 0ohm
I2C_SCL	95	OD3V3	Input	I2C clock	I2C_SCL
I2C_A0	96	3V3	Input	I2C address bit 0 to EEPROM	I2C_A0
notALARM_OD	97	OD1V8		Not used	Not used
I2C_A1	98	3V3	Input	I2C address bit 1 to EEPROM	I2C_A1
MDETECT	99	3V3	Output	Optional status signal pin, to determine if a RFM module is installed	connected to 3V3_SYS (pin 100)
3V3_SYS	100	Power	Input	3V3 voltage supply, always on	shorted to pin 88 AND PIN 99 via 0ohm

6.4 Mechanical outline

The size of the transceiver module 47.3x45.3x9.14mm.

Figure 8: Package and module interface connector



7 Schematics

Reference schematics are available upon request.

8 Typical performance characteristics

This section shows typical antenna performance. The measurements are performed with the RFIC in a power saturated mode and CW (non-modulated).

Figure 9: Radiation pattern

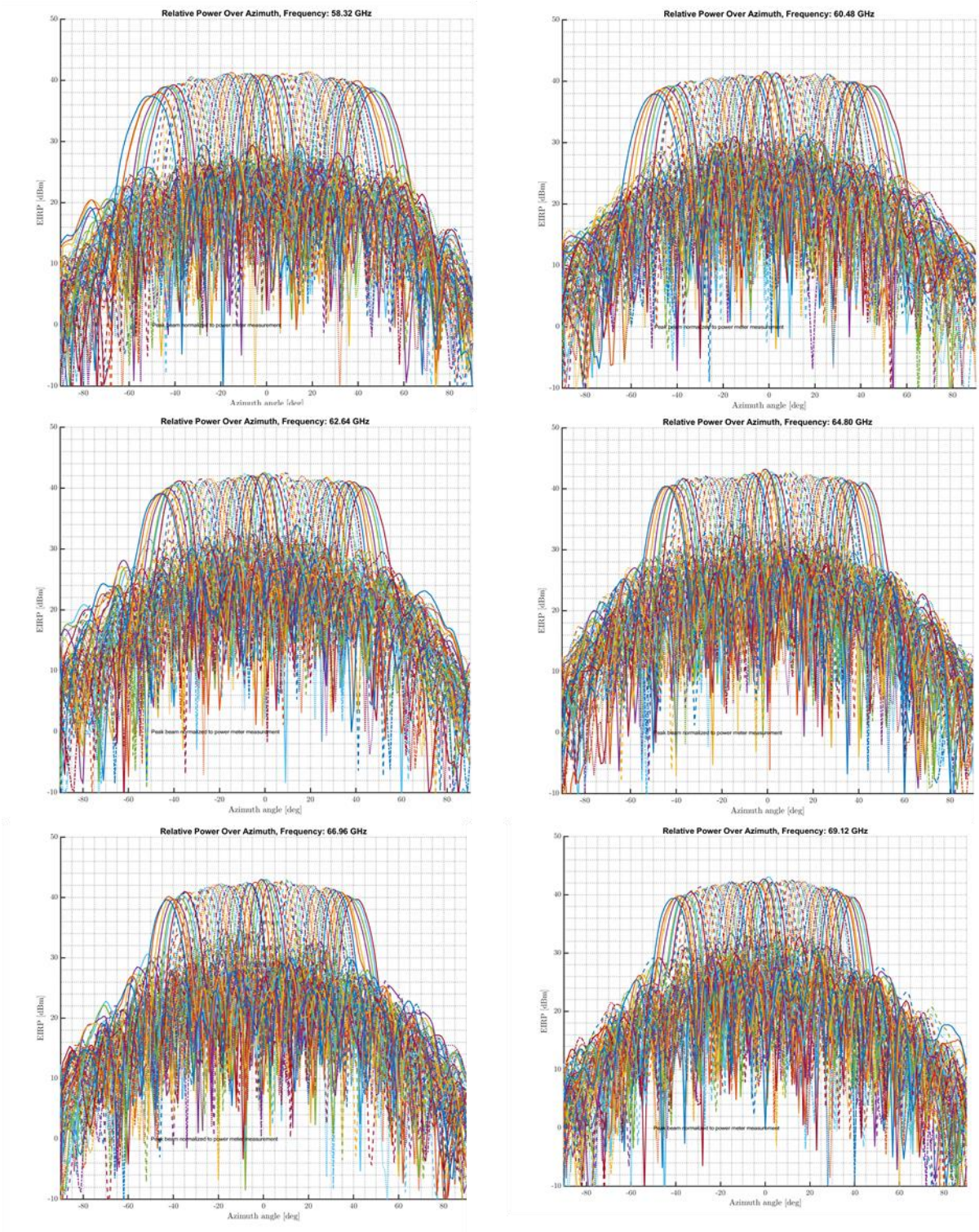
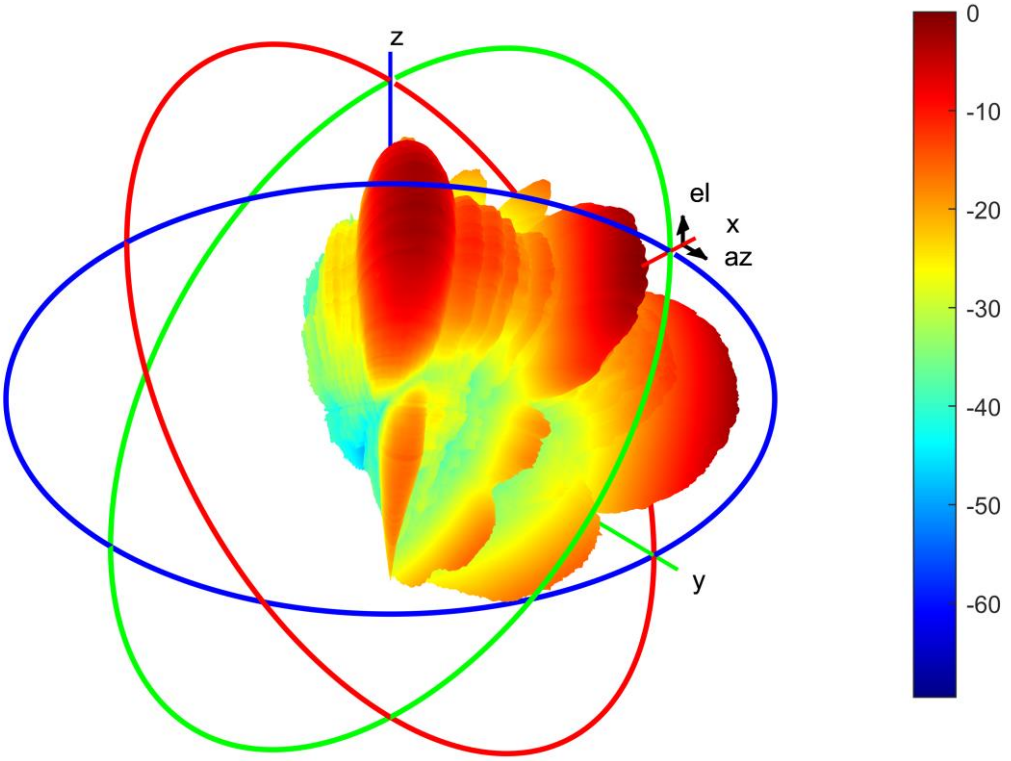


Figure 10: 3D Antenna plot beam 1, 32, 63)



9 Ordering Information

Table 13: Ordering information

Package Type	Shipping Package	Version	Orderable Part No.	Top-Side Marking
SMT PCB with connector	Single unit in ESD Bag	External Clk Ref	BFM06010 R2.2	BFM06010 R2.2 MMyywwnnnnnn*
SMT PCB with connector	In shipping tray	External Clk Ref	BFM06010 R2.2	BFM06010 R2.2 MMyywwnnnnnn*
SMT PCB with connector	In shipping tray	Internal Clk Ref	BFM06011 R2.2	BFM06011 R2.2 MMyywwnnnnnn*

*:M are manufacturer, yy ww is year/work week, and nnnnn is a five-digit sequential number.