
Processing Gain of a Direct Sequence Spread Spectrum, FCC CFR 47, Para.15.247(e)

Product Name : AWL-1100P

FCC Requirements: The Processing gain of a direct sequence system shall be at least 10 dB.

The Processing gain shall be determined from the ratio in dB of the signal-to-noise ratio with the system spreading code turned off to the signal to noise ratio with the system spreading code turned on, as measured at the demodulated out of the receiver.

Environmental Condition: Room temperature and Humidity : + 25 °C and 50%

Power Input: DC Power from the computer

Test Equipment :

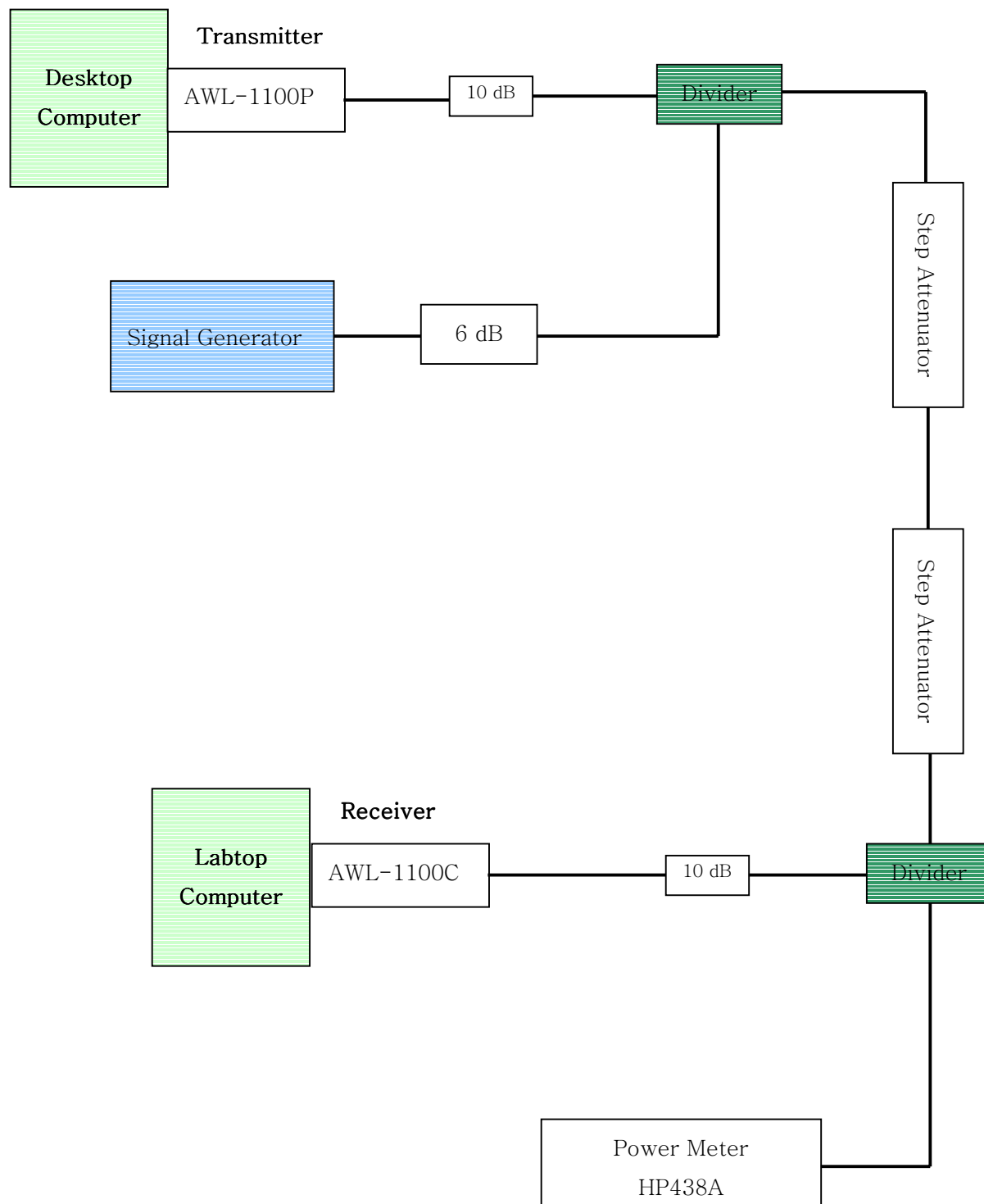
NO	Equipments	Vendor	Model Name	Description
1	Spectrum Analyzer	Agilent	HP8595E	9KHz ~ 22 GHz
2	Signal Generator	Agilent	E4421A	
3	Power Meter	Agilent	HP438A	
4	Attenuator			10 dB, 20 dB
5	Step Attenuator	Weinschel	AE117A-69-11	70 dB
6	Step Attenuator	Weinschel	AF119A-99-33	99 Db
7	Power Splitter	AceTeq.		
8	Computer	Sambo	Dreamsys	

Method of measurement: Jamming Margin Method

The processing gain may be measured using the CW jamming method. Figure1 shows the test configuration. The test consists of stepping a signal generator in 50 KHz increments across the passband of the system. At each point, the generator level required to produce the recommended Bit Error Rate(BER) is recorded. This level is the jammer level. The output power of the transmitting unit is measured at the same point. The Jammer to Signal(J/S) ratio is the calculated. Discard the worst 20% of the J/S data points. The lowest remaining J/S ratio is used when calculating the Process Gain.

Theoretical Calculation : The use of 8% FER frame error rate(or PER packet error rate) as a substitute for the recommended BER bit error rate and the ideal signal to noise ratio per symbol(E_b/N_o) is derived in the attached documents

Processing Gain Test Set Up



◆ Processing Gain Test

1. Test Background and Procedure

According to FCC regulations[1], a direct sequence spread spectrum system must have a processing gain, G_p of at least 10 dB. Compliance to this requirement can be shown by demonstrating a relative bit-error-ratio(BER) performance improvement between the case where spread spectrum process(coding, modulation) are engaged relative to the process being bypassed. In some practical systems, the spread spectrum processing cannot simply be bypassed. In these cases, the processing gain can be indirectly measured by a jamming margin test [2].

2. Theoretical calculations

The processing gain is related to the jamming margin as follows [2]

$$G_p = [S/N]_{\text{output}} + [J/S] + L_{\text{system}}$$

Where $BER_{\text{reference}}$ is the reference bit error ratio with its corresponding theoretical output signal to noise ratio per symbol, $(S/N)_{\text{output}}$, (J/S) is the jamming margin(jamming signal power relative to desired signal power)m, and L_{System} are the system implementation losses.

The maximum allowed total system implementation loss is 2 dB.

The HFA3861A direct sequence spread spectrum baseband processor uses CCK modulation which is a form of M-ary Orthogonal Keying. The BER performance curve is given by [5].

“The probability of error for generalized M-ary Orthogonal signaling using coherent demodulation is given by:

$$P_e = 1 - P_{c1} = 1 - \frac{1}{\sqrt{2\pi}} \int_{-\frac{S_{01}}{N_0}}^{\infty} [2(1 - Q\left\{z + \sqrt{2 \frac{Eb}{\eta}}\right\})]^{\frac{M}{2}-1} \exp\left\{-\frac{z^2}{2}\right\} dz$$

This integral cannot be solved in closed form, and numerical integration must be used.

This is done in a MATHCAD environment and is

2.1 1000 byte PER vs. Es/No

The reference PER is specified as 8%. The corresponding Es/No(signal to noise ratio per symbol) is 16.4 dB. The Eb/No required to achieve the desired BER with maximum system implementation losses is 18.4 dB. The minimum processing gain is again, 10 dB,

$$Gp = \left(\frac{Es}{No} \right)_{output} + \left(\frac{J}{S} \right) + L_{system} = 16.4dB + 2.0dB + \left(\frac{J}{S} \right) \geq 10dB$$

$$Gp = 18.4dB + \left(\frac{J}{S} \right) \geq 10dB$$

The minimum jammer to signal ratio is as follows:

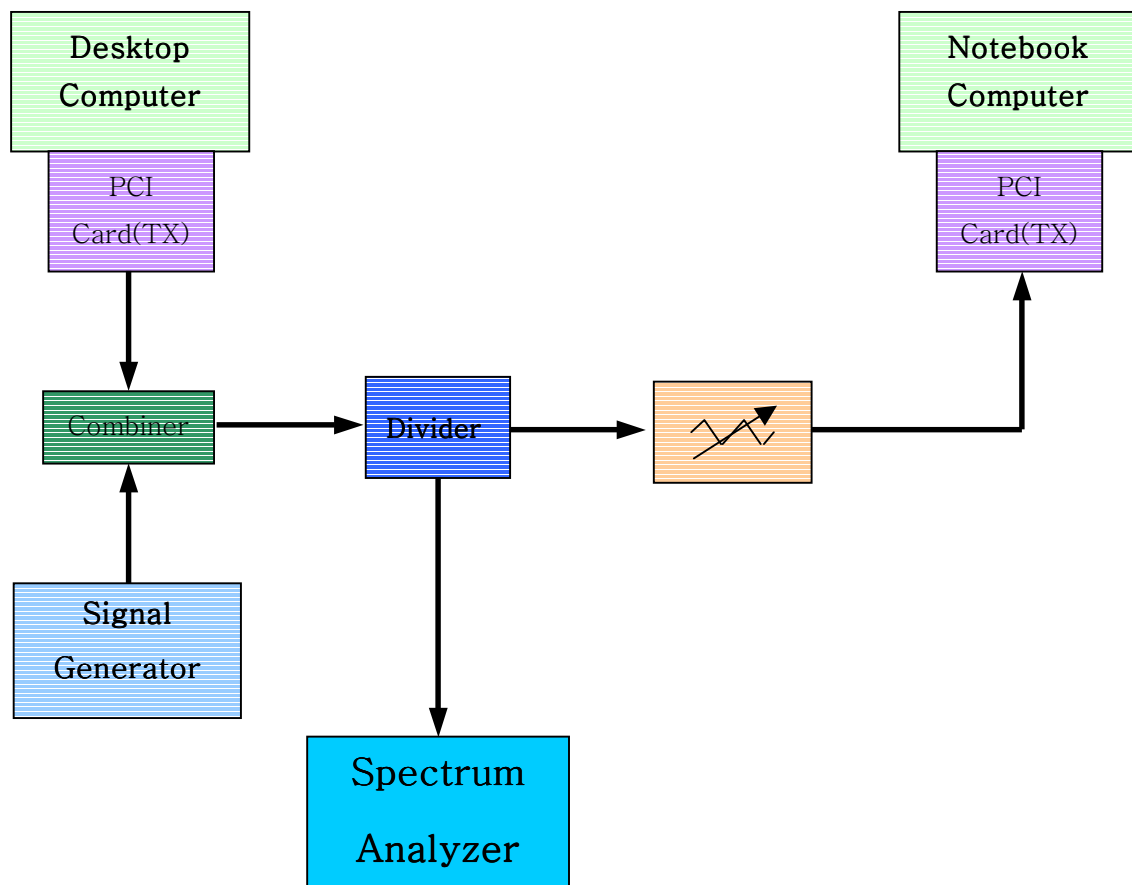
$$\left(\frac{J}{S} \right) \geq -8.4dB$$

For the case of the HFA3861A, the bit rates are 1,2,5.5, and 11 Mbps. The corresponding symbol rates are 1,1, 1.375, and 1.375 MSps. The chip rate is always 11 Mcps, so the ratio of chip rate to symbol rate is 11:1 for the 1 and 2 Mbps rates and 8:1 for the 5.5 and 11 Mbps rates. Since the symbol rate to bit rate is less than 10 for the higher rates, we supply the theoretical processing gain calculation for these cases where both spread spectrum processing gain and coding gain are utilized. This is reasonable in that they cannot be separated in the demodulation process. If a separable FEC coding scheme were used, we would not be comfortable making this assertion.

The PER can be related to a BER of 1e-5 on 1000 byte packets. With 8 bits per symbol, the Eb/No of BPSK is 9.6 dB for 1e-5 BER, so therefore the coding gain of CCK over BPSK is 2.2 dB. We add this to the processing gain of 9 dB to get 11.2 dB overall processing gain for the CW jammer test.

Taking the calculations above, if the $\left(\frac{J}{S} \right) \geq -8.4dB$ then the equipment passes the CW jamming test.

* Test Block Diagram



* Test Procedure

Obtain the simplex link shown. Perform all independent instrumentation calibrations prior to this procedure. Set operating power levels using fixed and variable attenuators in system to meet the following objectives:

1. Signal Power at receiver approximately -50 dBm
2. Signal Power at power meter between -5 and -10 dBm for optimal linearity.
3. Use spectrum analyzer to monitor test and measure the power.
4. Ensure that Signal Generator RF output is disabled and measure the power.
This is the relative signal power S_r .
5. Set CW jammer generator RF output frequency equal to the carrier frequency and enable generator output.



Set reference CW jammer power level at power meter port 8.4 dB below S_r (minimum J/S, or 10 dB processing gain reference level) . Note the power level setting on the generator, this is the reference CW jammer power setting, J_r .

6. Disable CW jammer , re-establish link. PER test should be operating essentially error free.
7. Enable CW jammer at the reference power level and verify that the PER test indicates a PER of less than 8 % .
8. Alternatively, adjust the CW jammer level to that which causes 8% PER and verify that the S/J is less than 8.4 dB.
9. Repeat step 7 for uniform steps in frequency increments of 50 KHz across the receiver passband with the CW jammer. In this case the receiver passband is ± 8.5 MHz.

The number of points where the PER fails to achieve 8% is determined and if this is above 20% of the total, the test is failed otherwise it is passed.

The margin by which the radio passes the test can be determined from the average of the remaining points 'PERs scaled on the PER curve above.

The numerical data associated with the following radio channels is tabulated and presented for:

Channel 1 : 2142 MHz

Channel 6 : 2437 MHz

Channel 11 : 2462 MHz