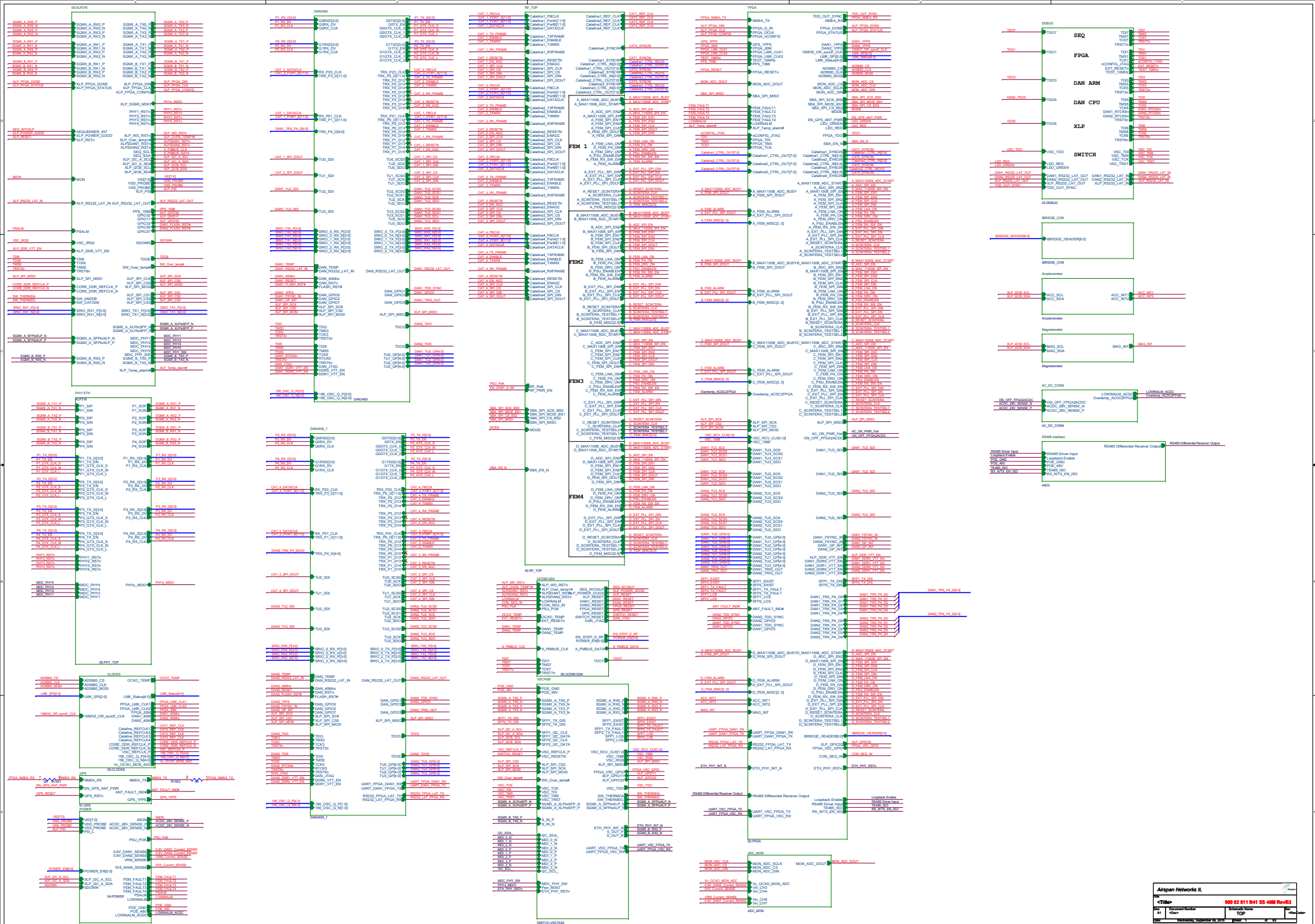
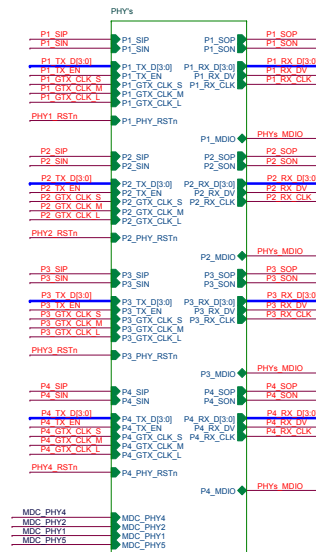
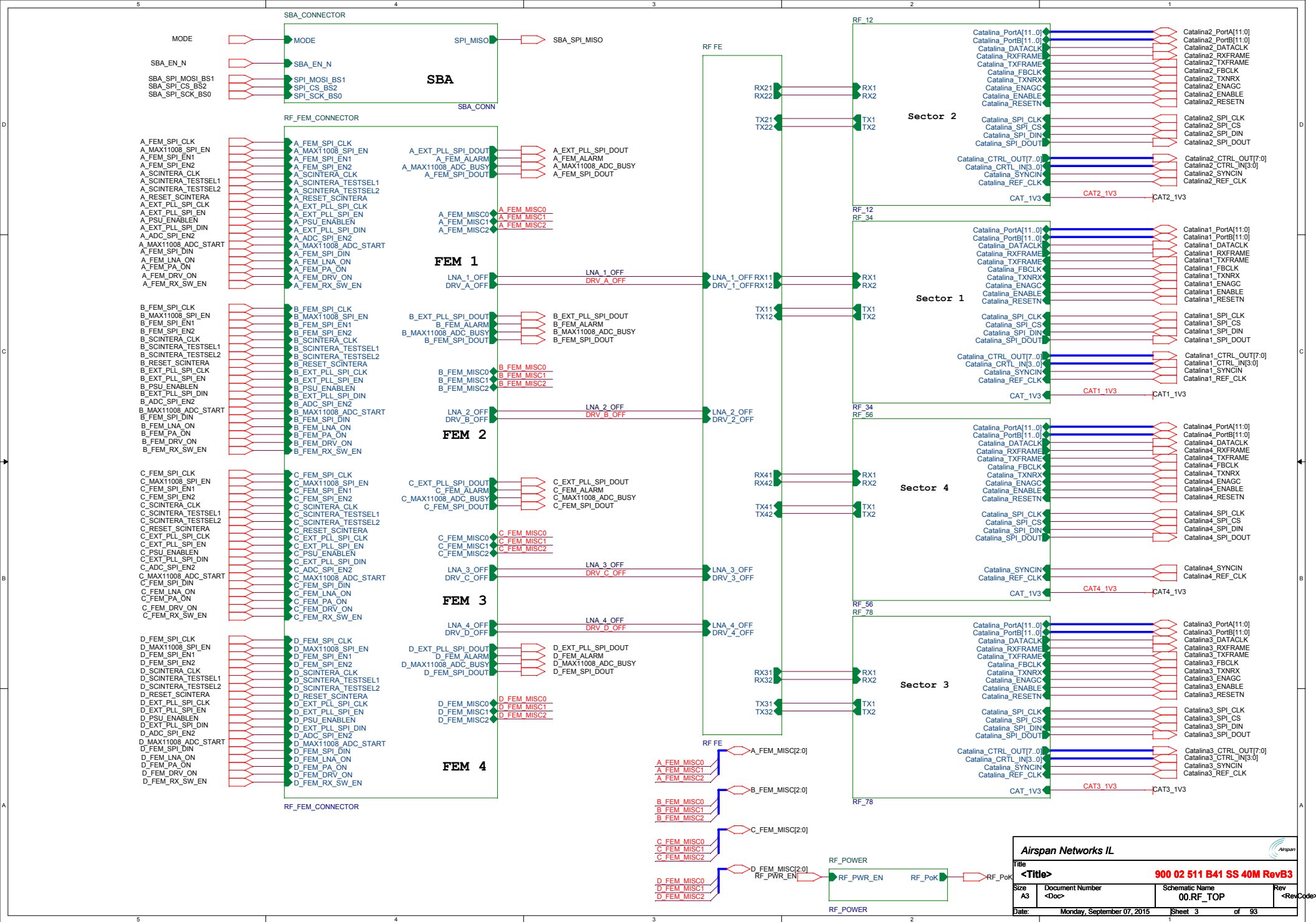
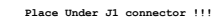


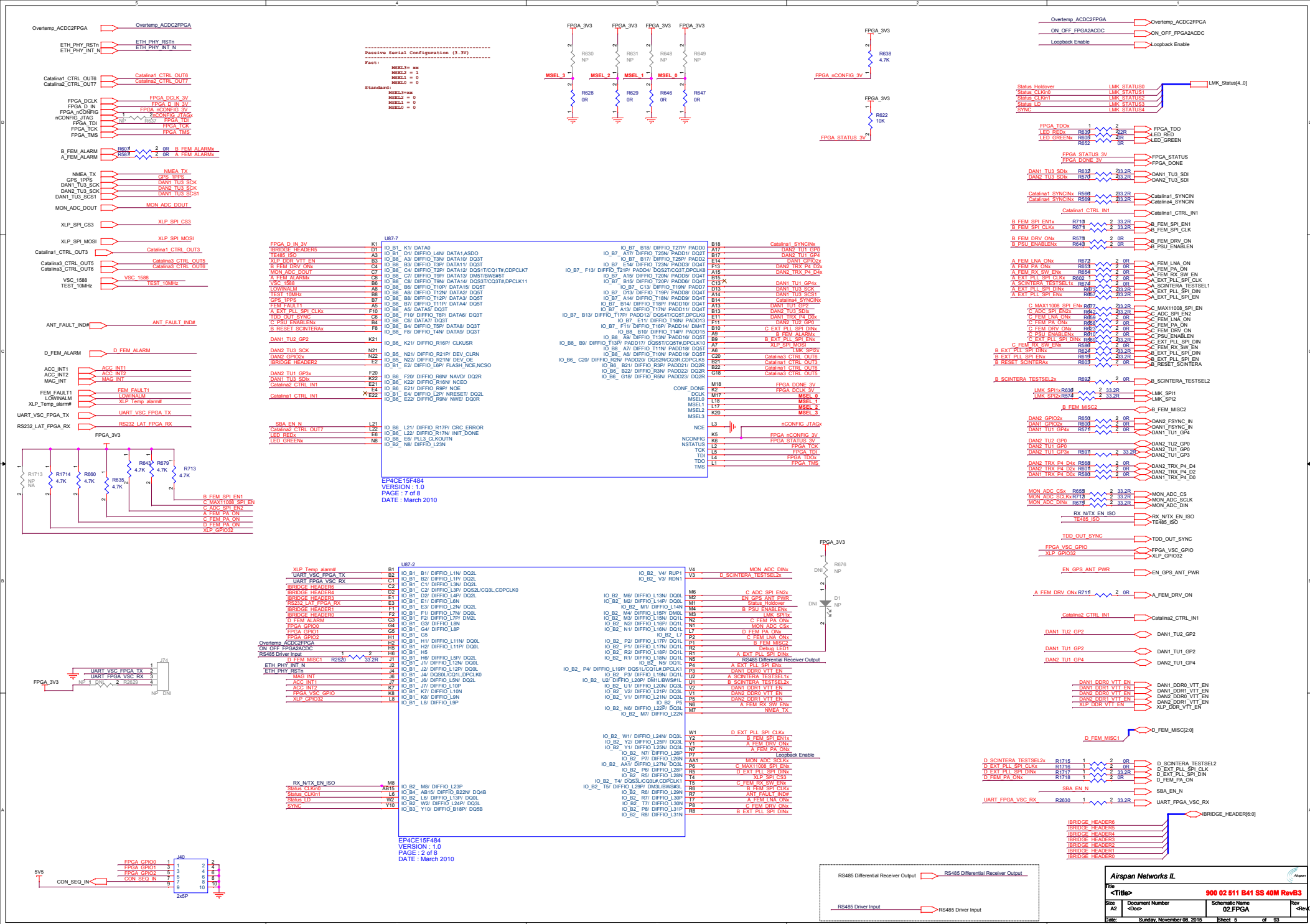


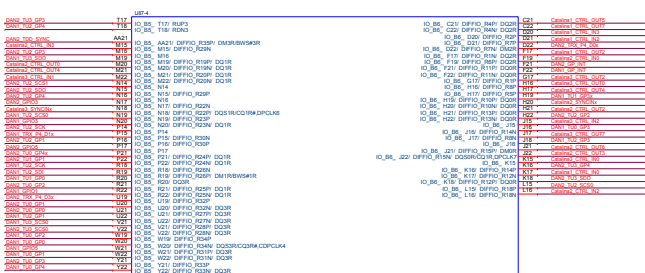
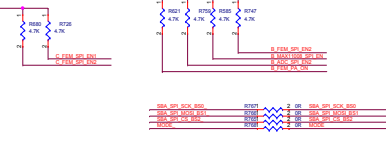
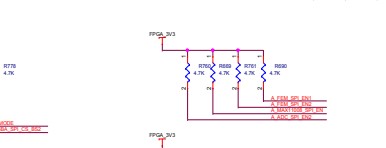
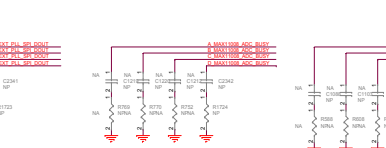
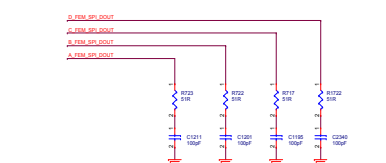
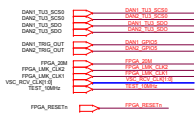
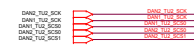
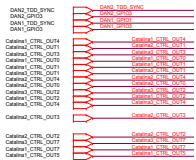




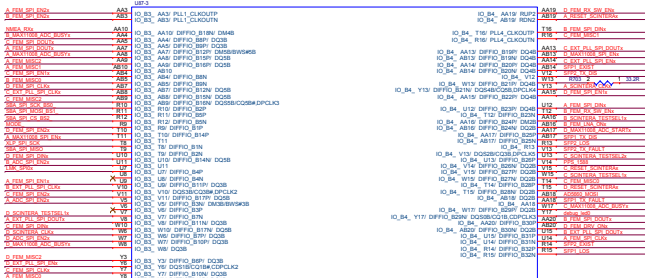
GPS



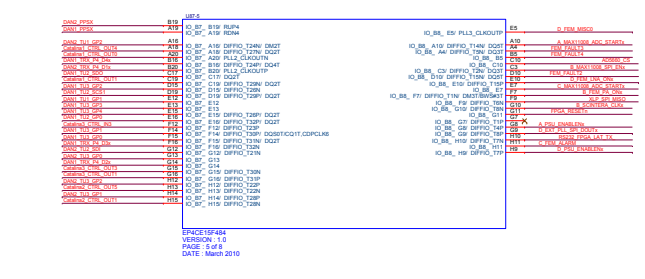




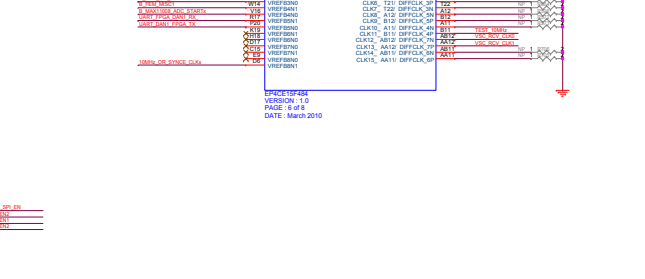
EPIC4T0P484
VERSION 1.0
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DATE March 2010



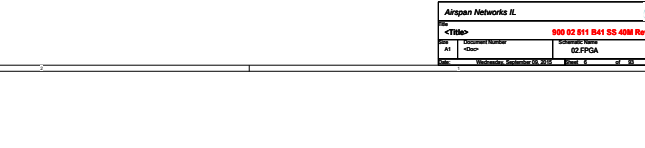
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VERSION 1.0
PAGE 3 of 8
DATE March 2010

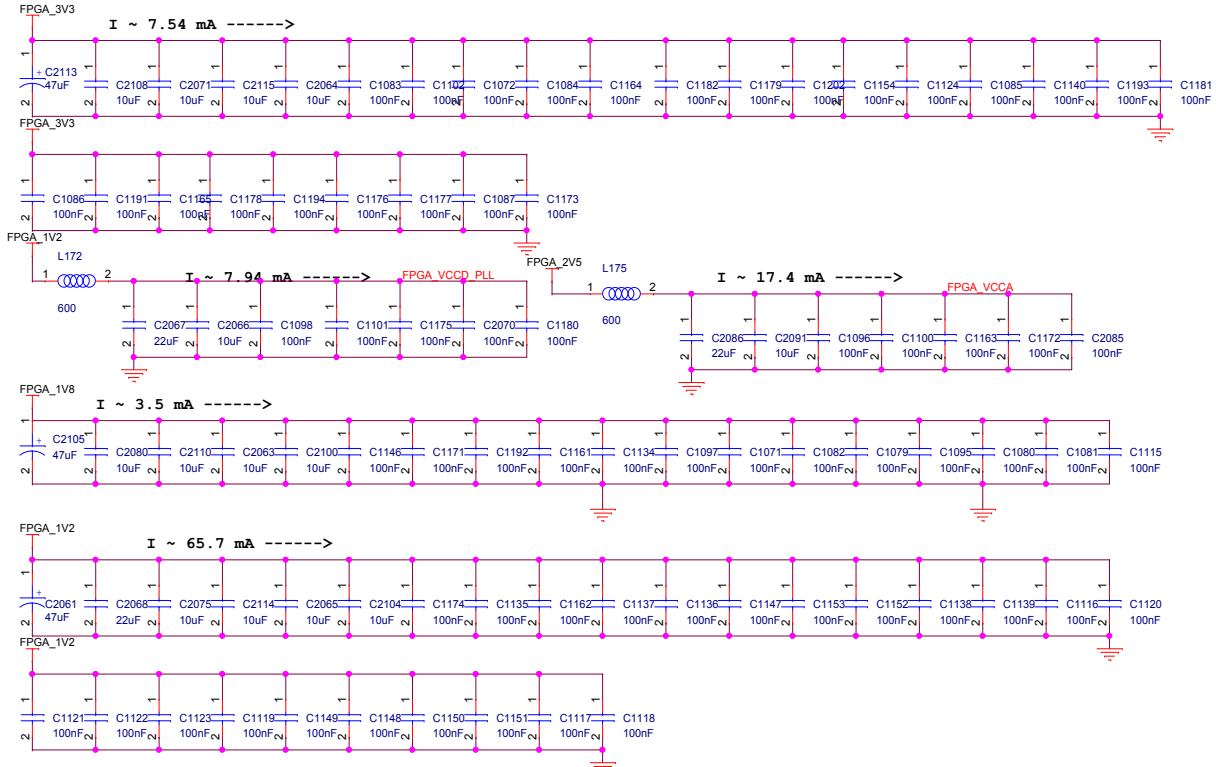
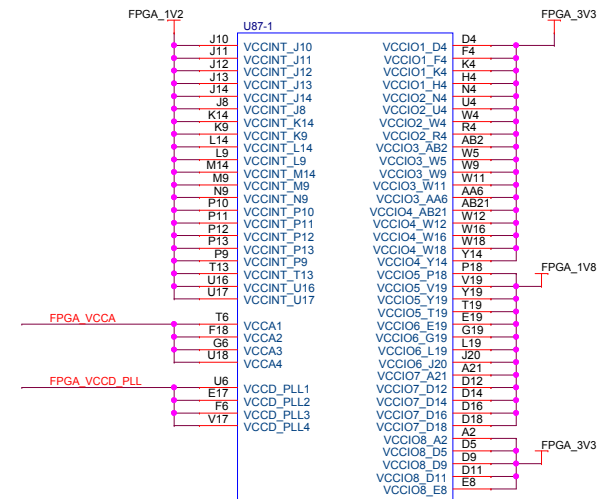
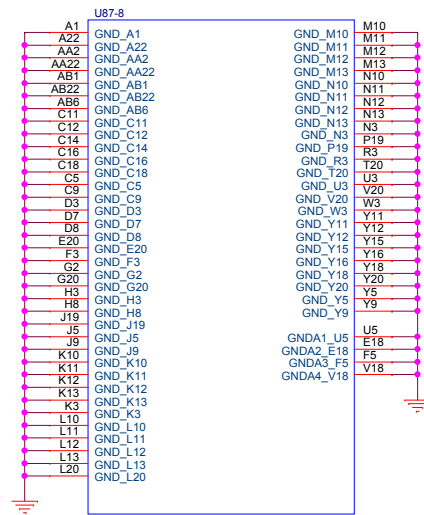


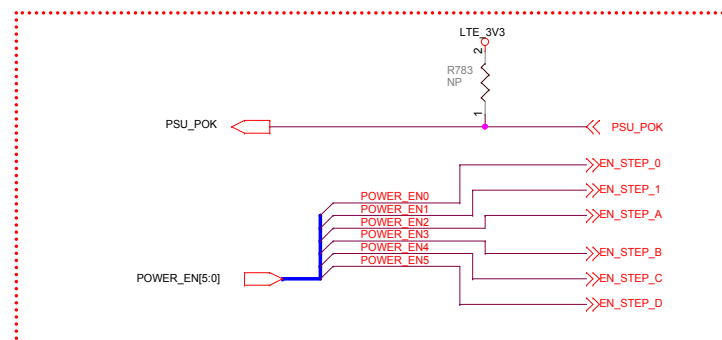
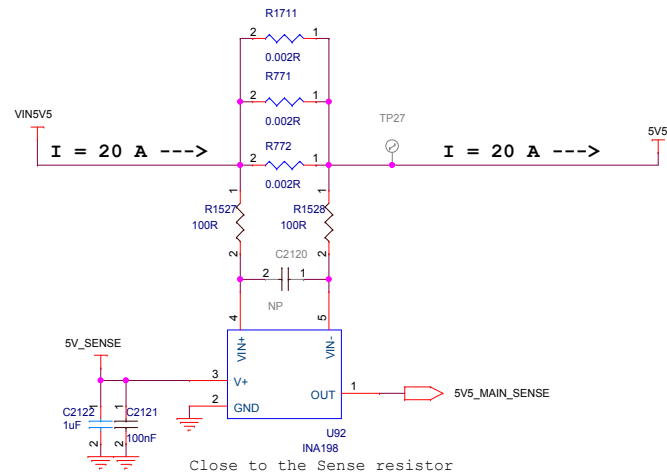
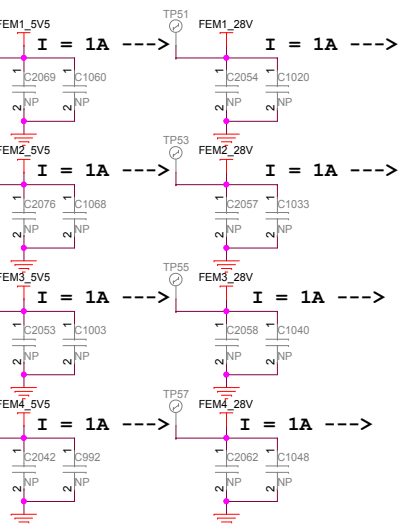
EPIC4T0P484
VERSION 1.0
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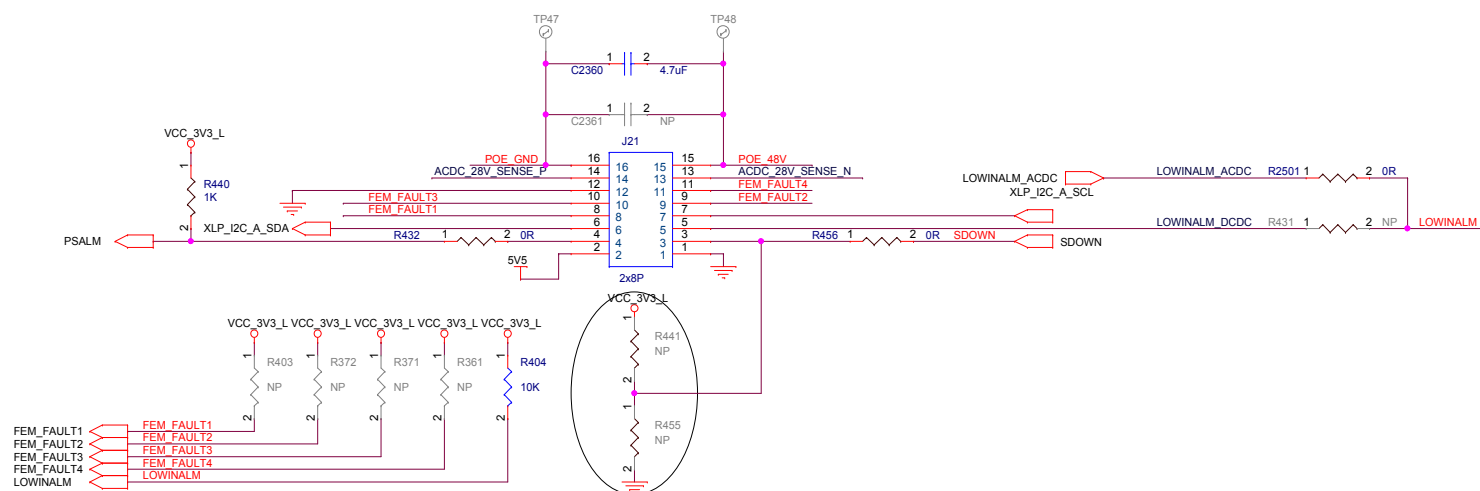
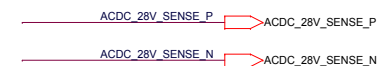
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VERSION 1.0
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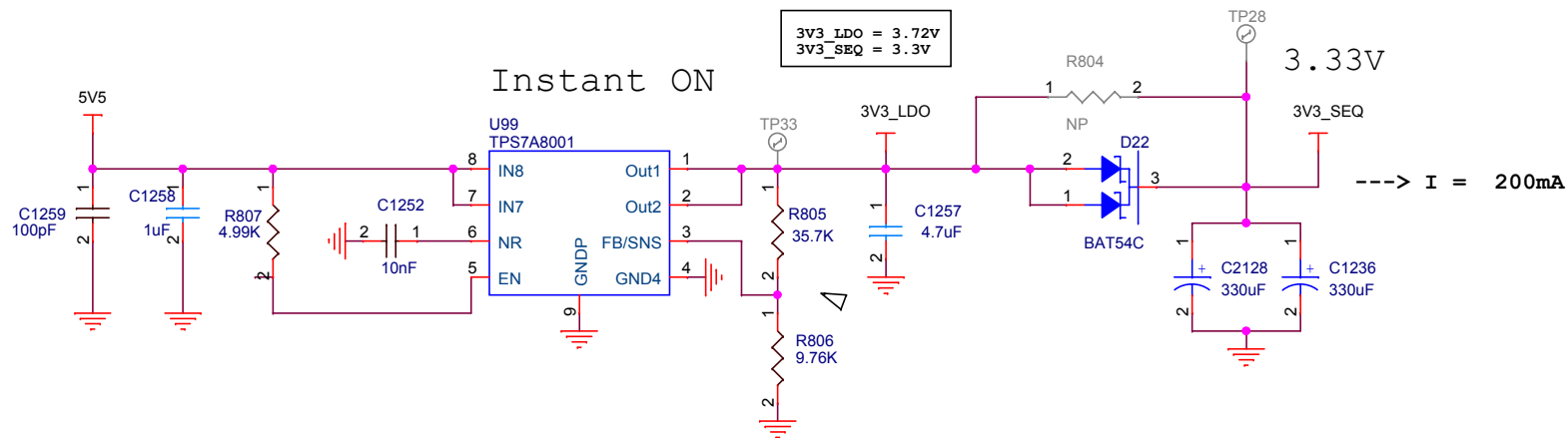




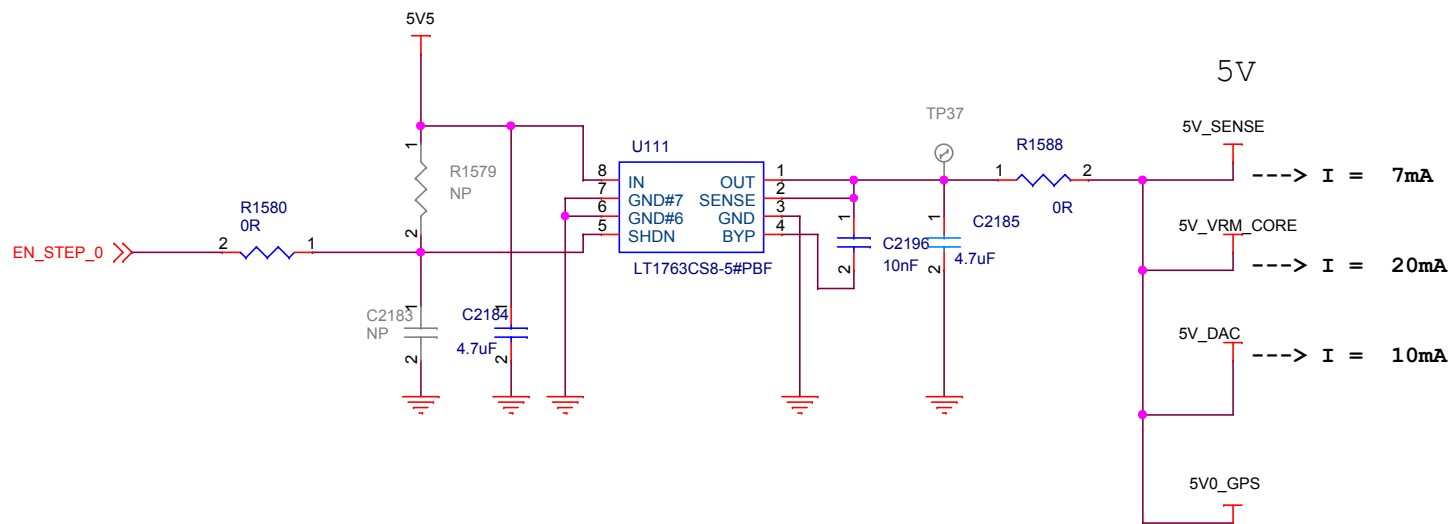


VIN28V FEMs Current is 600 - 700 mA each
VIN5V5 FEMs Current is 1.5A each



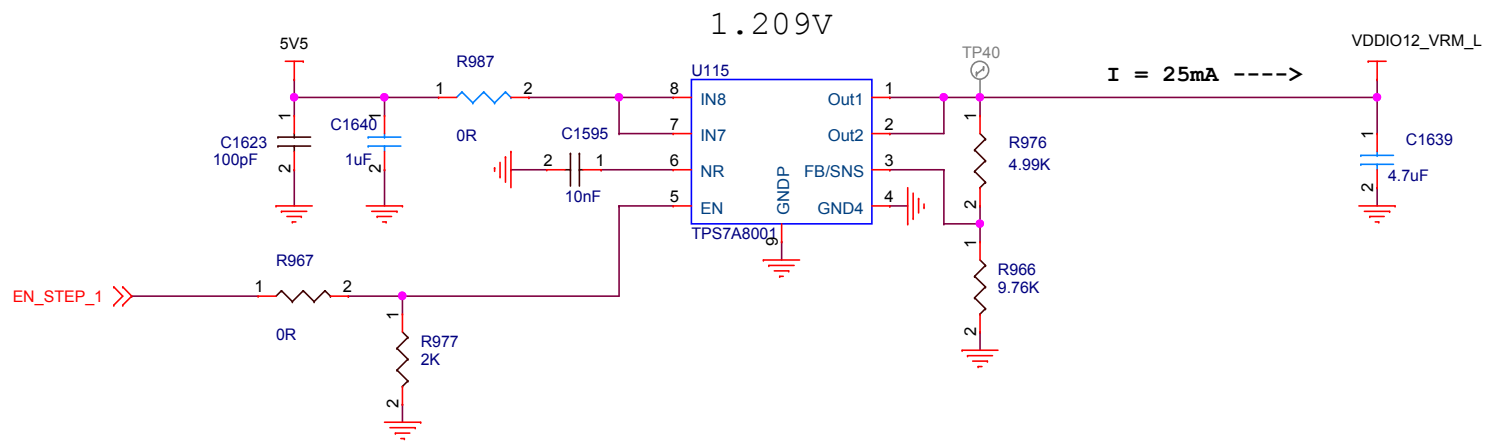


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Size	Document Number	Schematic Name	Rev
A4	<Doc>	04.POWER	<RevCo
Date:	Sunday, September 06, 2015	Sheet 10	of 93

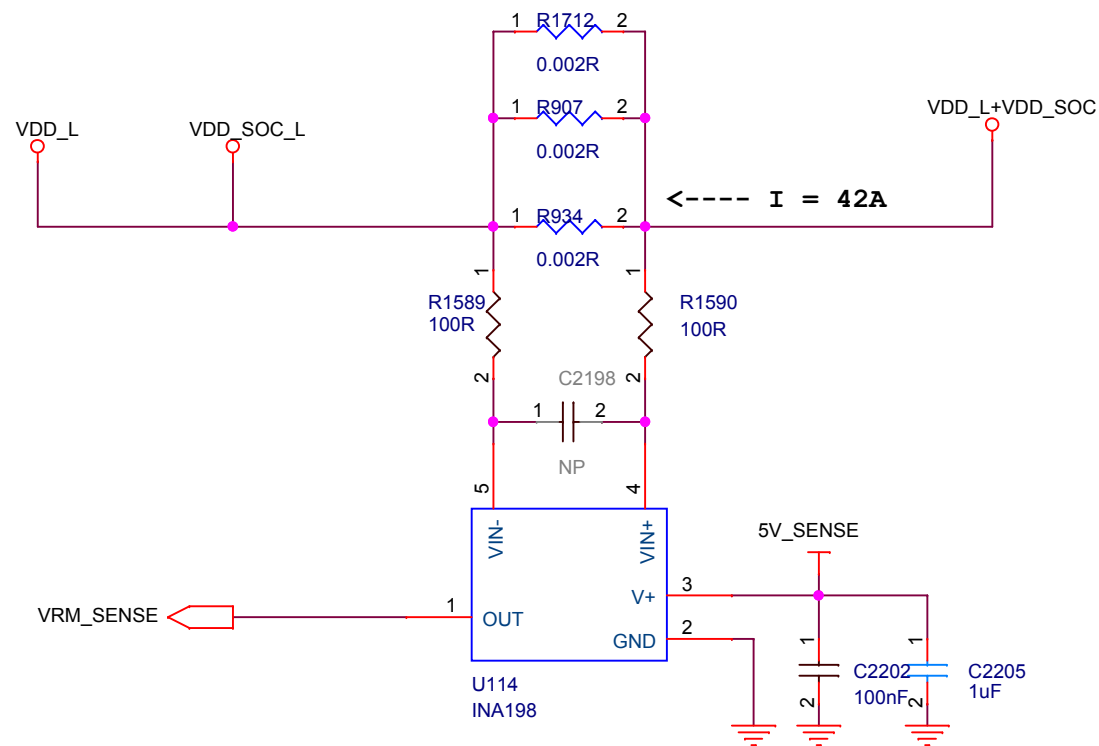


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Size	Document Number	Schematic Name	Rev
A4	<Doc>	04.POWER	<RevCo>
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1 - XLP- VRM CORE



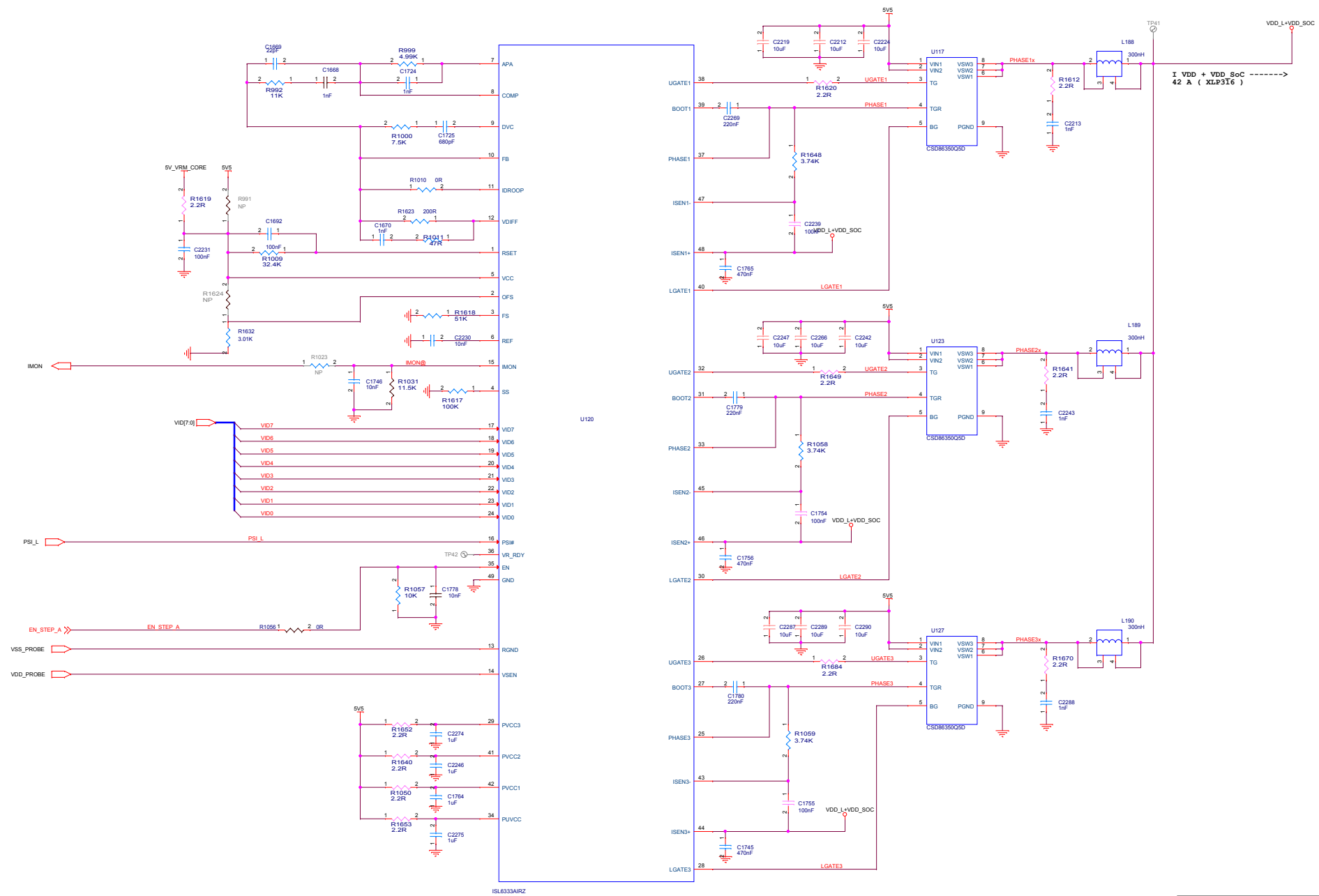
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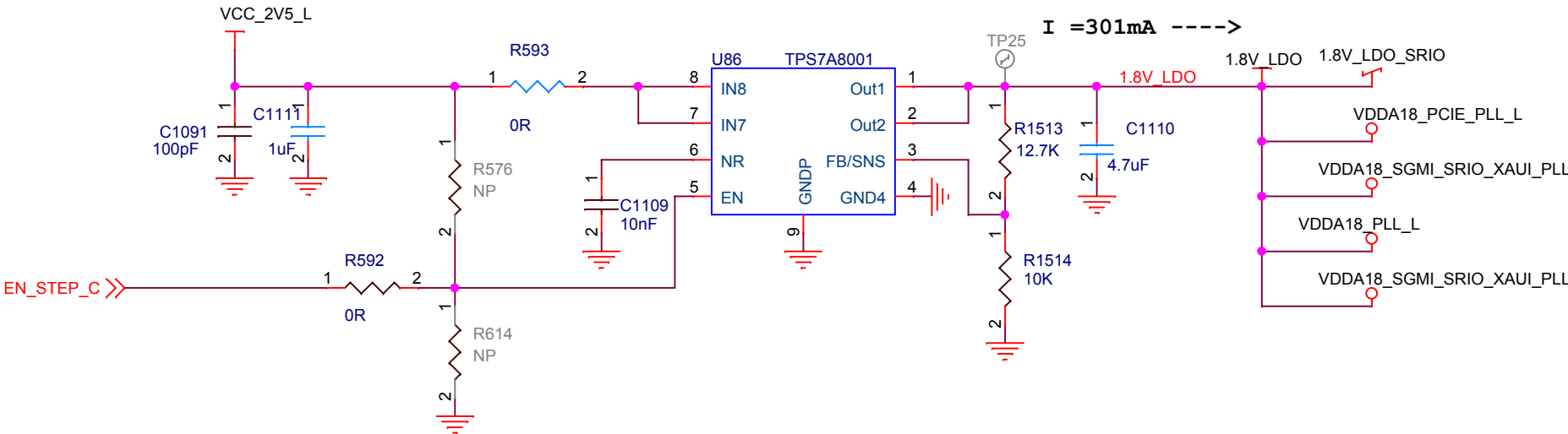
Close to the Sense resistor

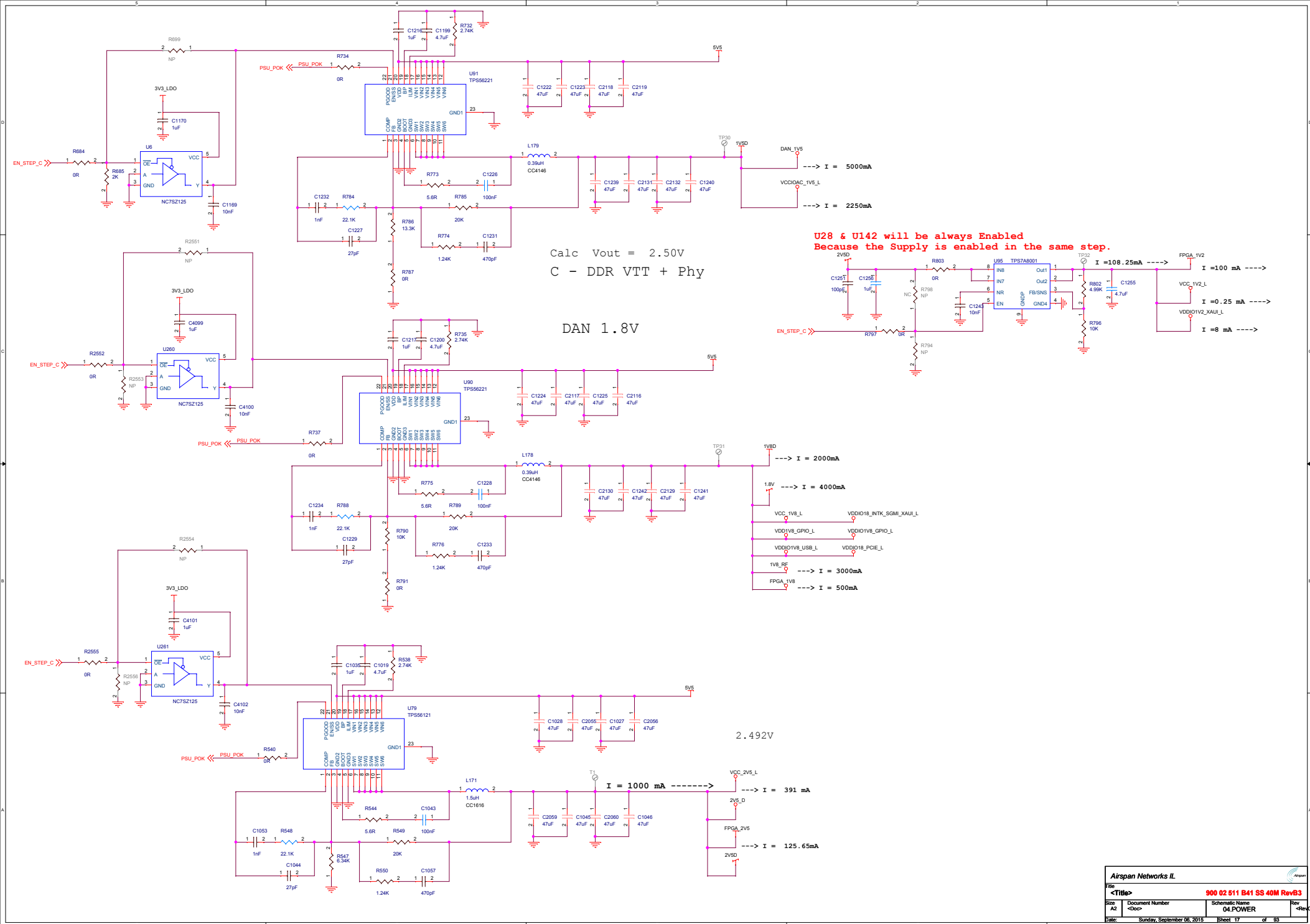
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Size A	Document Number <Doc>	Schematic Name 04.POWER	Rev <RevCo>
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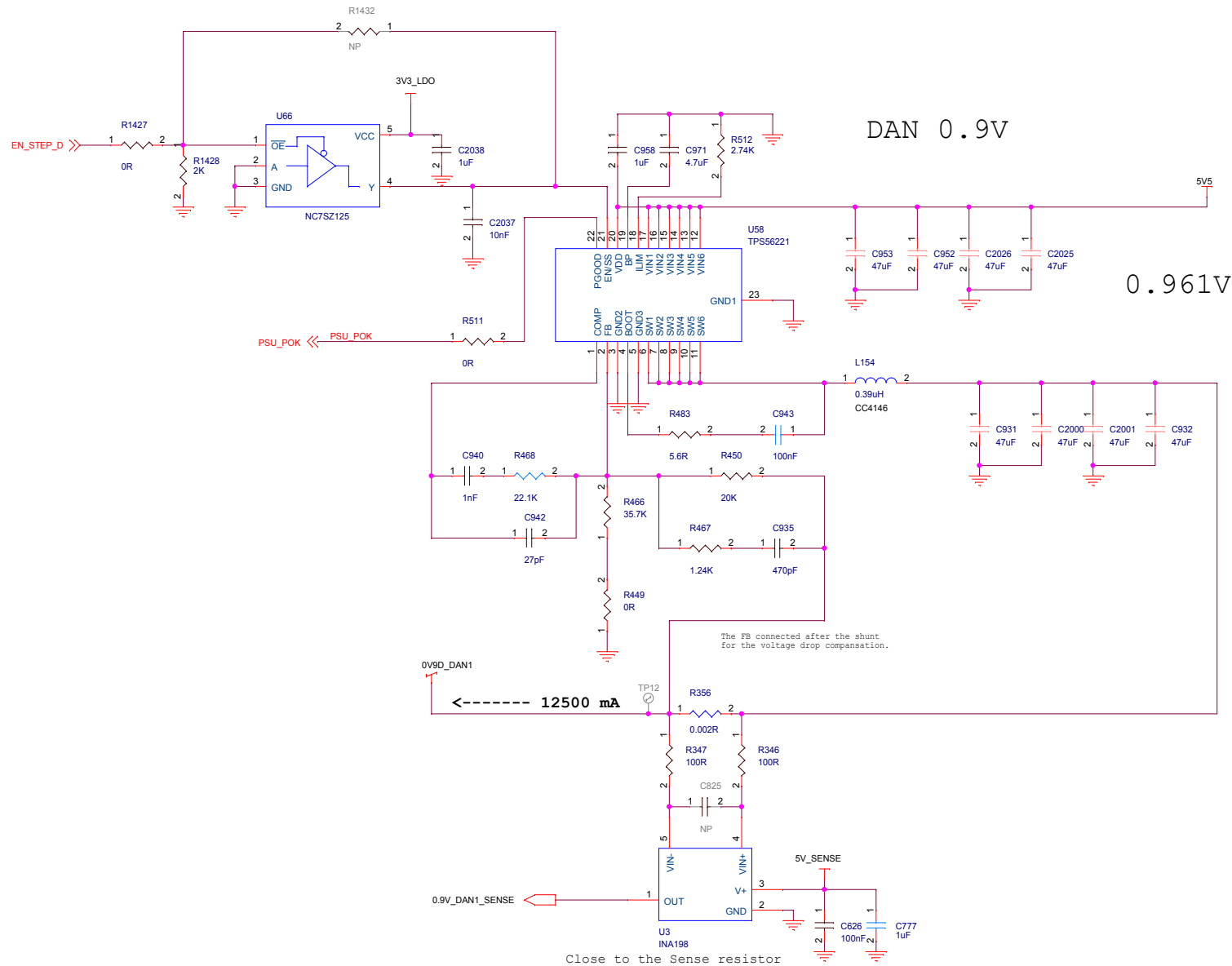
VRM - VDD_SoC & VDD_L



C - LDO 1.8V





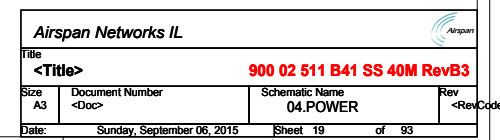


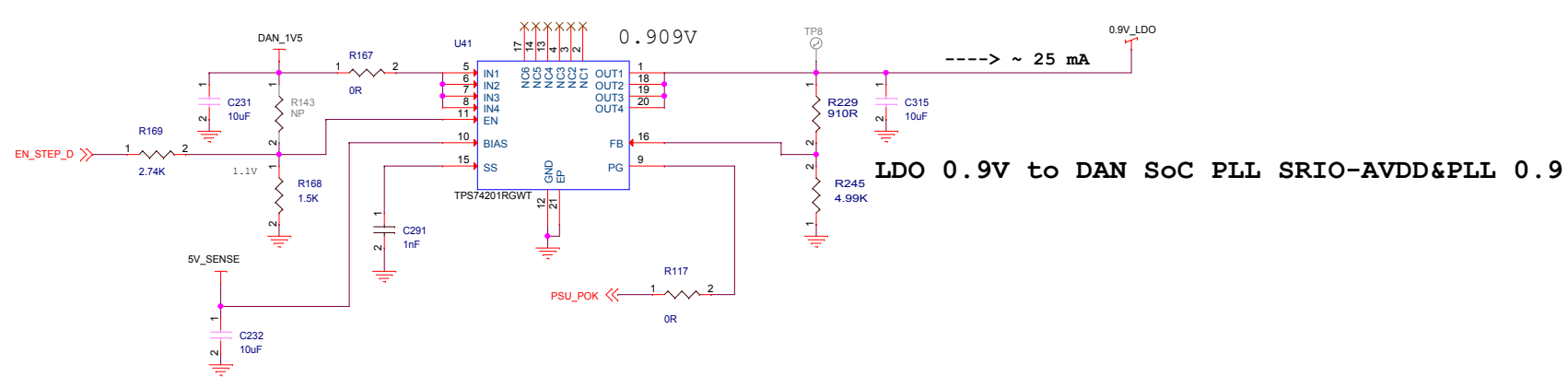
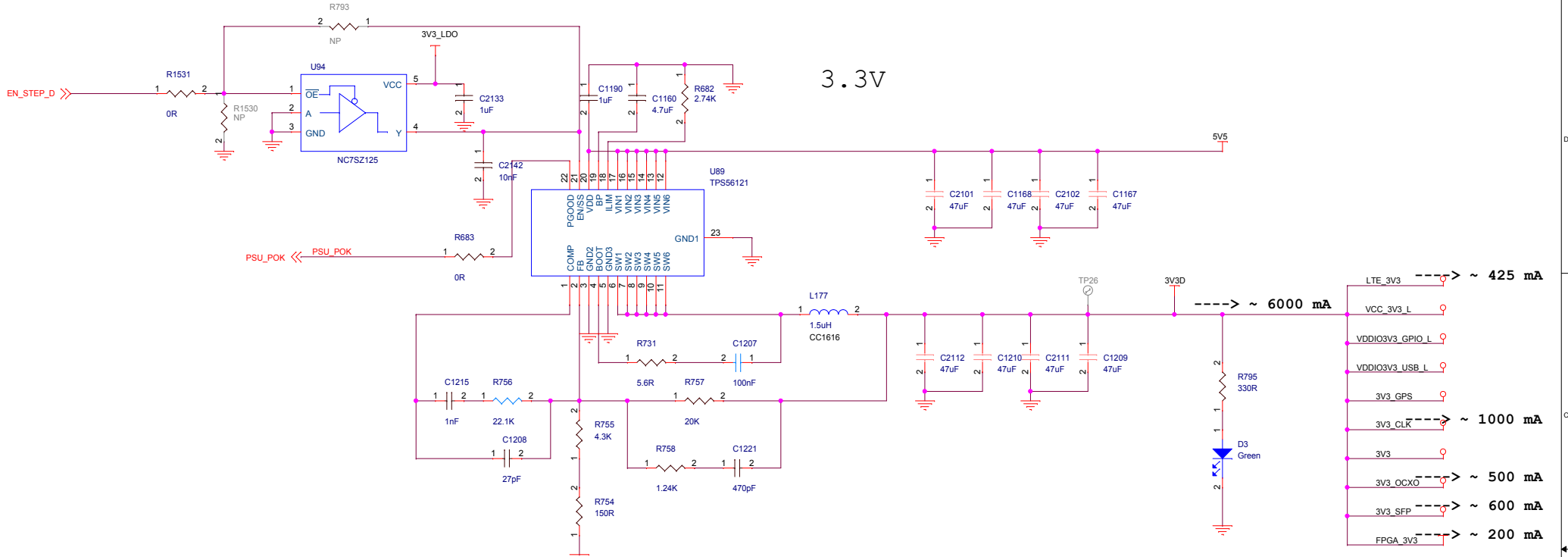
Airspan Networks IL

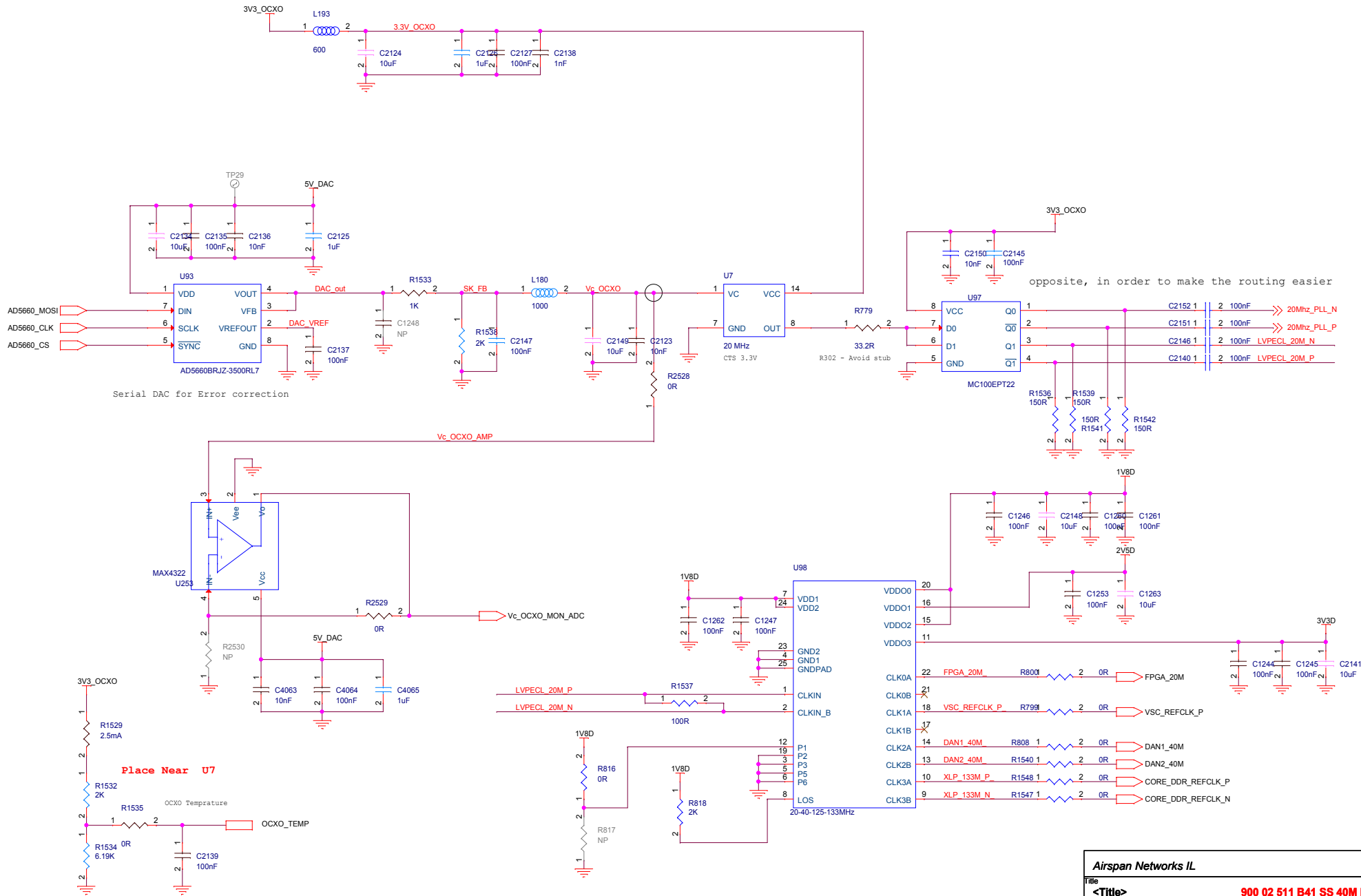
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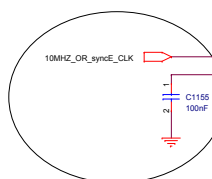
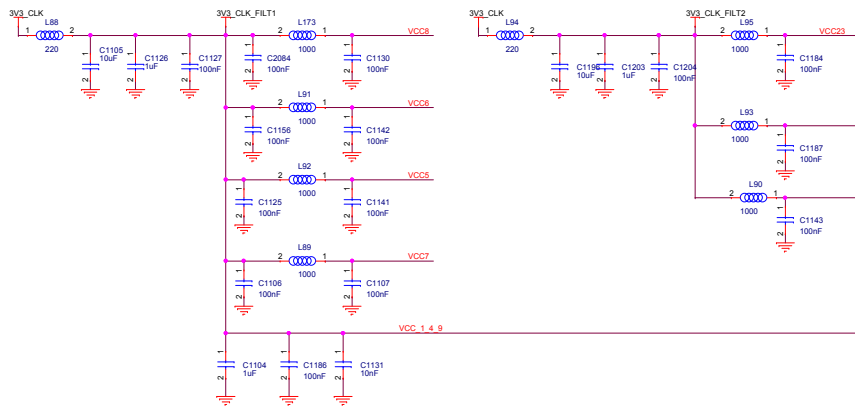
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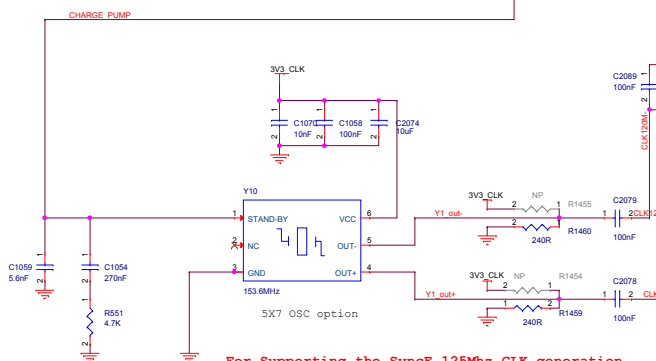




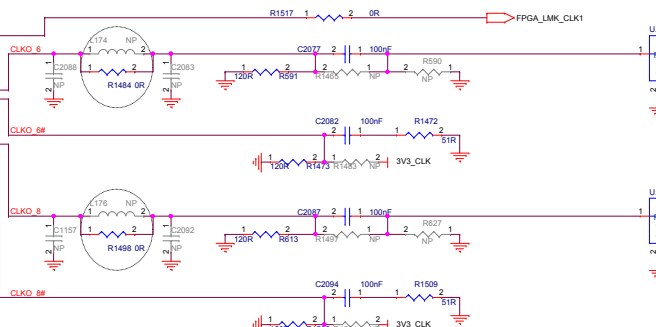
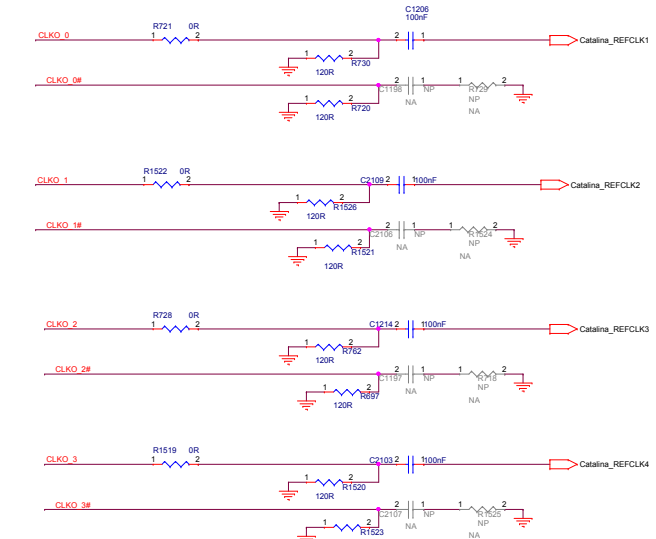
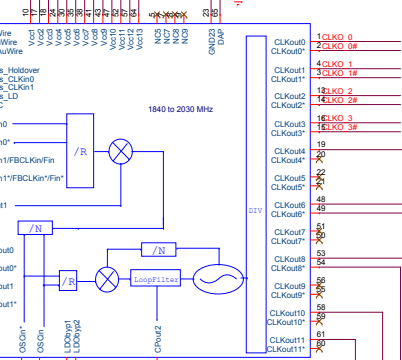




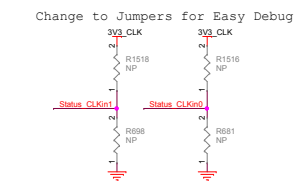
Check if termination is needed ???



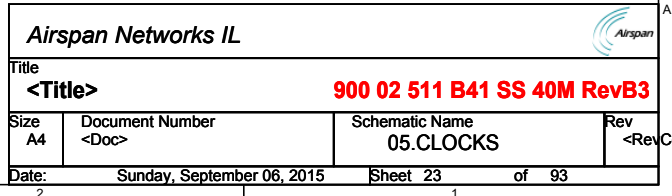
For Supporting the SyncE 125MHz CLK generation
The VCXO need to be changed to 125Mhz!!



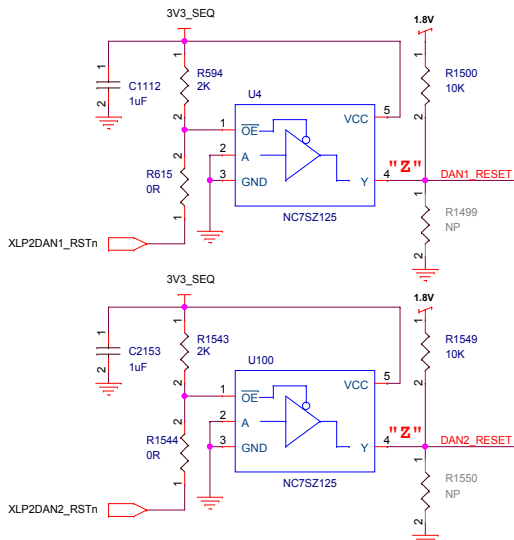
Check if termination is needed ???



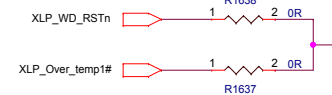
Status_CLKin1	Status_CLKin0	Active Clock
0	0	CLKin0
0	1	CLKin1
1	0	Reserved
1	1	Holdover



THE DAN RESET LINE
MUST BE DEFINED IN THE SEQUENCER AS
ACTIVE LOW OPEN DRAIN !!!

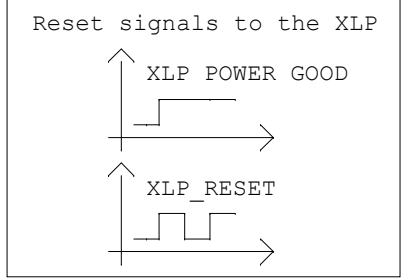
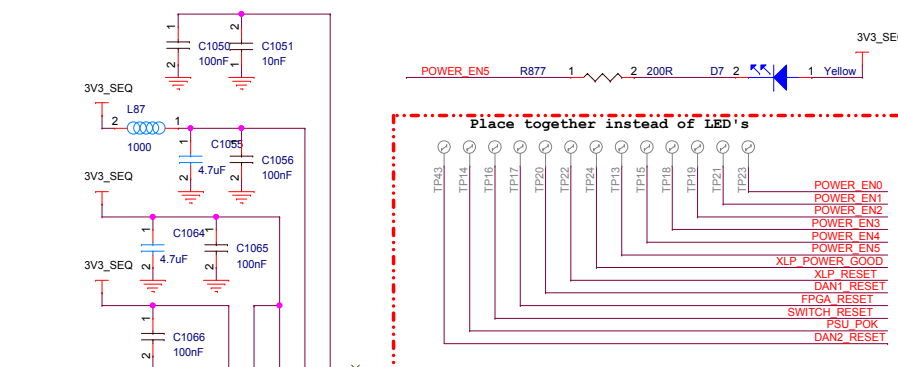
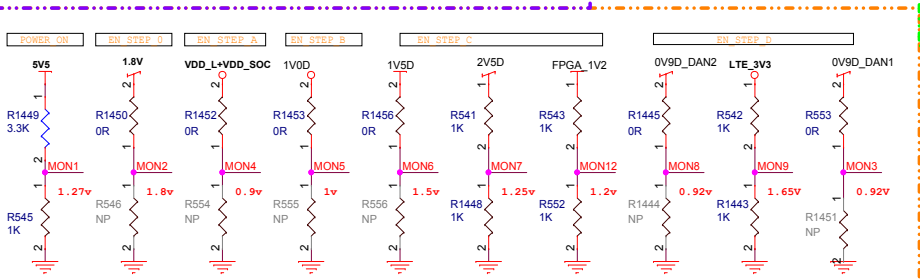
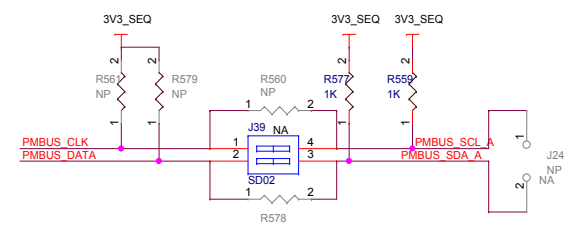


XLP Reset sequence need to be triggered
when XLP watchdog is expired or XLP is over heated.

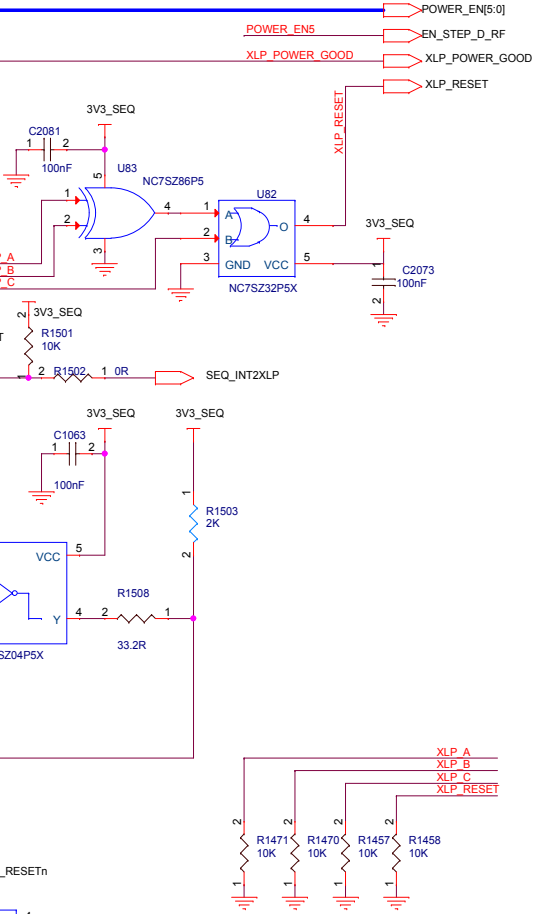
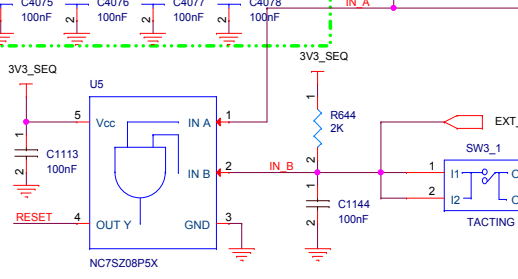
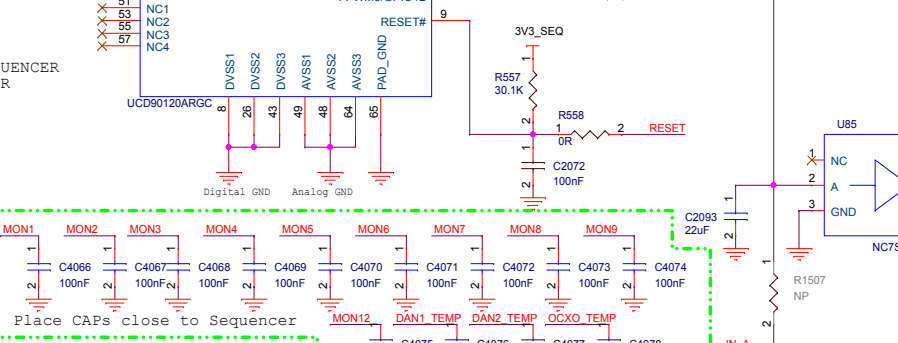
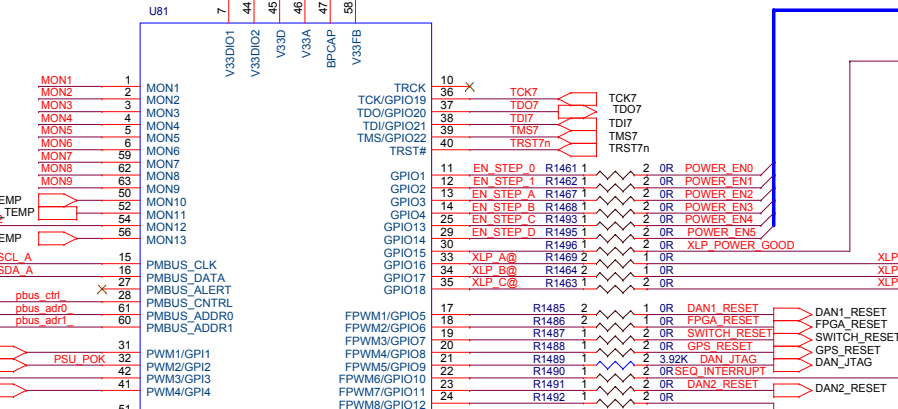


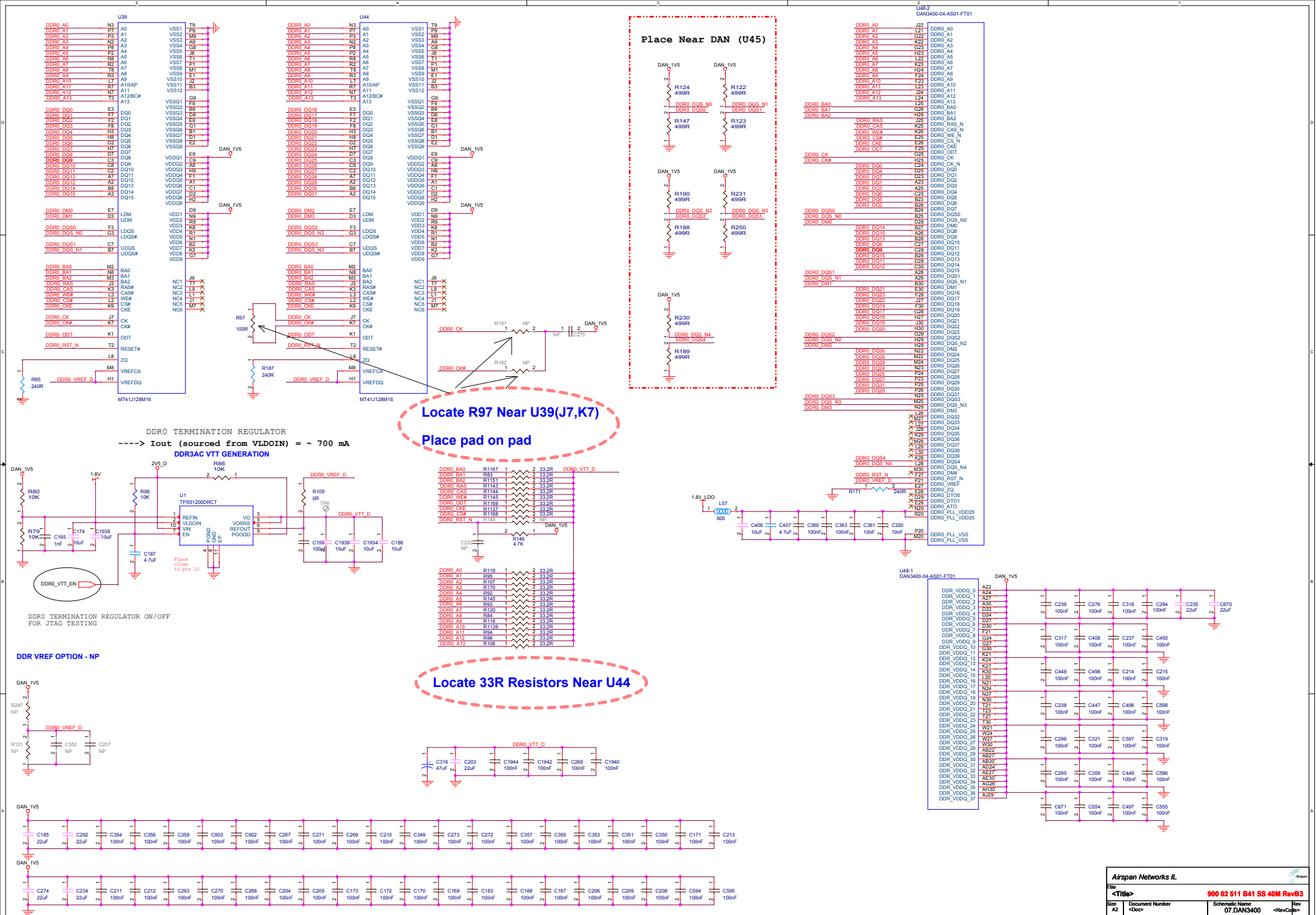
X_PMBUS_CLK
X_PMBUS_DATA

OPTION TO BURN THE SEQUENCER
FROM EXTERNAL CONNECTOR



The RF power supplies
will be enabled in step D





Place Near DAN (U45)

Locate R97 Near U39(J7,K7)

Place pad on pad

Locate 33R Resistors Near U44



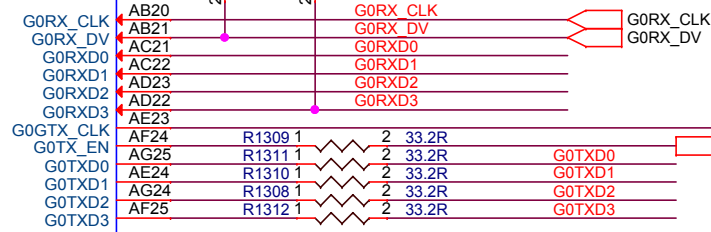
G0RXD[3:0]  G0RXD[3:0]
G1RXD[3:0]  G1RXD[3:0]

RGMII Ethernet Port

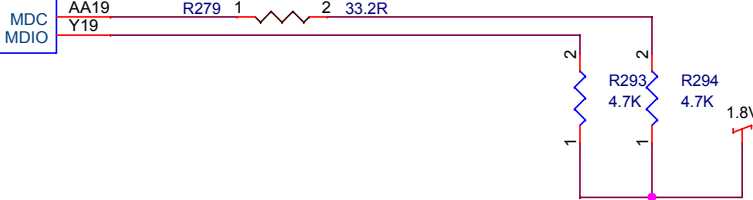
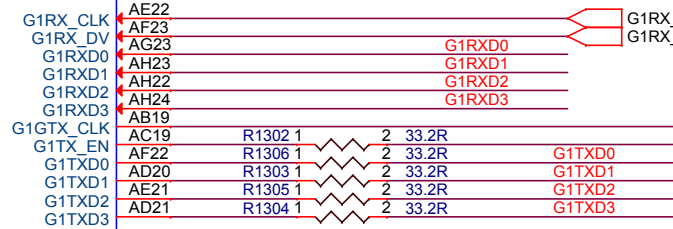
Avoid stub! R535 R536

G0TXD[3:0]  G0TXD[3:0]
G1TXD[3:0]  G1TXD[3:0]

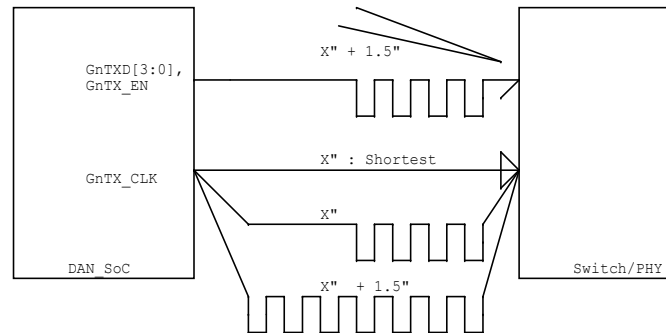
U48-4
DAN3400-04-AS01-FT01



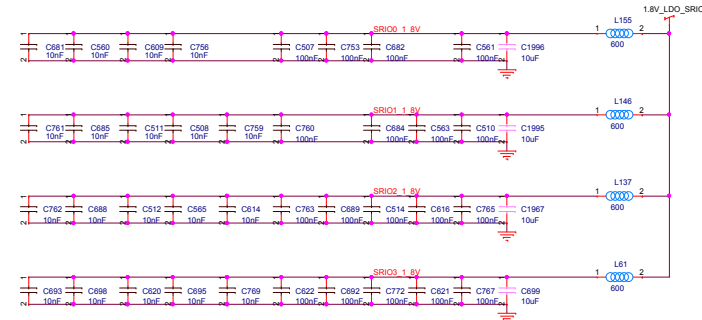
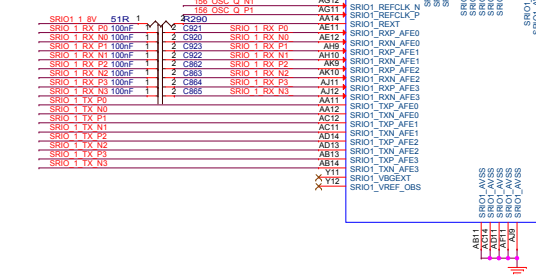
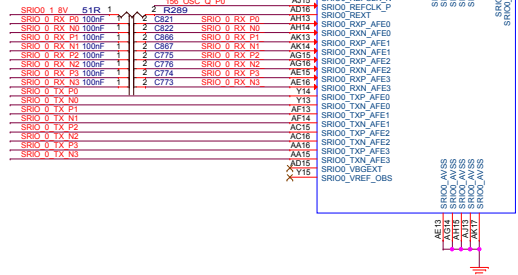
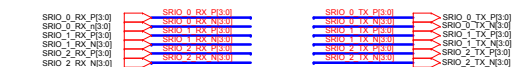
 PAD ON PAD

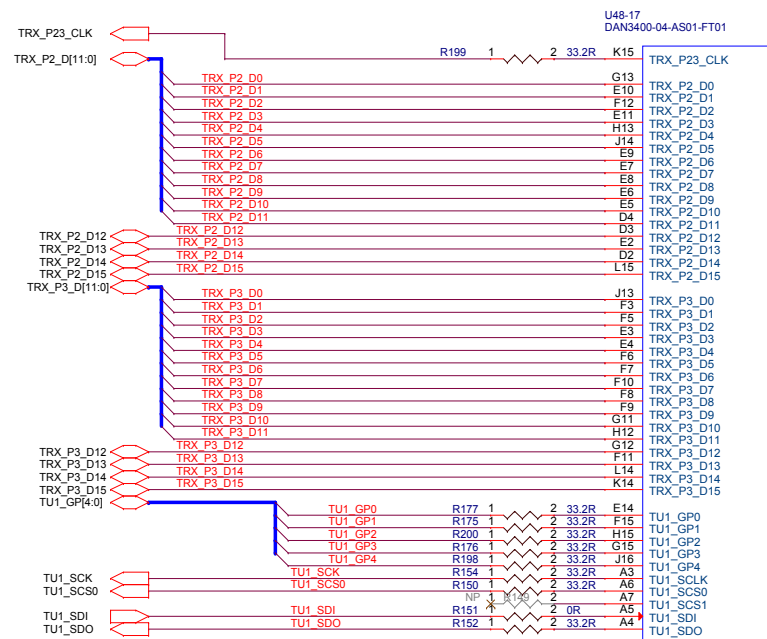
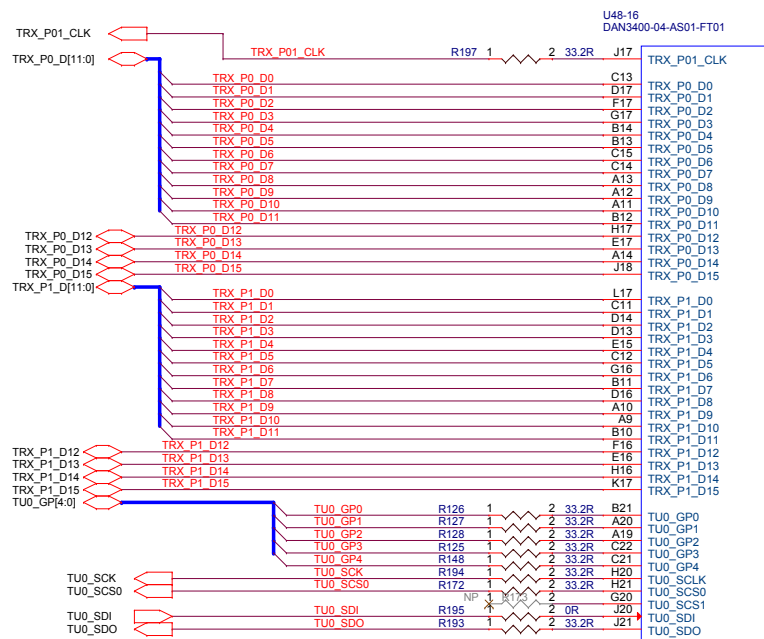


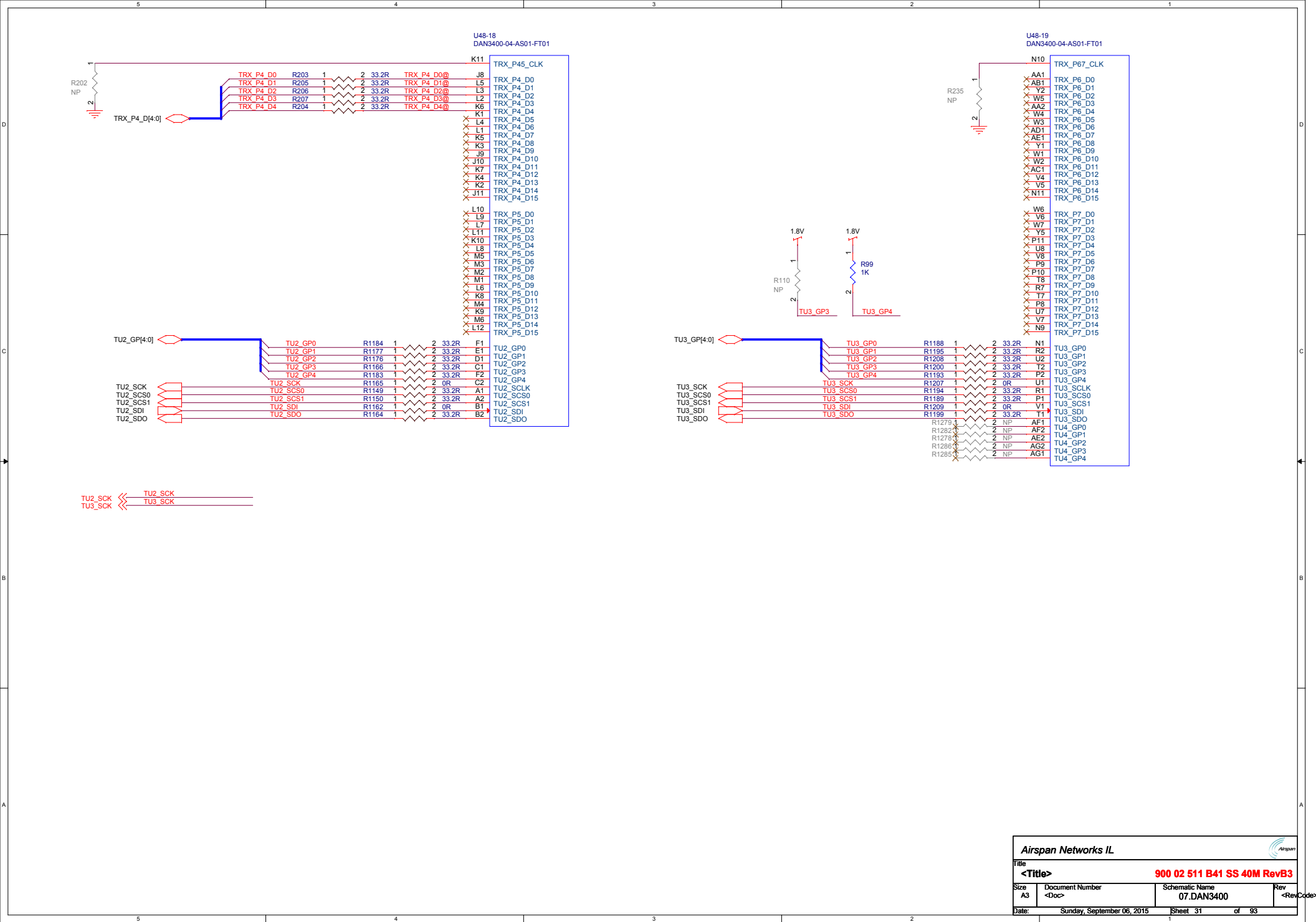
RGMII_TX layout

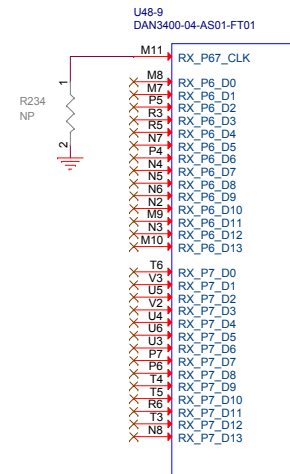
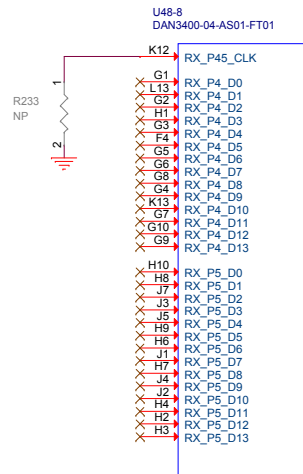
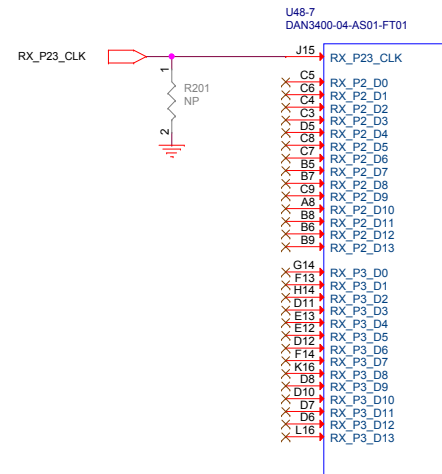
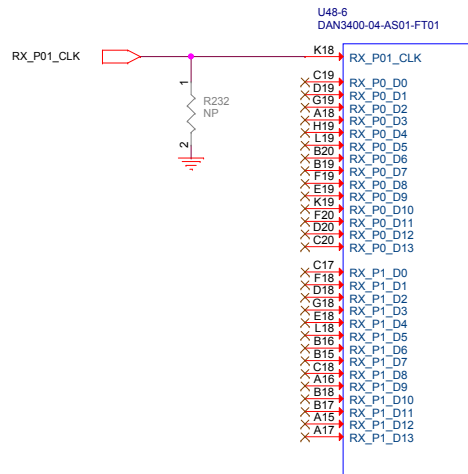


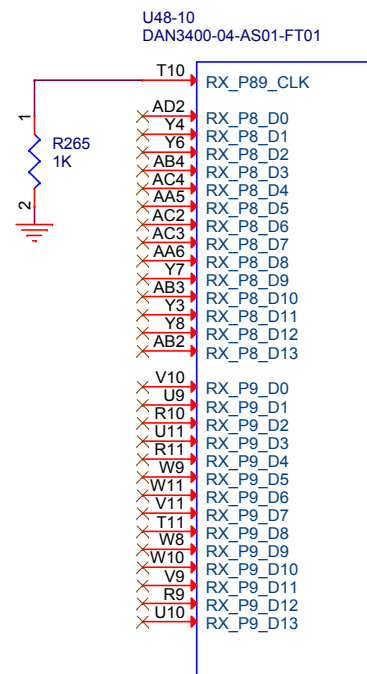
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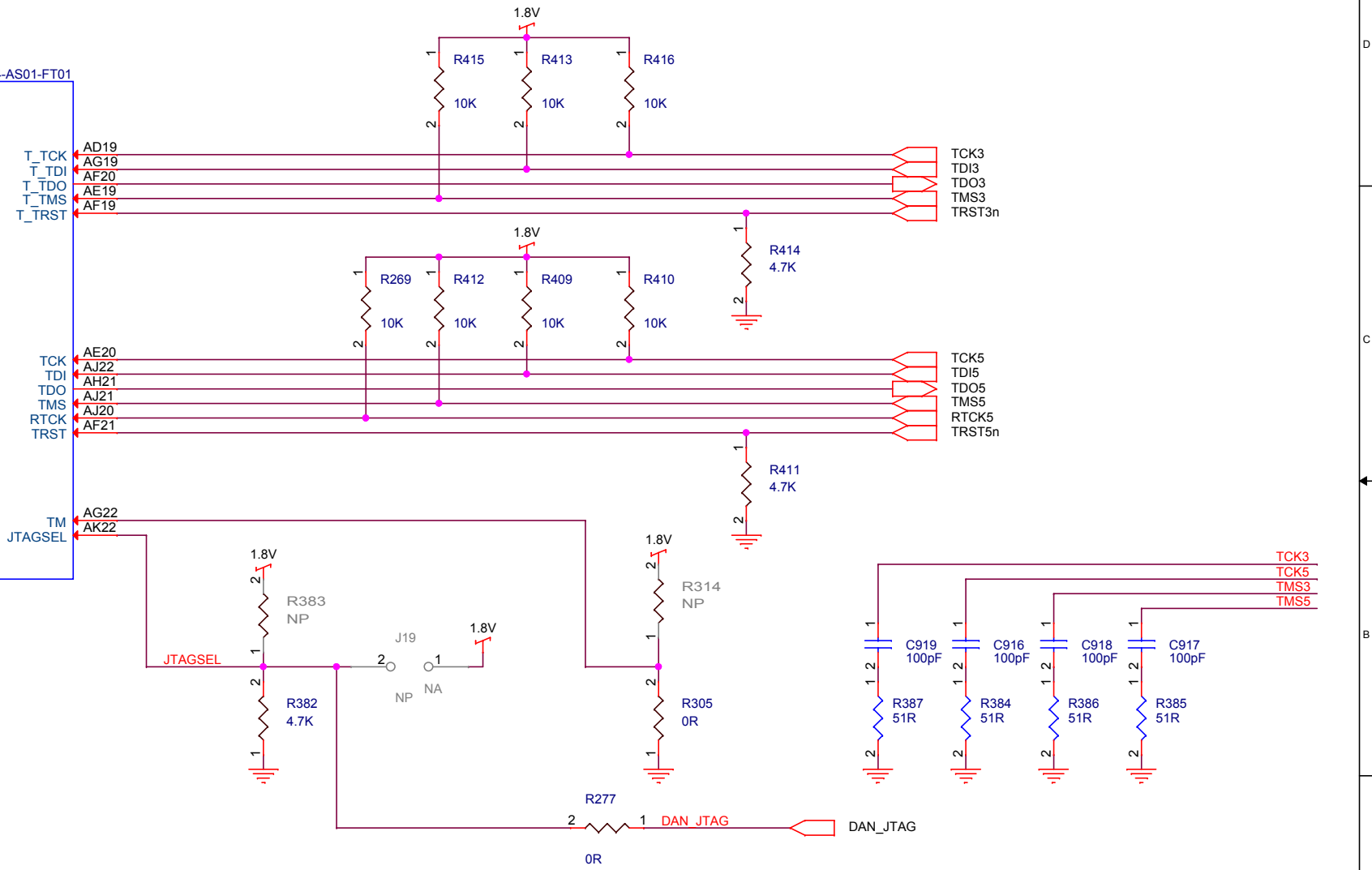






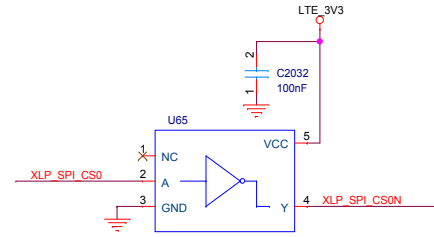
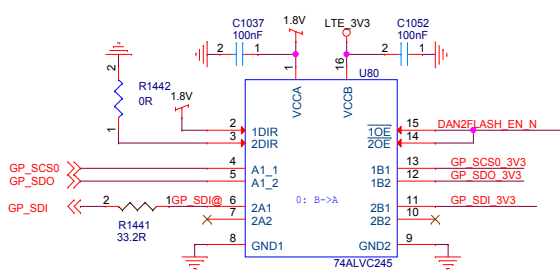
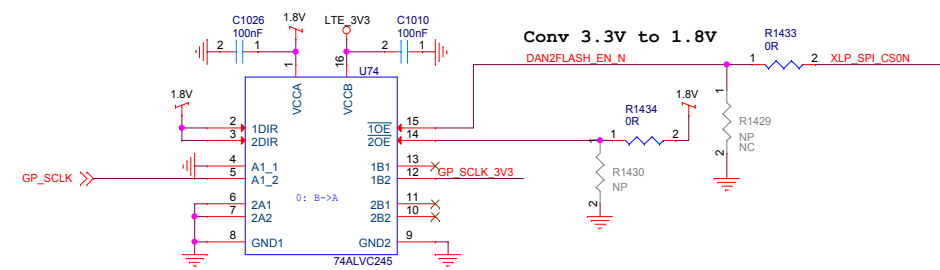
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Date: Thursday, September 03, 2015 Sheet 34 of 93			

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DAN3400-04-AS01-FT01



Airspan Networks IL			
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A4	<Doc>	07.DAN3400	<RevCo
Date: Sunday, September 06, 2015			
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If the flash is Burnt externally the I/Os became 3-State

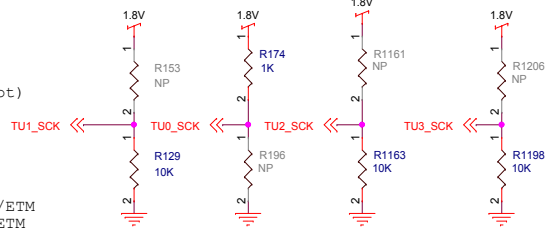


BOOT OPTIONS:
1, 0:

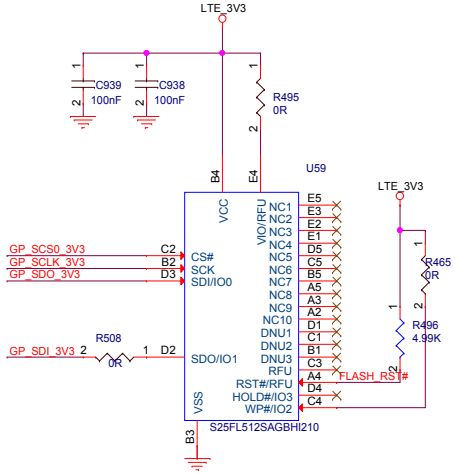
{TU1_SCLK, TU0_SCLK} = 00 -> ARM0
{TU1_SCLK, TU0_SCLK} = 01 -> RX DSP0
{TU1_SCLK, TU0_SCLK} = 10 -> TX CPU0 (Secured boot)
{TU1_SCLK, TU0_SCLK} = 11 -> TX CPU0 (Secured boot)
2:

0 - ETM/ETB is not part of the JTAG scan chain
1 - ETM/ETB is part of the JTAG scan chain
3:

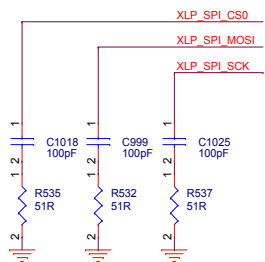
0 - ETB is in the JTAG scan chain before the ARM/ETM
1 - ETB is in the JTAG scan chain after the ARM/ETM



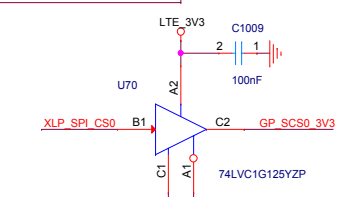
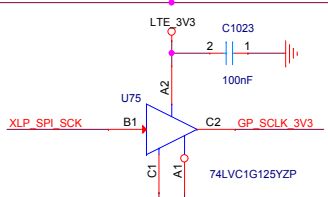
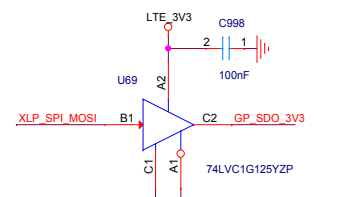
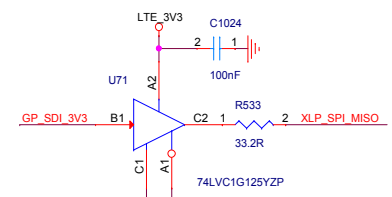
BANK 0 (CS0)



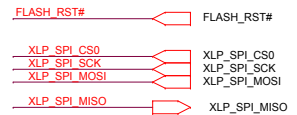
PLACE AT THE END OF SPI BUS DAISY-CHAIN



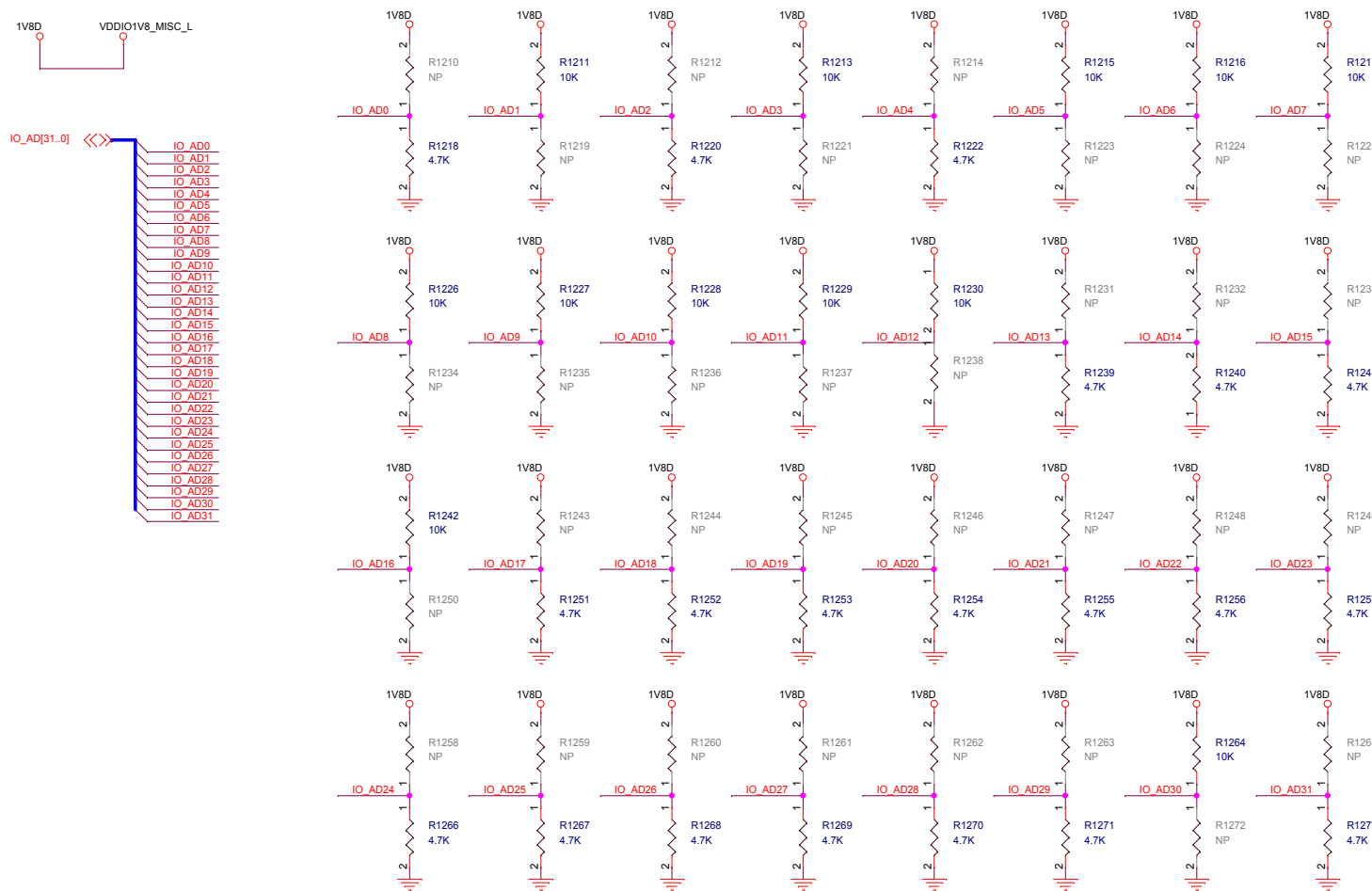
OPTION for burning the Flash from XLP
(The output is in 3 state by default)



Common SPI bus to FLASH, FPGA, XLP and XLP_UARTB



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Size			
A3			
Document Number		Schematic Name	
<Doc>		07.DAN3400	
Date:		Rev	
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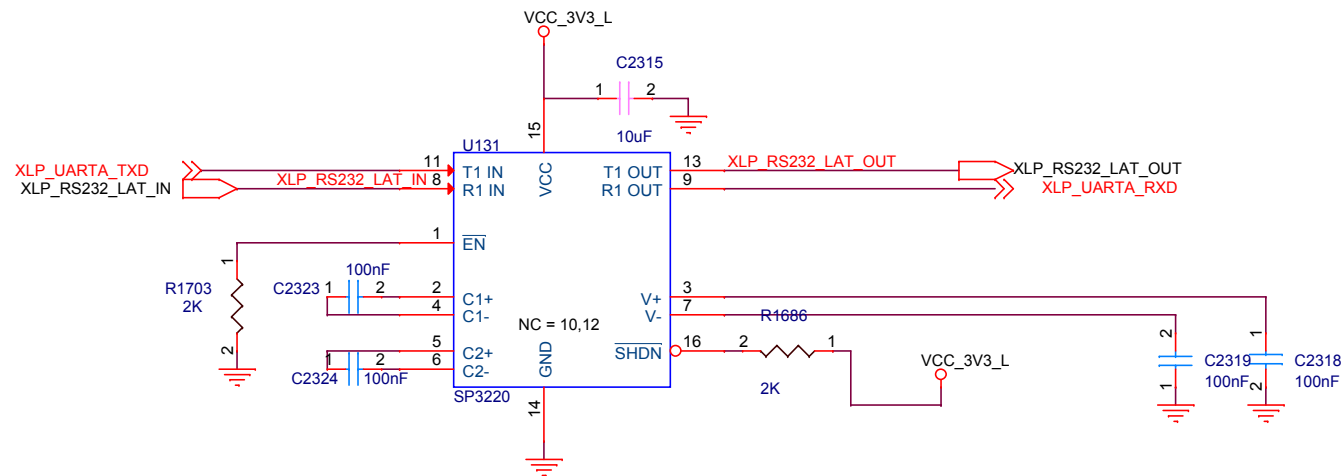
1200 Mhz
Doc No:
11027V141DB-CR 10/2/12

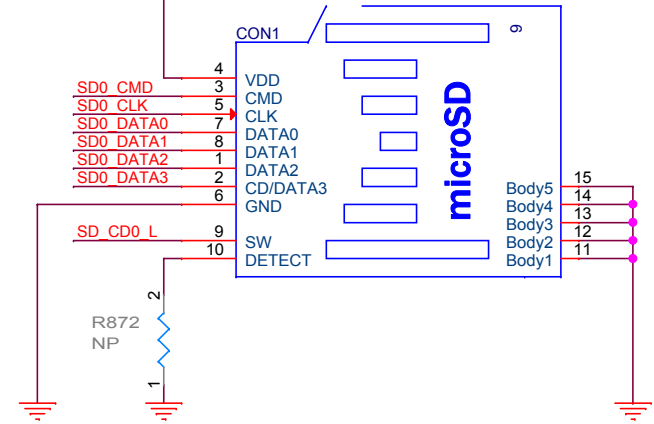
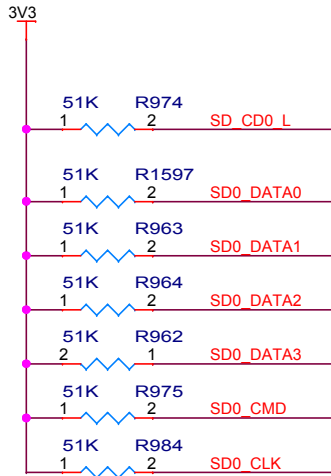
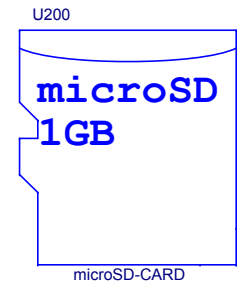
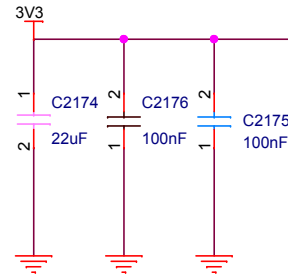
SIGNAL	Description	Pull down = 0 ; Pull up = 1
IO_AD[31:30]	PLL DFS Divider	01 (1200 Mhz)
IO_AD[29:26]	Reserved	Must be set to '0000'
IO_AD25	USB mode	Device set to '0'
IO_AD[24:19]	PCIe mode	All set to '0'
IO_AD[18:17]	CPU DFS divider value	00 (1200 Mhz)
IO_AD[16:10]	Core PLL feedback divider value	1000111 (1200 Mhz)
IO_AD[9:8]	Core PLL feedback reference divider value	11 (1200 Mhz)
IO_AD7	Reserved	Must be set to '1'
IO_AD6	BIST Enable	Enable set to '1'
IO_AD5	Endian Select	BIG set to '1'
IO_AD[4:0]	Boot device Select	SD - 01010

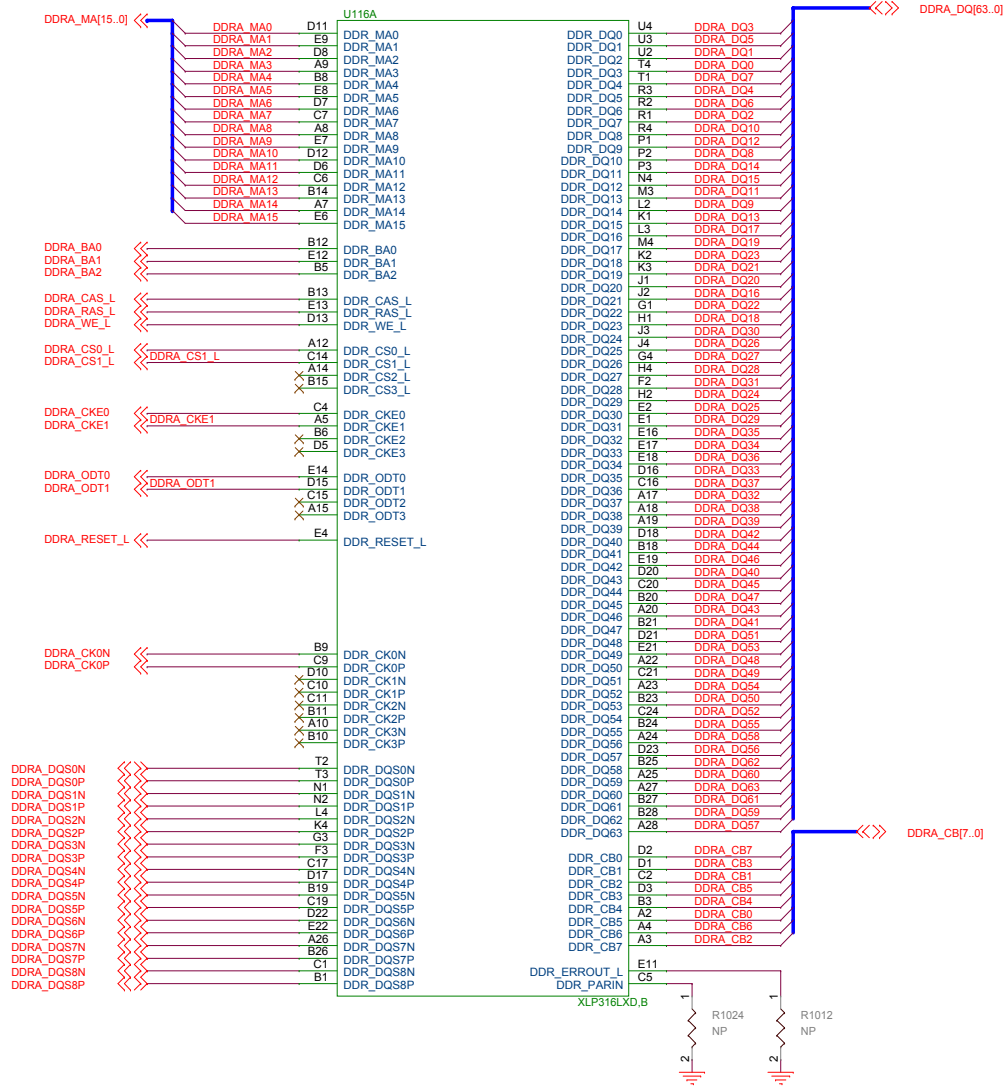
IO_AD[4:0]	Boot device Select
00000	Parallel Nor - non-multiplexed x8: IO_AD[23:0] - Address , DATA = IO_AD[31:24]
00001	Parallel Nor - multiplexed x8 : IO_AD[31:0] - Address , DATA = IO_AD[7:0]
00010	Parallel Nor - multiplexed x16: IO_AD[31:0] - Address , DATA = IO_AD[15:0]
00011	Parallel Nor - multiplexed x32: IO_AD[31:0] - Address , DATA = IO_AD[31:0]
00100	Parallel Nor - multiplexed x16 - word address adjust
00101	Parallel Nor - multiplexed x32 - word address adjust
00110	Nand - x8
00111	Reserved
01000	SPI Nor
01001	SPI Nand
01010	MMC/SD boot
Other	Reserved

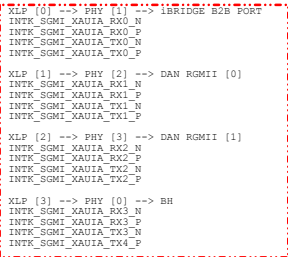
CPU Frequency (MHz)	IO_AD Strapping Pins													
	PLL DFS Divider		CPU DFS Divider		Core PLL Feedback Divider								Core PLL Divider	
	31	30	18	17	16	15	14	13	12	11	10	9	8	
500	1	1	0	0	0	1	1	1	0	1	0	1	1	
800	0	1	0	0	0	1	0	1	1	1	1	1	1	
1000	0	1	0	0	0	1	1	1	0	1	1	1	1	
1200	0	1	0	0	1	0	0	0	1	1	1	1	1	
1400	0	1	0	0	1	0	1	0	0	1	1	1	1	
1500	0	0	0	0	0	1	0	1	1	0	0	1	1	
1600	0	0	0	0	0	1	0	1	1	1	1	1	1	

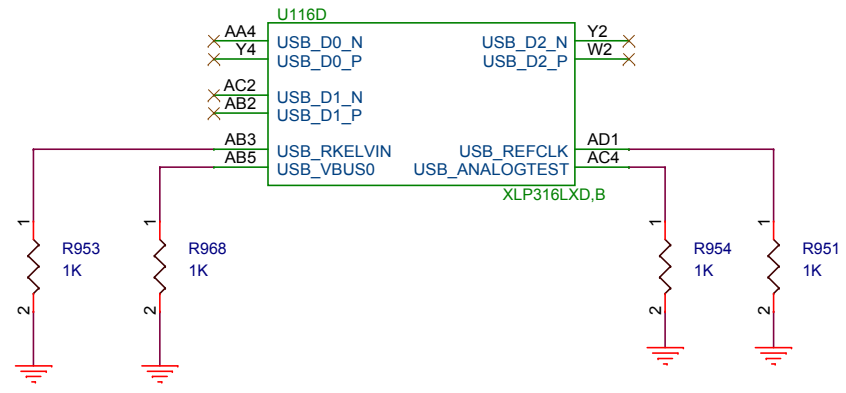
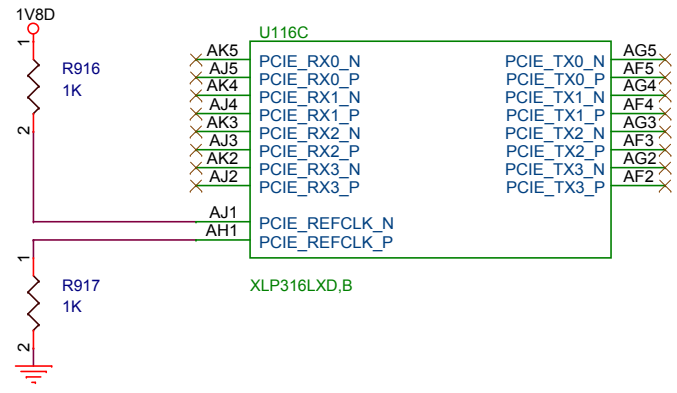
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900 02 511 B41 SS 40M RevB3			
Size	Document Number	Schematic Name	Rev
A3	<Doc>	08.XLP316	<RevCode>
Date: Thursday, October 15, 2015			
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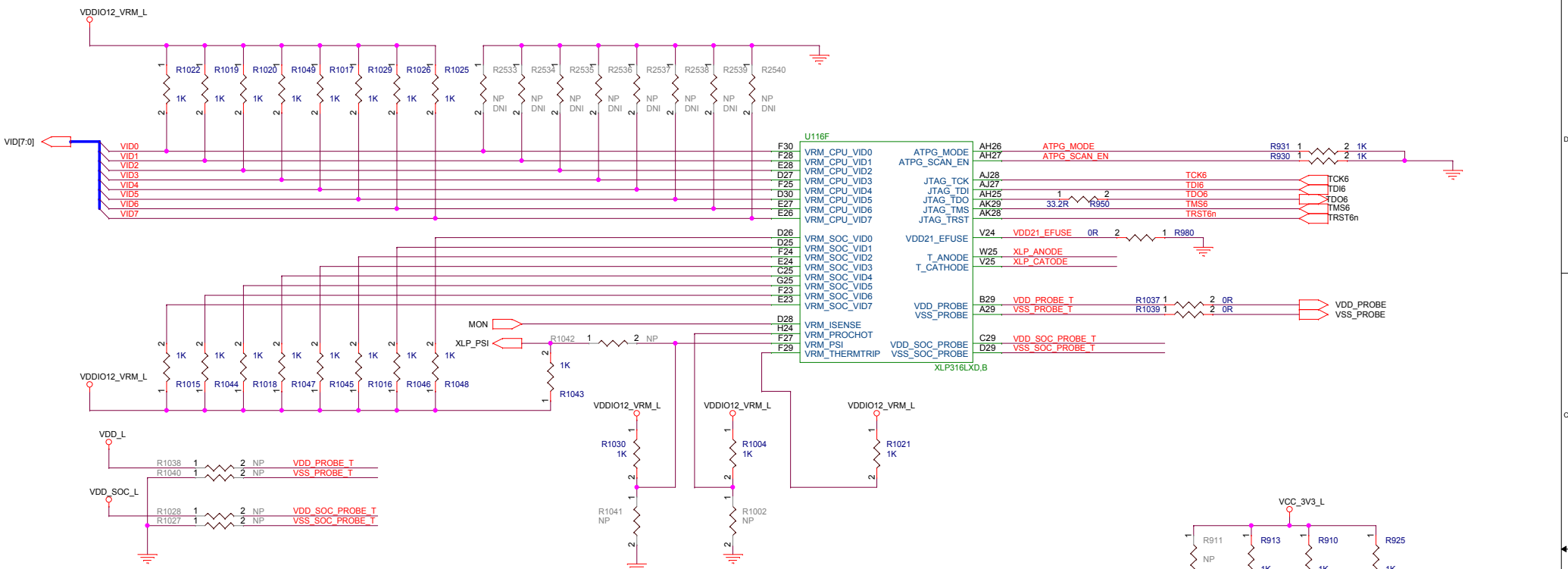




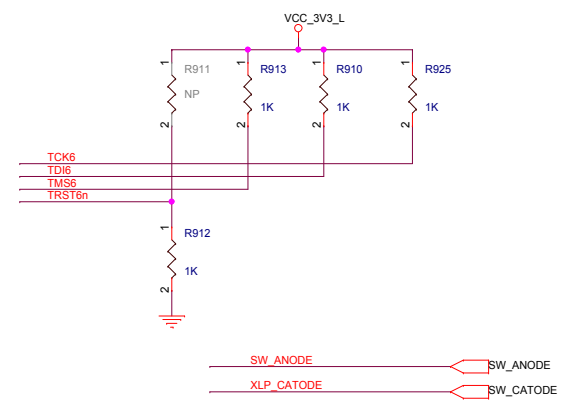
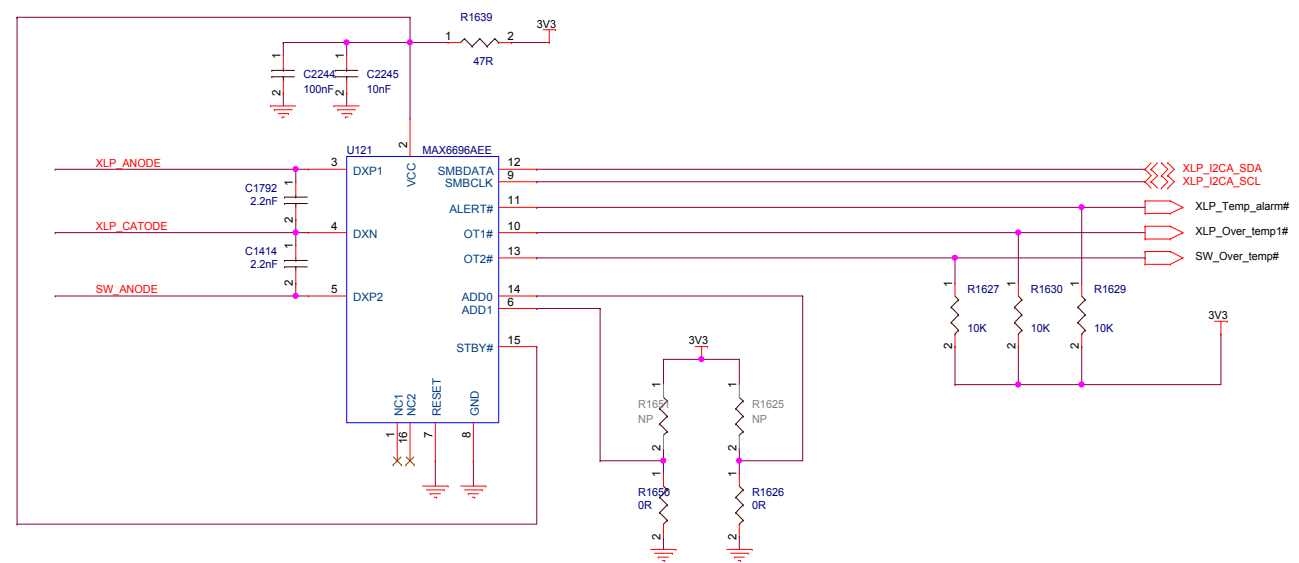


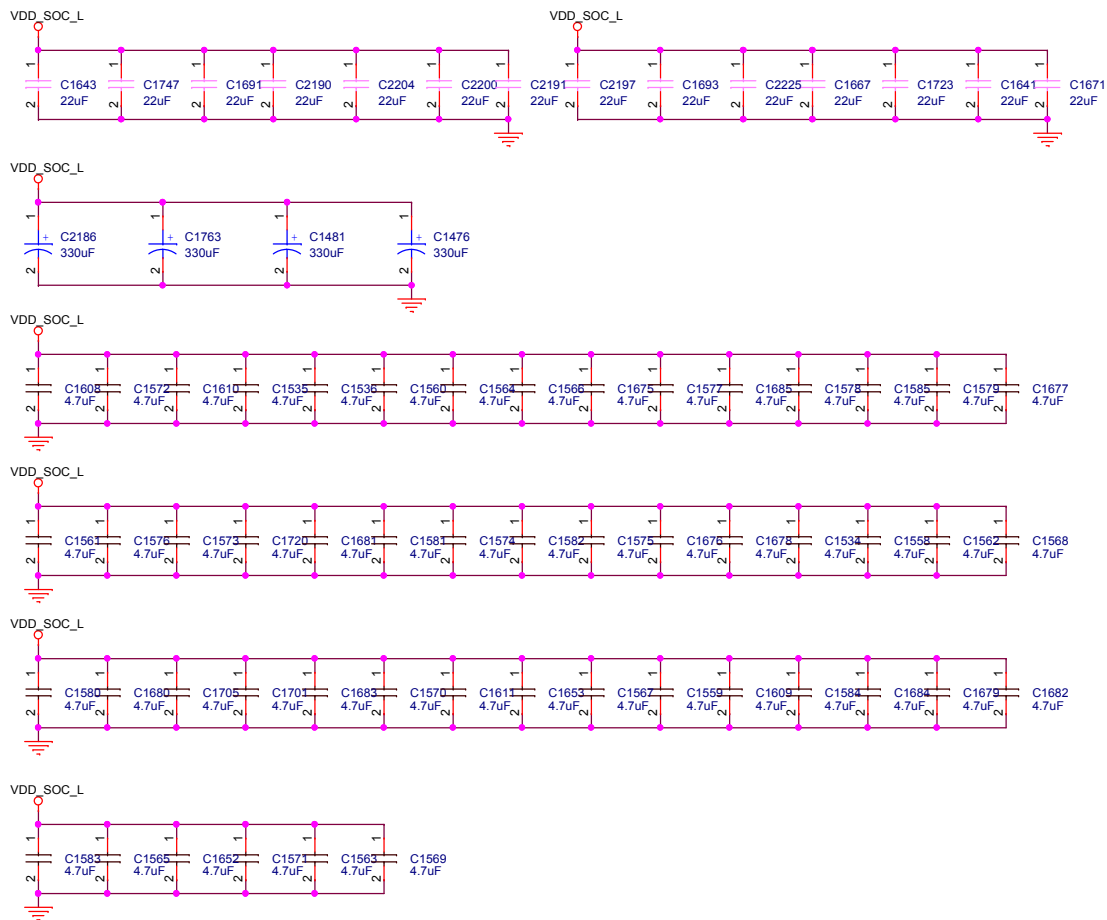
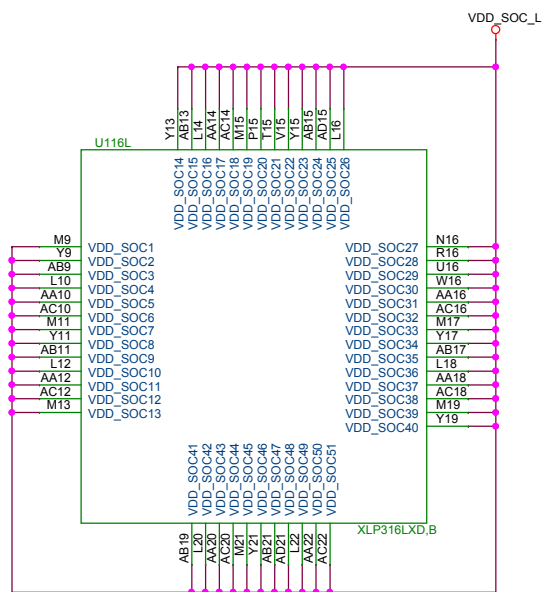




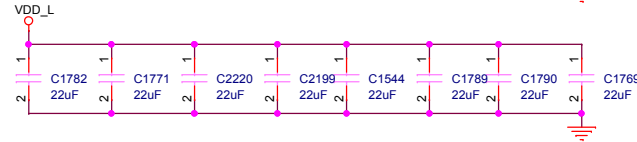
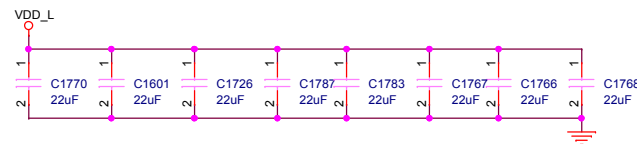
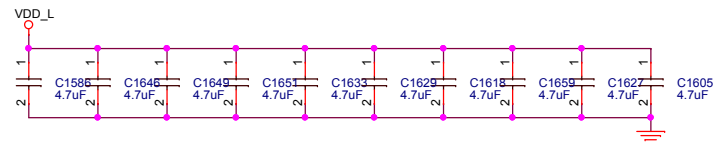
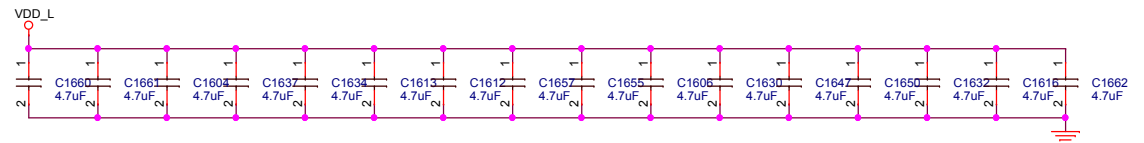
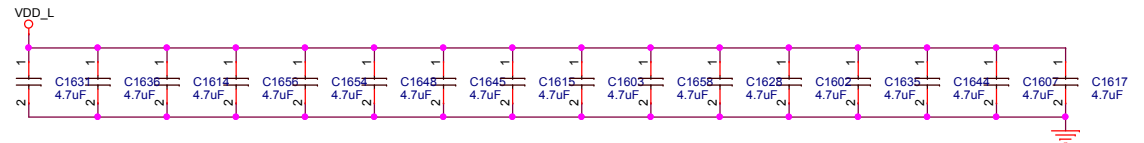
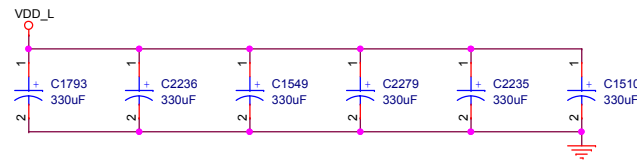
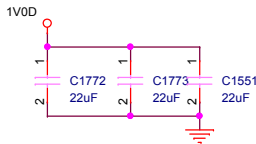
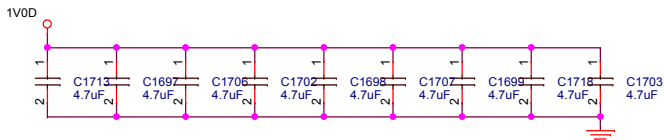
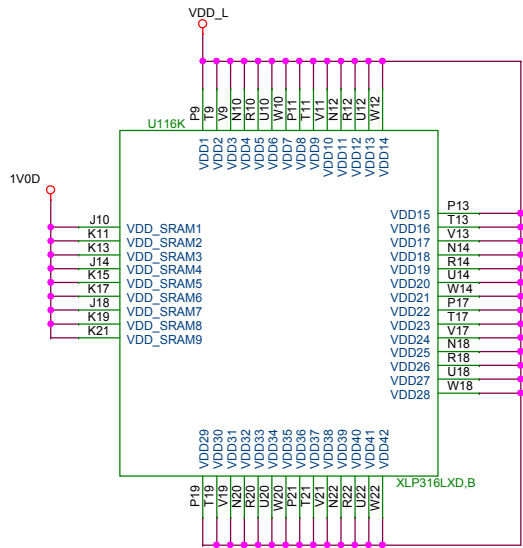


XLP Temperature supervisor

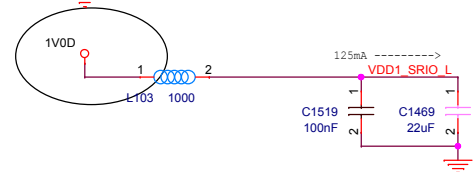
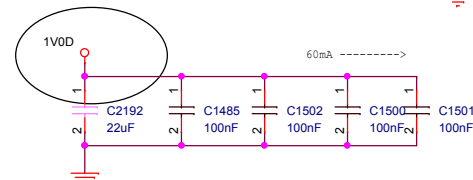
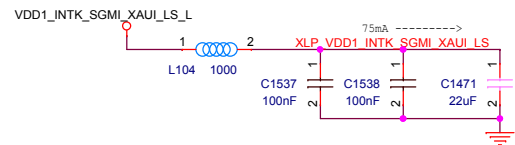
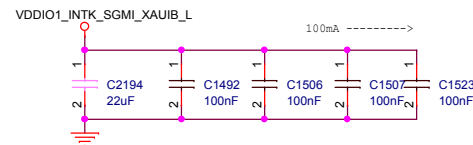
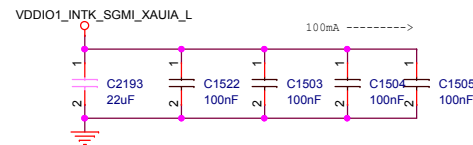
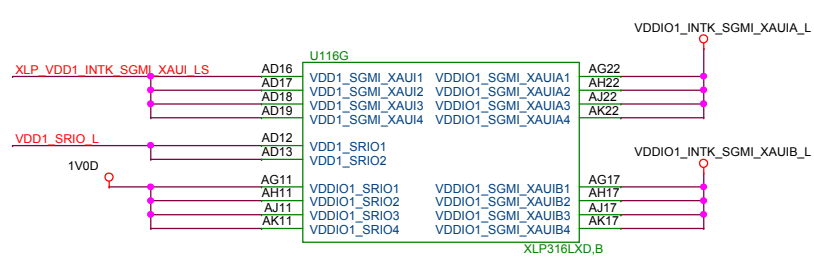
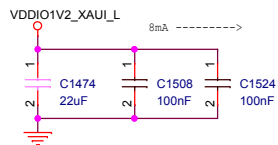
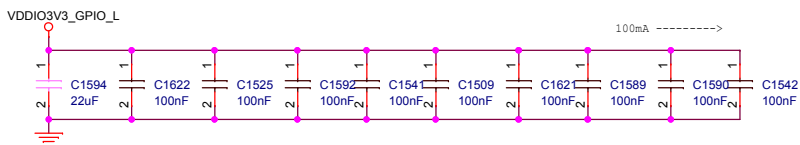
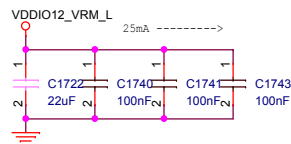
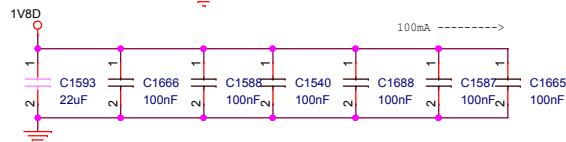
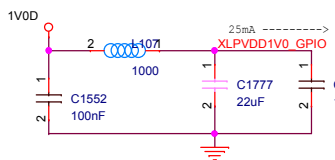
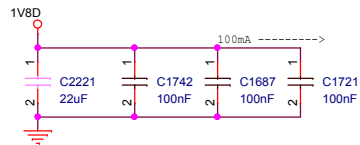
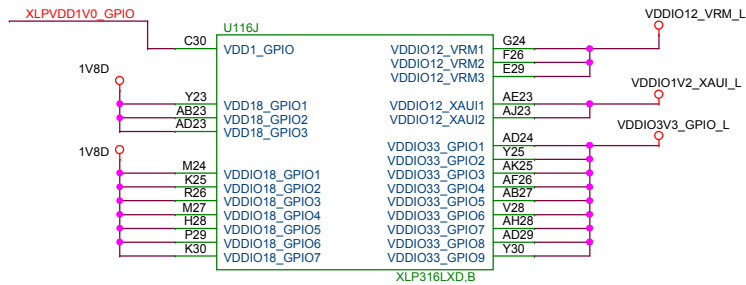




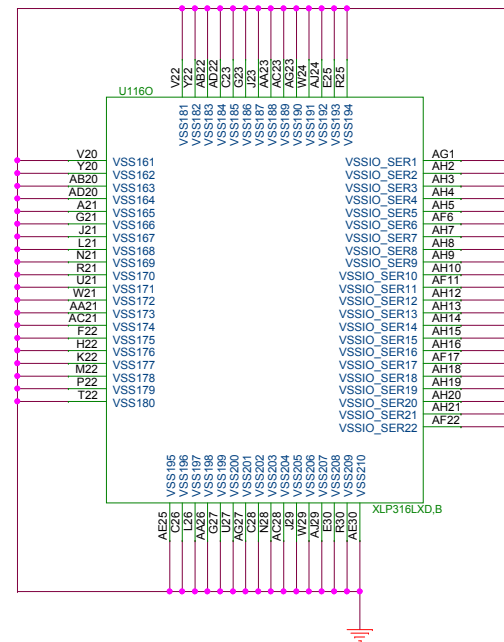
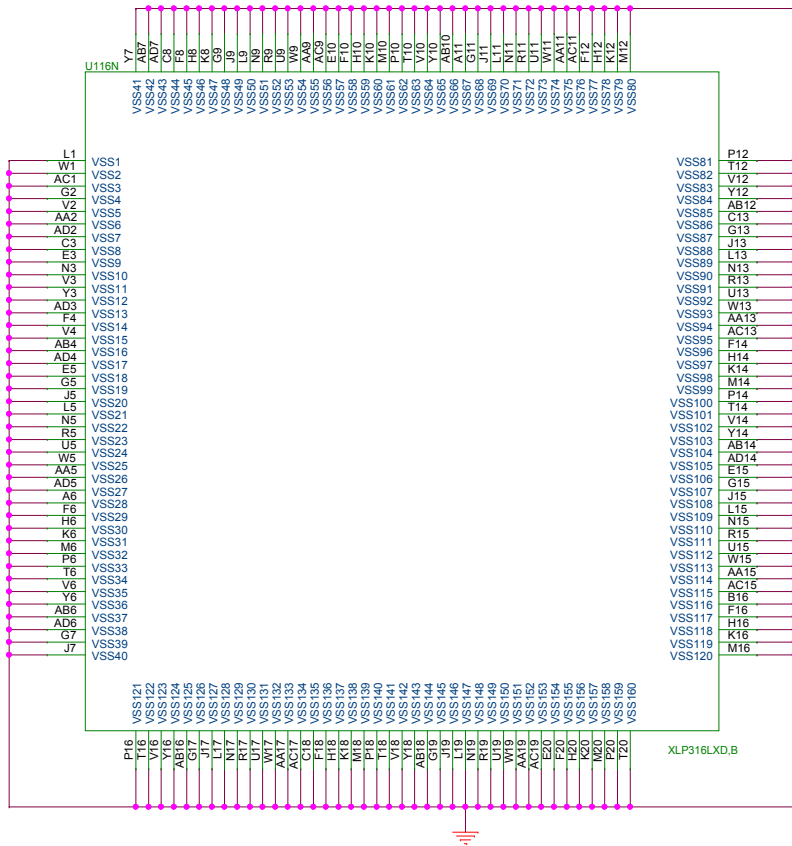
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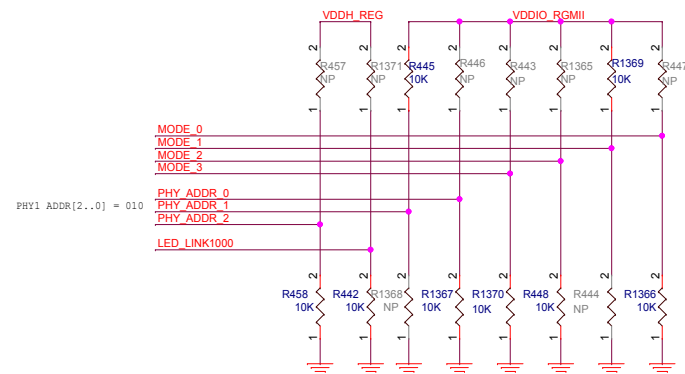
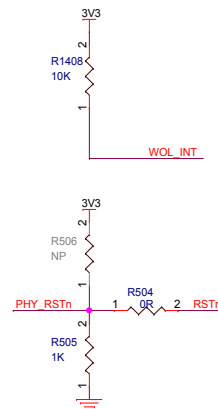
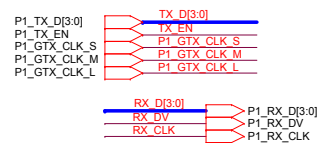
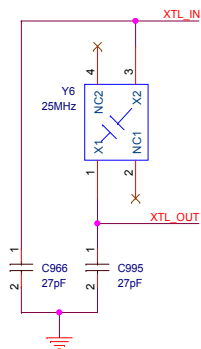
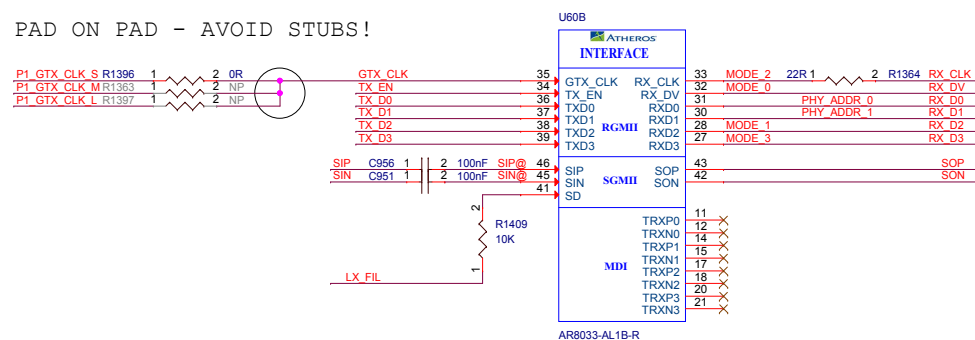
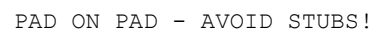


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```

MODE[3:0]
1011 Auto-Media Selection (In schematic)
0000 1000BASE-T, RGMII;
0001 1000BASE-T, SGMII;
0010 1000BASE-X, RGMII, 50Ω;
0011 1000BASE-X, RGMII, 75Ω;
0100 1000M Converter, 50Ω;
0101 1000M, Converter, 75Ω;
0110 100BASE-FX, RGMII, 50Ω;
0111 100M Converter, 50Ω;
1110 100BASE-FX, RGMII, 75Ω;
1111 100M Converter, 75Ω;

```

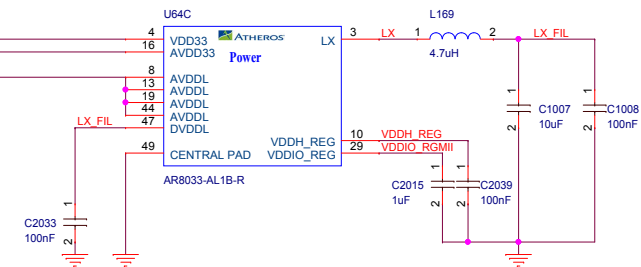
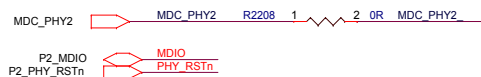
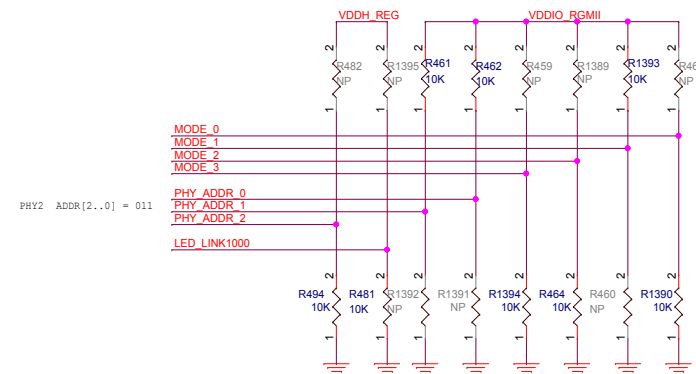


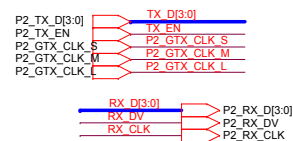
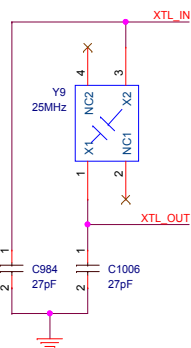
Diagram illustrating the pin connections for the AR8033-AL1B-R component. The component is shown as a blue box with pins numbered 1 to 46. Connections include:

- Pin 1:** P2 GTX_CLK S R1405
- Pin 2:** P2 GTX_CLK M R1407
- Pin 1:** P2 GTX_CLK L R1406
- Pin 35:** GTX_CLK
- Pin 34:** TX_EN
- Pin 36:** TX_D0
- Pin 37:** TX_D1
- Pin 38:** TX_D2
- Pin 39:** TX_D3
- Pin 46:** SIP C970
- Pin 45:** SIN C969
- Pin 46:** SIP@
- Pin 45:** SIN@
- Pin 46:** R1421 10K
- Pin 46:** LX_FIL
- Pin 33:** GTX_CLK
- Pin 32:** RX_CLK
- Pin 33:** MODE_2 22R1
- Pin 32:** MODE_0
- Pin 31:** PHY_ADDR_0
- Pin 30:** PHY_ADDR_1
- Pin 28:** MODE_1
- Pin 27:** MODE_3
- Pin 33:** RX_D0
- Pin 32:** RX_D1
- Pin 31:** RX_D2
- Pin 30:** RX_D3
- Pin 28:** RX_D0
- Pin 27:** RX_D1
- Pin 43:** RX_D2
- Pin 42:** RX_D3
- Pin 43:** SIP
- Pin 42:** SIN
- Pin 43:** SGMII
- Pin 42:** SON
- Pin 11:** TRXP0
- Pin 12:** TRXN0
- Pin 14:** TRXP1
- Pin 15:** TRXN1
- Pin 17:** TRXP2
- Pin 18:** TRXN2
- Pin 20:** TRXP3
- Pin 21:** TRXN3

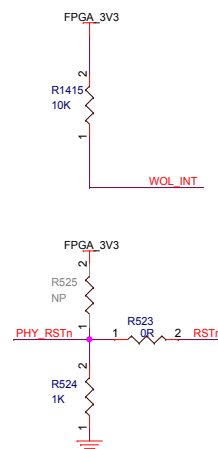
AR8033-AL1B-R



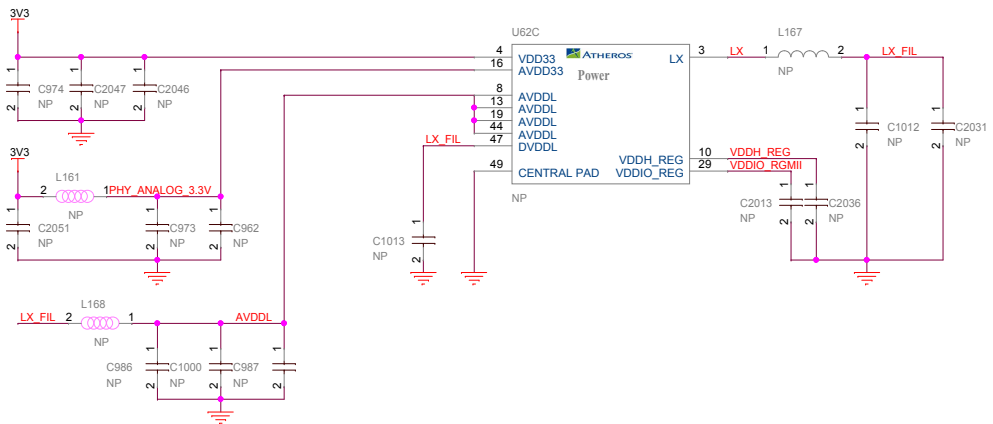
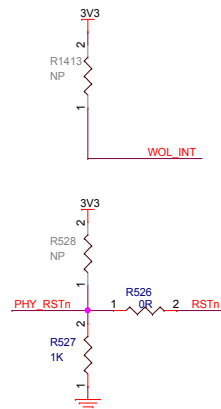
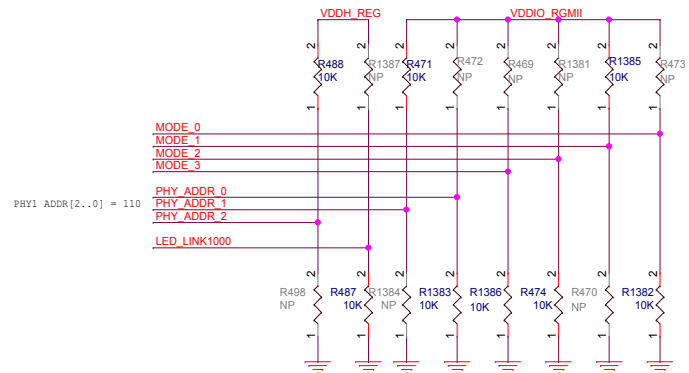
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PHY2  ADDR[2..0] = 011
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P2_SIP SIP
P2_SIN SIN
P2_SOP SOP
P2_SON SON



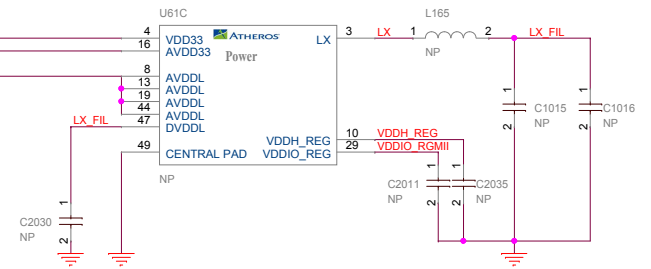
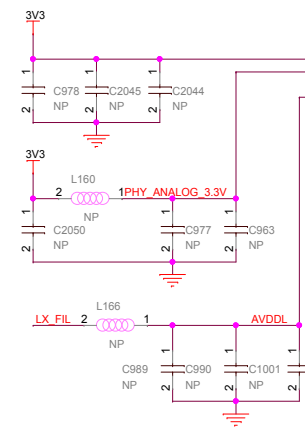
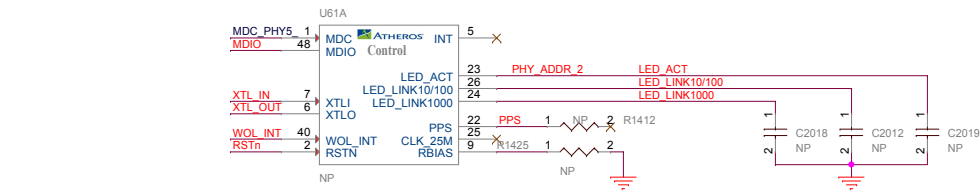
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MODE[3:0]
1011 Auto-Media Selection (In schematic)
0000 1000BASE-T, RGMII;
0001 1000BASE-T, SGMII;
0010 1000BASE-X, RGMII, 50Q;
0011 1000BASE-X, RGMII, 75Q;
0100 1000M Converter, 50Q;
0101 1000M, Converter, 75Q;
0110 100BASE-FX, RGMII, 50Q;
0111 100M Converter, 50Q;
1110 100BASE-FX, RGMII, 75Q;
1111 100M Converter, 75Q;
```

[illegible]

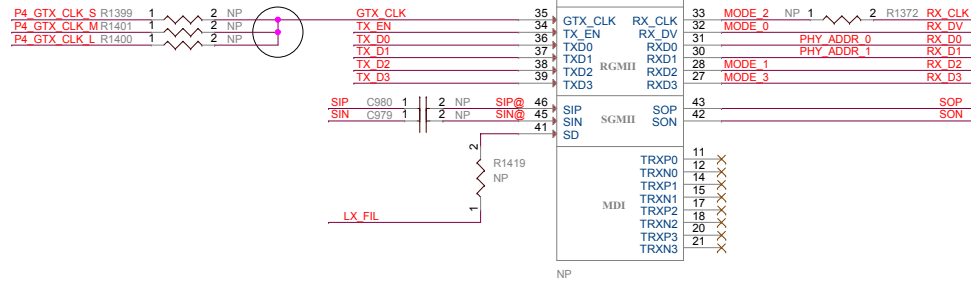
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MODE[3:0]
1011 Auto-Media Selection (In schematic)
0000 1000BASE-T, RGMII;
0001 1000BASE-T, SGMII;
0010 1000BASE-X, RGMII, 50Ω;
0011 1000BASE-X, RGMII, 75Ω;
0100 1000M Converter, 50Ω;
0101 1000M, Converter, 75Ω;
0110 100BASE-FX, RGMII, 50Ω;
0111 100M Converter, 50Ω;
1110 100BASE-FX, RGMII, 75Ω;
1111 100M Converter, 75Ω;

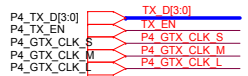
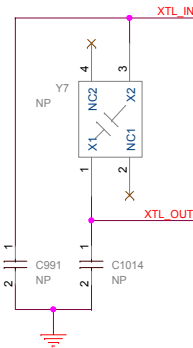
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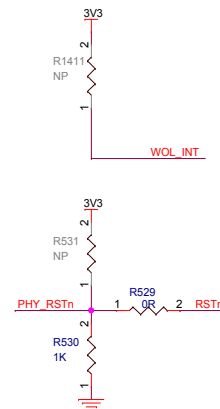
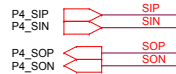
PAD ON PAD - AVOID STUBS!



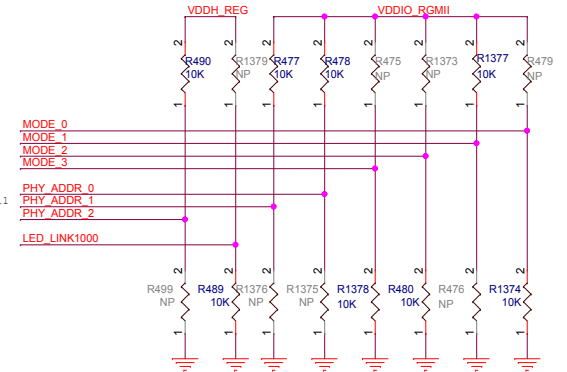
Place Close to the PHY !!!



SGMII



PHY1 ADDR[2..0] = 111



MODE[3:0]

1011 Auto-Media Selection (In schematic)
 0000 1000BASE-T, RGMII;
 0001 1000BASE-T, SGMII;
 0010 1000BASE-X, RGMII, 50Ω;
 0011 1000BASE-X, RGMII, 75Ω;
 0100 1000M Converter, 50Ω;
 0101 1000M, Converter, 75Ω;
 0110 100BASE-FX, RGMII, 50Ω;
 0111 100M Converter, 50Ω;
 1110 100BASE-FX, RGMII, 75Ω;
 1111 100M Converter, 75Ω;

Airspan Networks IL

<Title>

900 02 511 B41 SS 40M RevB3

Size A3

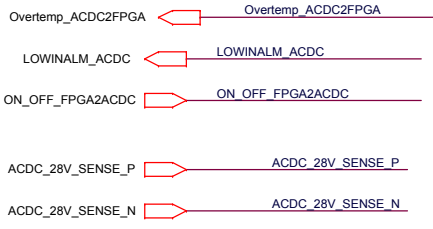
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Schematic Name 09. PHY's

Rev <RevCode>

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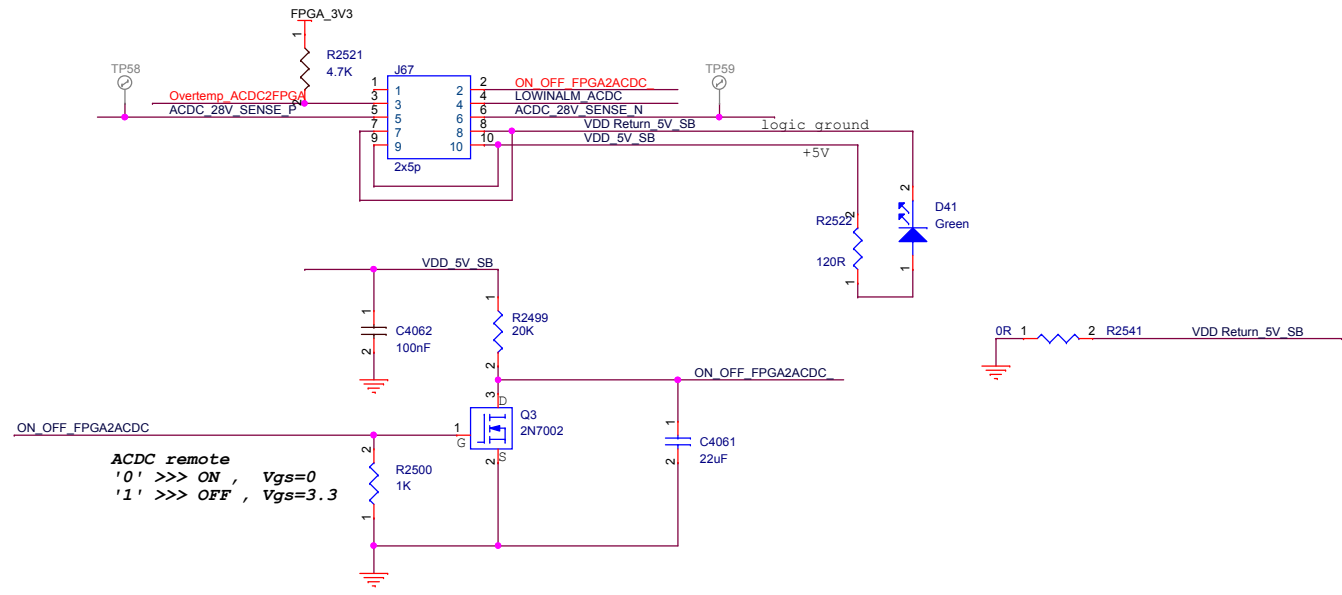


AC_OK_PWR_Fail = LOWINALM_ACDC

HOLD UP TIME = 20ms

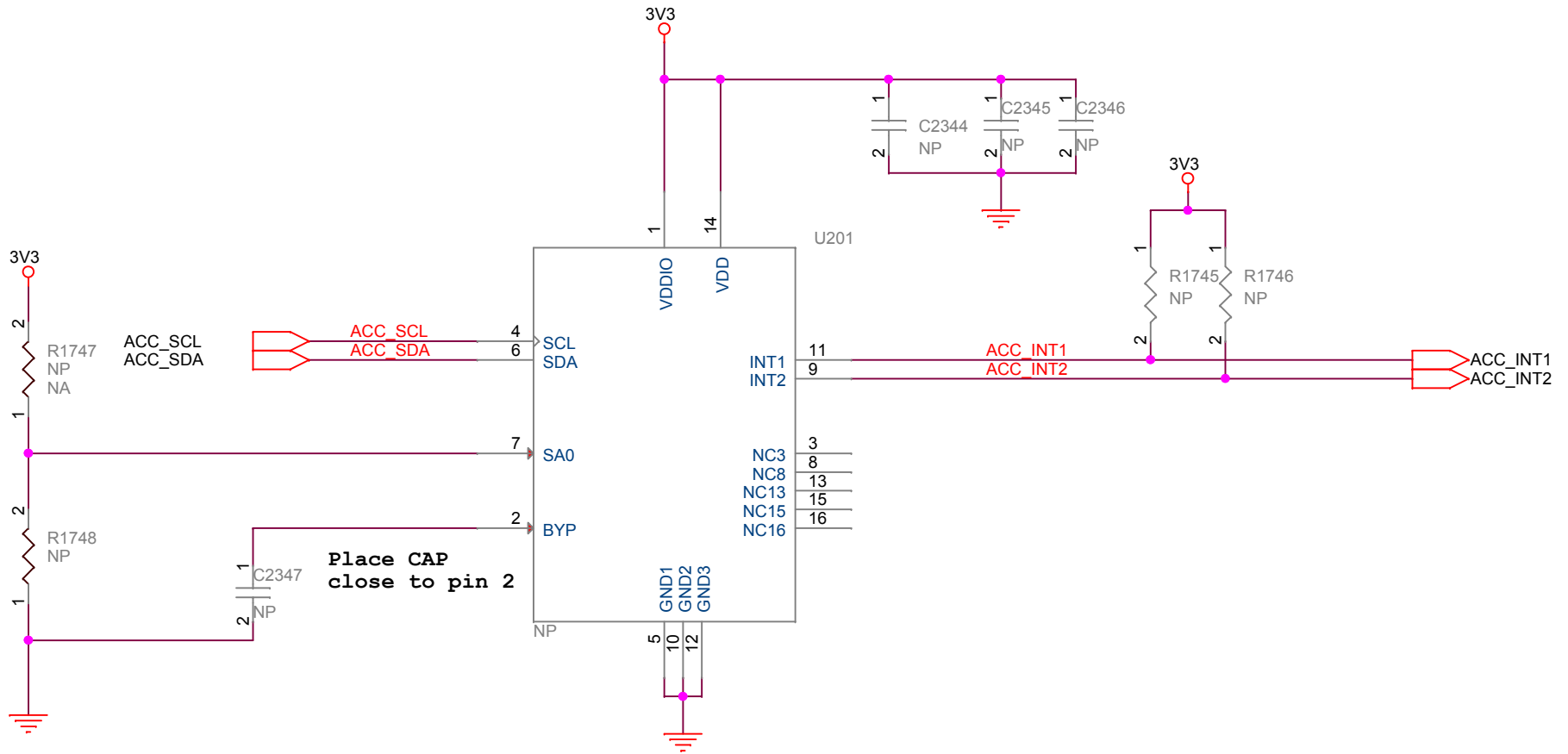
Transistor On (<0.8): AC NOT OK

Transistor Off (>4.5): AC OK

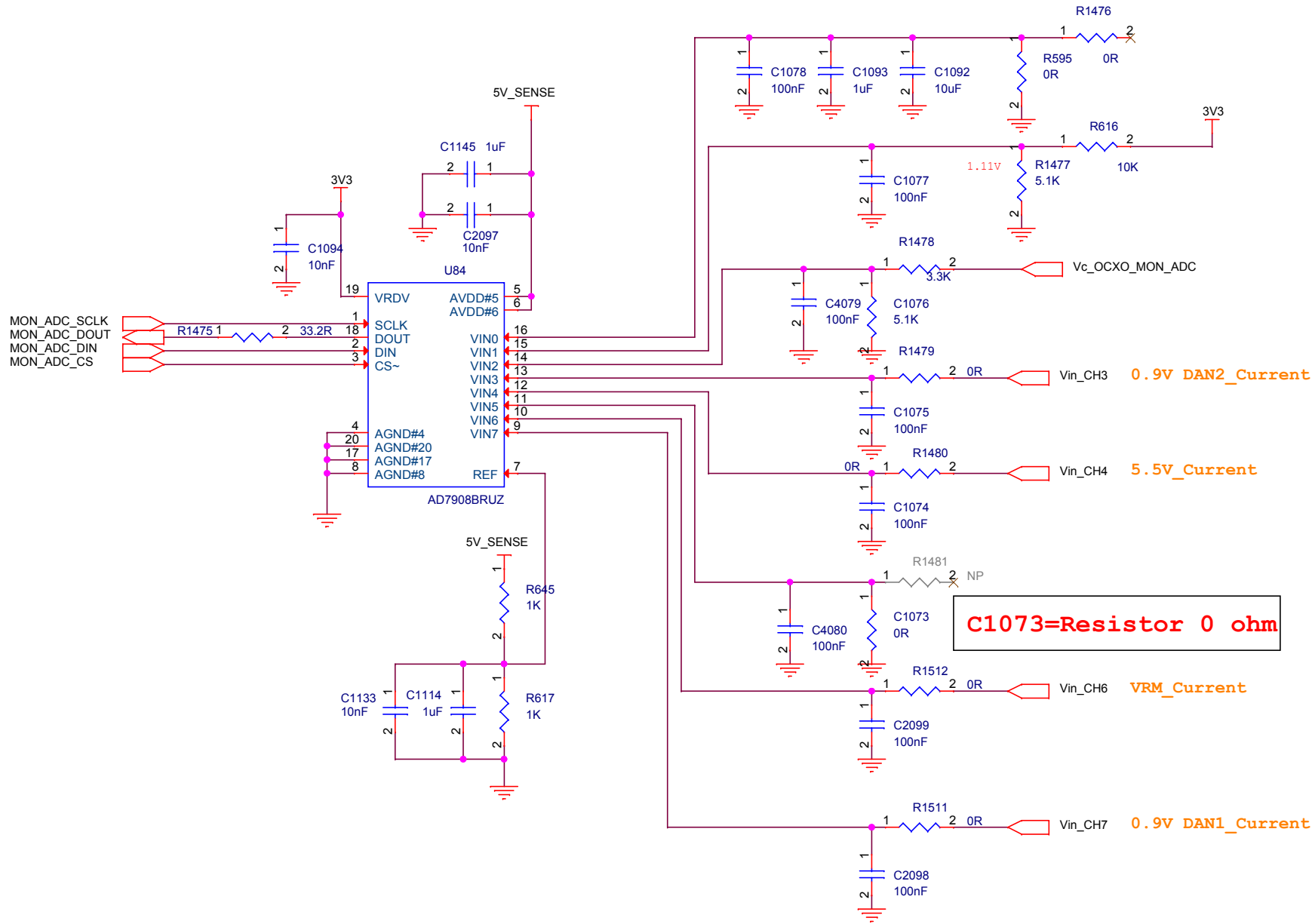


Accelerometer

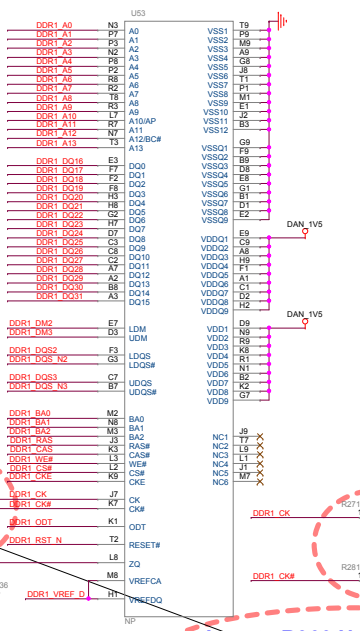
I2C ADDR:
001,1100



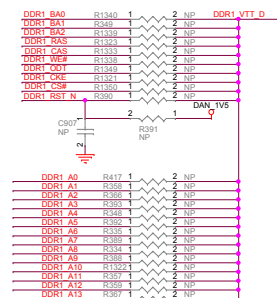
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<Title>		900 02 511 B41 SS 40M RevB3	
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A	<Doc>	Accelerometer	<RevCo
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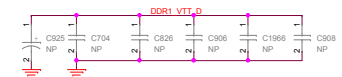
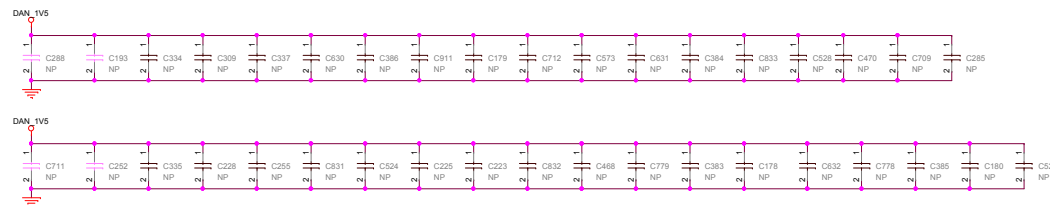
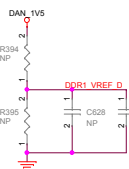
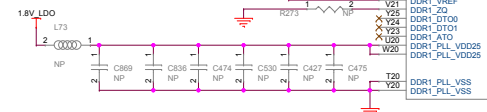
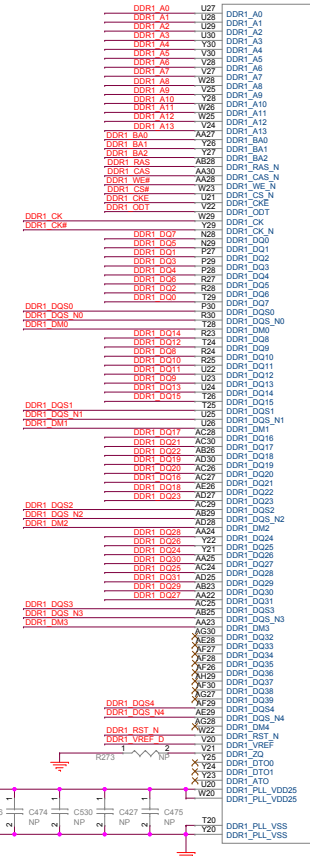
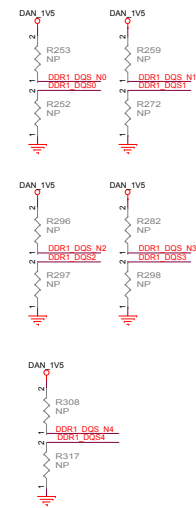
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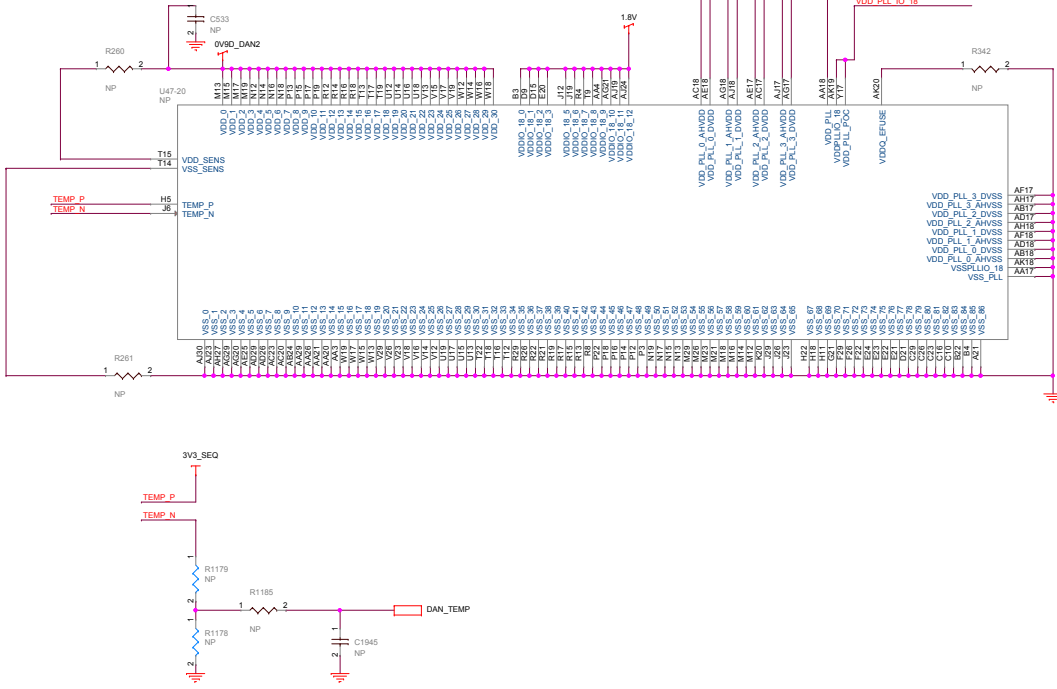
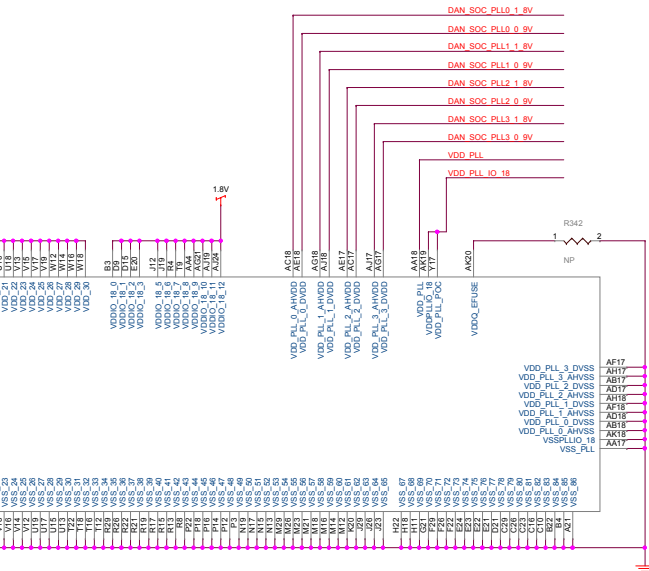
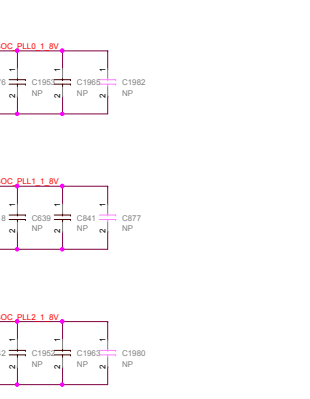
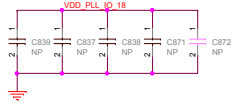
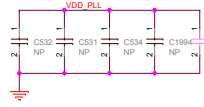
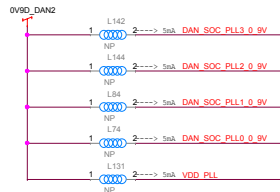


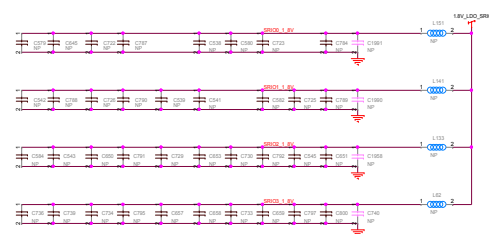
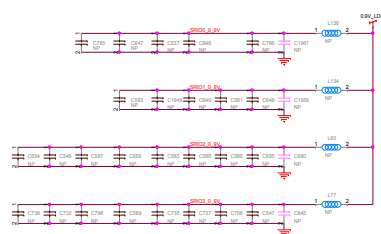
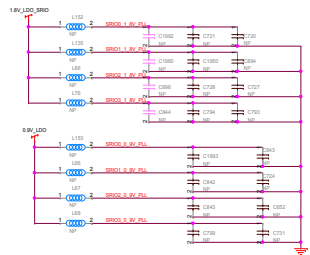
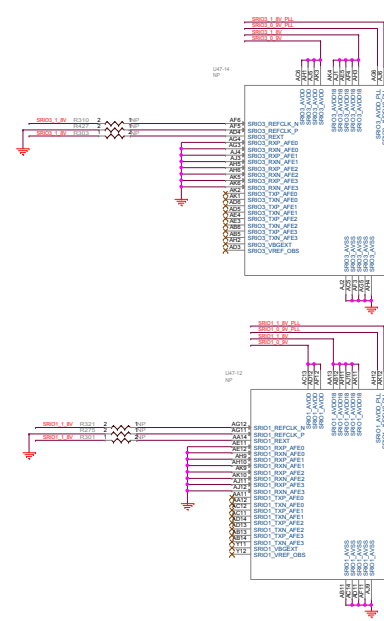
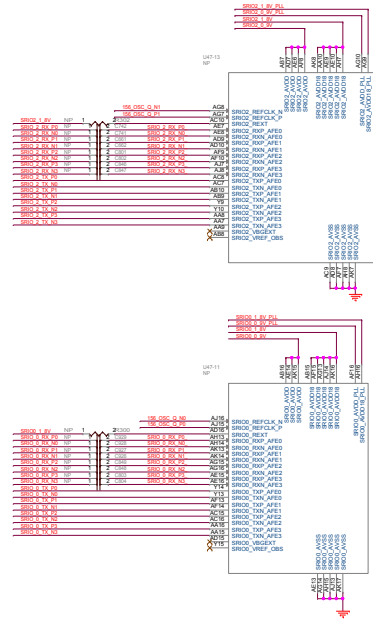
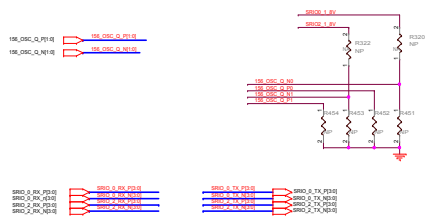
Place pad on pad

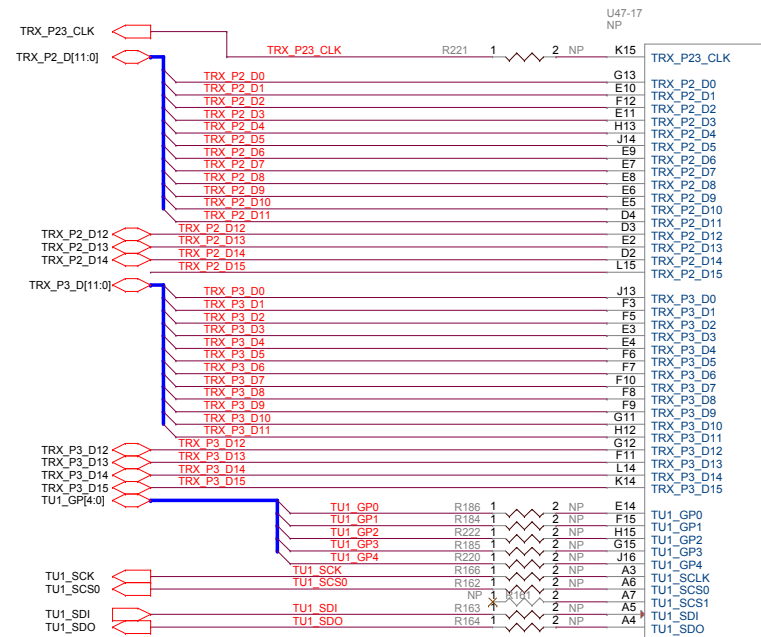
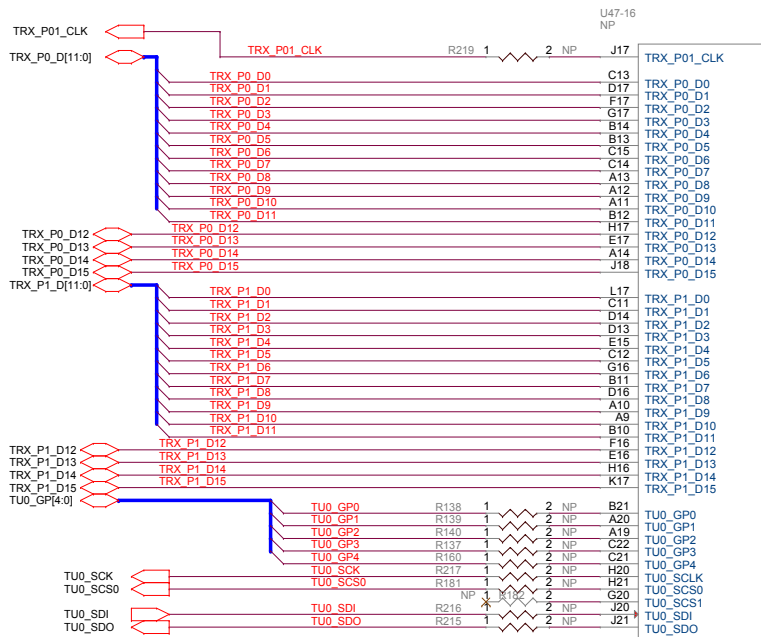


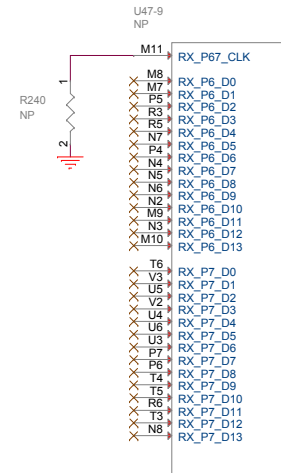
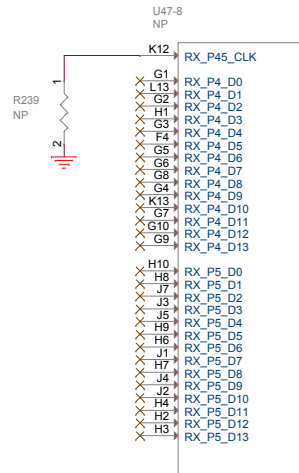
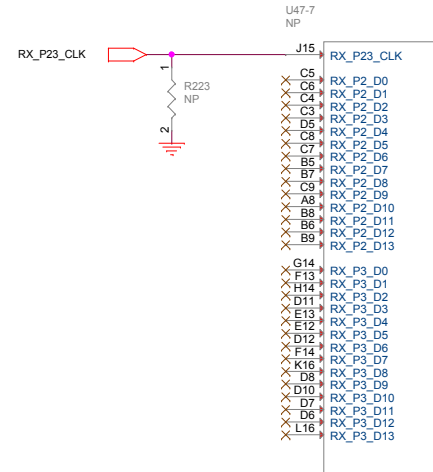
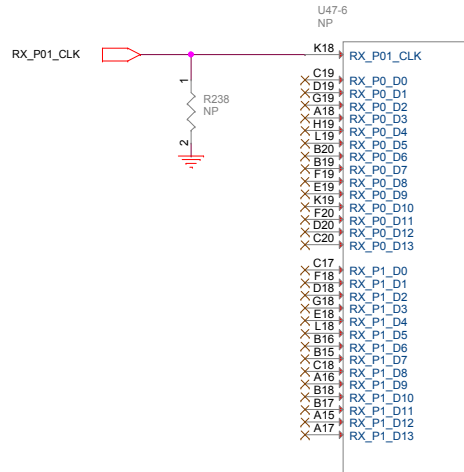
Locate 33R Resistors Near U48

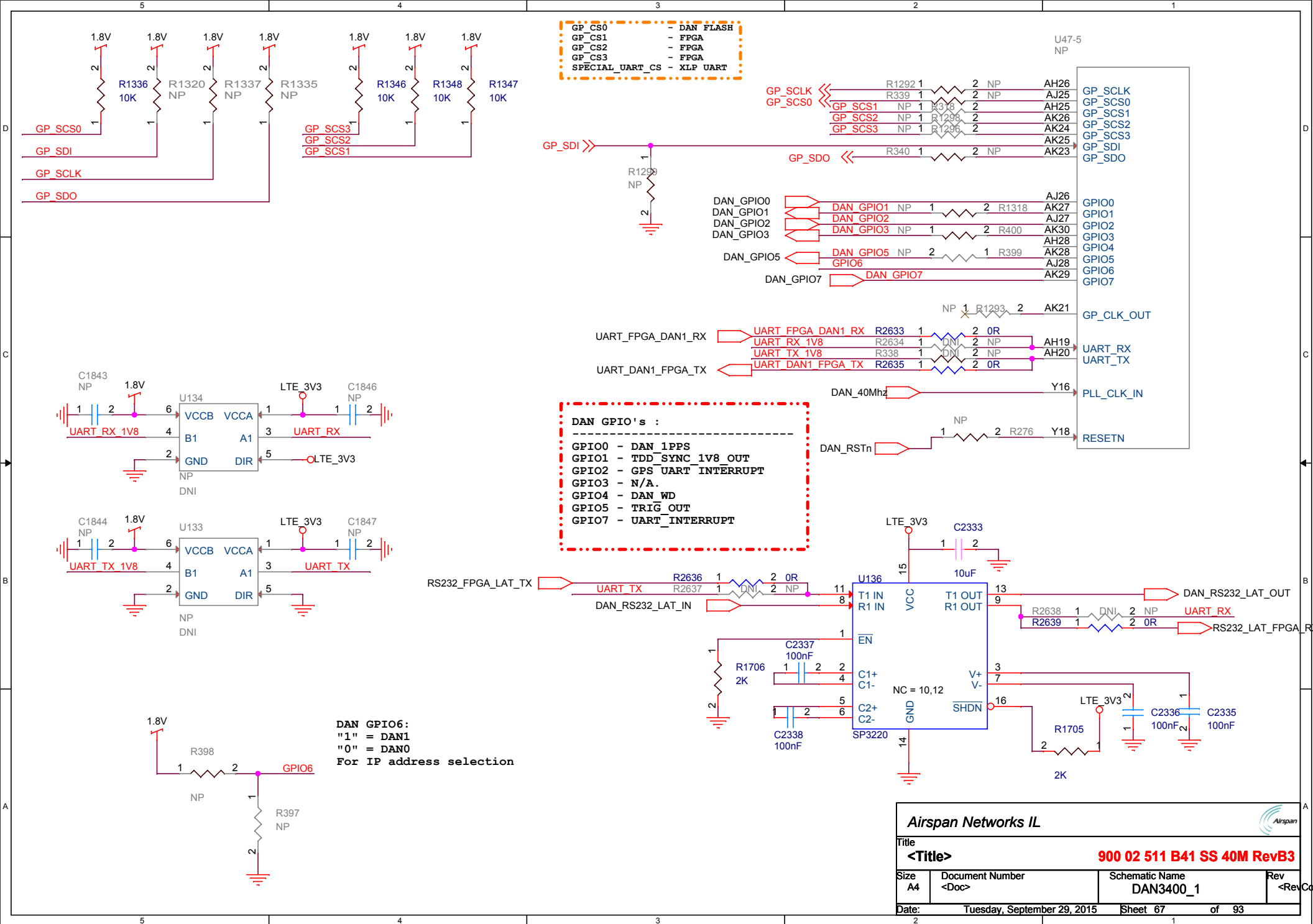


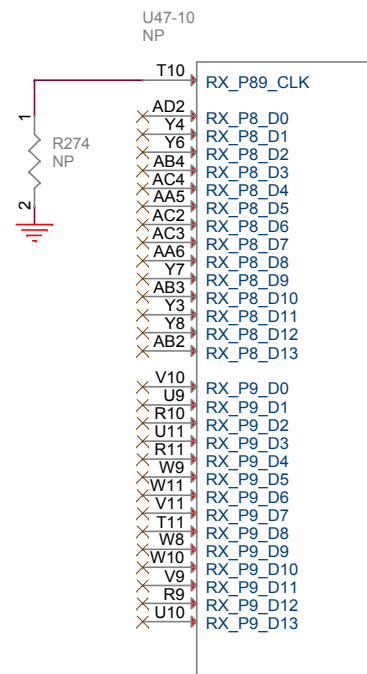












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Net should be daisy-chained from JTAG connector to DAN_1 to DAN_0

U47-15
NP

T_TCK
T_TDI
T_TDO
T_TMS
T_TRST

AD19
AG19
AF20
AE19
AF19

TCK3
TDI3
TDO3
TMS3
TRST3n

TCK
TDI
TDO
TMS
RTCK
TRST

AE20
AJ22
AH21
AJ21
AJ20
AF21

TCK5
TDI5
TDO5
TMS5
RTCK5
TRST5n

TM
JTAGSEL

AG22
AK22

1.8V

R319
NP

R418
NP

R280
NP

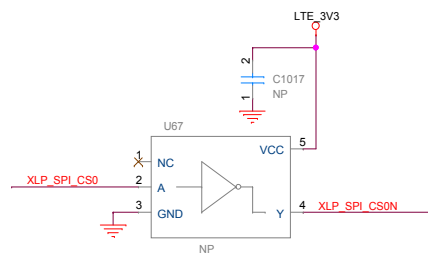
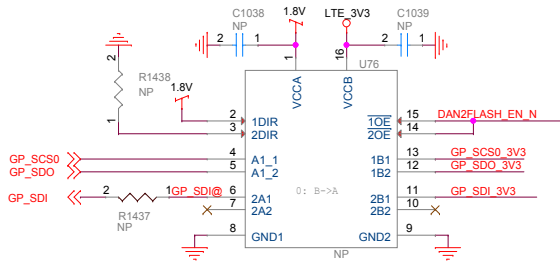
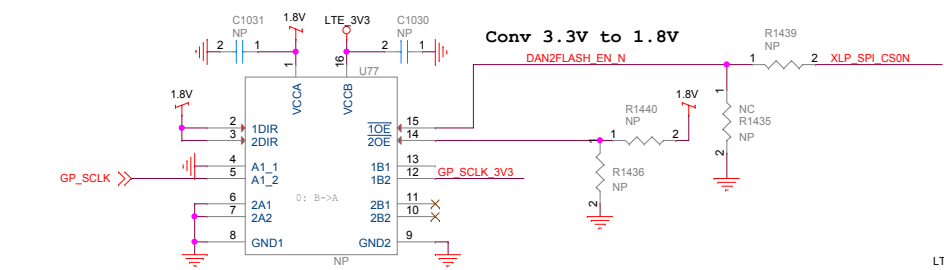
JTAGSEL

DAN_JTAG

DAN_JTAG

Airspan Networks IL			
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<Title>		900 02 511 B41 SS 40M RevB3	
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If the flash is Burnt externally the I/Os became 3-State

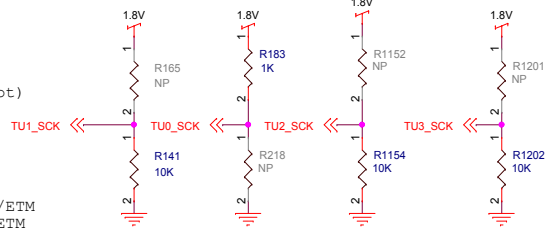


BOOT OPTIONS:
1, 0:

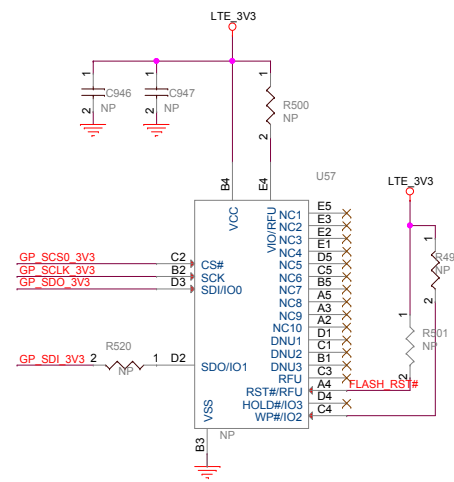
{TU1_SCLK, TU0_SCLK} = 00 -> ARM0
{TU1_SCLK, TU0_SCLK} = 01 -> RX DSP0
{TU1_SCLK, TU0_SCLK} = 10 -> TX CPU0
{TU1_SCLK, TU0_SCLK} = 11 -> TX CPU0 (Secured boot)
2:

0 - ETM/ETB is not part of the JTAG scan chain
1 - ETM/ETB is part of the JTAG scan chain
3:

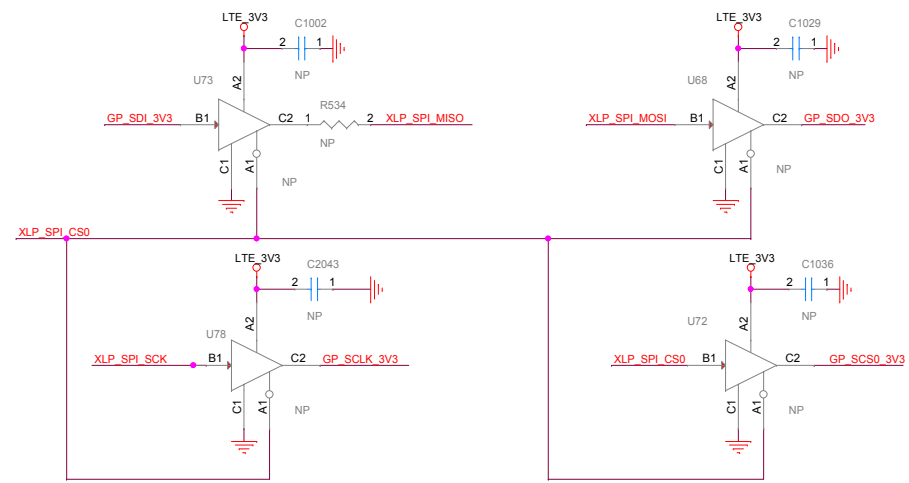
0 - ETB is in the JTAG scan chain before the ARM/ETM
1 - ETB is in the JTAG scan chain after the ARM/ETM



BANK 0 (CS0)



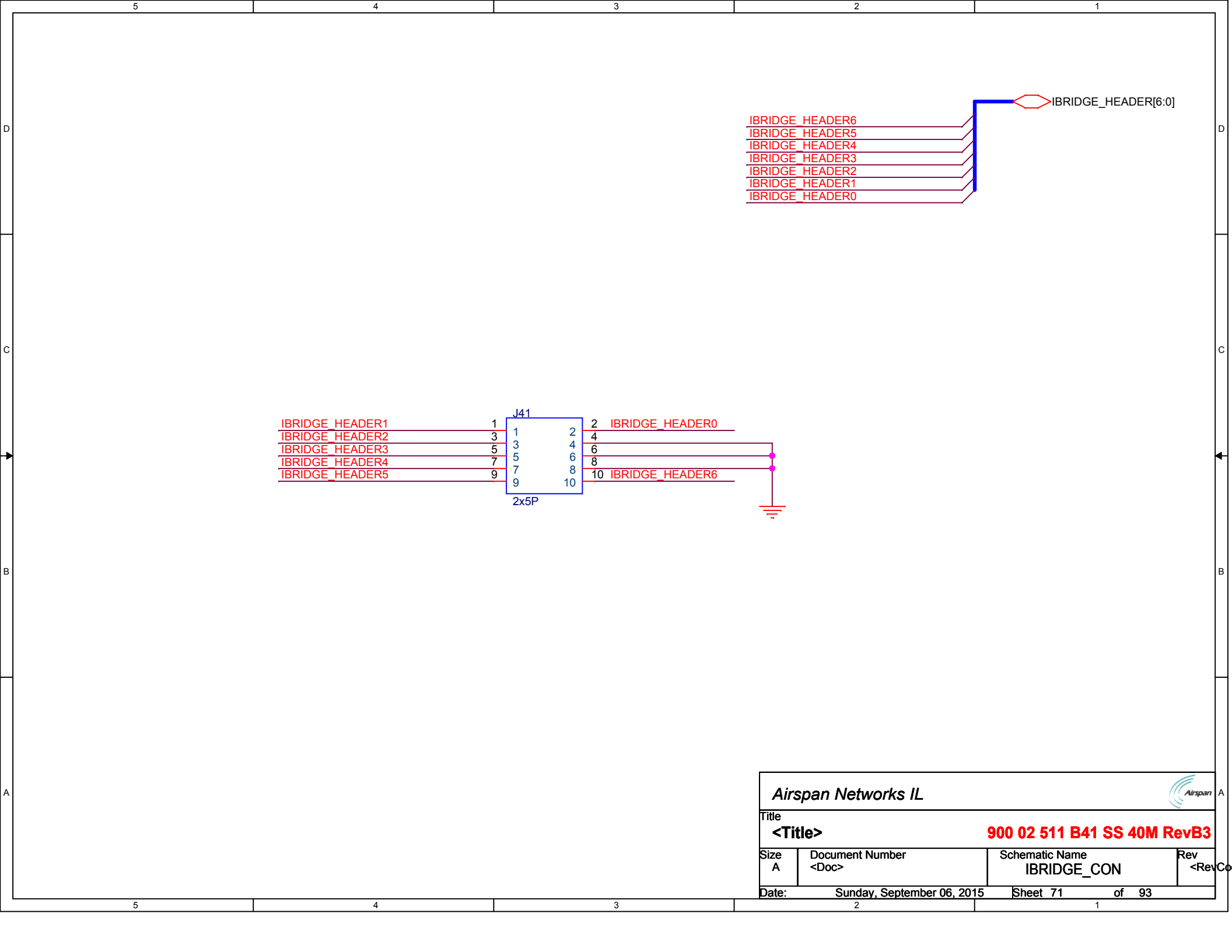
OPTION for burning the Flash from XLP
(The output is in 3 state by default)



Common SPI bus to FLASH, FPGA, XLP and XLP_UARTB

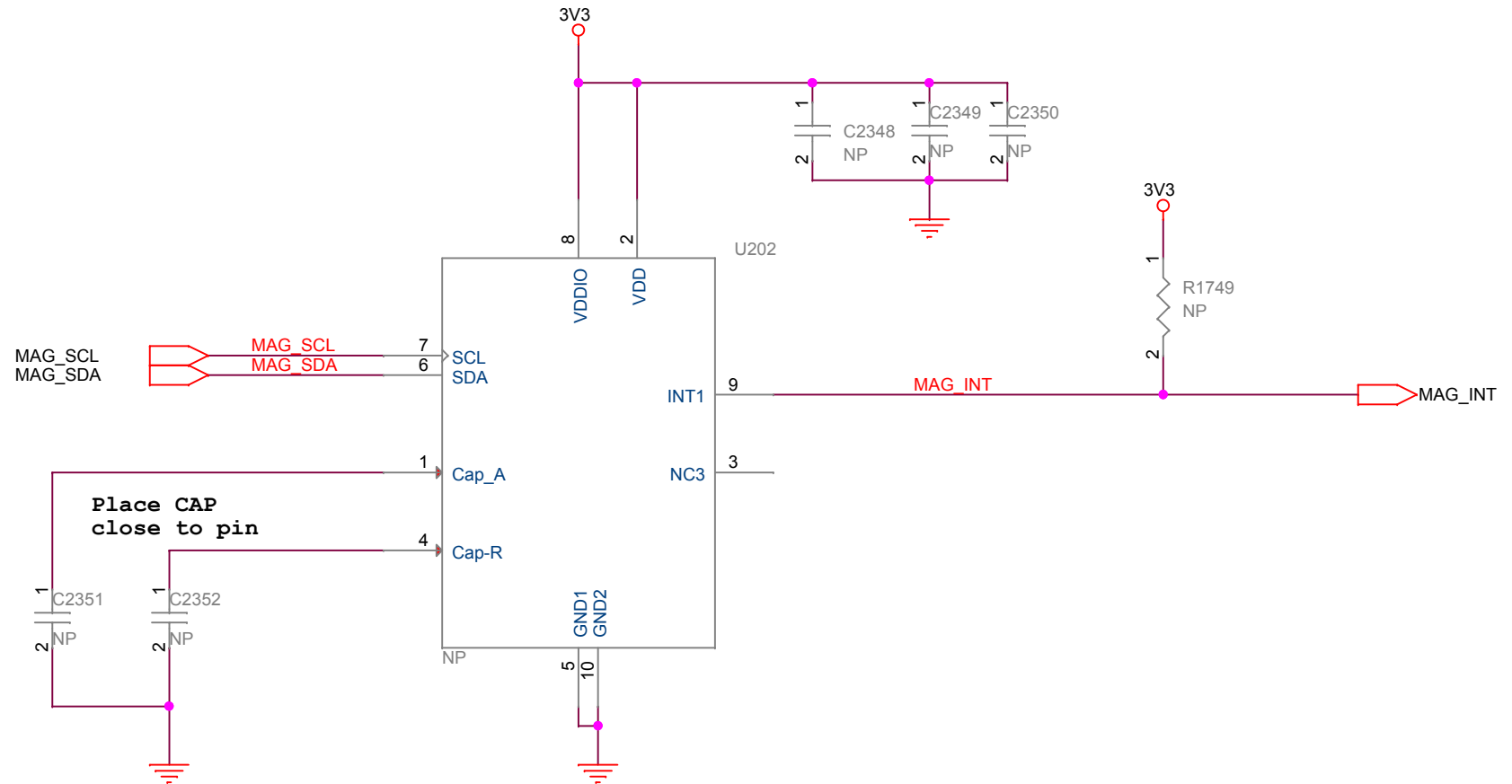


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A3			
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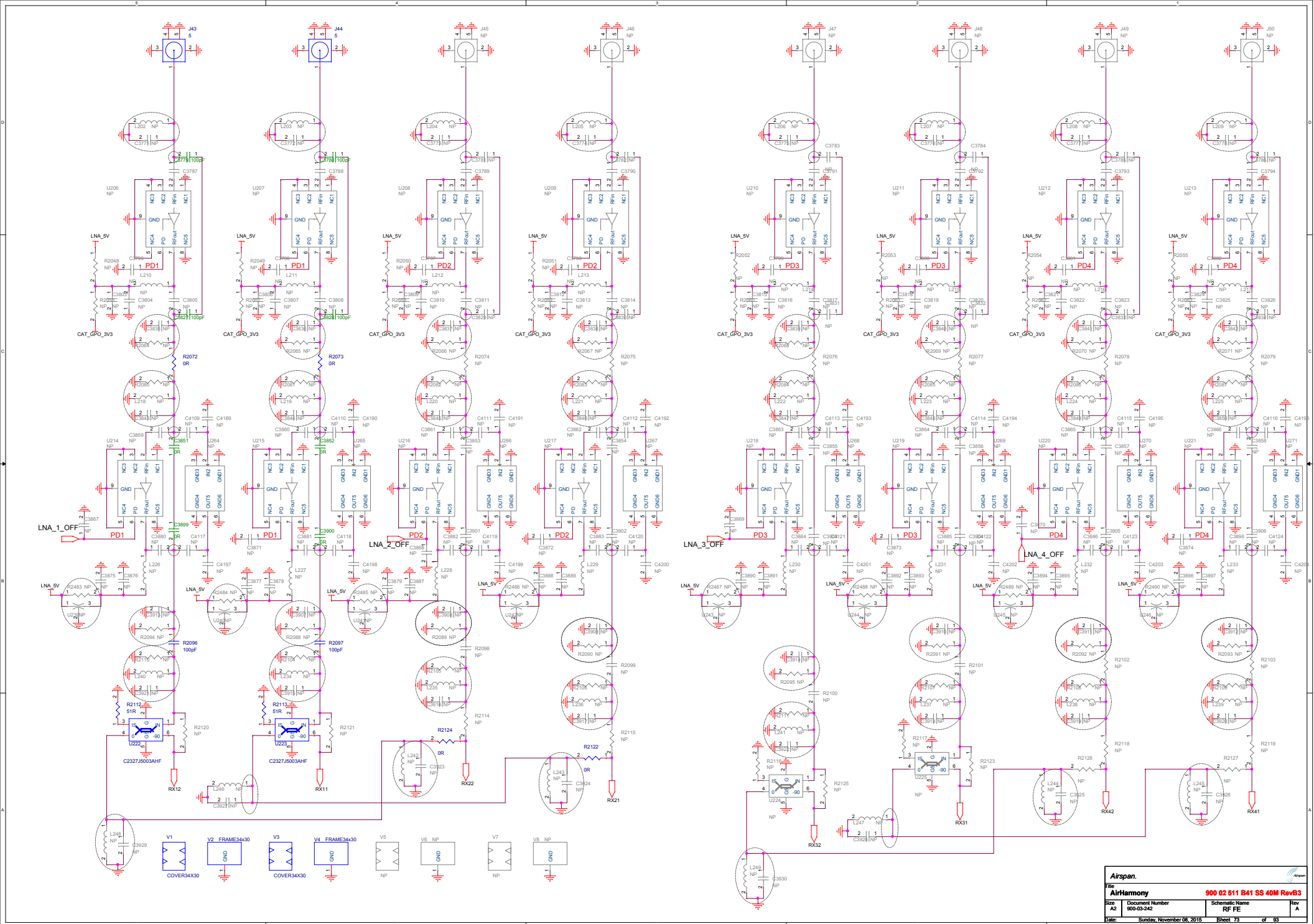


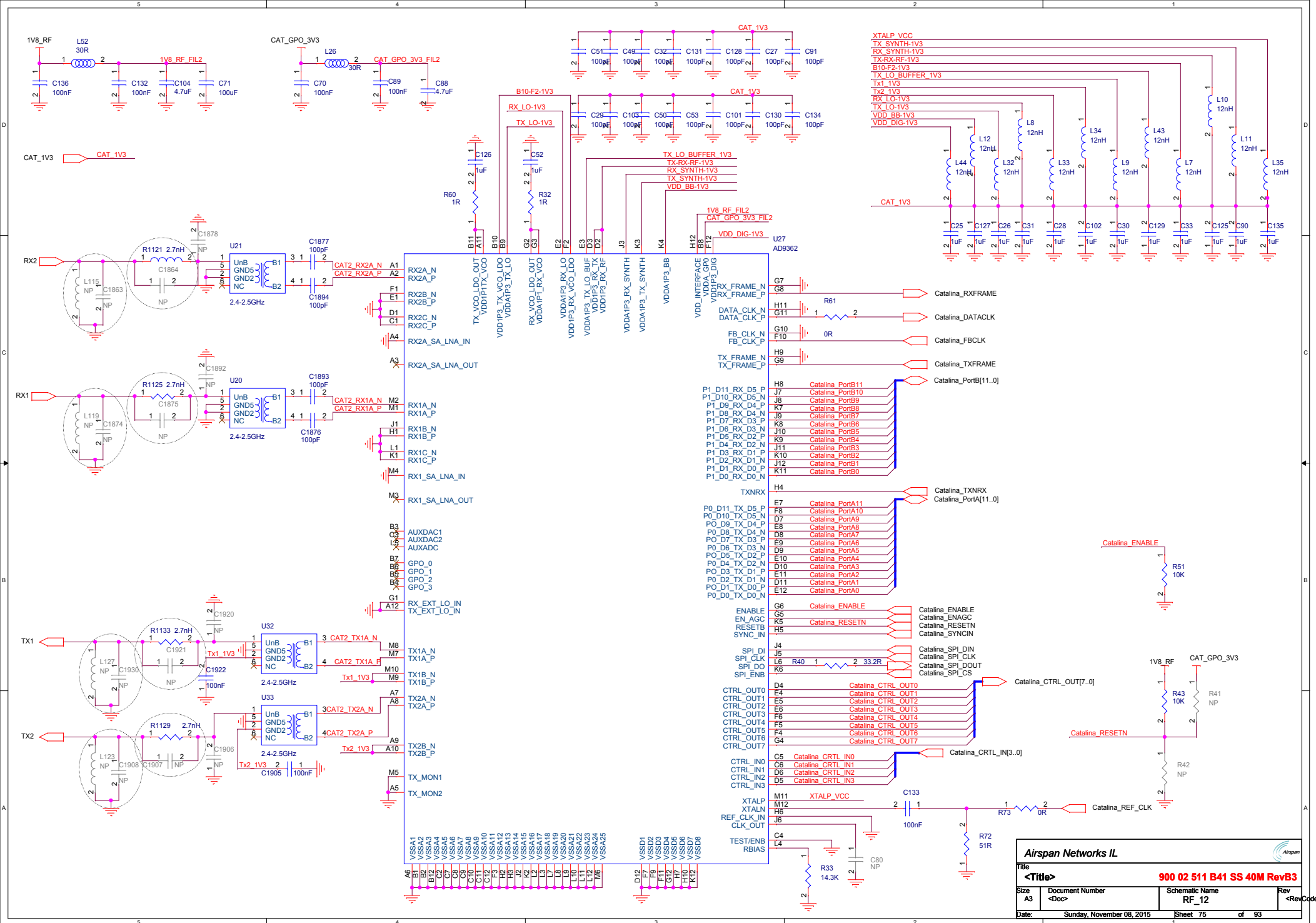
Magnetometer

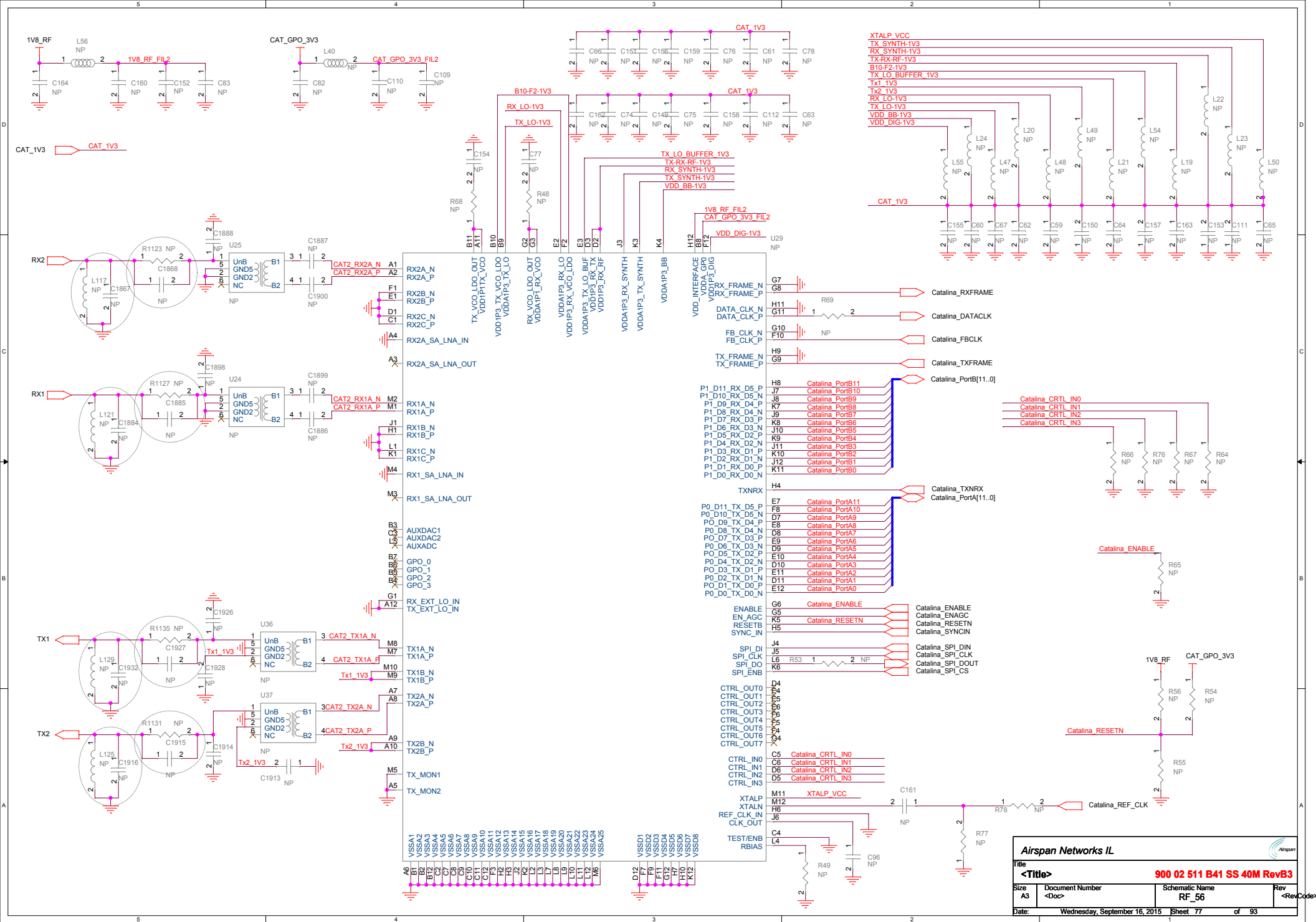
I2C ADDR:
0x0E

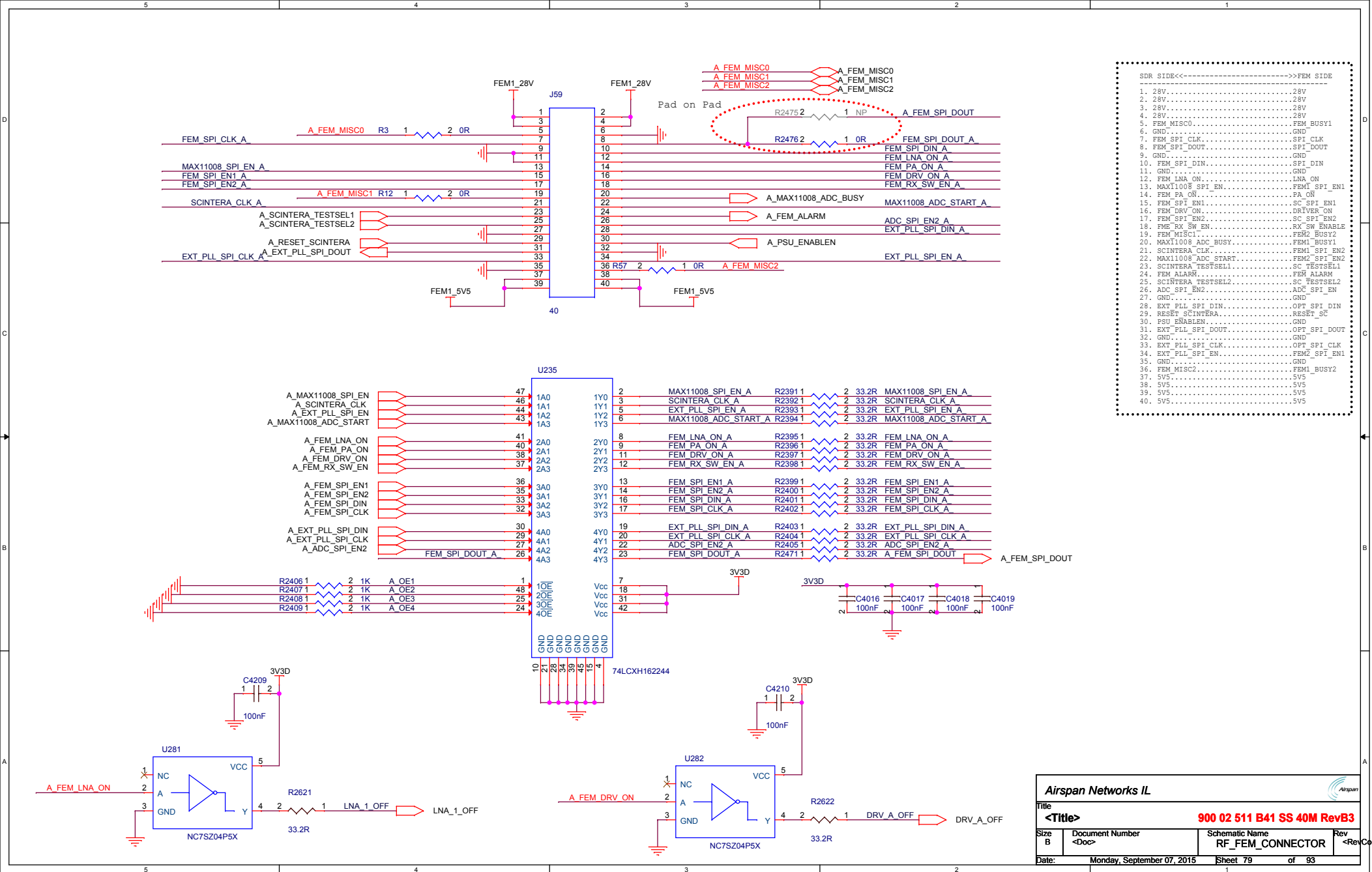


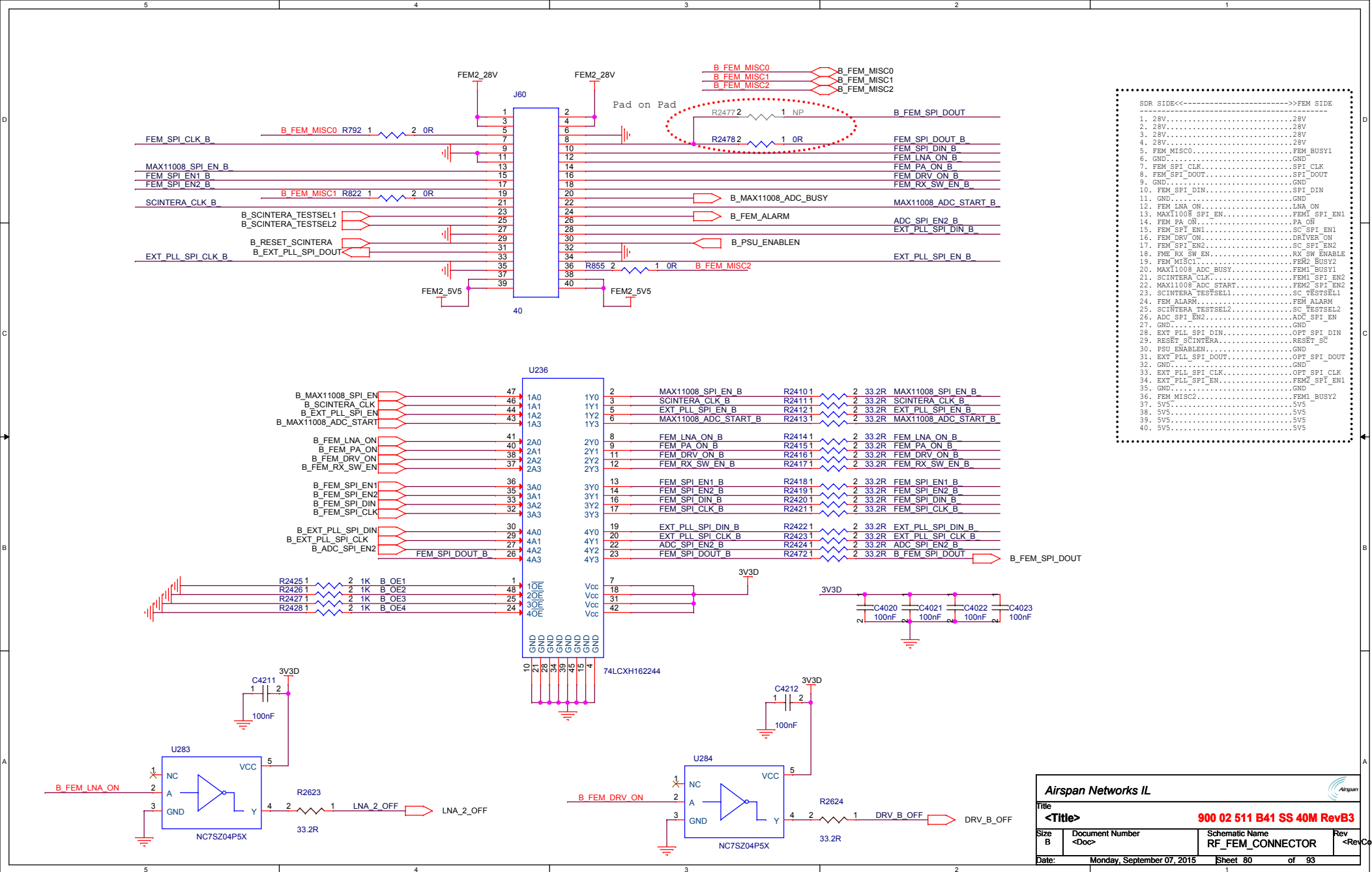
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A	<Doc>	Magnetometer	<RevCo
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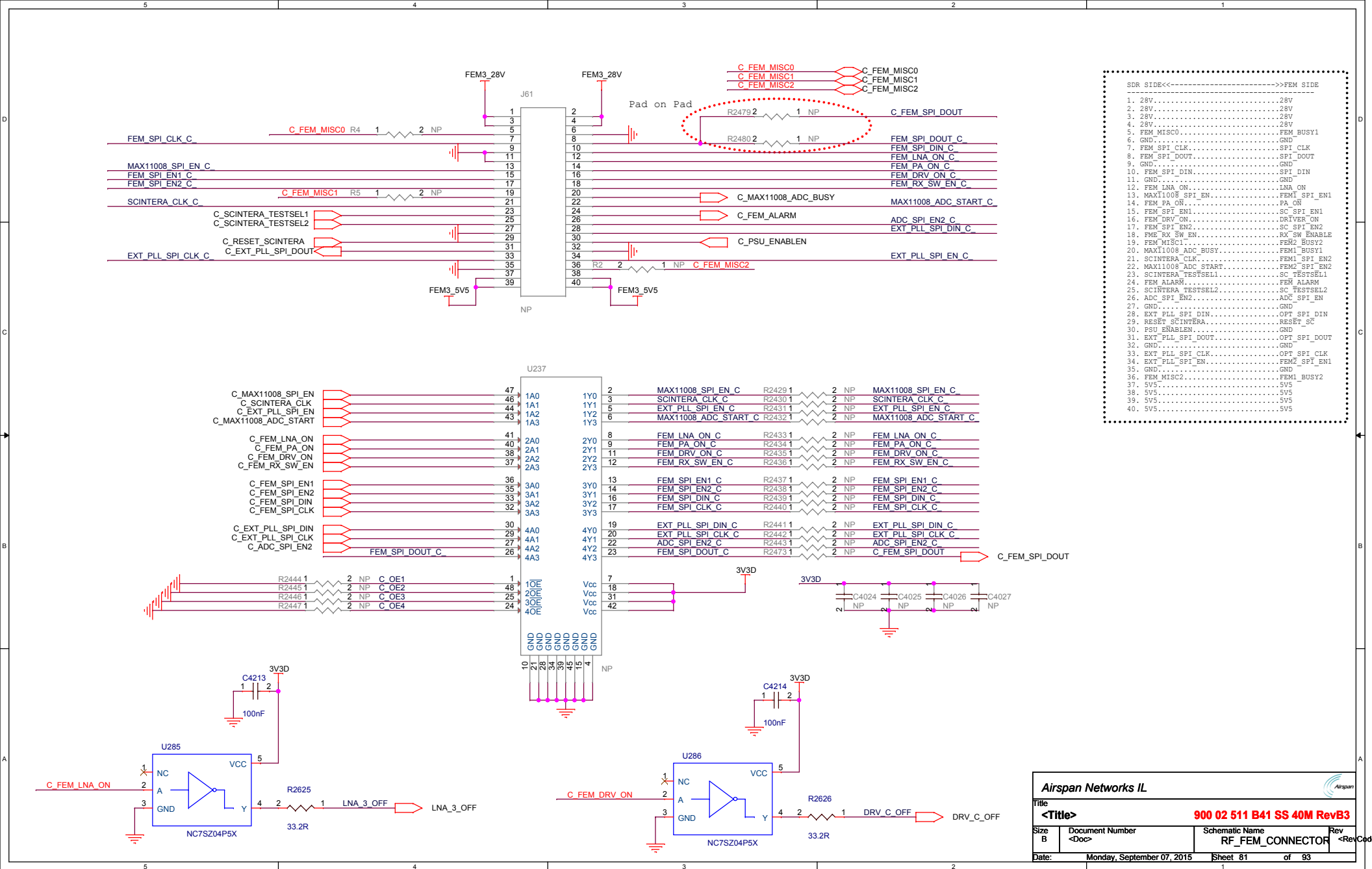


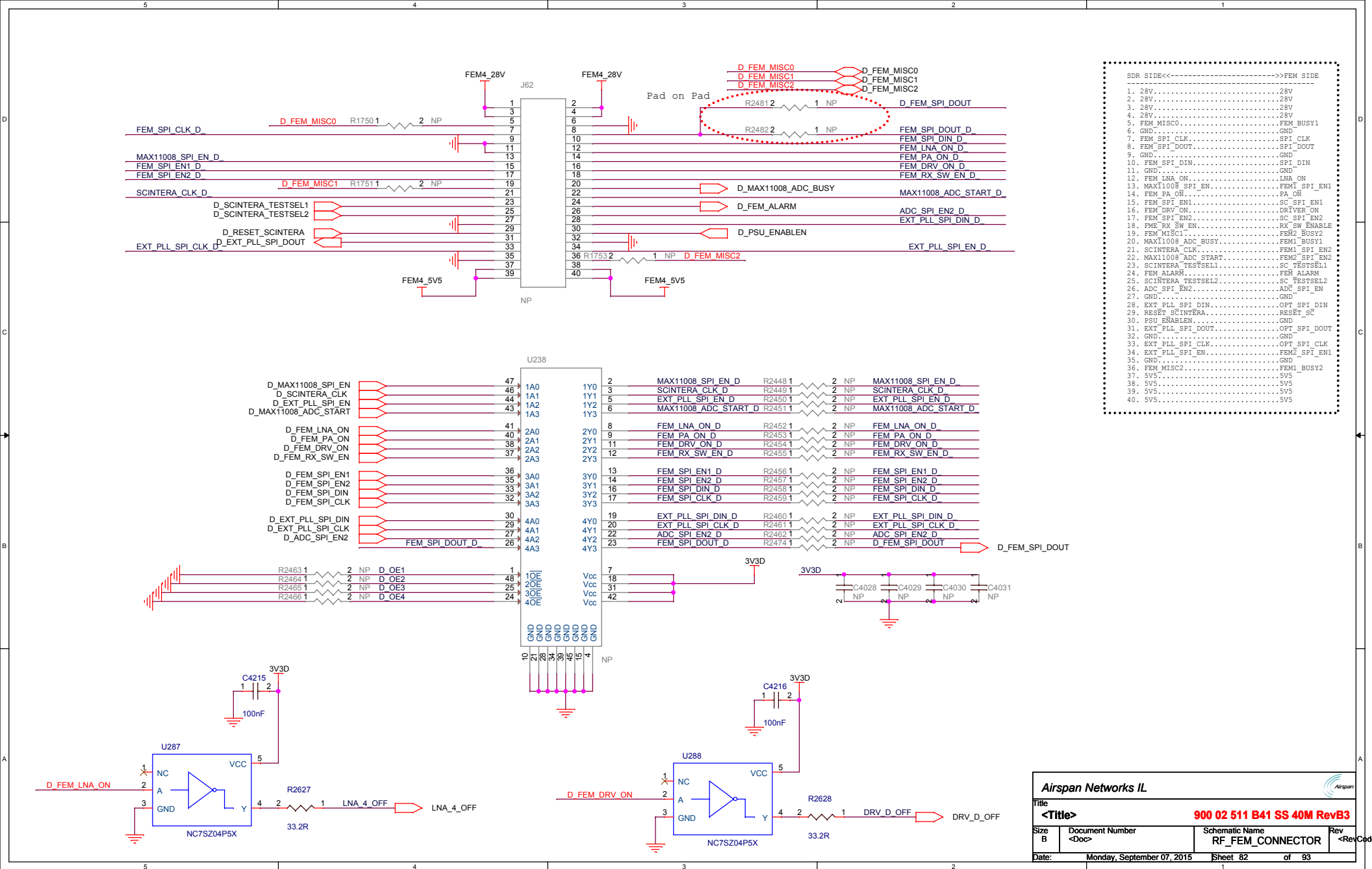


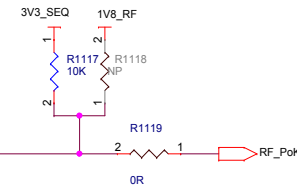
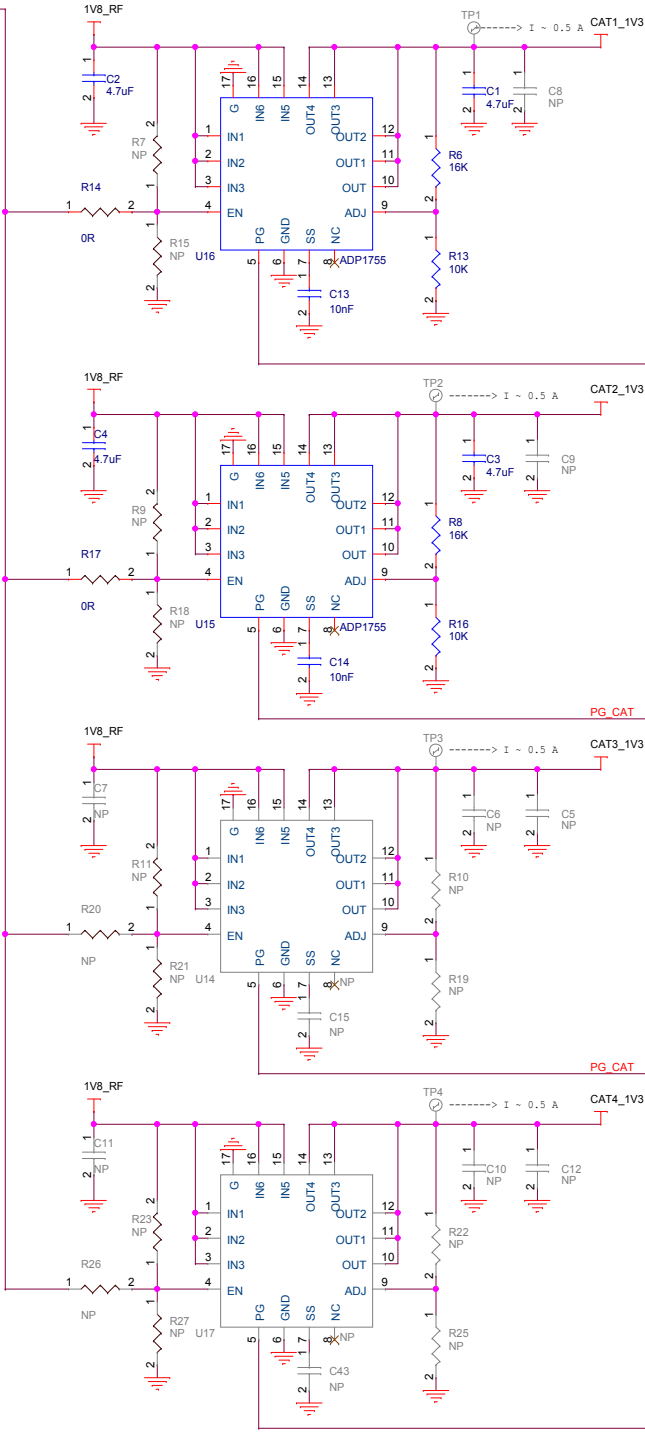
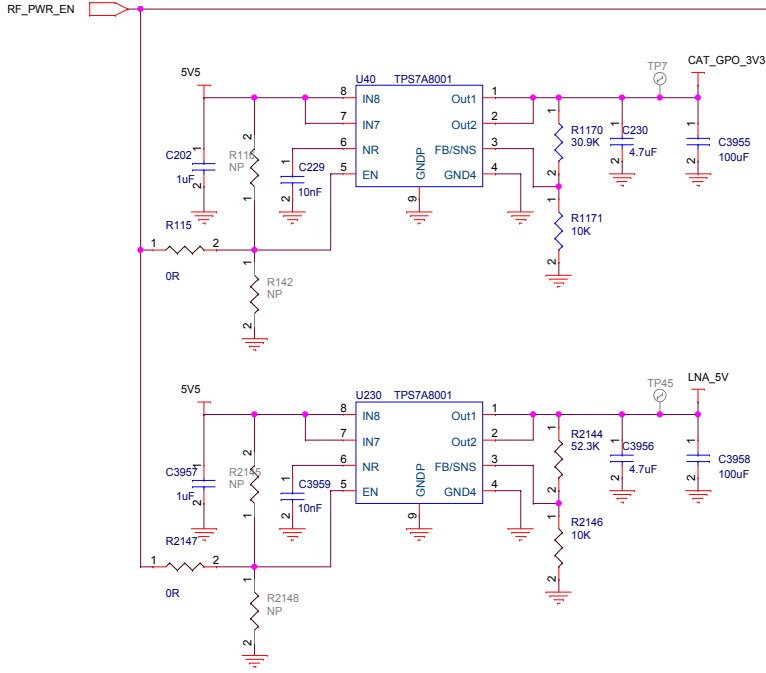


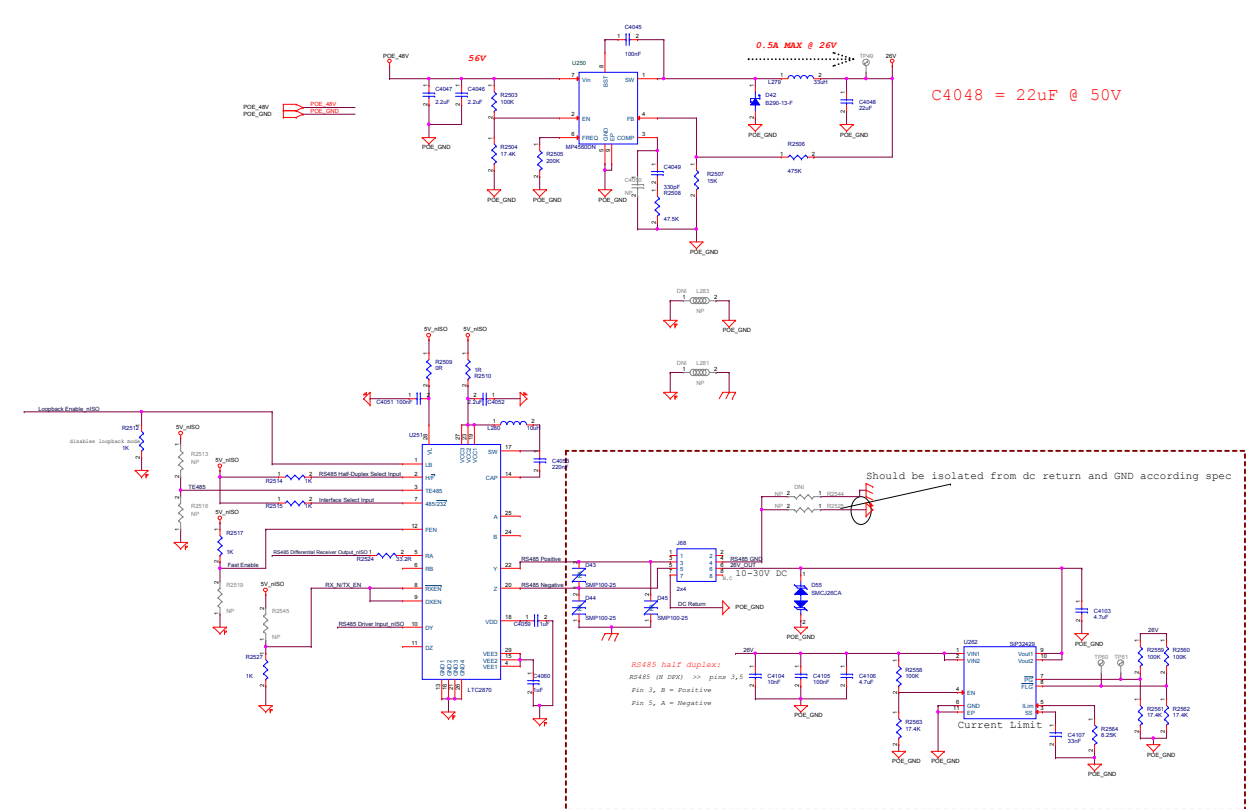
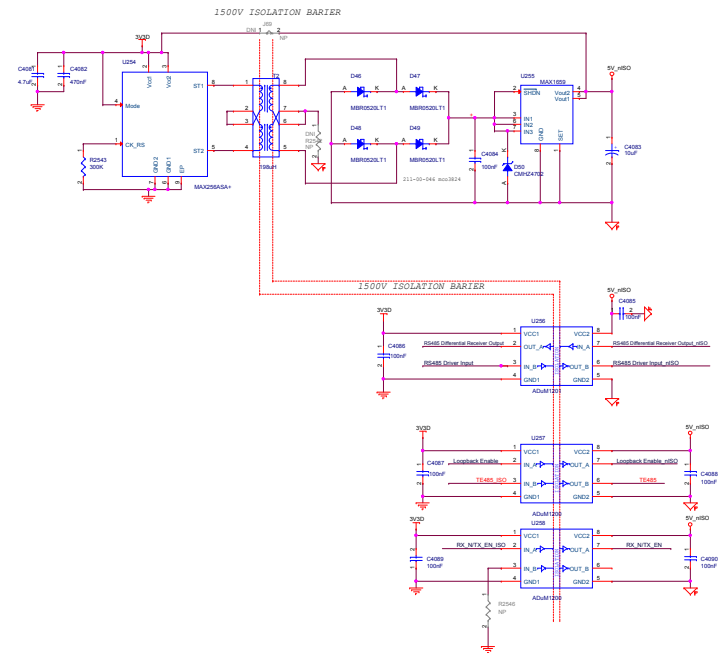


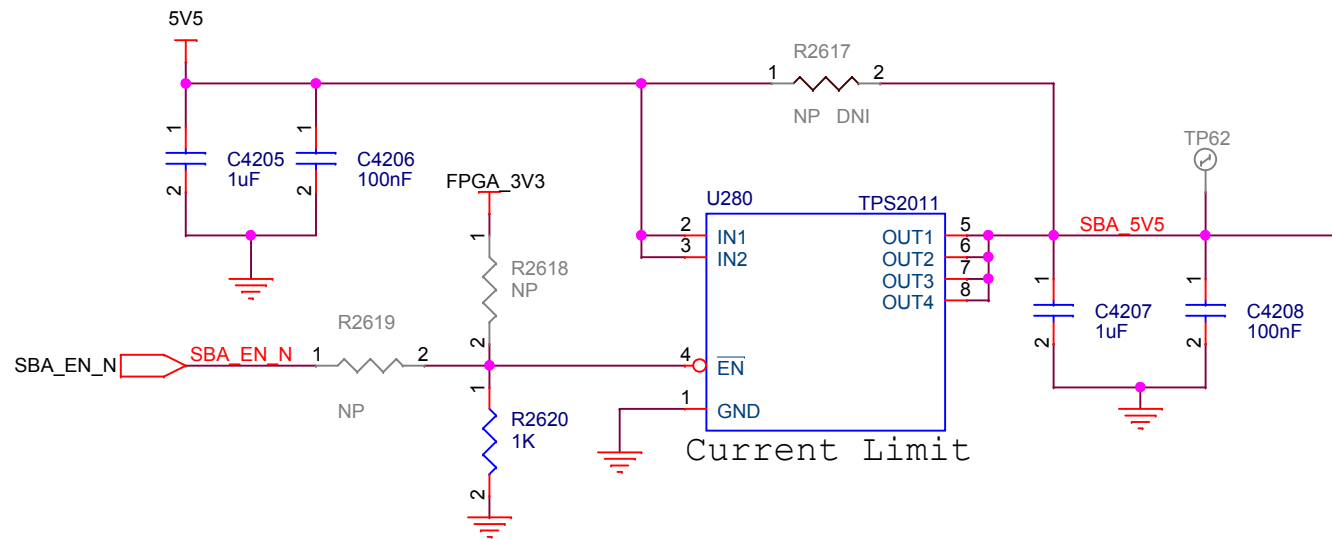
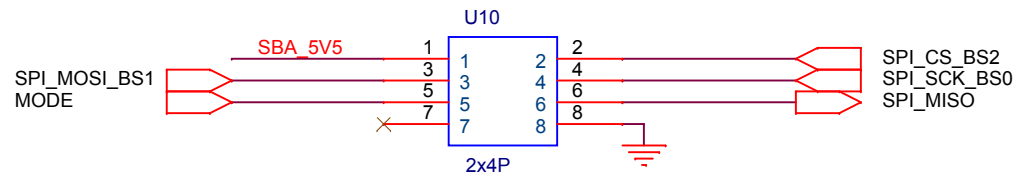












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