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# N720 Hardware User Guide

Version 1.3

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LET'S ENJOY WIRELESS LIFE

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| Revision Record | | |
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| V1.0 | • Initial draft | 2016-08 |
| V1.1 | • Added bands information of different areas | 2016-09 |
| V1.2 | • Modified pin the description | 2016-10 |
| V1.3 | • Modify the UIM card part and delete the UIM2 part<br>• Improve band information<br>• Modify part of the pin definition (the original pin78 RING, pin80 LIGHT are modified to pin13 RING, pin83 LIGHT. Pin13 and pin83 are NC)<br>• Modify part of description | 2016-12 |

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# 1 Introduction to N720

## 1.1 Overview

N720 is an industrial 4G module that is developed on Qualcomm platform. Its dimensions are 30mm x 28 mm x 2.8mm and it is with industrial-grade high-performance: ultra-wide operating temperature of -40 ℃ to +85 ℃, electrostatic capacity of 8KV. It is well applicable to electric terminals, in-vehicle computers, POS, industrial routers, and other IoT terminals with the following features:

- ARM Cortex-A7 processors, 1.2 GHz main frequency, 256 kB L2 cache, 28 nm
- GSM/GPRS/EDGE &WCDMA R99
- SIM/ADC/UART

N720 series include the following versions:

| Band | LTE | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Version | B1 | B2 | B3 | B4 | B5 | B7 | B8 | B9 | B12 | B17 | B19 | B20 | B28 | B38 | B39 | B40 | B41 |
| CN | • | | • | | • | | • | | | | | | | • | • | • | • |
| JP | • | | • | | | | • | • | | | • | | | | | | |
| EU | • | | • | | | • | • | | | | | • | | | | • | |
| US | | • | | • | • | • | | | • | • | | | | | | | |

| Band | UMTS | | | | | | | GSM | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Version | B1 | B2 | B4 | B5 | B8 | B9 | B19 | 850 | 900 | 1800 | 1900 |
| CN | • | | | | • | | | | • | • | |
| JP | • | | | | • | • | • | | | | |
| EU | • | | | | • | | | • | • | • | • |
| US | | • | • | • | | | | • | • | • | • |

NOTE

CN: China JP: Japan EU: Europe US：The United States

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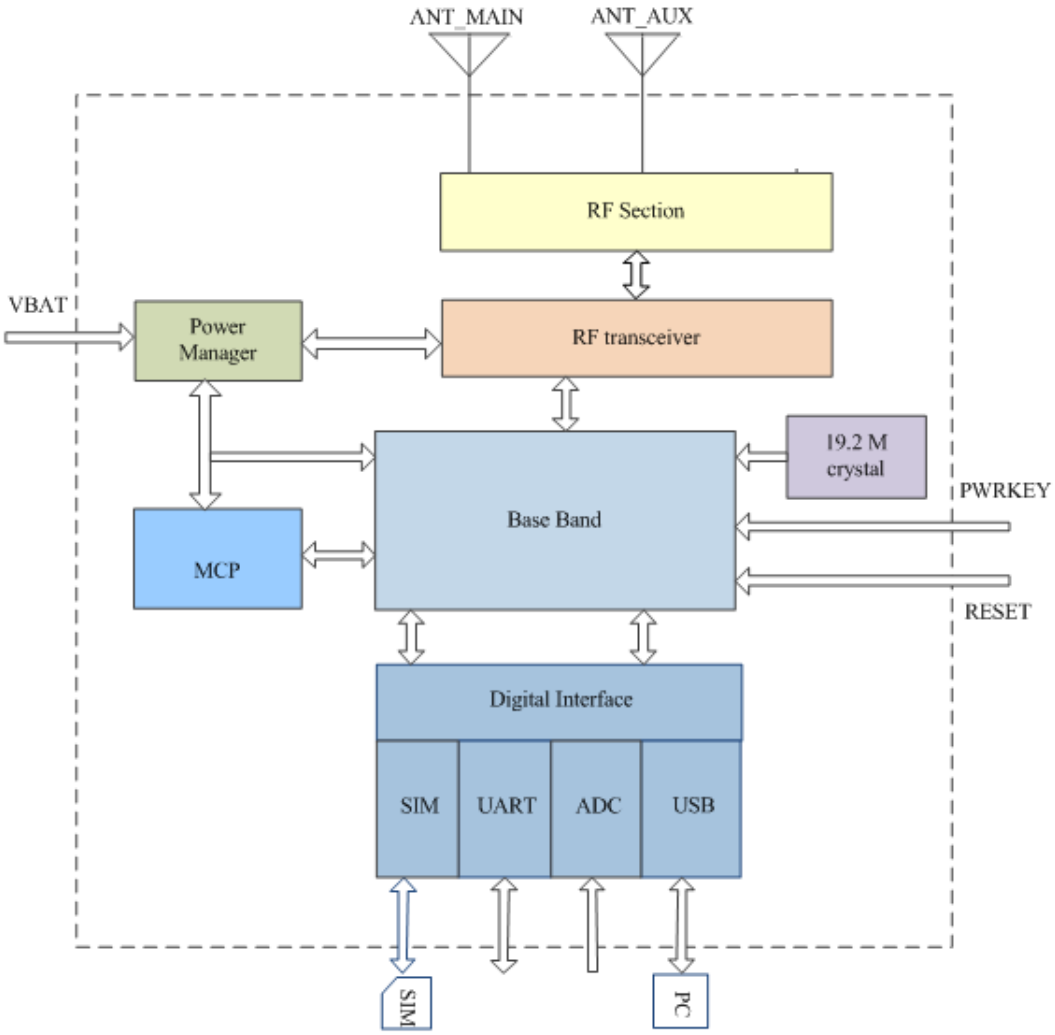
## 1.2 Block Diagram

Figure 1-1 shows the block diagram of N720 Modular only,

**Figure 1-1** N720 block diagram




## 1.3 Features

**Table 1-1** N720 baseband and wireless features

| Specifications | Description |
|---|---|
| Power supply | VBAT: 3.3V to 4.3V, TYP: 3.8 V |
| Current in sleep mode | 4mA |

| | |
|---|---|
| Temperature | Operating temperature: -40°C to +85°C |
| | Limited: -40°C to +85°C |
| | Storage temperature: -40°Cto +85°C |
| Processor | ARM Cortex-A7 processor<br>Main frequency: 1.2 GHz<br>256kB L2 cache |
| Band | **CN**:<br>• GSM/GPRS/EDGE:900M/1800M<br>• TD_SCDMA:B34/B39<br>• UMTS:B1/B8<br>• LTE-FDD B1/B3/B5<br>• LTE-TDD B38/B39/B40/B41<br>**JP**:<br>• UMTS: B1/B8/B9/B19<br>• FDD-LTE: B1/B3/B8/B9/B19<br>**EU**:<br>• GSM/GPRS/EDGE:850M/ 900M/1800M/1900M<br>• UMTS: B1/B8<br>• FDD-LTE: B1/B3/B5/B7/B8/B20<br>• TDD-LTE: B40；<br>**US**:<br>• GSM/GPRS/EDGE: 850M/1900M<br>• UMTS: B2/B4/B5<br>• FDD-LTE: B2/B4/B5/B7/B12/B17 |
| Rate | GSM:GPRS,EDGE<br>WCDMA:<br>LTE FDD: non-CA cat4, Max 150Mbps(DL)/Max 50Mbps(UL)<br>LTE TDD: non-CA cat4,Max 130Mbps(DL)/Max 35Mbps(UL) |
| Transmit power | GSM850: +34dBm (Power Class 4)<br>EGSM900: +34dBm (Power Class 4)<br>DCS1800: +31.5dBm (Power Class 1)<br>PCS1900: +31.5dBm (Power Class 1)<br>EDGE 850MHz: +28.5dBm (Power Class E2)<br>EDGE 900MHz: +28.5dBm (Power Class E2) |

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| | |
|---|---|
| | EDGE1800MHz: +27.5dBm (Power Class E2)<br>EDGE1900MHz: +27.5dBm (Power Class E2)<br>UMTS: 24dBm (Power Class 3)<br>LTE: +23dBm (Power Class 3) |
| Antenna feature | 50Ω impedance |
| UART | At most 4 Mbps, 1 group |
| UIM | 1 groups, 1.8V/3V dual-voltage adaptive |
| USB | 1 group of USB2.0 high-speed interface |
| ADC | 2 groups of 16-bit ADC, input voltage ranging from 0.1 to 1.7V |

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# 2 Application Interfaces

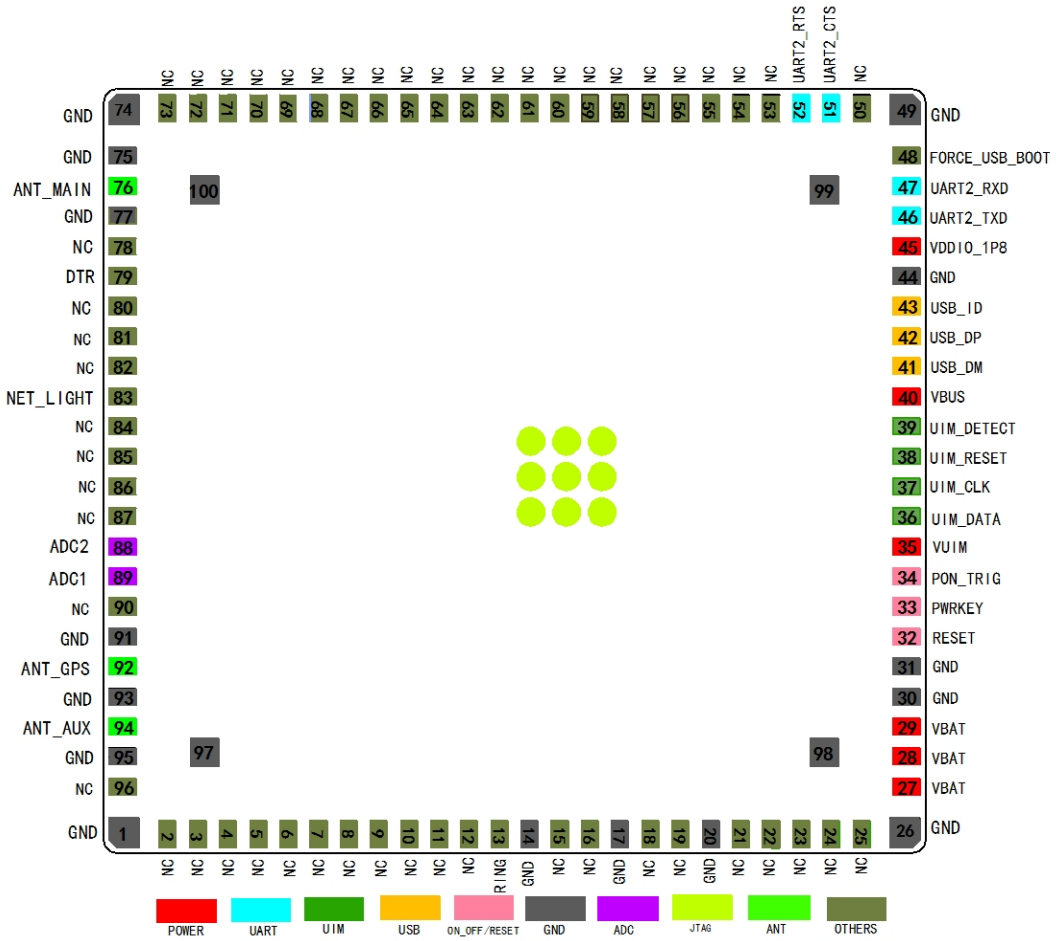
N720 adopts 100-pins LGA encapsulation.

## 2.1 Specifications and Pin Definition

**Table 2-1** N720 dimensions

| Specifications | N720 |
|---|---|
| Dimensions | 30mm*28 mm*2.8mm(H*W*D) |
| Weight | 5.1g |
| Package | 100-Pin LGA |

**Figure 2-1** Top view of N720



## 2.2 Pin Description

NOTE

IO: input/output

DI: Digital input

DO: Digital output

PI: Power input

PO: Power output

AI: Analog input

AO: Analog output

**Table 2-2** N720 pin description

| Name | Pin | I/O | Function | Level Feature (V) | Power Domain | Remarks |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| VABT | 27, 28, 29 | PI | Main power supply input | Vmax=4.3V | | The power supply can provide up to 3A current |
| VDDIO _1P8 | 45 | PO | 1.8 V power supply output | Vnorm=1.8V;<br>Imax=100mA | 1.8V | Supply power for IO level shifting circuit. Leave it disconnected if you do not use it. |
| GND | 1, 14, 17, 20, | | GND | | | |

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| | | | | | | |
|---|---|---|---|---|---|---|
| | 26, 30, 31, 44, 49, 74, 75, 77, 91, 93, 95, 97, 98, 99, 100 | | | | | |
| **Power on/off and reset** | | | | | | |
| RESET | 32 | DI | Reset input | $V_{IL}$ min=-0V; $V_{IL}$ max=0.5V; $V_{IH}$ min=1.2V; $V_{IH}$ max=2.1V; | 1.8V | Low level triggers the ON status and can control the power off and reset. |
| PWRKEY | 33 | DI | Power ON/OFF | | 1.8V | Low level triggers the ON status.<br>It is pulled up by an internal 200 KΩresistor. |
| PON_TRIG | 34 | DI | PON_TRIG | | 1.8V | High level triggers the ON status.<br>It is pulled up by an internal 200 KΩresistor.<br>Ground it if you do not use it. |
| **UART** | | | | | | |
| UART2_TXD | 46 | DO | UART data transmit | $V_{OL}$ max=0.45V; $V_{OH}$ min=1.35V; | 1.8V | Data communication<br>Leave them disconnected if you do not use them. |
| UART2_RXD | 47 | DI | UART data receive | $V_{IL}$ min=-0.3V; | 1.8V | |

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| | | | | | | |
|---|---|---|---|---|---|---|
| | | | | $V_{IL}$ max=0.45V;<br>$V_{IH}$ min=1.35V;<br>$V_{IH}$ max=2.1V | | |
| UART2_CTS | 51 | DI | Clear to send | $V_{OL}$ max=0.45V;<br>$V_{OH}$ min=1.35V; | 1.8V | Leave it disconnected if you do not use it. |
| UART2_RTS | 52 | DO | Request to send | $V_{IL}$ min=-0.3V;<br>$V_{IL}$ max=0.45V;<br>$V_{IH}$ min=1.35V;<br>$V_{IH}$ max=2.1V | 1.8V | Leave it disconnected if you do not use it. |
| **UIM** | | | | | | |
| VUIM | 35 | PO | UIM power supply output | 1.8V USIM:<br>Vmax = 1.9V ;<br>Vmin = 1.7V;<br>3V USIM:<br>Vmax = 3.05V;<br>Vmin = 2.7V;<br>IO max =50mA | 1.8V/3V | Compatible with 1.8/3V UIM card |
| UIM_RESET | 38 | DO | UIM reset | 1.8V USIM:<br>$V_{OL}$ max = 0.45V;<br>$V_{OH}$ min = 1.35V;<br>3V USIM: | 1.8V/3V | |

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| | | | | | | |
|---|---|---|---|---|---|---|
| | | | | $V_{OL}$ max = 0.4V;<br>$V_{OH}$ min = 2.6V; | | Compatible with 1.8/3V UIM card |
| UIM_DATA | 36 | IO | UIM data input, output | 1.8V USIM:<br>$V_{IL}$ max = 0.6V;<br>$V_{IH}$ min = 1.2V;<br>$V_{OL}$ max = 0.45V;<br>$V_{OH}$ min = 1.35V;<br>3V USIM:<br>$V_{IL}$ max = 0.8V<br>$V_{IH}$ min = 1.95V<br>$V_{OL}$ max = 0.45V<br>$V_{OH}$ min = 2.6V | 1.8V/3V | |
| UIM_CLK | 37 | DO | UIM clock output | 1.8V USIM:<br>$V_{OL}$ max = 0.45V<br>$V_{OH}$ min = 1.35V<br>3V USIM:<br>$V_{OL}$ max = 0.4V<br>$V_{OH}$ min = 2.6V | 1.8V/3V | |
| UIM_DETECT | 39 | DI | UIM detect | $V_{IL}$ min = -0.3V<br>$V_{IL}$ max = 0.63V | 1.8V | |
| **USB** | | | | | | |

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| | | | | | | |
|---|---|---|---|---|---|---|
| USB_DM | 41 | IO | USB data negative signal | USB2.0 | | Used for firmware download and data transmission<br>Differential trace for DM and DP<br>90Ω impedance resistance |
| USB_DP | 42 | IO | USB data positive signal | USB2.0 | | |
| VBUS | 40 | PI | USB voltage test | 3.3V~5.2V, typically 5V | | |
| USB _ID | 43 | AI | Identify host and device | | 1.8V | Leave it disconnected if you do not use it. |
| **ADC** | | | | | | |
| ADC2 | 88 | AI | Analog-to-digital signal conversion | Vmax=1.7V<br>Vmin=0.1V | 1.8V | 16-bit, detectable voltage range: 0.1 V to 1.7 V |
| ADC1 | 89 | AI | Analog-to-digital signal conversion | Vmax=1.7V<br>Vmin=0.1V | 1.8V | |
| **Network LED Indicator** | | | | | | |
| NET_LIGHT | 83 | DO | Indicate network status | $V_{OL}$ max=0.45V;<br>$V_{OH}$ min=1.35V; | 1.8V | Leave it disconnected if you do not use it. |
| **Sleep Mode Control** | | | | | | |
| DTR | 79 | DI | Sleep mode control | $V_{IL}$ min=-0.3V;<br>$V_{IL}$ max=0.45V;<br>$V_{IH}$ min=1.35V;<br>$V_{IH}$ max=2.1V | 1.8V | Leave it disconnected if you do not use it. |
| **RING** | | | | | | |

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| | | | | | | |
|---|---|---|---|---|---|---|
| RING | 13 | DO | Incoming call ring | $V_{OL}$ max=0.45V;<br>$V_{OH}$ min=1.35V; | 1.8V | Leave it disconnected if you do not use it. |
| **Other Pins** | | | | | | |
| FORCE_USB_BOOT | 48 | DI | Force to download and upgrade control pin | $V_{IL}$ min=-0.3V;<br>$V_{IL}$ max=0.45V;<br>$V_{IH}$ min=1.35V;<br>$V_{IH}$ max=2.1V | 1.8V | Leave it disconnected if you do not use it. |
| ANT_MAIN | 76 | | Main antenna | | | 50 Ω impedance |
| ANT_GPS | 92 | | GPS antenna | | | 50 Ω impedance |
| ANT_AUX | 94 | | 4Gdiversity aerial | | | 50 Ω impedance |
| NC | 2、3、4、5、6、7、8、9、10、11、12、15、16、18、19、21、22、23、24、25、50、53、54、55、56、57、58、59、60、61、62、63、64、65、66、67、68、69、70、71、72、 | | NC | | | Leave them disconnected.<br>Do not use them. |

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| | | | | | | |
|---|---|---|---|---|---|---|
| | 73、78、80、81、82、84、85、86、87、90、96 | | | | | |

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## 2.3 Power Control Interfaces

| Name | Pin | I/O | Function | Remarks |
|---|---|---|---|---|
| VABT | 17/18/19 | P | Main power supply input | 3.3 V to 4.3 V (TYP: 3.8 V ) |
| VDDIO_1P8 | 45 | P | 1.8 V power supply output | Supply power for IO level shifting circuit.<br>Load capability: <100 mA<br>Advise to add ESD to protect while using. |
| RESET | 32 | DI | Reset input | Low level |
| PON_TRIG | 34 | DI | PON_TRIG | High level triggers the ON status |
| PWRKEY | 33 | DI | Power ON/OFF | Low level triggers the ON status |

### 2.3.1 VBAT

VBAT is the power supply input pin of the module. Its input voltage ranges from 3.3 V to 4.3 V and the preferable value is 3.8V. In addition to baseband, it supplies power for RF power amplifier. The performance of the VBAT power supply is a critical path to module's performance and stability. The peak input current at the VBAT pin can be up to3A when the signal is weak and the module works at the maximum transmitting power. The voltage will encounter a drop in such a situation. The module might restart if the voltage drops lower than 3.3 V.

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**Figure 2-2** Current peaks and voltage drops

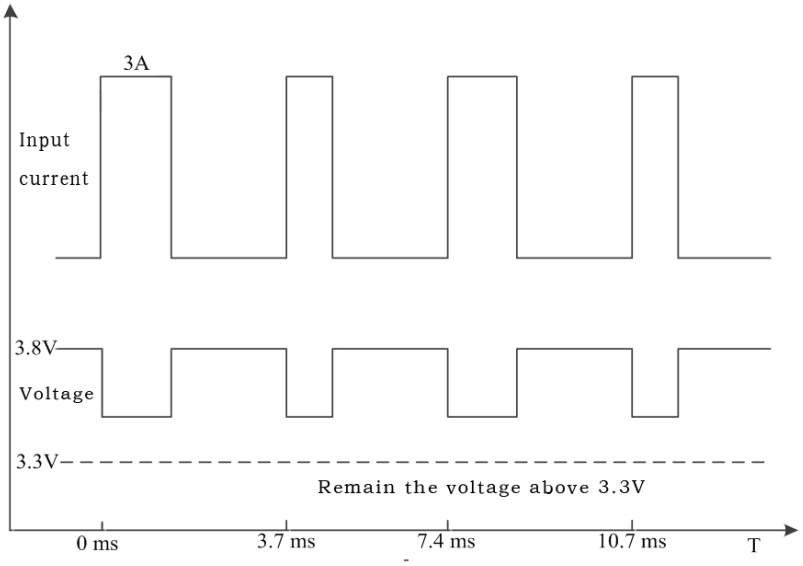
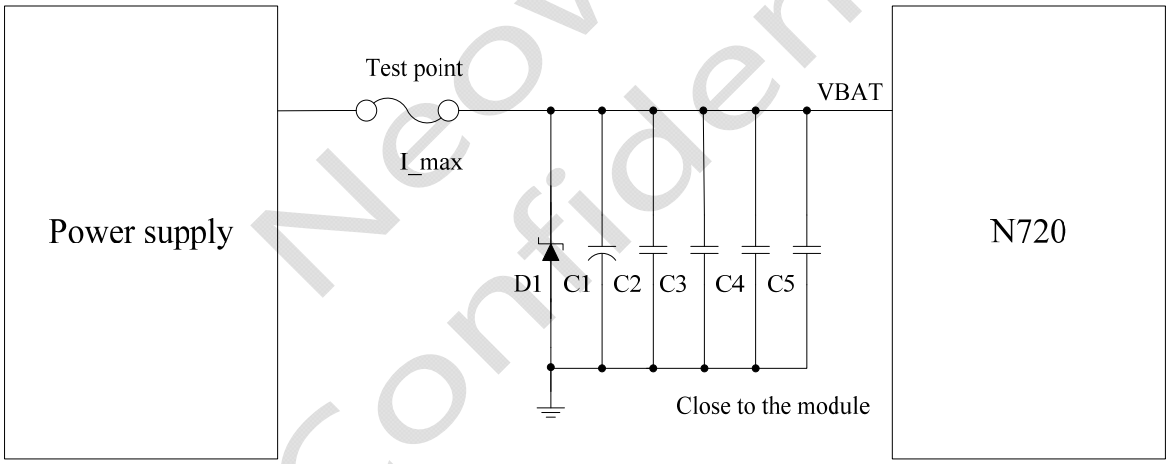



Figure 2-3 shows the reference design of the VRTC power supply.

**Figure 2-3** Capacitors used for the power supply




In Figure 2-3, you can use TVS at D1 to enhance the performance of the module during a burst. SMF5.0AG (Vrwm=5V&Pppm=200W) is recommended. A large bypass tantalum capacitor (220 μF or 100 μF) or aluminum capacitor (470 μF or 1000 μF) is expected at C1 to reduce voltage drops during bursts together with C2 (10-μF ceramics capacitor). It is recommended that you add 0.1 μF, 100 pF, and 33 pF filter capacitors to enhance the stability of the power supply.

The module might fail to reset or power on/off**in remote or unattended applications, or in an environment with great electromagnetic interference (EMI)**. A controllable power supply is

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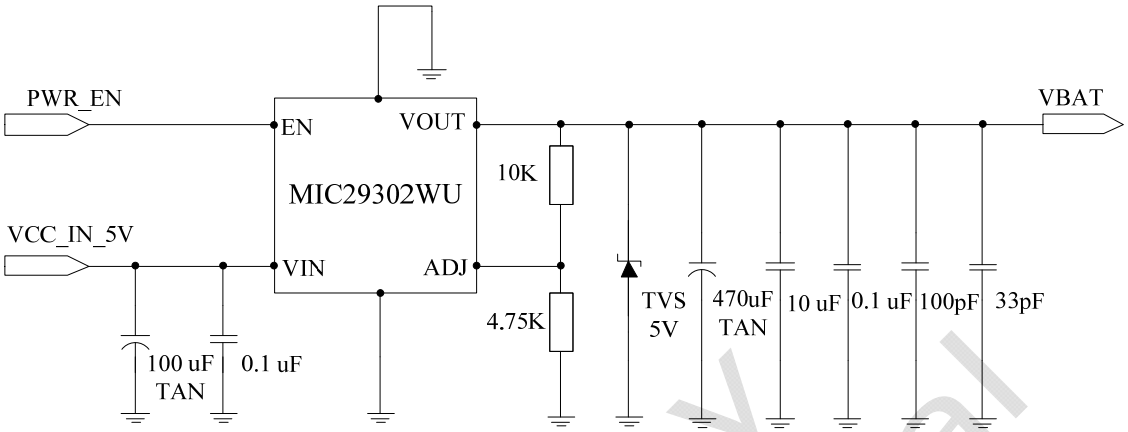
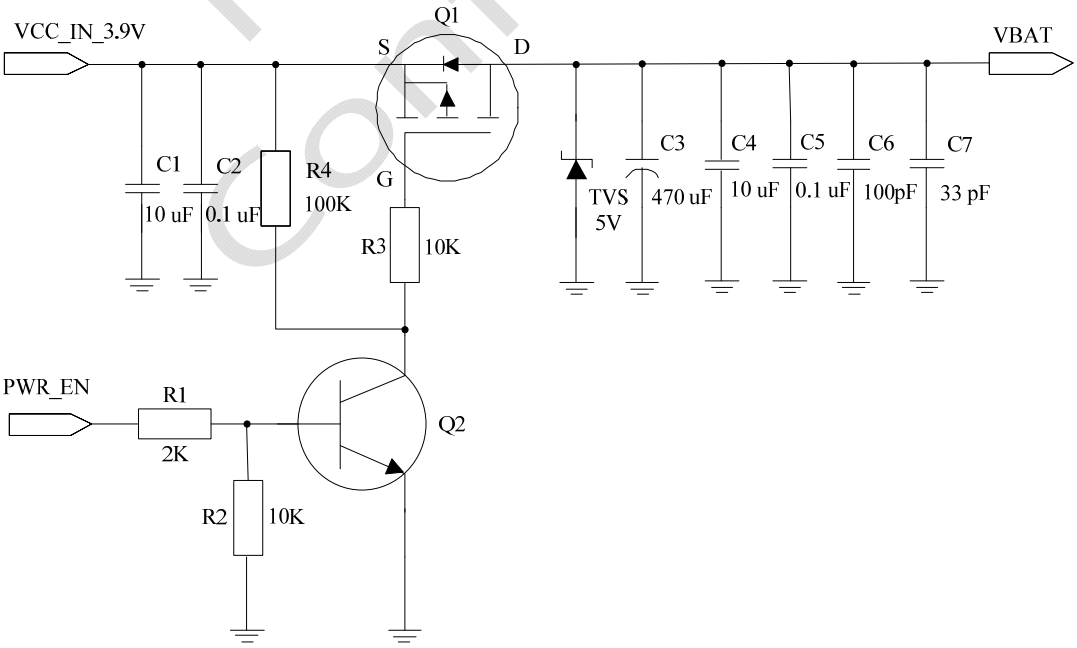
preferable if used in harsh conditions. You can use the EN pin on the LDO or DC/DC chipset to control the switch of the power supply as shown inFigure 2-4if a 5V power supply is used. MIC29302WU in Figure 2-4 is an LDO and outputs 3 A current to ensure the performance of the module.

**Figure 2-4** Reference design of power supply control




The alternative way is to use an enhancement mode p-MOSFET to control the module's power, as shown inFigure 2-5. When the external MCU detects the exceptions such as no response from the module or the disconnection of GPRS, power off/on can rectify the module exceptions. InFigure 2-5, the module is turned on when PWR_EN is set to high level.

**Figure 2-5** Reference design of power supply controlled by p-MOSFET

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Q2 is added to eliminate the need for a high enough voltage level of the host GPIO. In case that the GPIO can output a high voltage greater than VCCIN - |VGS(th)|, where VGS(th) is the Gate Threshold Voltage, Q2 is not needed.

Reference components:

- Q1 can be IRML6401 or low Rds(on) pMOSFET, which has higher, withstand voltage and drain current.
- Q2: a common NPN tripolar transistor, e.g. MMBT3904; or a digital NPN tripolar transistor, e.g. DTC123. If digital tripolar transistor is used, delete R1 and R2.
- C3: 470-μF tantalum capacitor rated at 6.3V, or 1000 μF aluminum capacitor. If lithium battery is used to supply power, C3 can be 220-μF tantalum capacitor.

## Power Supply Protection

Add TVS diodes (VRWM=5 V) on the VBAT power supply, especially in automobile applications. For some stable power supplies, Zener diodes can decrease the power supply overshoot. SMF5.0AG from ONSEMI is an option.

## Line Rules

The width of primary loop lines for VBAT on PCB must be able to support the safe transmission of 2 A current and ensure no obvious loop voltage decrease. Therefore, the loop line width of VBAT is required 2 mm and the ground level should be as complete as possible.

## Separation

The module works in burst mode that generates voltage drops on power supply. Furthermore, this results in a 217Hz TDD noise through power (One of the way generating noise. Another way is through RF radiation). Analog parts, especially the audio circuits, are subjected to this noise, known as a "buzz noise" in GSM systems. To prevent other parts from being affected, it is better to use separated power supplies. The module shall be supplied by an independent power, like a DC/DC or LDO. SeeFigure 2-6.

DC/DC or LDO should output rated peak current larger than 2 A.

The inductor used in Reference Design (b), should be a power inductor and have a very low resistance. The value of 10 μH, with average current ability greater than 1.2A and low DC resistance, is recommended.

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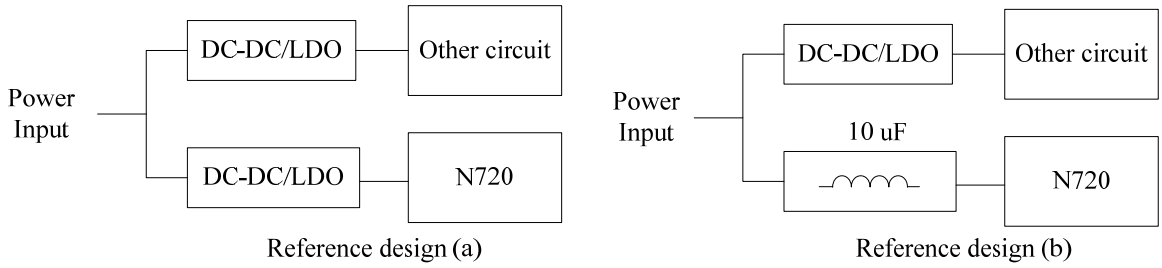
**Figure 2-6** Reference designs of separated power supply




**WARNING**

Never use a diode to make the drop voltage between a higher input and module power. Otherwise, Neoway will not provide warranty for product issues caused by this. In this situation, the diode will obviously decrease the module performances, or result in unexpected restarts, due to the forward voltage of diode will vary greatly in different temperature and current.

### EMC Considerations for Power Supply

Place transient overvoltage protection components like TVS diode on power supply, to absorb the power surges. SMAJ5.0A/C could be a choice.

## 2.3.2 VDDIO_1P8

VDDIO_1P8 supports output voltages of 1.8V. It is recommended that VDDIO_1.8V@100mAbe used only for interface level shifting and to add ESD to protect while using.

## 2.3.3 ON/OFF

### Power-On

After powering on the VBAT pin, you can use PWRKEY to start the module by inputting low-level pulse for 100 ms (200 ms is recommended). This pin is pulled up by 200Ω internally. Its typical high-level voltage is 1.8 V. The following circuit Figure 2-7 or Figure 2-8 is recommended to control PWRKEY.

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**Figure 2-7** Push switch controlling

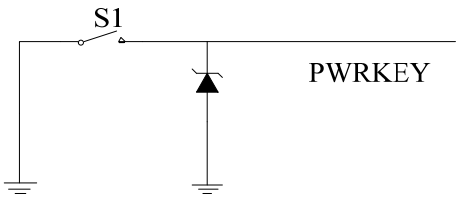
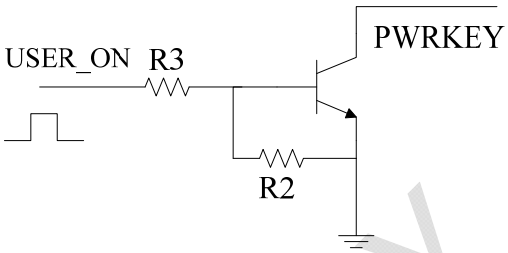
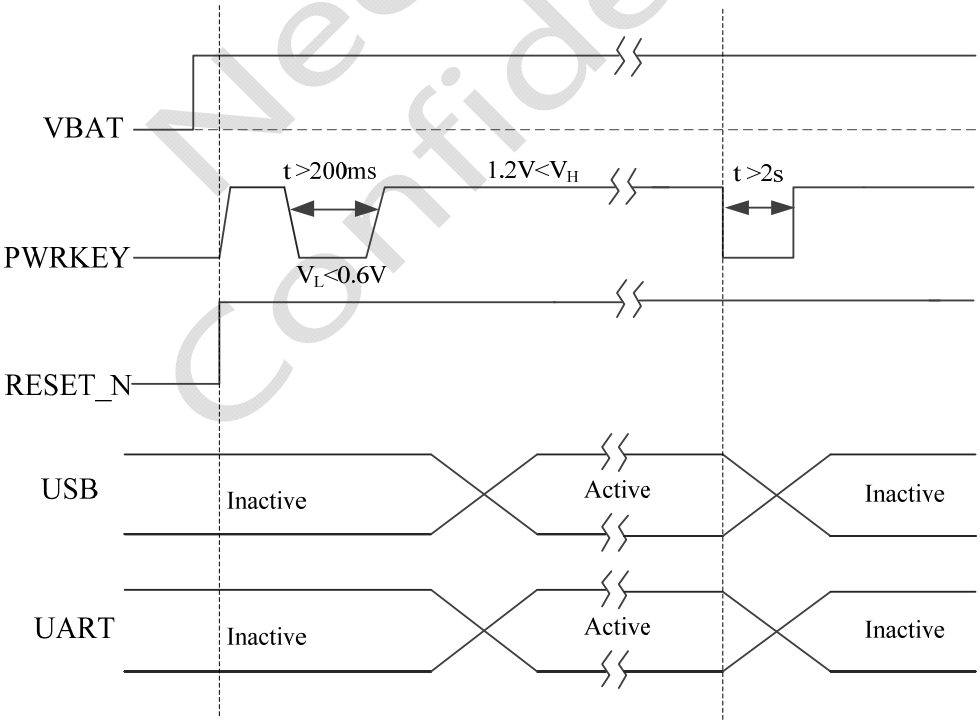



**Figure 2-8** MCU controlling




If the module is powered on but the power-on sequence has not been completed, the states of each pin are uncertain. The power-on sequence of the module is shown in Figure 2-9.

**Figure 2-9** N720 power-on/off sequence




If your application does not require ON/OFF control, you can pull the PWRKEY pin down to GND through 1.5K resistor. Then the module can start automatically after it is powered on. If you do

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not use the PWRKEY pin, it must be left disconnected. The PON_TRIG pin can trigger the ON status of the module by high level.

### Power-off

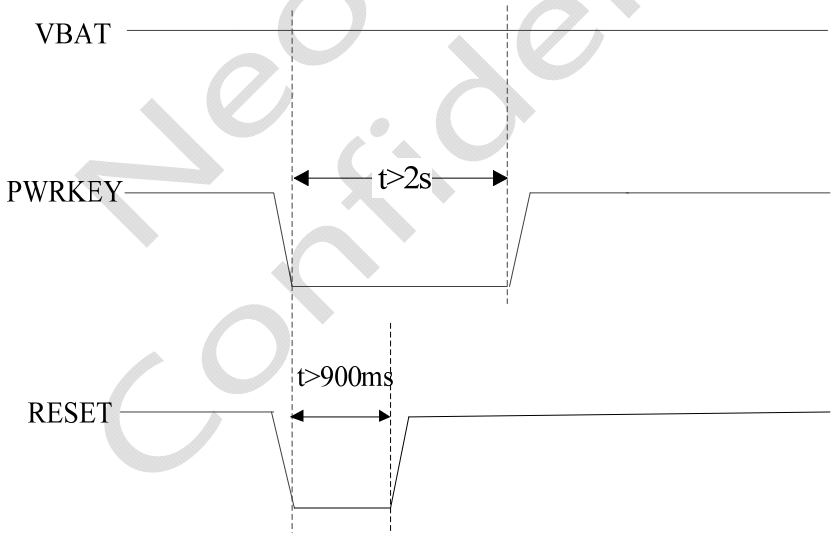
Power off can be achieved through two methods, one is to use PWRKEY input pin; the other is to use RESET pin.

1. Use PWRKEY pin. Low-level pulse input for 2 seconds can trigger the power-off status of the module. This pin is pulled up internally. Its typical high-level voltage is 1.8 V. Leave this pin disconnected if you do not use it.

2. Use RESET pin. Input more than 900ms low pulse when the module is at working status can trigger the module power off.

If 2.8V / 3.3V IO system is used, it is recommended to use external triode isolation. For details, refer to Section 2.3.4 RESET Pin Descriptions. Figure 2-10 shows the hard power-off sequence.

**Figure 2-10** N720 power-off sequence




## 2.3.4 RESET

The RESET pin is used to reset and power off the module. It triggers module reset when you input low-level pulse less than 900ms and the module will power off when input low-level pulse more than 900ms. (One second is recommended.). This pin is pulled up internally. Its typical

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high-level voltage is 1.8 V. Leave this pin disconnected if you do not use it. If you use a 2.8V/3.3V IO system, it is recommended that you add a triode to separate it. Refer to the following design.

**Figure 2-11** Reset controlled by button

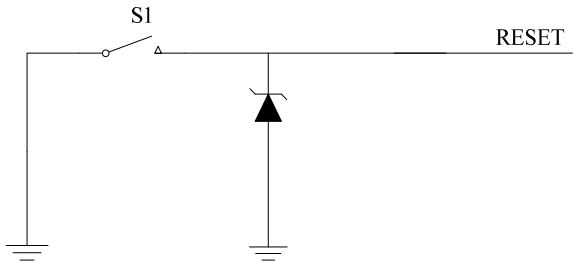
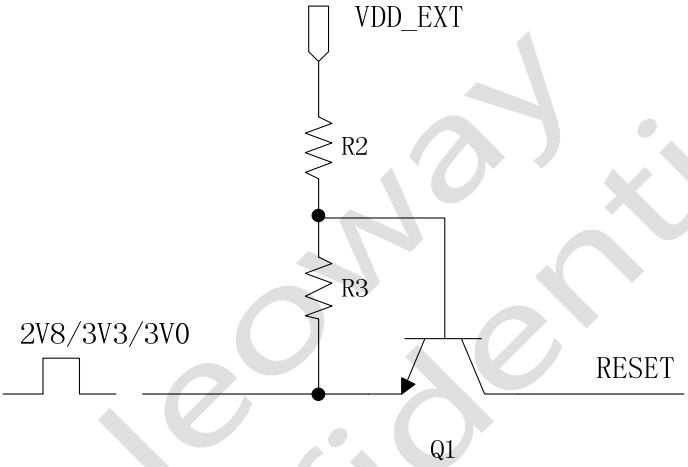



**Figure 2-12** Reset circuit with triode separating

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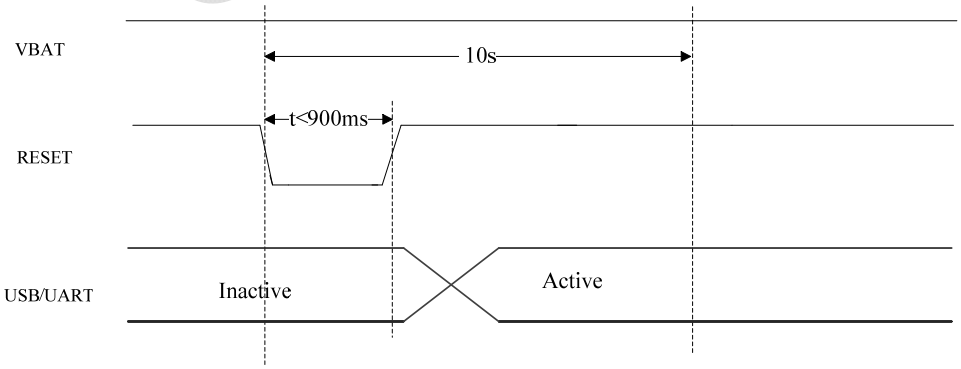
In a circuit shown in Figure 2-12, VDD_EXT=2.8V/3.3V/3.0V, R2=4.7K, R3=47K. Figure 2-13 shows the reset sequence.

**Figure 2-13** N720 reset sequence

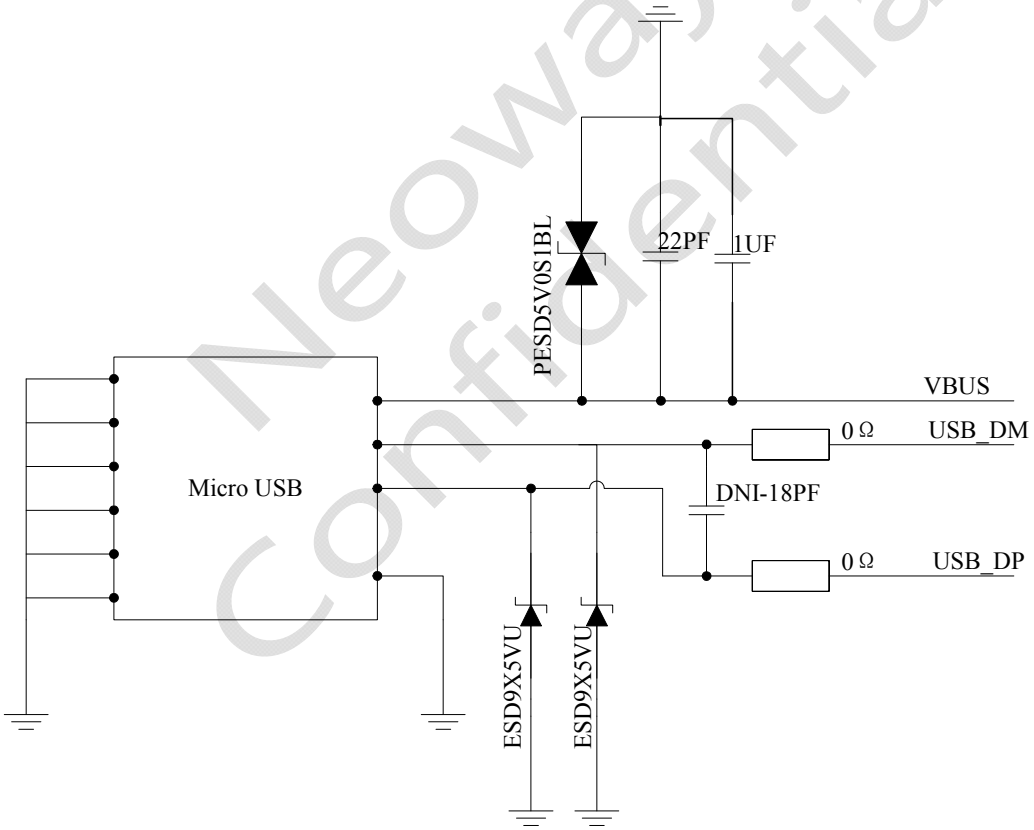


## 2.4 USB Interface

| Name | Pin | I/O | Function | Remarks |
|---|---|---|---|---|
| VBUS | 40 | P | USB voltage test | 3.3V~5.2V, typically 5V |
| USB_DM | 41 | IO | USB data negative signal | USB2.0, used for firmware download and data transmission |
| USB_DP | 42 | IO | USB data positive signal | |

You can download programs for N720 and establish data communication for commissioning through the USB interface. If the module is used only as USB Device, the recommended USB circuit is shown in Figure 2-14.

**Figure 2-14** USB circuit

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Parallel a 1μF and 22pF filter capacitors to the VBUS pin as close to the pin as possible. TVS components are required for the VBUS power line. The junction capacitance of the TVS protection diodes for USB_DP and USB_DM should be lower than 12pF as possible. USB data

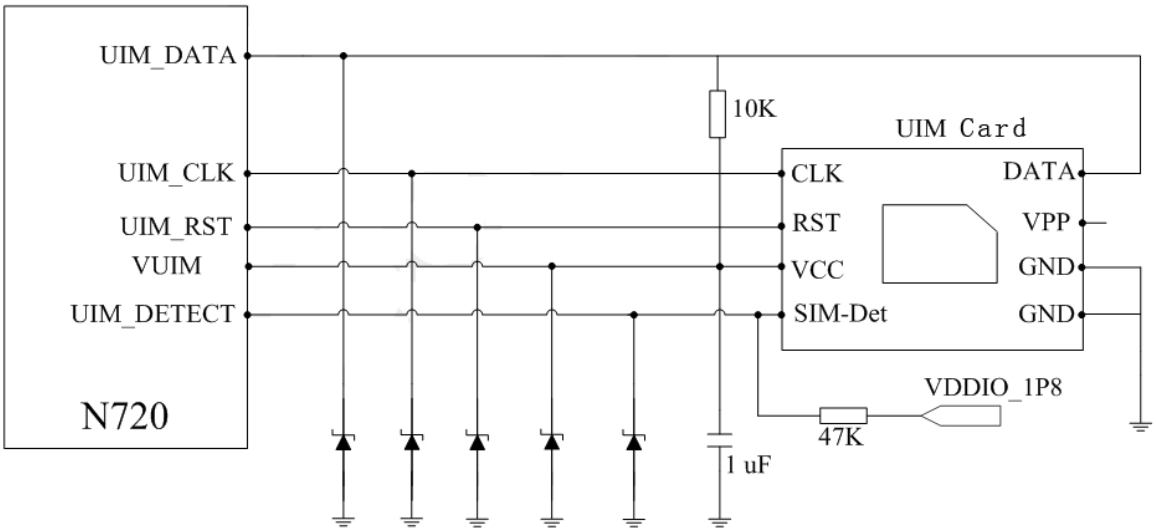
lines adopt differential trace design, in which the differential impedance is limited to 90 Ω characteristics impedance. Isolate the traces from other signal traces.

## 2.5 UIM Card Interface

| Name | Pin | I/O | Function | Remarks |
|---|---|---|---|---|
| VUIM | 35 | PO | UIM power supply output | Compatible with 1.8/3 V UIM card |
| UIM_DATA | 36 | IO | UIMdata I/O | A 10K resistor is required between VUIM and UIM-DATA. |
| UIM_CLK | 37 | DO | UIMclock output | |
| UIM_RESET | 38 | DO | UIMreset | |
| UIM_DETECT | 39 | DI | UIM detect | Advise to use a pull-up resistor |

N720 supports 1.8V/3V UIM cards.. VUIM is the power supply pin of the UIM card and its maximum load is 30 mA. The UIM_DATA pin is not pulled up internally, so you need to reserve external pull-up resistor in your design. UIM_CLK is the clock signal pin, supporting 3.25 GHz of clock frequency. Figure 2-15 shows the reference design of the UIM card interface.

**Figure 2-15** Reference design of SIM card interface

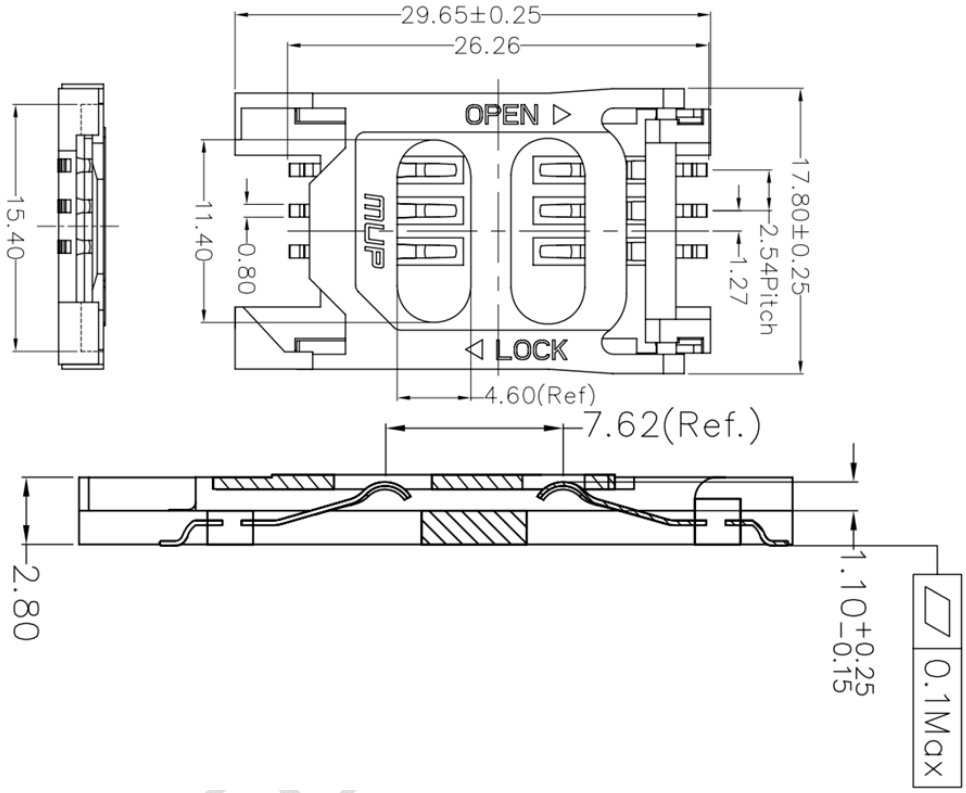


ESD protectors, such as ESD diodes or ESD varistors (with a junction capacitance of less than 33 pF), are recommended to be added on the SIM signals, especially in automotive electronics or other applications with badly ESD. Replace the ESD diodes with 27 pF to 33 pF capacitors connecting to GND in common applications. The ESD diodes or small capacitors should be close to UIM card.

N720 supports SIM card detection. UIM_DETECT is 1.8V interrupt pins. Low level means UIM card detected while high level mean no UIM card detected.

If you apply N720 to some electric terminals, MUP-C713(H2.8) is recommended.

**Figure 2-16** Encapsulation




**CAUTION**

The antenna should be installed far away from the UIM card and UIM card traces, especially to the build-in antenna.

The UIM traces on the PCB should be as short as possible and shielded with GND copper.

The ESD protection diodes or small capacitors should be close to UIM card on the PCB.

## 2.6 GPIO

N720supports UART. You can configure the GPIO to meet your requirements for connecting to different devices. For the open multi-function GPIO interface, please inquiry our technical support engineers. The level of the module interface is 1.8 V. Table 2-3lists GPIO pins.

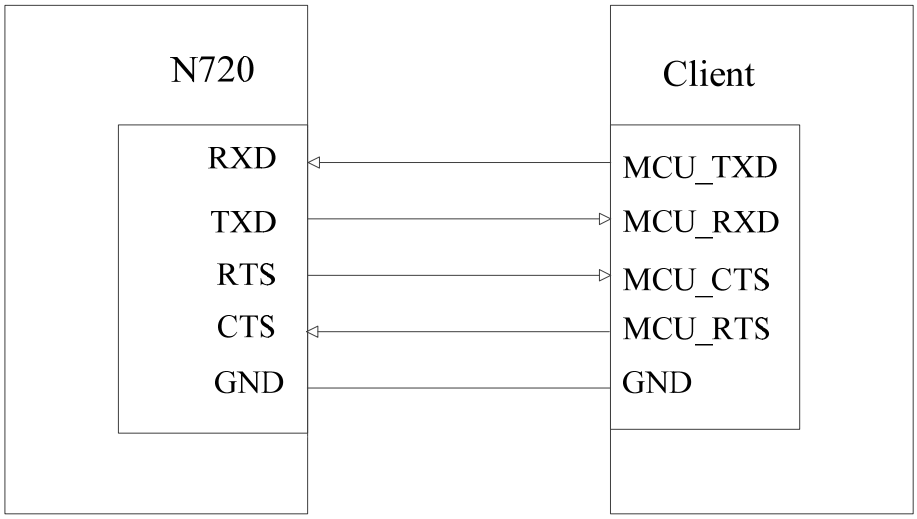
**Table 2-3** GPIO

| Name | Pin | I/O | Function | Remarks |
|---|---|---|---|---|
| UART2_TXD | 46 | DO | UART data transmit | Data communication |
| UART2_RXD | 47 | DI | UART data receive | |
| UART2_CTS | 51 | DI | Clear to send | |
| UART2_RTS | 52 | DO | Request to send | |
| ADC2 | 88 | AI | ADC2input | 16-bit, detectable voltage range: 0.1 V to 1.7 V |
| ADC1 | 89 | AI | ADC1input | |
| NET_LIGHT | 83 | DO | Indicate network status | |
| DTR | 79 | DI | Sleep mode control | |
| RING | 13 | DO | Incoming call ring | |

### 1.1.1 UART

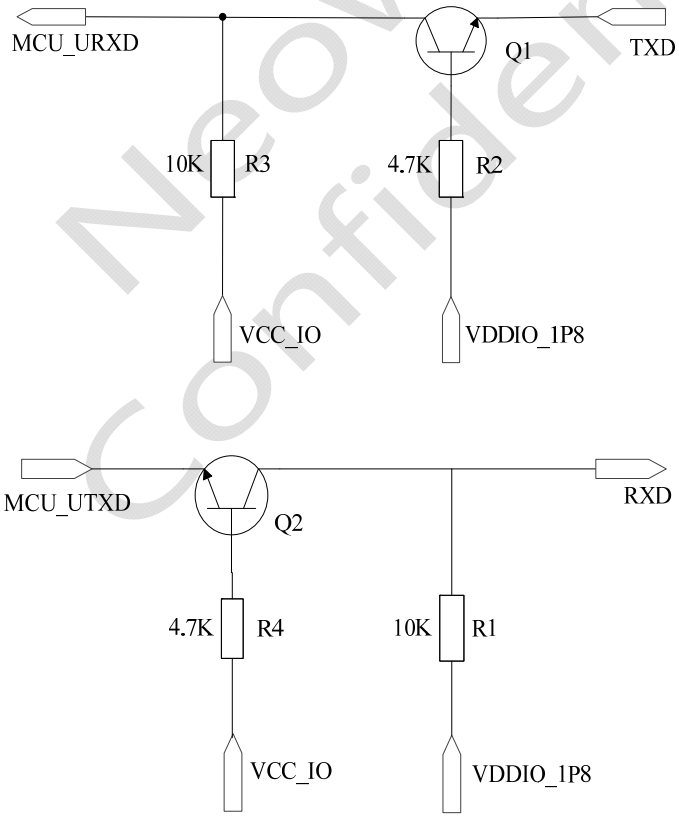
N720 provides one group of UART interfaces, which support hardware flow control and 4Mbps at most. The high level is 1.8V. Figure 2-17 shows the reference design of the UART interface.

**Figure 2-17** Reference design of the UART interface




If the UART does not match the logic voltage of the MCU, it is recommended that you add a level shifting circuit outside of the module as shown in Figure 2-18.

**Figure 2-18** Recommended level shifting circuit

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NOTE

Components:

R2/R4: 2K-10K. The greater the UART baud rate is, the lower the R2 value is.

R1/R3: 4.7K-10K The greater the UART baud rate is, the lower the R3 value is.

Q1: MMBT3904 or MMBT2222 High-speed transistor is better.

MCU_UTXD and MCU_URXD are respectively the TX and RX ports of the MCU while TXD and RXD are respectively the TX and RX ports of the module.

Voltage at VCC_IO is the voltage at the UART of the MCU while voltage at VDDIO_1V8 is the voltage at the UART of the module.

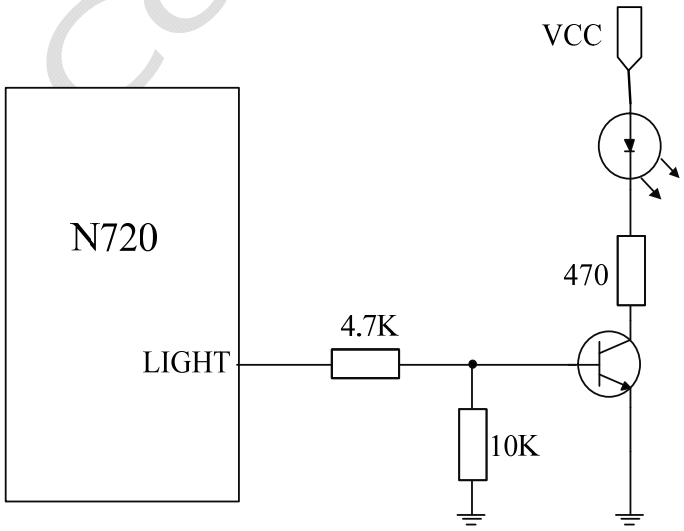
## 2.6.2 ADC

N720 provides two ADC channels, and the input voltage ranges from 0.1 to 1.7V. ADC pin supports highest precision of 16-bit and it can be used for temperature and other check. If you apply this pin to SIM card temperature check on electric terminals, refer to *Neoway GPRS Module ADC User Guide*.

## 2.6.3 NET_LIGHT

NET_LIGHT can output 1.8 V high level and is forbidden to be used to drive the LED indicator. Users can drive the LED with a transistor instead, as shown in Figure 2-18.

**Figure 2-19** LED indicator driven by transistor

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When the module is running, the LED indicator is driven by the NET_LIGHT pin to indicate different module status with its various blink behaviors. N720 supports multiple blink style and you can configure it using AT commands.

### 2.6.4 DTR

Generally, DTR is used to control sleep mode together with AT commands. Enable the sleep mode function by AT command. Then pulling DTR low will bring the module into sleep mode if the module is idle. In this mode, the idle current is less than 4 mA, depending on the DRX setting of network.

In sleep mode, the module can respond to the incoming call, SMS, and GPRS data. The host MCU can also control the module to exit sleep mode by controlling DTR.

Process of entering sleep mode:

1. Keep DTR high level in normal working mode. Activate the sleep mode by using the **AT+ENPWRSAVE=1** command.
2. Pull DTR low, and the module will enter sleep mode, but only after process and pending data finished.
3. In sleep mode, the external MCP can pull DTR high so that the module will exit from sleep mode actively. Then the module can transmit data and initiate calls. After processing is finished, pull DTR low again to take the module back to sleep mode.
4. In sleep mode, the module can be woken up by the events of incoming voice call, received data, or SMS. Meanwhile the module will send out the unsolicited messages through the UART.

   Upon receipt of the unsolicited messages, the host MCU should pull DTR high firstly, otherwise the module will resume sleep mode in two minutes after the service processing. Then the host MCU can process the voice call, received data, or SMS. After processing is finished, pull DTR low again to put the module into sleep mode.

### 2.6.5 RING Signal Indicator

- Calling: Once a voice call is incoming, UART outputs "RING" character strings and meanwhile the RING pin outputs 30 ms low pulses at 5s period. After the call is answered, the high level restores.

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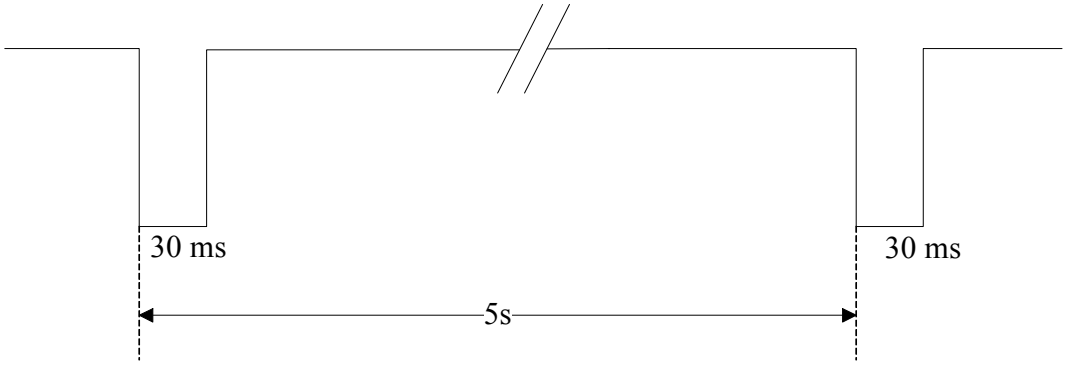
**Figure 2-20** RING indicator for incoming call




- SMS: Upon receipt of SMS, the module outputs one 35 ms low pulse.

**Figure 2-21** RING indicator for SMS

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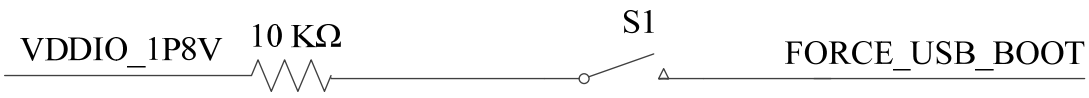
## 2.7 Commissioning Interfaces

To facilitate software update and commissioning, reserve the commissioning interfaces.

### 2.7.1 FORCE_USB_BOOT

The module can enter the fastboot mode by short connecting the FORCE_USB_BOOT pin and VDDIO_1P8V during the startup. This is the last method to troubleshoot the abnormality that the module cannot start or operation properly.

**Figure 2-22** Reference design of the fast boot interface



# 3 RF Interface

| Name | Pin | I/O | Function | Remarks |
|---|---|---|---|---|
| ANT_MAIN | 76 | AI/O | 2G/3G/4G main antenna | 50Ω characteristic impedance |
| ANT_GPS | 92 | AI | GPS antenna | |
| ANT_AUX | 94 | AI | 4Gdiversity aerial | |

## 3.1 2G/3G/4G RF Design and PCB Layout

ANT_MAIN and ANT_AUX is the antenna pin of N720. A 50 Ω antenna is required. VSWR ranges from 1.1 to 1.5. The antenna should be well matched to achieve best performance. It should be installed far away from high-speed logic circuits, DC/DC power, or any other strong disturbing sources.

A 50 Ω antenna is required. VSWR ranges from 1.1 to 1.5. The antenna should be well matched to achieve best performance.

For multiple-layer PCB, the trace between the antenna pad of module and the antenna connector, should have a 50 Ω characteristic impedance, and be as short as possible. The trace should be surrounded by ground copper. Place plenty of via holes to connect this ground copper to main ground plane, at the copper edge.

For dual-layer PCB, the width of recommended impedance trace is 0.8 mm to 1 mm and the grounding copper should away from the trace for 1 to 1.5 time of the trace width.

If the trace between the module and connector has to be longer, or built-in antenna is used, a π-type matching circuit is needed, as shown in Figure 3-1.

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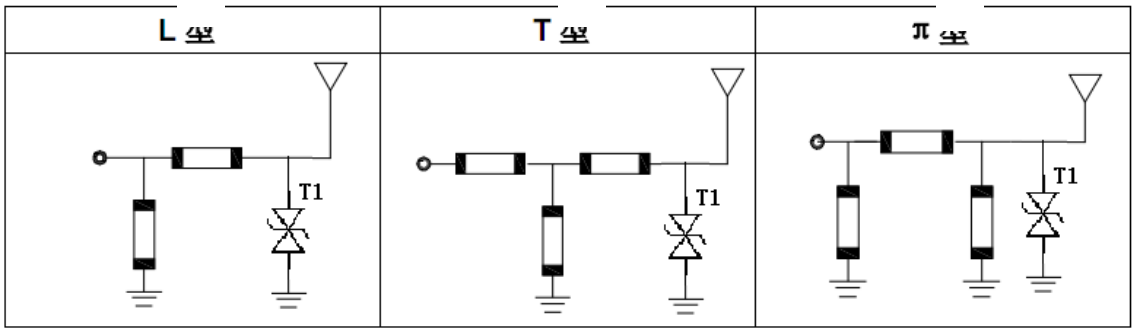
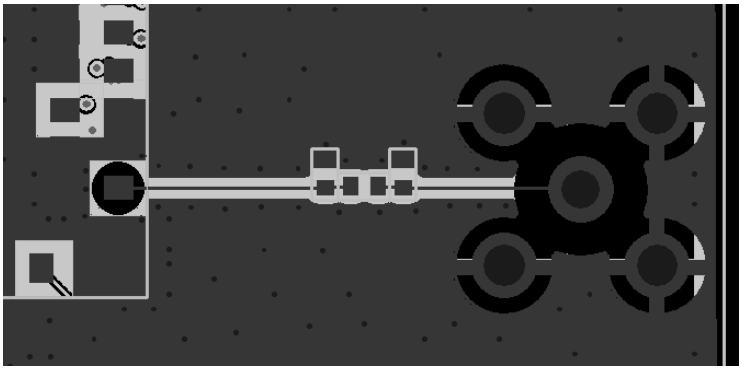
**Figure 3-1** Reference of antenna matching design



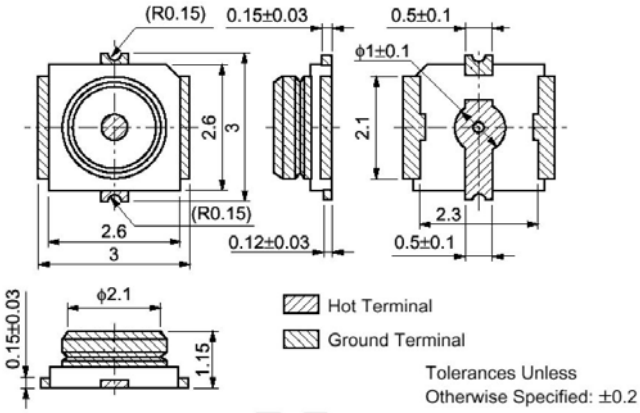
Big RF solder pad can result in great parasitic capacitance, which will affect the antenna performance. Remove the copper on the first and second layers under the RF solder pad.

**Figure 3-2** Recommended RF PCB design



If you adopt RF antenna connections, the GSC RF connector MM9329-2700RA1 from Murata is recommended..Figure 3-3shows the encapsulation specifications.

**Figure 3-3** Encapsulation specifications of Murata RF connector




RF antenna can also be connected to the module by soldering. In this manner, you must ensure proper soldering in case of damage that lowers RF performance. Figure 3-4shows the pictures of these two connections.

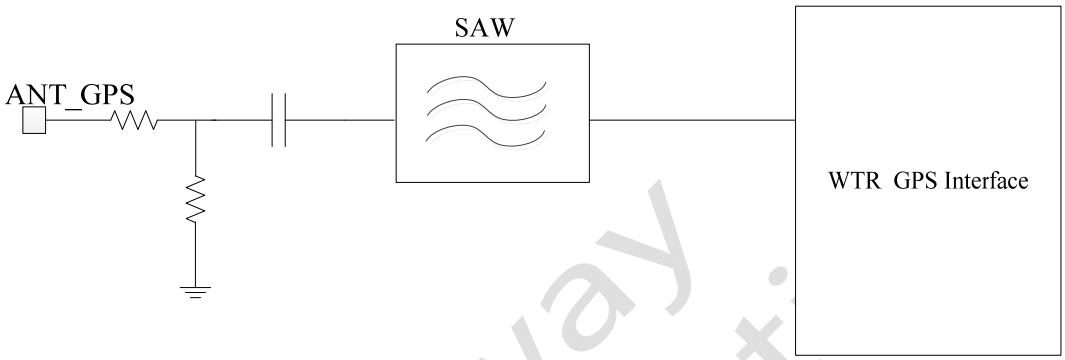
**Figure 3-4** RF connections

# 3.2 GPS RF Design and PCB Layout

## 3.2.1 GPS Impedance

The 92nd pin is the GPS interface of the module, which also requires a 50 Ω. The PCB layout for GPS is similar to that for GPRS. For details, refer to the previous section. Figure 3-5 shows the internal structure of the GPS RF.

**Figure 3-5** GPS RF structure




In addition to the basic rules, the GPS routing has higher requirements because the air wireless GPS signal has lower strength, which results in weaker electrical signal after the antenna receives. Weaker signals are more susceptible to interference. Therefore, active antenna are commonly used for GPS. The active GPS antenna amplifies the weak signals received to stronger signals through the low-noise amplifier (LNA) and then transmits the signals through the feeder.

If you use a passive antenna, add LNA near the feeder because the module does not embed one.

If the antenna and layout are not designed reasonably, the GPS will be insensitive, resulting in long time on positioning or inaccurate position.

Keep the GPRS and GPS far away from each other in layout and antenna layout.

## 3.2.2 Active GPS Antenna Design

Ceramic GPS chip antenna is monly used. In general, it is recommended that you use the active ceramic antenna. After the antenna receives GPS satellite signals, the LNA amplifies them first and then they are transmitted to the 92nd pin (GPS_ANT) through the feeder and PCB traces. 50Ω resistance is required for both the feeder and PCB traces and the traces should be as short

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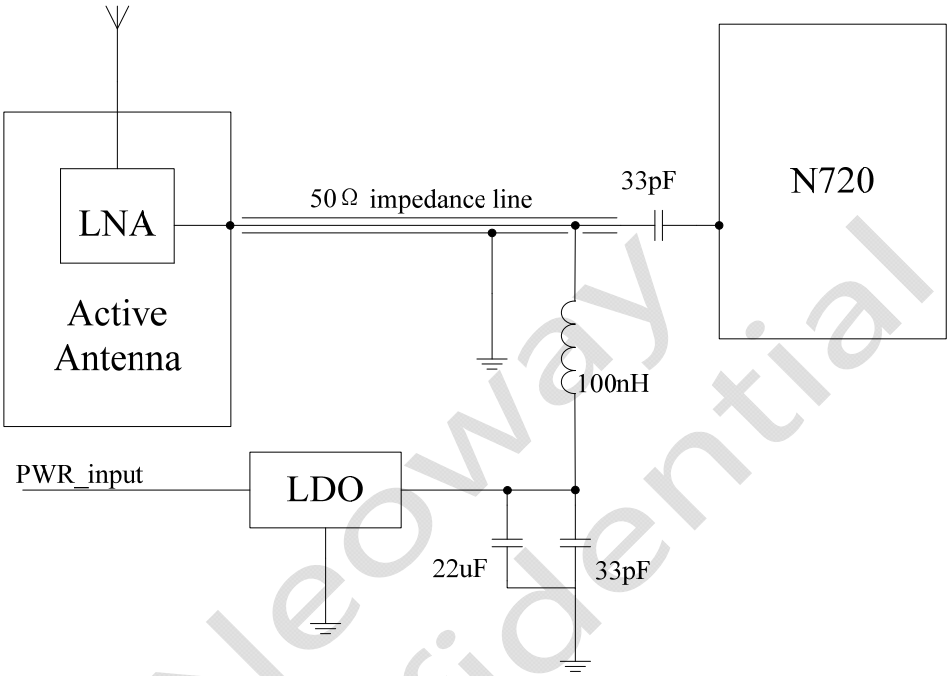
as possible. The power supply of the active antenna is fed by the 100 nH inductance through the signal traces.

Common active antenna requires 3.3V to 5V power supply. Though the active antenna has a low power consumption, it requires stable and clean power supply. You are advised to use high-performance LDO to supply power for the antenna through a 100 nH inductance, as shown inFigure 3-6.

**Figure 3-6** Power supply reference for active antenna

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**CAUTION**

It is recommended that you add an ESD protection diode to the antenna interface in an environment with great electromagnetic interference and other applications with badly ESD. The ESD protection diode must have ultra-low capacitance (lower than 0.5 pF). Otherwise, it will affect the impedance of the RF loop or result in attenuation of RF signals. RCLAMP0521P from Semtech or ESD5V3U1U from Infineon is recommended.

On the PCB, keep the RF signals and RF components away from high-speed circuits, power supplies, transformers, great inductors, the clock circuit of single-chip host, etc.

# 4 Electric Feature and Reliability

## 4.1 Electric Feature

**Table 4-1** N720 Electric Feature

| Module Status | | Minimum Value | Typical Value | Maximum Value |
|---|---|---|---|---|
| VBAT | Vin | 3.3V | 3.8V | 4.3V |
| | Iin | / | / | 3A |

**CAUTION**

If the voltage is too low, the module might fail to start. If the voltage is too high or there is a voltage burst during the startup, the module might be damaged permanently.

If you use LDO or DC-DC to supply power for the module, ensure that it output at least 3 A current.

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## 4.2 Temperature

**Table 4-2** Temperature Feature

| Module Status | Minimum Value | Typical Value | Maximum Value |
|---|---|---|---|
| Work | -40°C | 25°C | 85°C |
| Limit | -40°C | | 85°C |
| Storage | -40°C | | 85°C |

**CAUTION**

If the module works in temperature exceeding the thresholds, its RF performance might be worse but it can still work properly.

## 4.3 ESD Protection

Electronics need to pass sever ESD tests. The following table shows the ESD capability of key pins of our module. It is recommended that you add ESD protection to those pins in accordance to the application to ensure your product quality when designing your products.

Humility: 45%  Temperature: 25°C

**Table 4-3** N720 ESD feature

| Testing Point | Contact Discharge | Air Discharge |
|---|---|---|
| VBAT | ±8KV | ±15KV |
| GND | ±8KV | ±15KV |
| ANT | ±8KV | ±15KV |
| Cover | ±8KV | ±15KV |
| Others | ±2KV | ±4KV |

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# 5 RF Feature

## 5.1 Work Band

**Table 5-1** N720 work band

| Work band | Uplink | Downlink |
|---|---|---|
| GSM850 | 824~849MHz | 869~894MHz |
| PCS1900 | 1850~1910MHz | 1805~1880MHz |
| UMTS B2 | 1850~1910MHz | 1805~1880MHz |
| UMTS B4 | 1710~1755MHz | 2110~2155MHz |
| UMTS B5 | 824~849MHz | 869~894MHz |
| LTE-FDD B2 | 1850~1910MHz | 1805~1880MHz |
| LTE-FDD B4 | 1710~1755MHz | 2110~2155MHz |
| LTE-FDD B5 | 824~849MHz | 869~894MHz |
| LTE-FDD B7 | 2500~2570MHz | 2620~2690MHz |
| LTE-FDD B12 | 699.7 – 715.3 MHz | 729.7– 745.3 MHz |
| LTE-FDD B17 | 704~716MHz | 734~746MHz |

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## 5.2 TX Power and RX Sensitivity

**Table 5-2** N720 RF power and RX sensitivity

| Band | Transmitting Power | Receiving Sensitivity |
|---|---|---|
| GSM850 | 34 dBm | <-108 dBm |
| PCS1900 | 31.5 dBm | <-108 dBm |
| UMTS B2 | 24 dBm | <-108 dBm |
| UMTS B4 | 24 dBm | <-108 dBm |
| UMTS B5 | 24 dBm | <-108 dBm |
| LTE-FDD B2 | 23 dBm | <-95 dBm |
| LTE-FDD B4 | 23 dBm | <-97 dBm |
| LTE-FDD B5 | 23 dBm | <-95 dBm |
| LTE-FDD B7 | 23 dBm | <-95 dBm |
| LTE-FDD B12 | 23 dBm | <-95 dBm |
| LTE-FDD B17(10MHz) | 23 dBm | <-95 dBm |

NOTE

All the values above are obtained in the lab environment. In your actual applications, there might be a difference because of the network environment.

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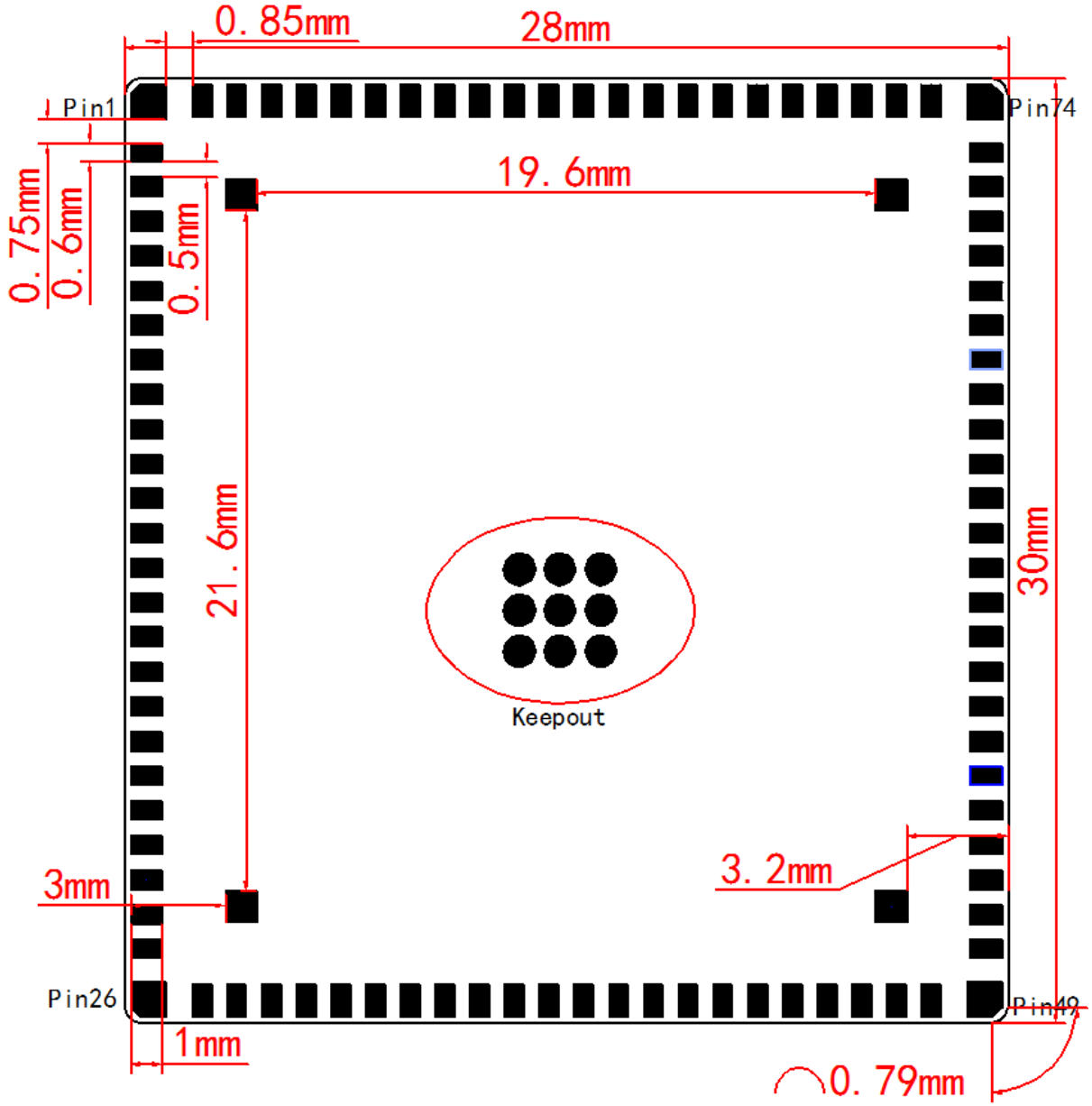
# 6 Mechanical Feature

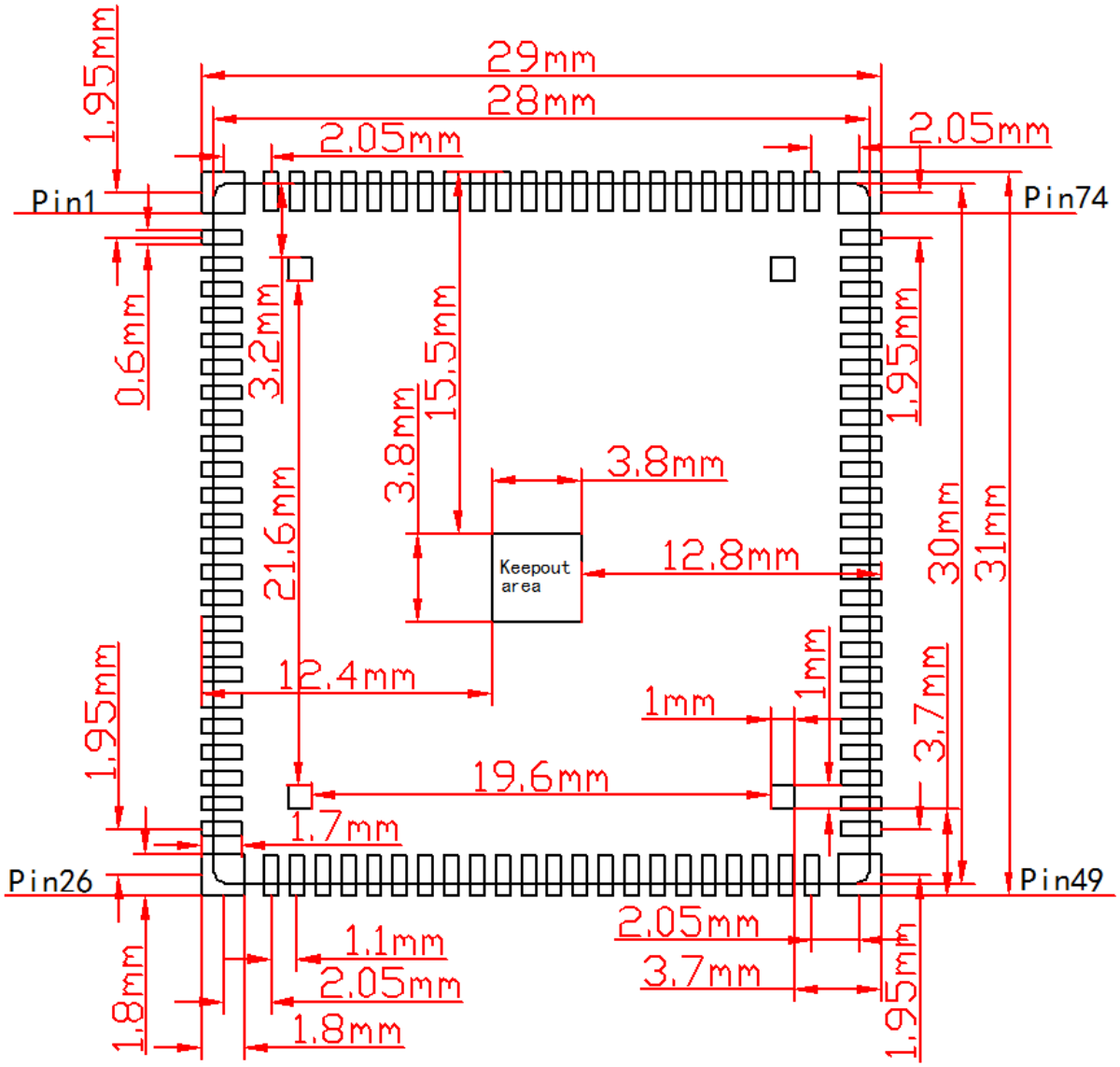
## 6.1 Dimensions

**Figure 6-1** Dimensions of N720



## 6.2 PCB Foot Print

**Figure 6-2** N720PCBFoot Print(Top View)




**CAUTION**

A test point is reserved at the Silk Area. It is recommended that you add a layer of white ink in case short circuit. Do not lay out any trace under the JTAG pin.

# 7 Mounting and Packaging

## 7.1 Mounting the Module onto the Application Board

N720 is compatible with industrial standard reflow profile for lead-free SMT process.

The reflow profile is process dependent, so the following recommendation is just a start point guideline:

- Only one flow is supported.
- Quality of the solder joint depends on the solder volume. Minimum of 0.12 mm to 0.15stencil thickness is recommended.
- Use bigger aperture size of the stencil than actual pad size.
- Use a low-residue, no-clean type solder paste.

For information about cautions in N720 storage and mounting, refer to *Neoway Module Reflow Manufacturing Recommendations*.

When you maintain and manually solder it, use heat guns with great opening, adjust the temperature to 250 degrees (depending on the type of the solder paste), and heat the module till the solder paste is melt. Then remove the module using tweezers. Do not shake the module in high temperature when you remove it. Otherwise, the components inside the module might be misplaced.

## 7.2 Package

N720 modules are packaged in sealed bags on delivery to guarantee a long shelf life. Package the modules again in case of opening for any reasons.

If exposed in air for more than 48 hours at conditions not worse than 30°C/60% RH, a baking procedure should be done before SMT. Or, if the indication card shows humidity greater than 20%, the baking procedure is also required. Do not bake modules with the package tray directly.

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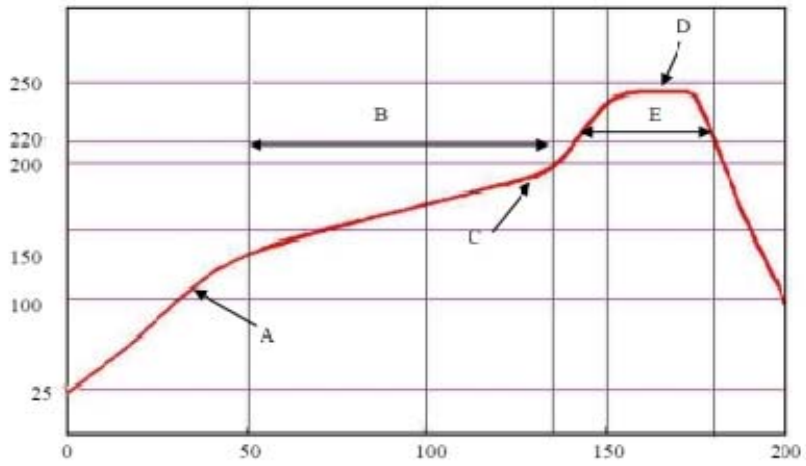
# 8 SMT TemperatureCurve

**Figure 8-1** Temperature curve




X: Time (s) Y Temperature (°C)

Technicalparameters:

- Ramp up rate: 1to 4°C/sec; Ramp down rate: -3 to-1°C/sec
- Soaking zone: 150-180°CTime: 60-100s
- Reflow zone:>220°CTime: 40-90s
- Peak temperature: 235-250°C

It is not recommended that you use the kind of solder paste different from our module technique.

- The melting temperature of solder paste with lead is 35°Clower than that of solder paste without lead. It is easy to cause faulty joints for BGA inside the module after second reflow soldering.
- If you can use only solder pastes with lead, please ensure that the reflow temperature is kept at 220°C for more than 45 seconds and the peak temperature reaches 240°C.

**WARNING**

Neoway will not provide warranty for heat-responsive element abnormalities caused by improper temperature control.

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# 9 Abbreviations

| | |
|---|---|
| ADC | Analog-Digital Converter |
| CPU | Central Processing Unit |
| DTR | Data Terminal Ready |
| EGSM | Enhanced GSM |
| ESD | Electronic Static Discharge |
| GPRS | General Packet Radio Service |
| GSM | Global Standard for Mobile Communications |
| IMEI | International Mobile Equipment Identity |
| LED | Light Emitting Diode |
| PCB | Printed Circuit Board |
| RF | Radio Frequency |
| SIM | Subscriber Identification Module |
| UART | Universal asynchronous receiver-transmitter |

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## FCC Information

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide residential protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on. The user is encouraged to try to correct the interference by one or more of the following measures:
Reorient or relocate the receiving antenna.
Increase these paration between the equipment and receiver.
Connect the equipment into an outlet on the circuit different from that to which the receiver is connected.
Consult the dealer or an experienced radio/TV technician for help.

## CAUTION!

The manufacturer is not responsible for any radio or TV interference caused by unauthorized modifications to this equipment. Such modifications could void the user authority to operate the equipment.

If the FCC identification number is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. This exterior label can use wording such as the following:
"Contains Transmitter Module FCC ID: PJ7-1705 Or Contains FCC ID: PJ7-1705"

## FCC RADIATION EXPOSURE STATEMENT

This equipment complies with FCC RF radiation exposure limits set for an uncontrolled environment. This transmitters must not be co-located or operating in conjunction with any other antenna or transmitter. This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions: (1)This device may not cause harmful interference, and (2) This device must accept any interference, including interference that may cause undesired operation.

The distance between user and product include antenna should be no less than 25 cm.
The maximum permissible antenna gain is 0 dBi for each band, and under no conditions may an antenna gain be used that would exceed the ERP and EIRP power limits as specified in Parts 22, 24 and 27.

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