

Reversion History:

Rev1.0 to 2.0:

1. Flash Byte swap.
2. EMI improvement in ETHERNET.

Rev2.0 to B 1.1 :

1. Change Project name from ARESGATE 1000 to ARESGATE 1000 PRO
2. Low the height of JP1 and JP2.

ARESCOM

AG1000PRO

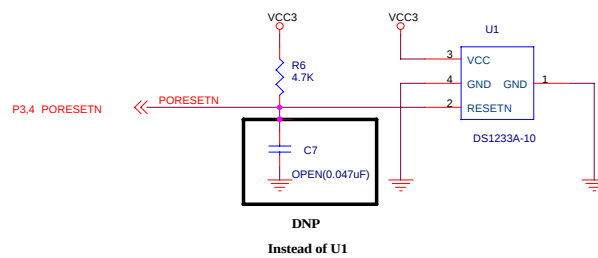
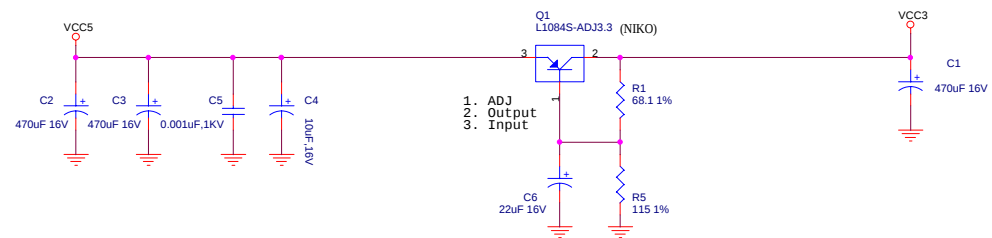
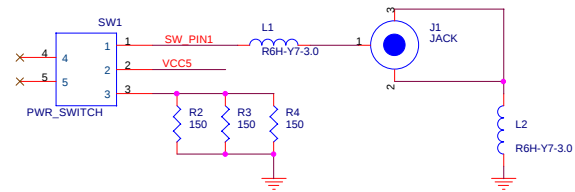
56K MODEM WLAN

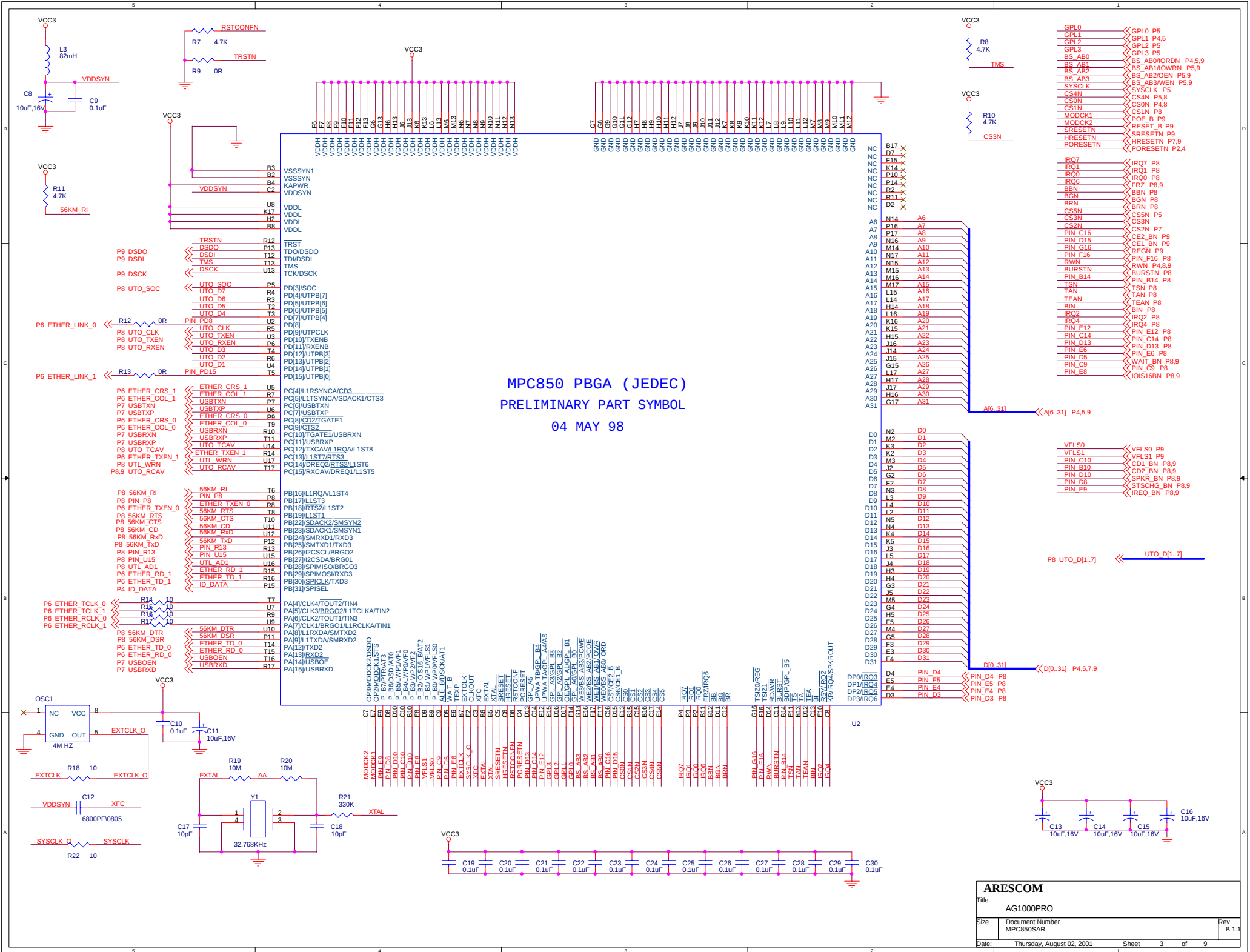
MOTOROLA MPC850 MAIN BOARD

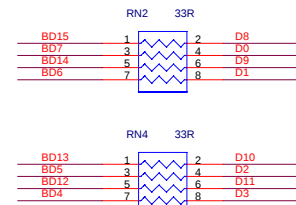
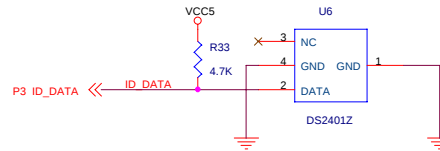
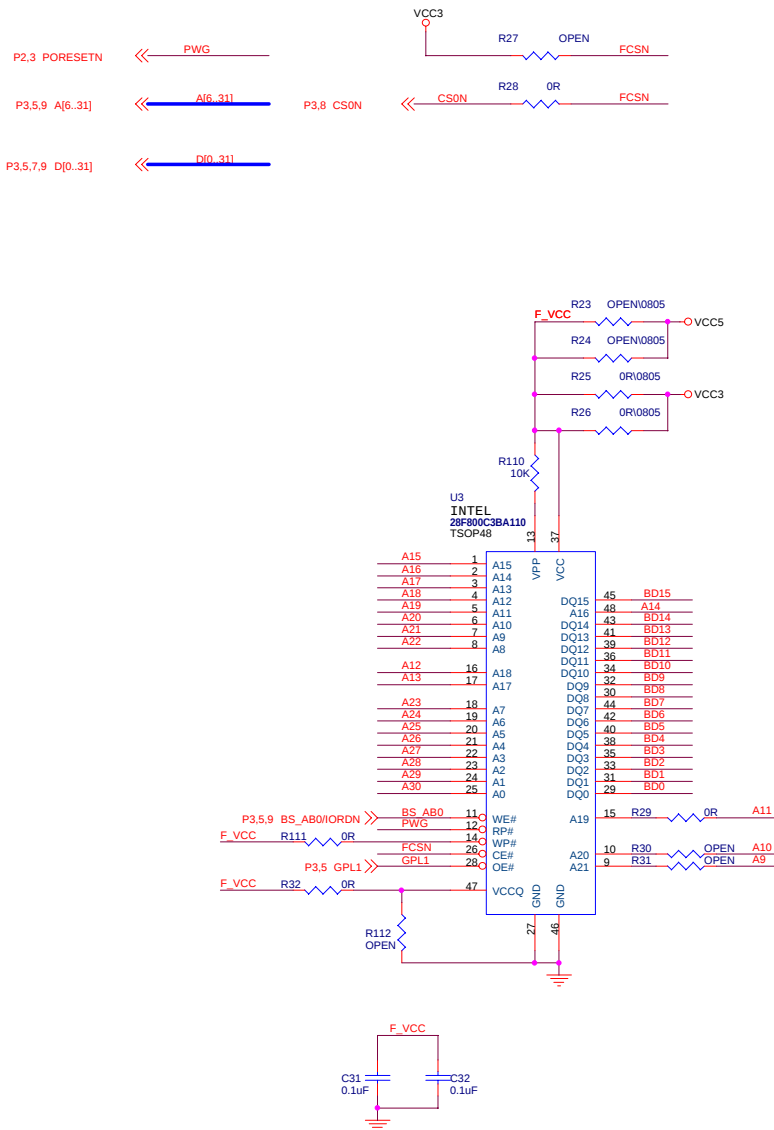
PCB P/N : 109000000143

Revision : B 1.1

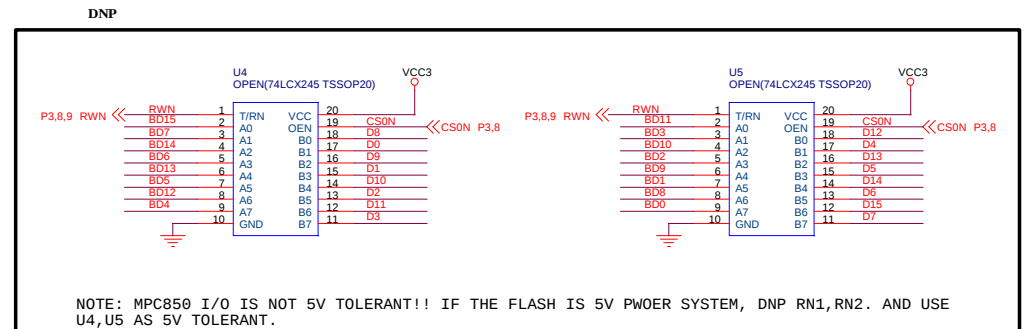
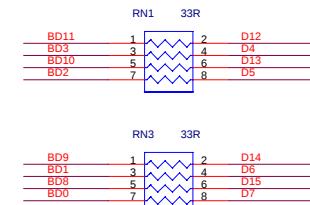
ARESCOM INC			
Title AG1000PRO			
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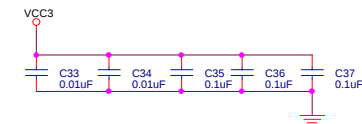
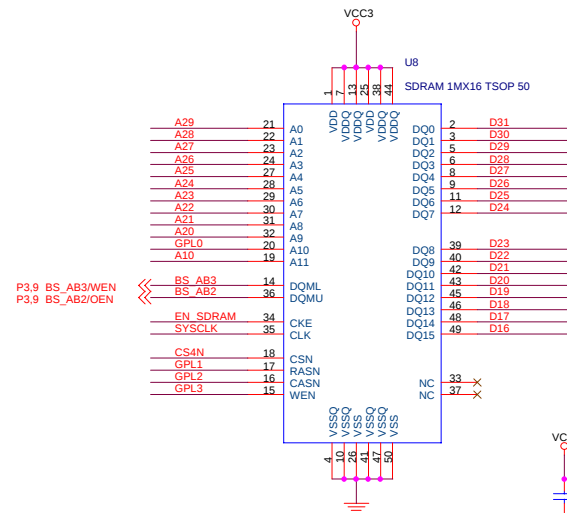
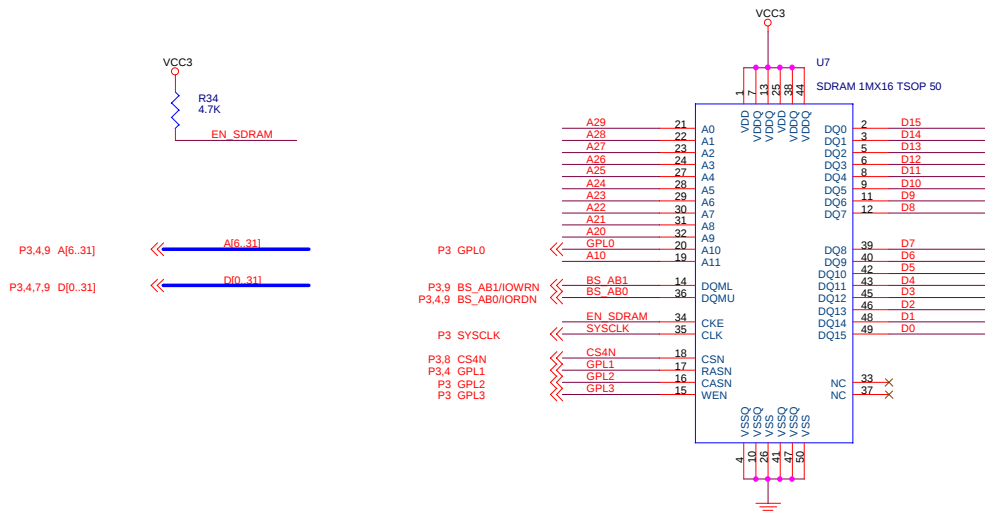




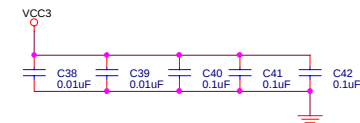
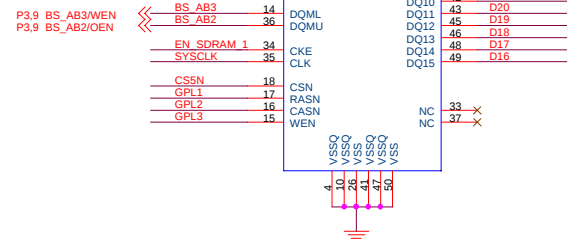
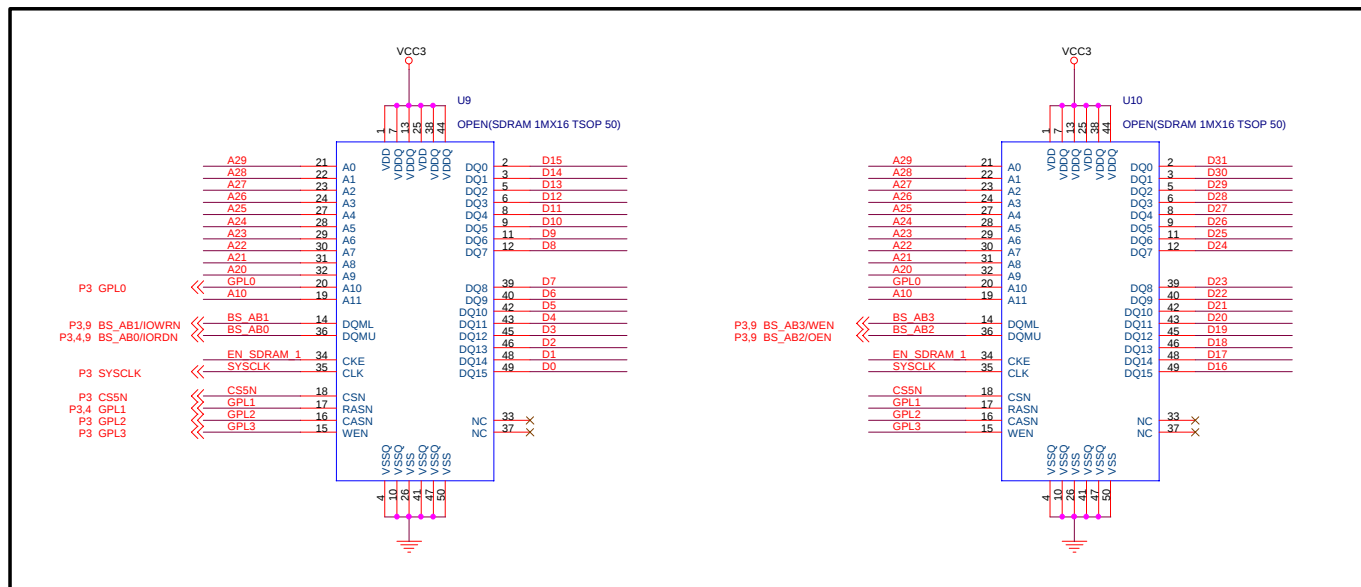


BD0	D7
BD1	D6
BD2	D5
BD3	D4
BD4	D3
BD5	D2
BD6	D1
BD7	D0
BD8	D15
BD9	D14
BD10	D13
BD11	D12
BD12	D11
BD13	D10
BD14	D9
BD15	D8

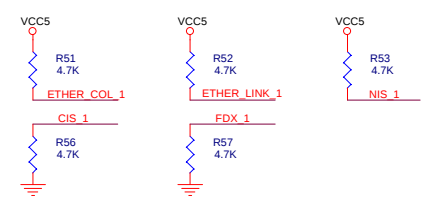
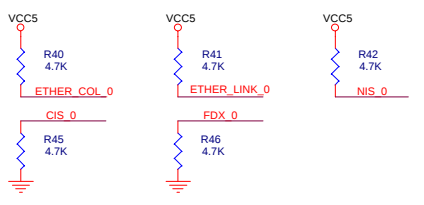
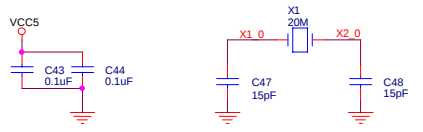
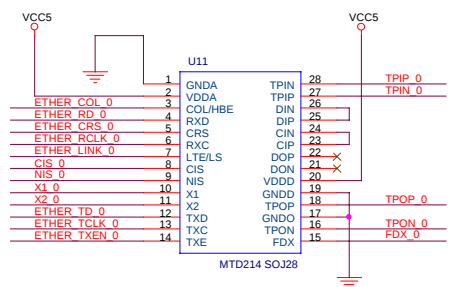




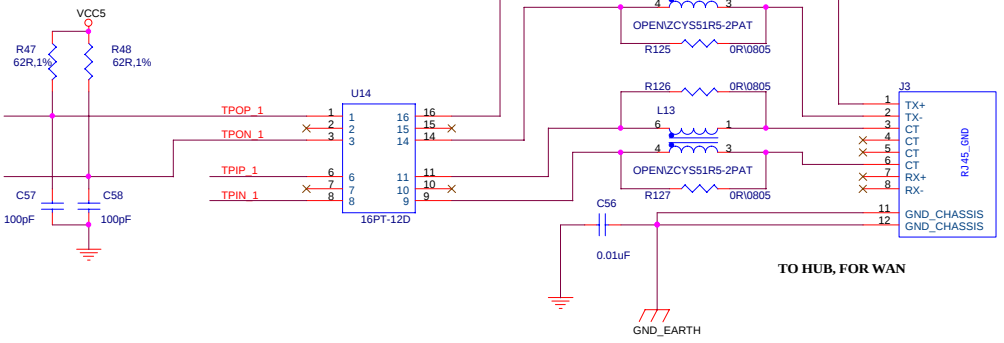
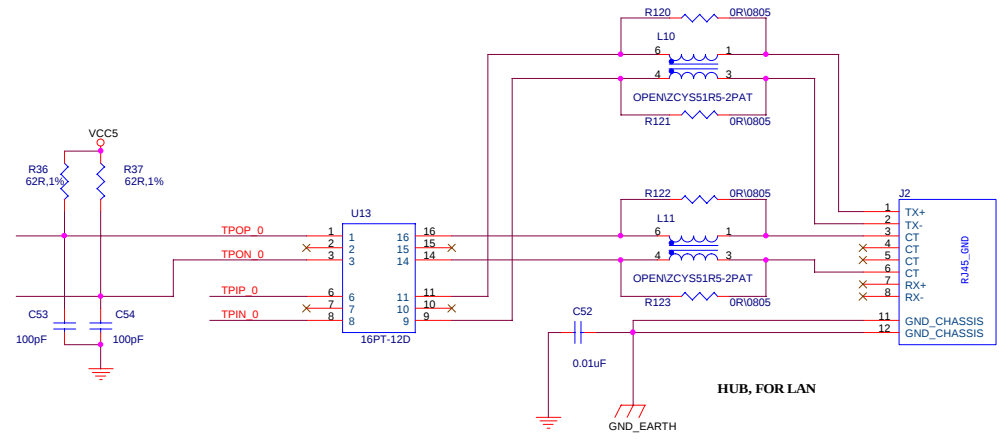
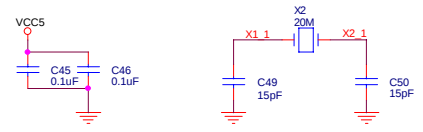
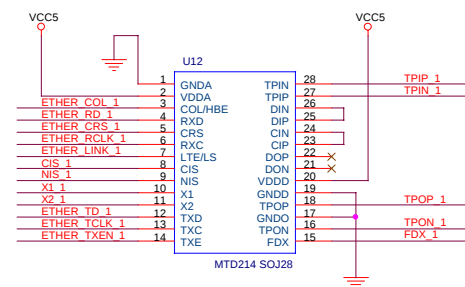
DNP, OPTIONAL

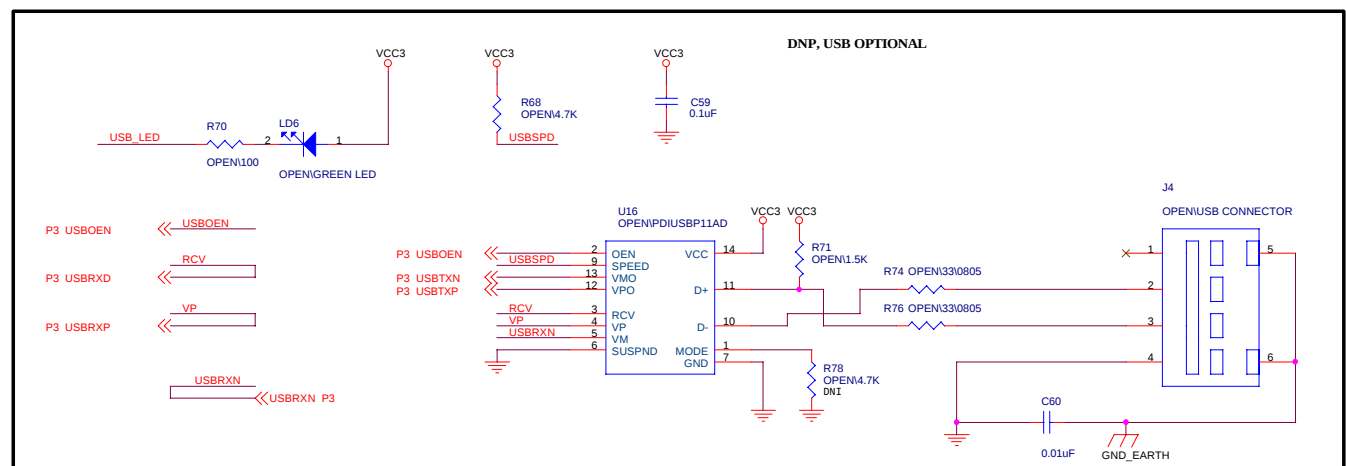
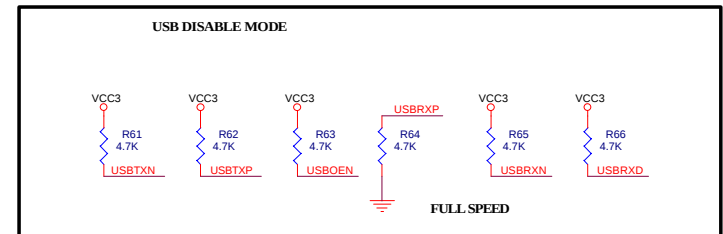
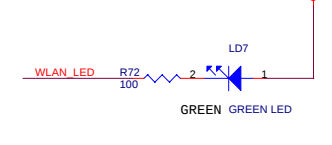


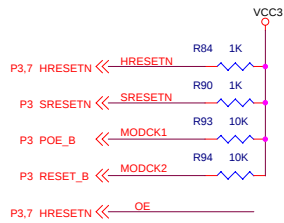
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ETHER_RCLK_0 << ETHER_RCLK_0_P3
ETHER_TD_0 << ETHER_TD_0_P3
ETHER_TXEN_0 << ETHER_TXEN_0_P3
P3_ETHER_COL_0 << ETHER_COL_0
P3_ETHER_RD_0 << ETHER_RD_0
P3_ETHER_LINK_0 << ETHER_LINK_0
P3_ETHER_TCLK_0 << ETHER_TCLK_0



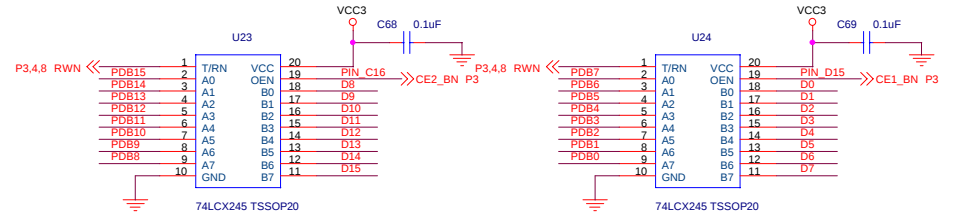
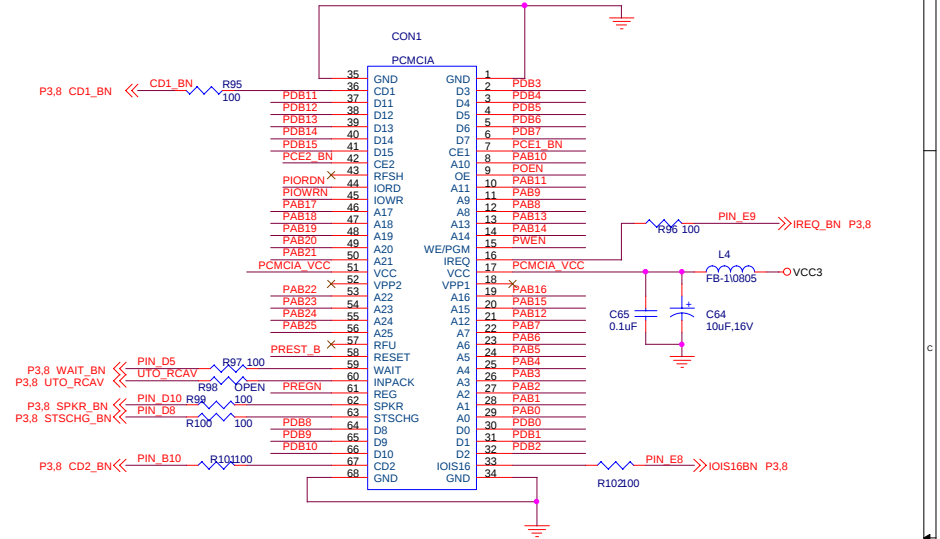
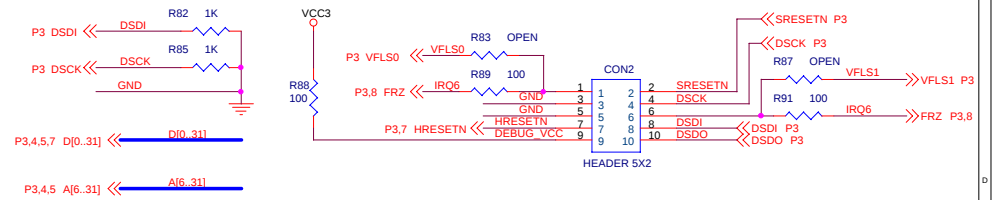
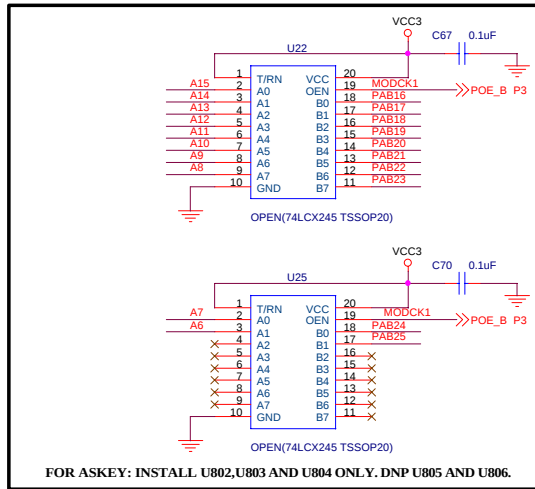
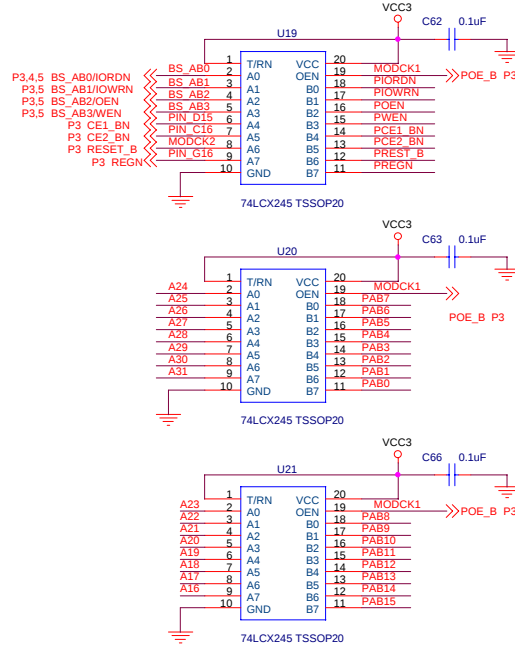
ETHER_CRS_1 << ETHER_CRS_1_P3
ETHER_RCLK_1 << ETHER_RCLK_1_P3
ETHER_TD_1 << ETHER_TD_1_P3
ETHER_TXEN_1 << ETHER_TXEN_1_P3
P3_ETHER_COL_1 << ETHER_COL_1
P3_ETHER_RD_1 << ETHER_RD_1
P3_ETHER_LINK_1 << ETHER_LINK_1
P3_ETHER_TCLK_1 << ETHER_TCLK_1



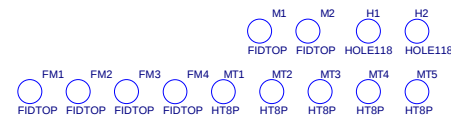




(D9,D10)=(0,0) for PCMCIA's DBGK.
(D4,D5)=(1,0) for 16-bit boot port size.



Note: Read is data from PCMCIA to MPC850. RWN=1, A to B



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