

ARESCOM AG2000S/AG2000

Motorola MPC 850 CPU SINGLE BOARD

WLAN AP + 10BTWLAN

AG2000S WITH 4 PORTS 10/100BT

AG2000 WITH 10BT LAN

PCB P/N: 109000000229

MPC 850 SAR PIN ASSIGMENTS:

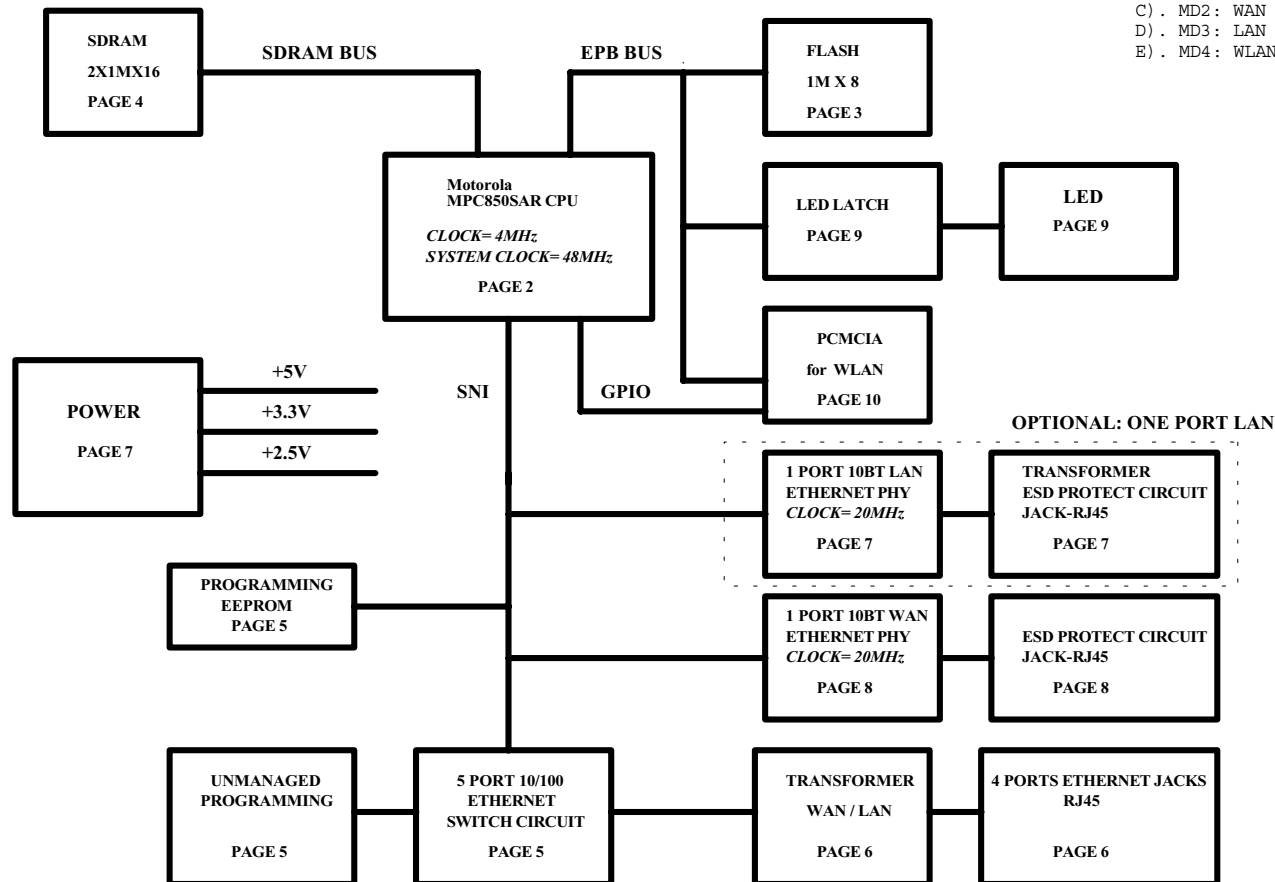
1. CHIP SELECT ASSIGNMENTS:

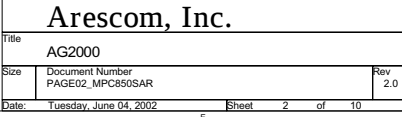
- A). CS0: FLASH.
- B). CS2: LED.
- C). CS4: SDRAM.

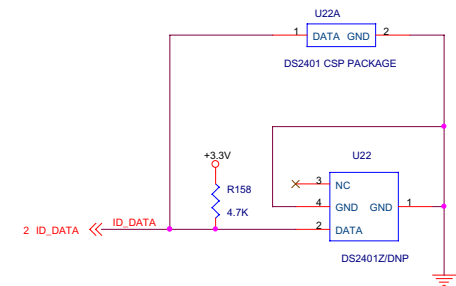
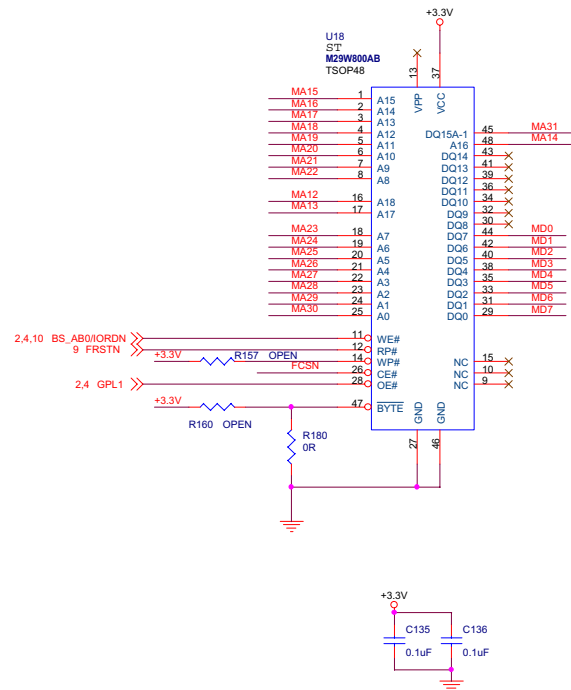
MPC 850 SAR BLOCK DIAGRAM:

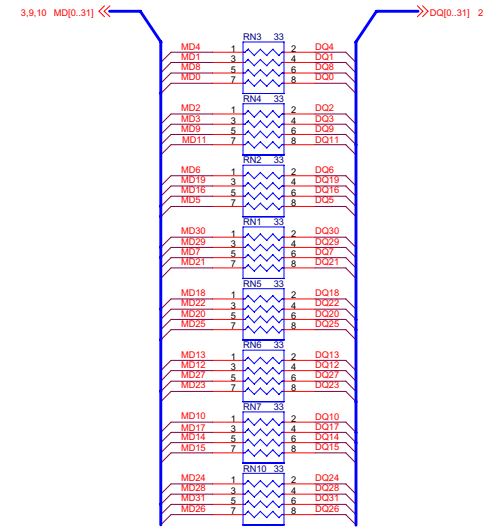
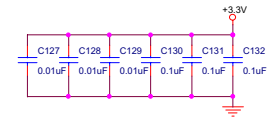
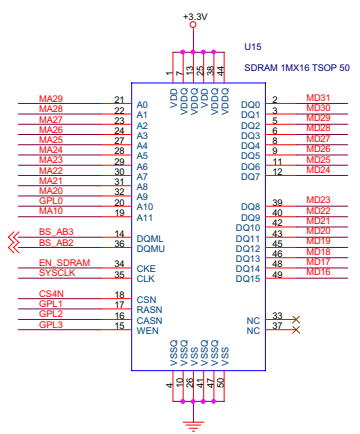
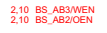
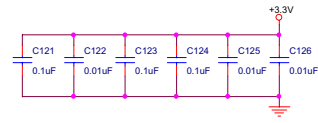
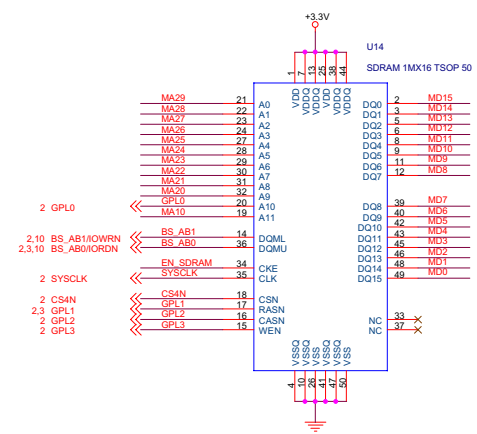
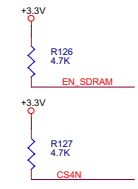
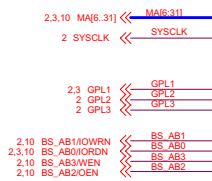
2. LED ASSIGNMENTS: (ACTIVE LOW)

- A). MD0: DIAG (AMBER) .
- B). MD1: RESERVED .
- C). MD2: WAN LINK/ACT (GREEN) .
- D). MD3: LAN LINK/ACT (GREEN) .
- E). MD4: WLAN LINK/ACT (GREEN) .









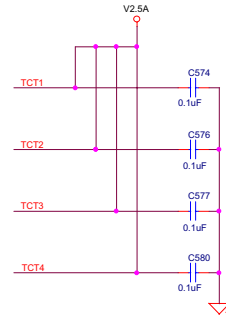
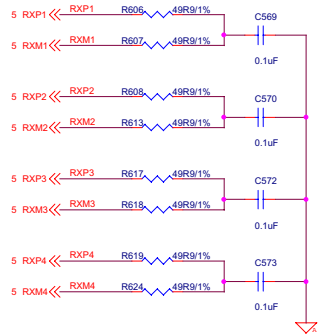


Recommended configuration for normal operation		
PIN NAME	UNMANAGED PROGRAMMING	FUNCTION DESCRIPTION
LED1_3	UP	Flow control on all PHY ports
LED1_2	UP	Flow control on ext MAC port
LED1_1	DOWN	205 buffers max per port (default)
LED1_0	DOWN	205 buffers max per port (default)
LED2_3	UP	5 Min. MAC address aging in address look up table
LED2_2	DOWN	Pull down for normal operation
LED2_1	UP	Back pressure in half duplex
LED2_0	UP	Aggressive back off in half duplex
LED3_3	UP	No drop after 16 collisions
LED3_2	UP	25%-3% limit of broadcast frames
LED3_1	FLOAT	Port 5 Auto-negotiation enable
LED3_0	FLOAT	Port 4 Auto-negotiation enable
LED4_3	FLOAT	Port 3 Auto-negotiation enable
LED4_2	FLOAT	Port 2 Auto-negotiation enable
LED4_1	FLOAT	Port 1 Auto-negotiation enable
LED4_0	DOWN	Port 5 half duplex and Auto-negotiation enabled
LED5_3	DOWN	Port 4 half duplex and Auto-negotiation enabled
LED5_2	DOWN	Port 3 half duplex and Auto-negotiation enabled
LED5_1	DOWN	Port 2 half duplex and Auto-negotiation enabled
LED5_0	DOWN	Port 1 half duplex and Auto-negotiation enabled
MRXD3	DOWN	*Port 5 enable Auto-negotiation
MRXD2	DOWN	*Port 4 enable Auto-negotiation
MRXD1	DOWN	*Port 3 enable Auto-negotiation
MRXD0	DOWN	*Port 2 enable Auto-negotiation
MCOL	DOWN	*Port 1 enable Auto-negotiation
P5EXT	DOWN	5 port IS mode

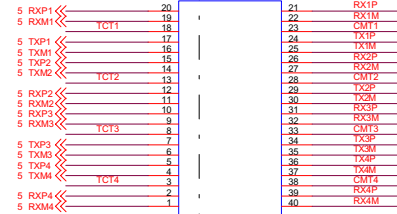
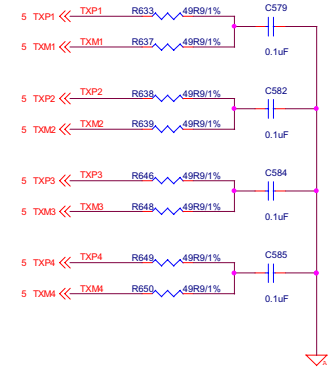
Port 5 reverse SNI application		
PIN NAME	UNMANAGED PROGRAMMING	FUNCTION DESCRIPTION
P5SNI	UP / DOWN	SNI MODE / Port 5 MII interface
P5EXT	UP	External MAC interface
MRXD3	UP	Disable Auto negotiation on port 5
LED4_0	UP / DOWN	Port 5 full duplex / half duplex
LED3_1	DOWN / UP	Port 5 force 10BaseT / 100BaseT
LED1_2	UP	Flow control enable on external MAC port



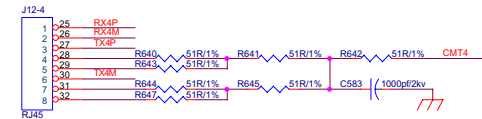
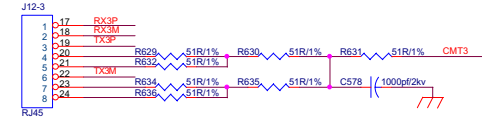
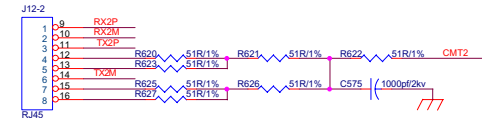
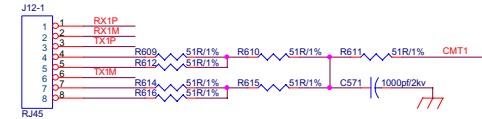
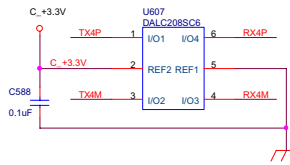
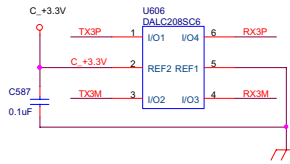
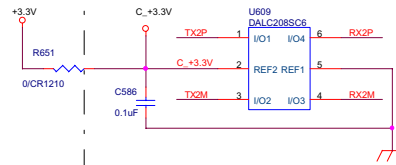
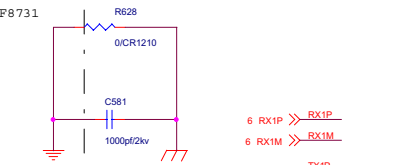
NULL POWER & GROUND AREA



FOR KS9995:
INSTALL R102 TO
R106 and C28 to
C34



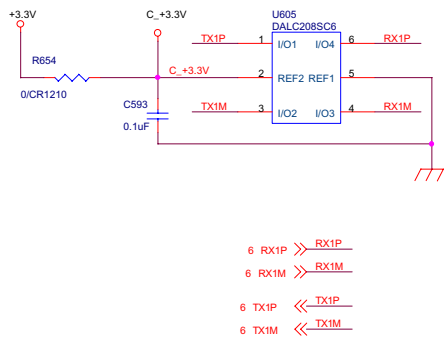
Pulse H1164
Bel Fuse 558-5999+Q9
YCL PH406466
Transpower HB826-2
DELTA LP8731

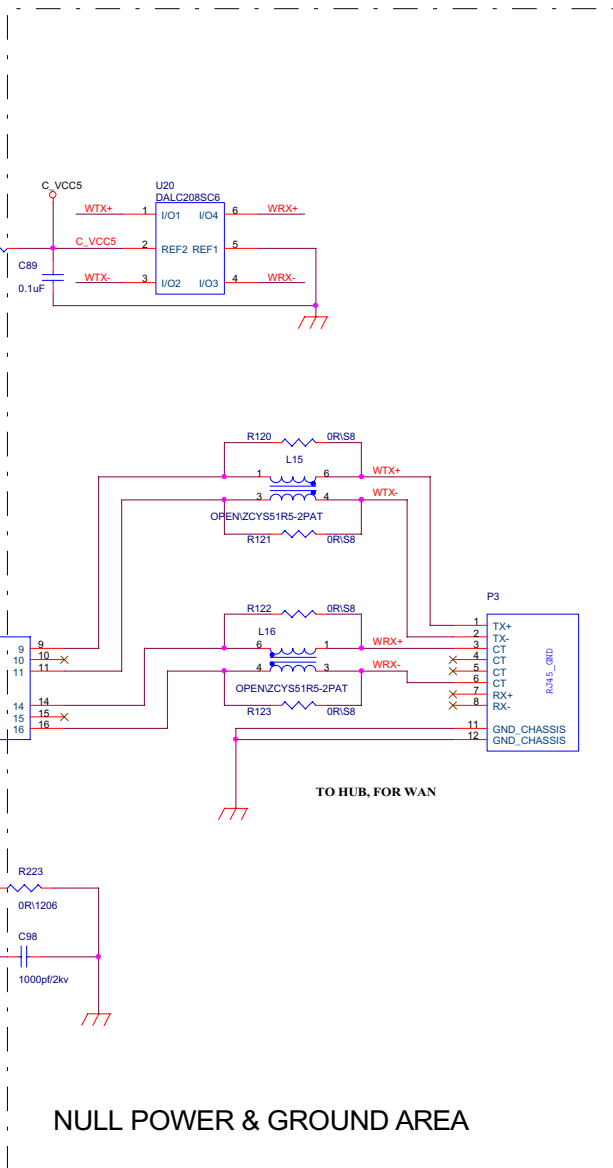
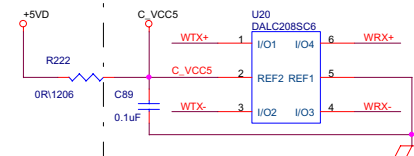
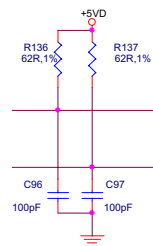
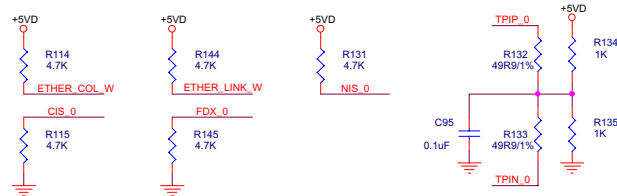
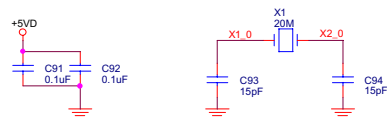
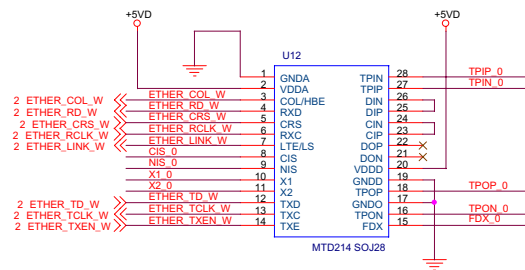


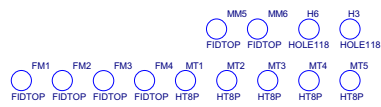
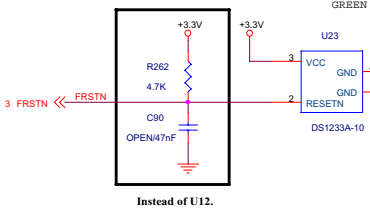
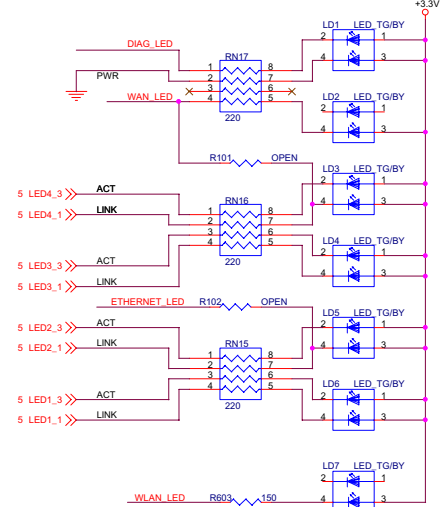
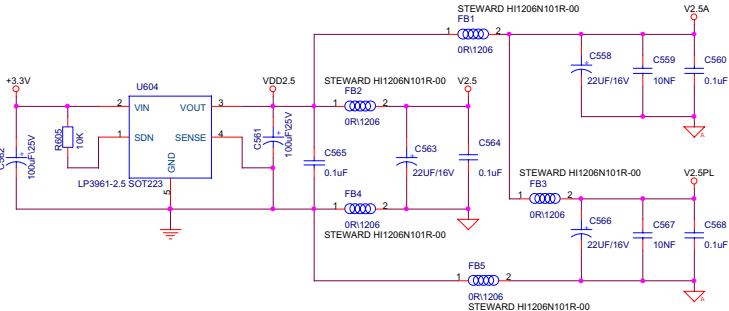
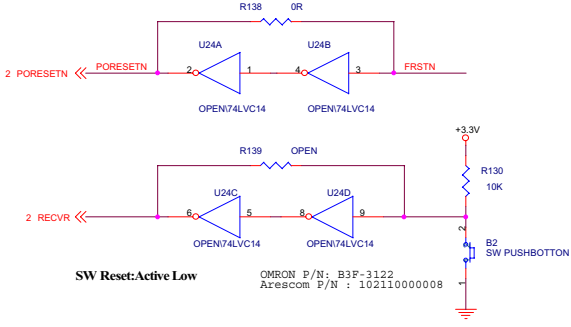
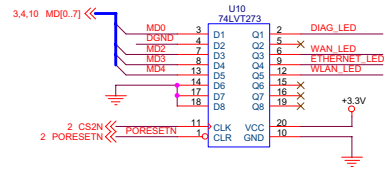
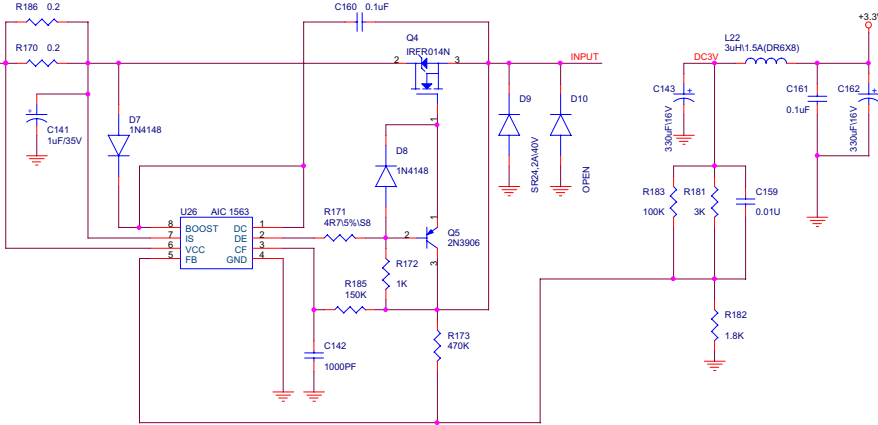
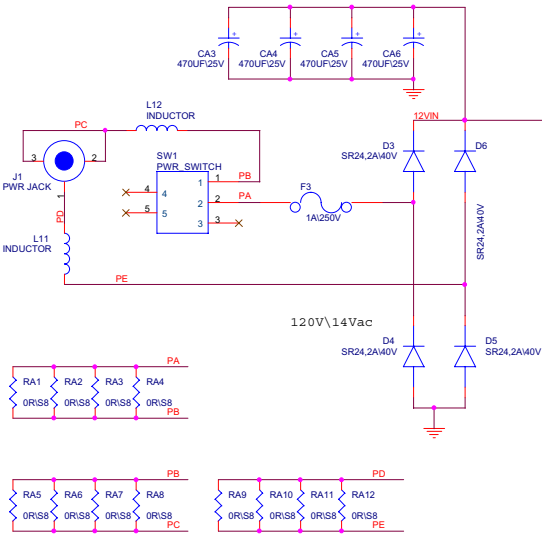
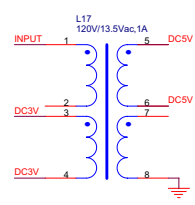
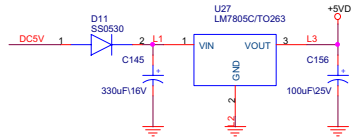
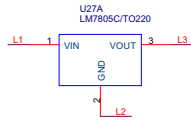
Arescom, Inc.

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Date:	Tuesday, June 04, 2002	Sheet	6 of 10

NULL POWER & GROUND AREA







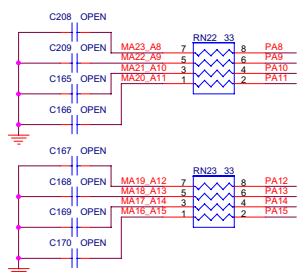
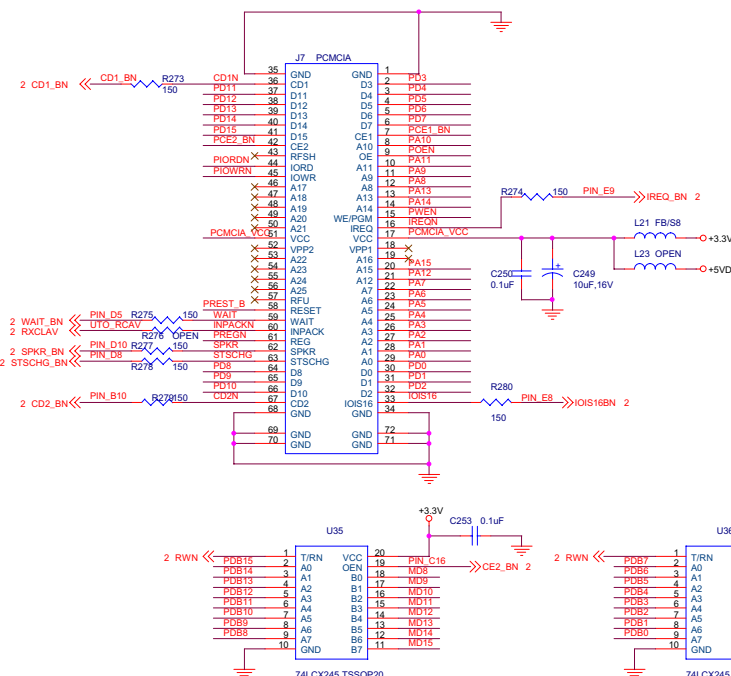
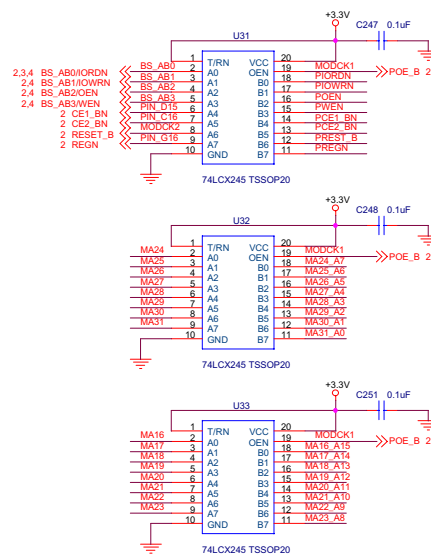
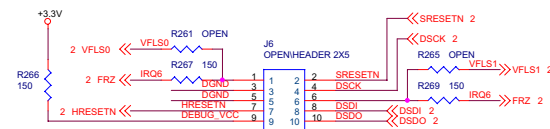
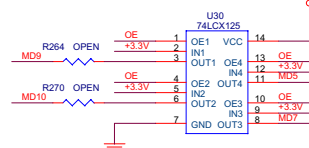
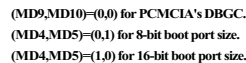
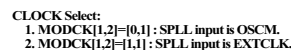


Figure 10 illustrates the pin connections for the 16-bit parallel data bus. The diagram shows four sections of the bus, each with a 16-bit parallel data bus (RN24, RN25, RN26, RN27) connected to a 16-bit parallel data bus (PDB0-PDB15). The connections are as follows:

- Section 1 (RN24):** PDB15 (7) to RN24 33 (8), PDB14 (6) to RN24 33 (7), PDB13 (5) to RN24 33 (6), PDB12 (4) to RN24 33 (5).
- Section 2 (RN25):** PDB11 (7) to RN25 33 (8), PDB10 (6) to RN25 33 (7), PDB9 (5) to RN25 33 (6), PDB8 (4) to RN25 33 (5).
- Section 3 (RN26):** PDB7 (7) to RN26 33 (8), PDB6 (6) to RN26 33 (7), PDB5 (5) to RN26 33 (6), PDB4 (4) to RN26 33 (5).
- Section 4 (RN27):** PDB3 (7) to RN27 33 (8), PDB2 (6) to RN27 33 (7), PDB1 (5) to RN27 33 (6), PDB0 (4) to RN27 33 (5).



Note: Read is data from PCMCIA to MPC850. RWN=1, A to B

