

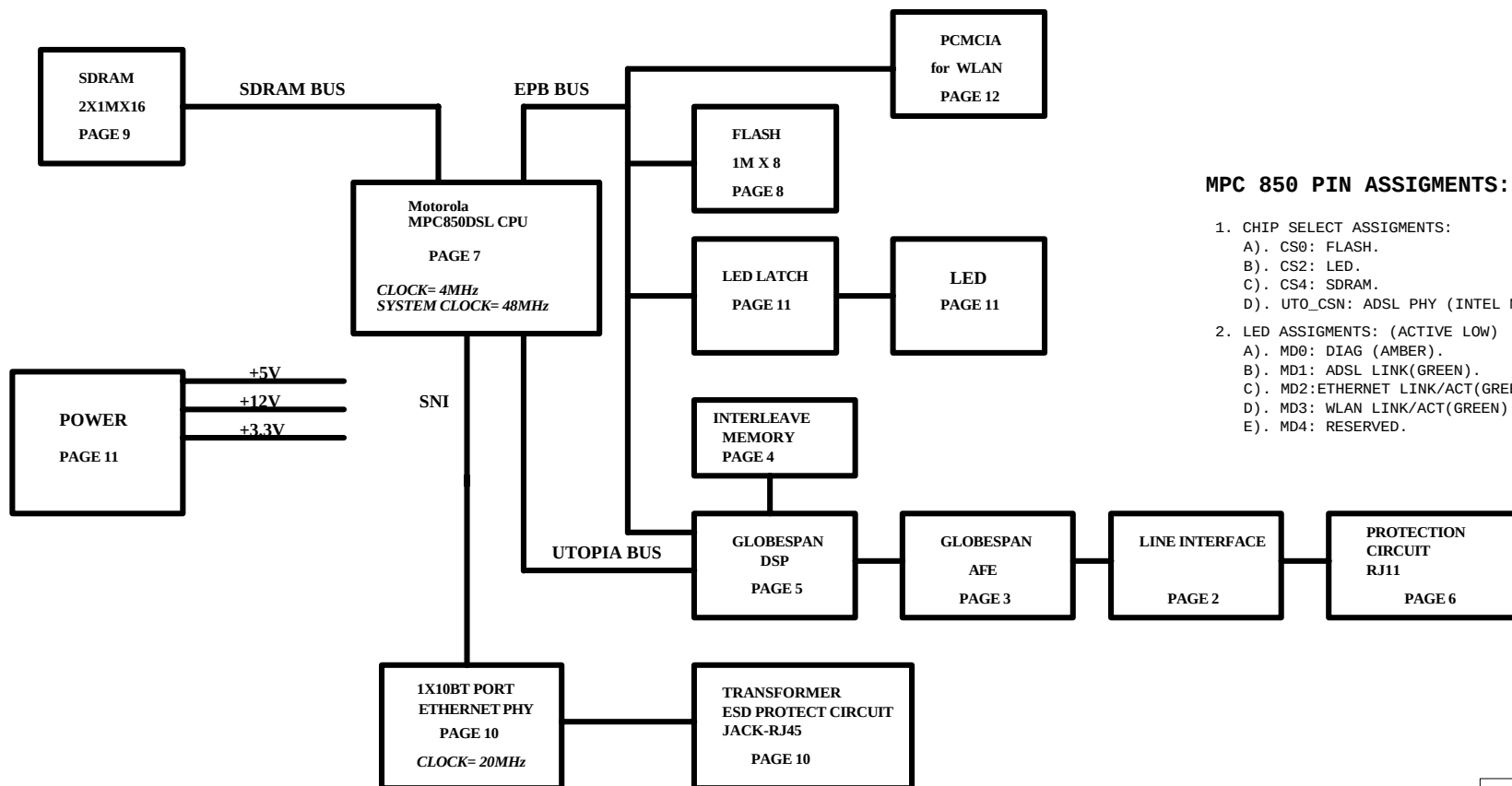
ARESCOM AG2560

Motorola MPC 850 CPU SINGLE BOARD

10BT LAN + WLAN (802.11b)
AG2560 WITH GLOBESPAN 1124 PHY
ANNEX A

PCB P/N: 109000000205

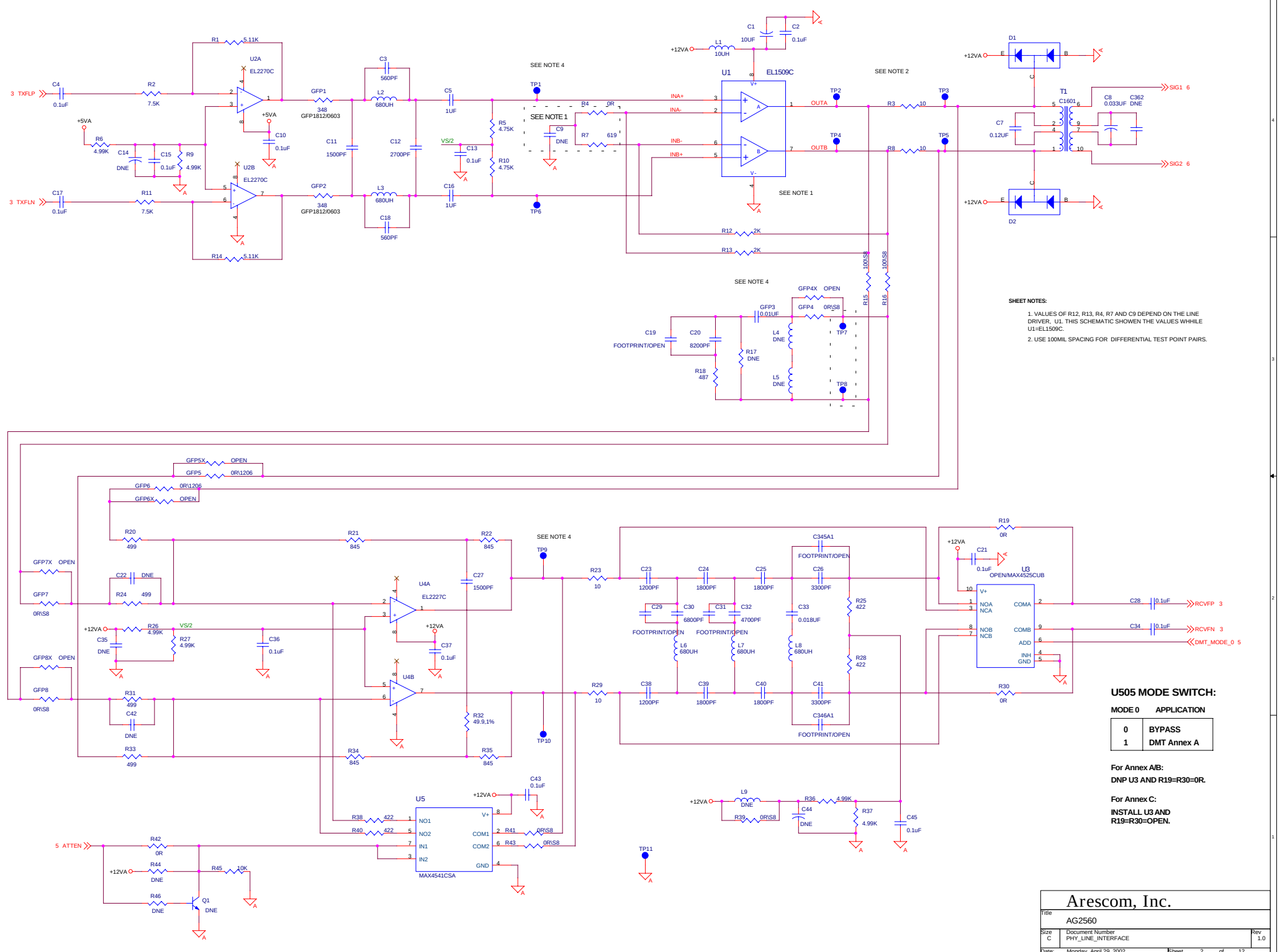
BLOCK DIAGRAM:



MPC 850 PIN ASSIGNMENTS:

1. CHIP SELECT ASSIGNMENTS:
 - A). CS0: FLASH.
 - B). CS2: LED.
 - C). CS4: SDRAM.
 - D). UTO_CSN: ADSL PHY (INTEL MODE).
2. LED ASSIGNMENTS: (ACTIVE LOW)
 - A). MD0: DIAG (AMBER).
 - B). MD1: ADSL LINK(GREEN).
 - C). MD2: ETHERNET LINK/ACT(GREEN).
 - D). MD3: WLAN LINK/ACT(GREEN).
 - E). MD4: RESERVED.

Arescom, Inc.



SHEET NOTES:

1. VALUES OF R12, R13, R4, R7 AND C9 DEPEND ON THE LINE DRIVER. U1 THIS SCHEMATIC SHOWN THE VALUES WHILE U1=EL1509C.

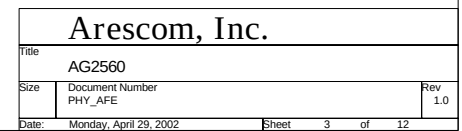
2. USE 100MIL SPACING FOR DIFFERENTIAL TEST POINT PAIRS.

U505 MODE SWITCH:

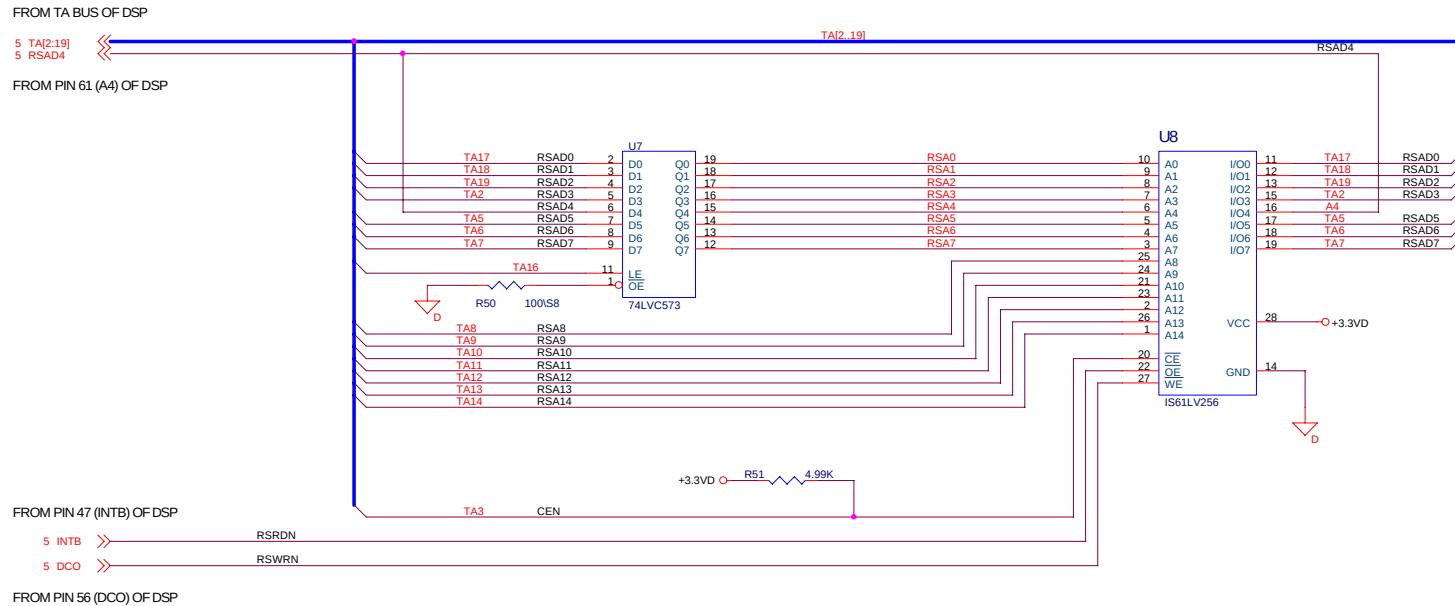
MODE 0	APPLICATION
0	BYPASS
1	DMT Annex A

For Annex A/B:
DNP U3 AND R19=R30=0R.

For Annex C:
INSTALL U3 AND
R19=R30=OPEN.



INTERLEAVING MEMORY



INTERLEAVING MEMORY PIN/FUNCTION ASSIGNMENTS:

TA2, TA[5..7], RSAD4, TA[17..19] = ADDRESS[0..7]

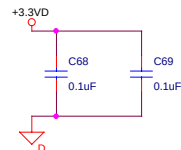
TA[8..15], RSA16 = ADDRESS[8..16]

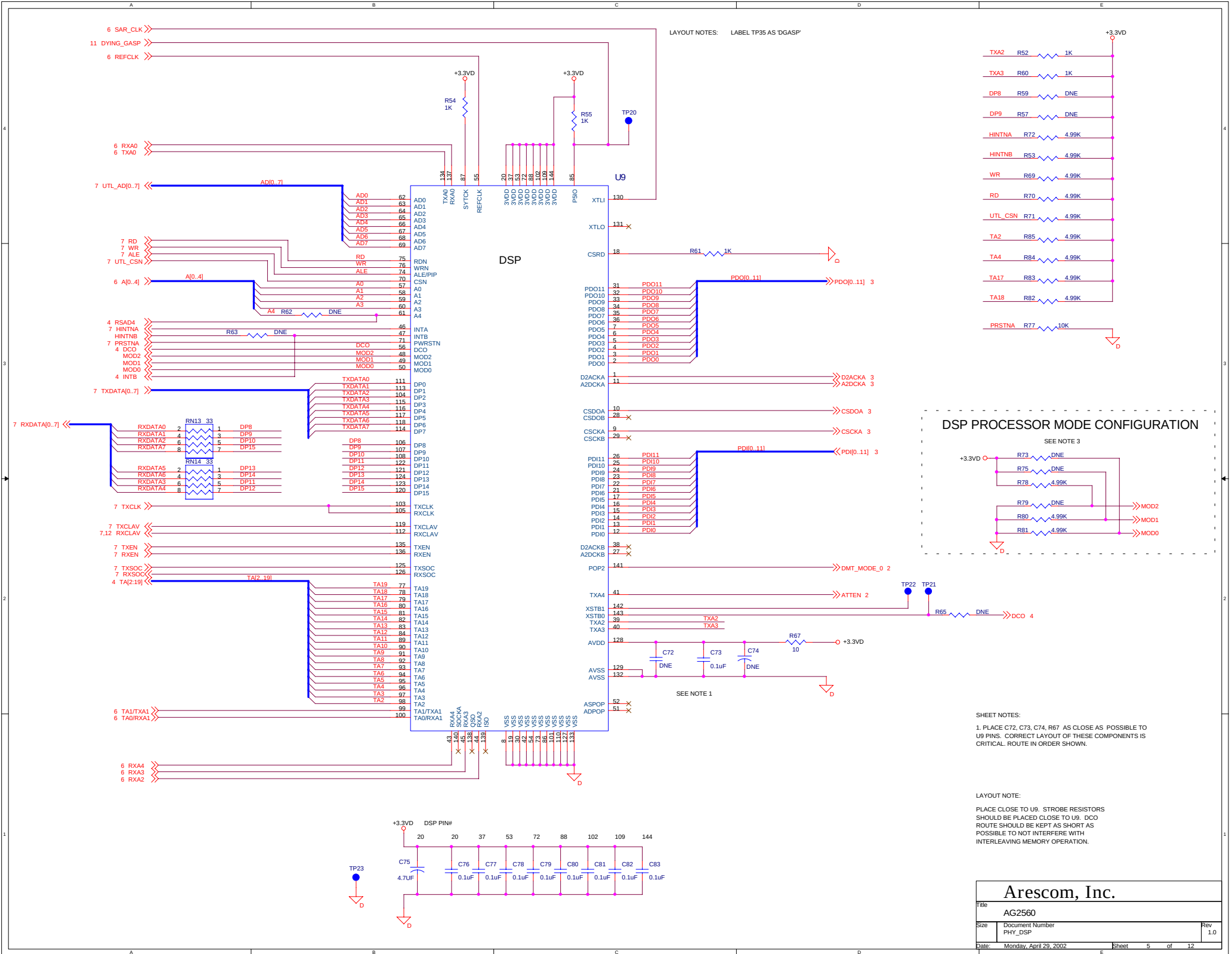
TA[16] = ALE

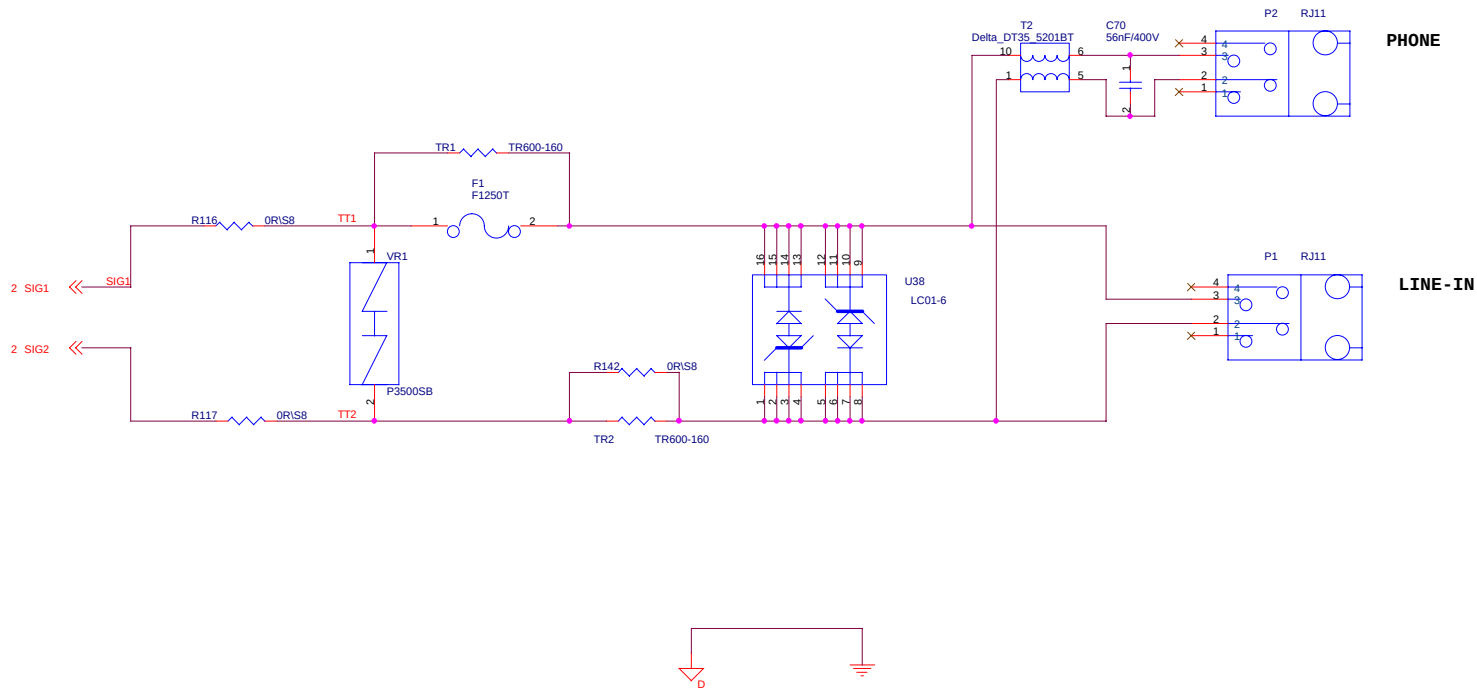
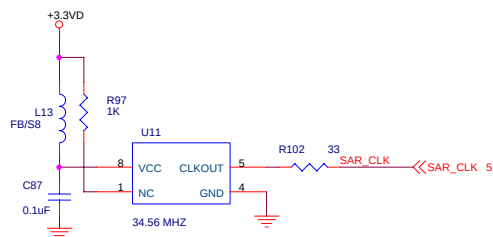
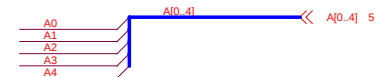
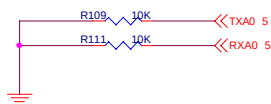
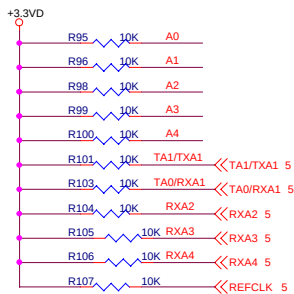
TA[3] = CEN

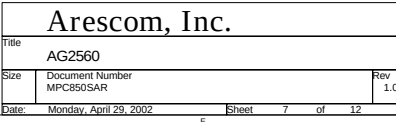
INTB = RSRDN

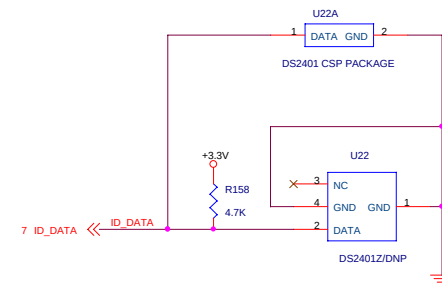
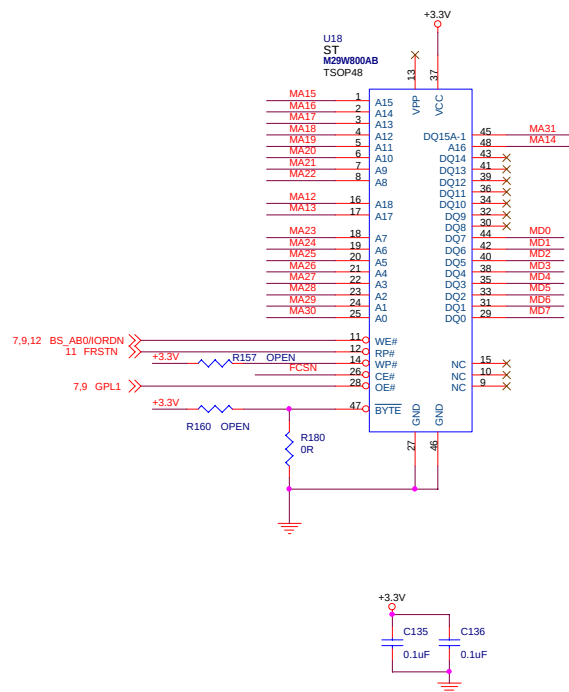
DCO = RSWRN

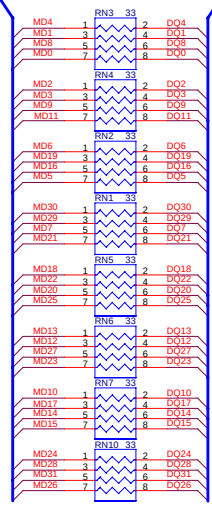
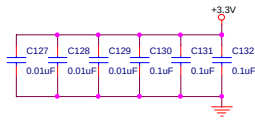
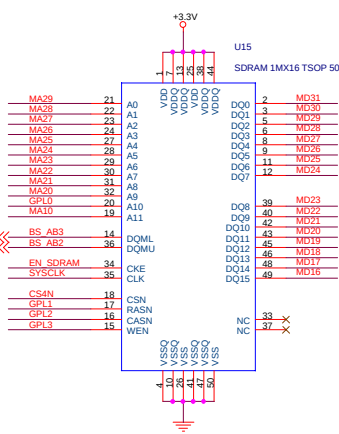
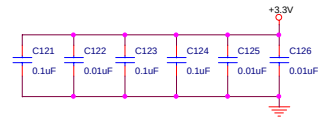
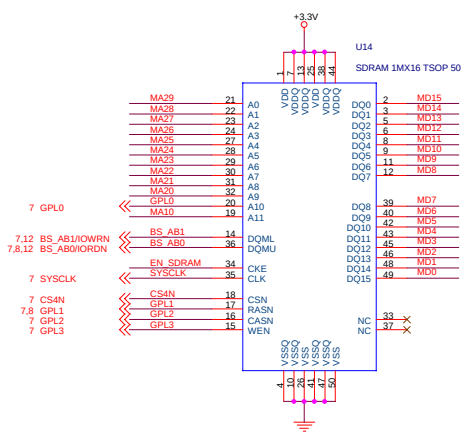
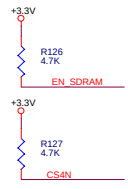
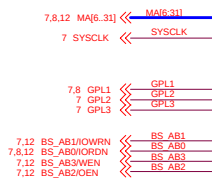


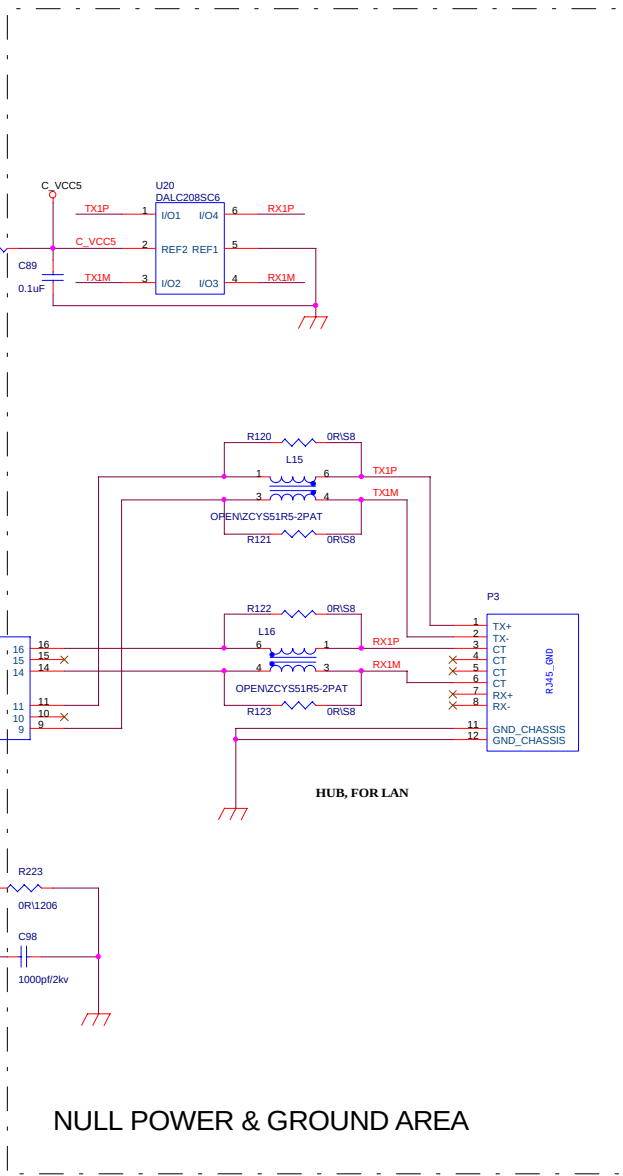
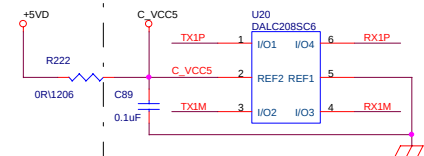
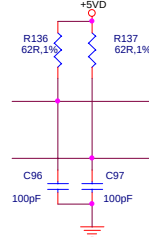
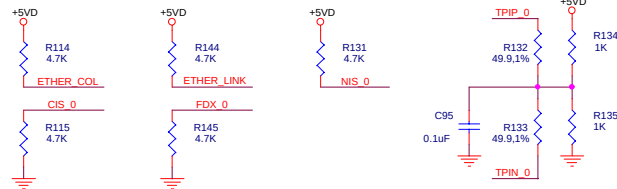
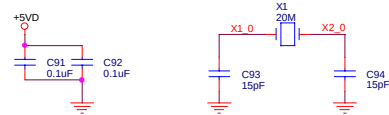
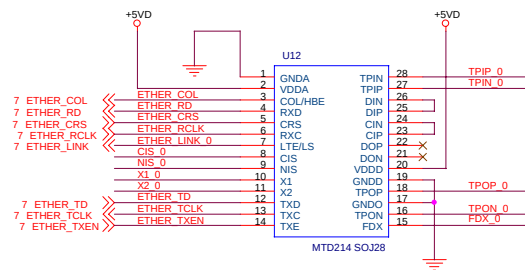


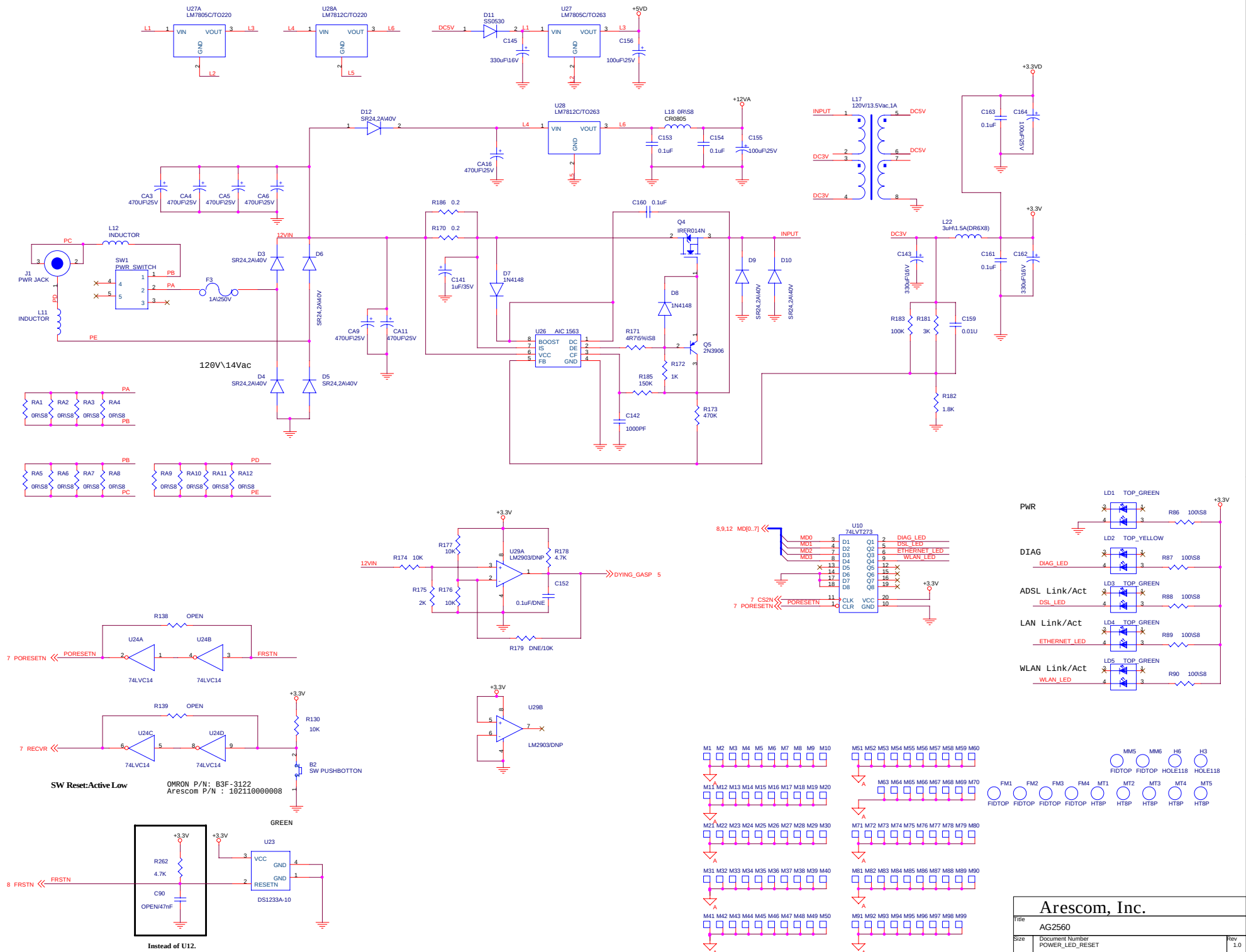


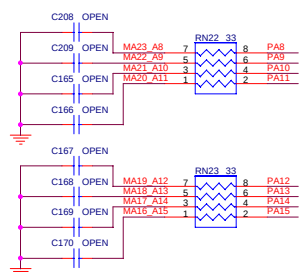






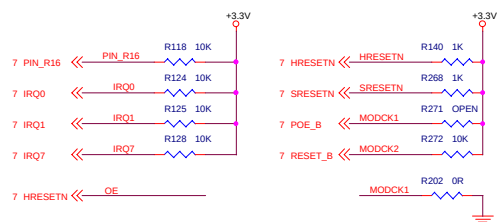
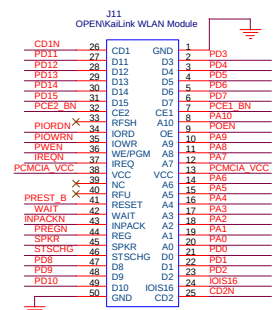
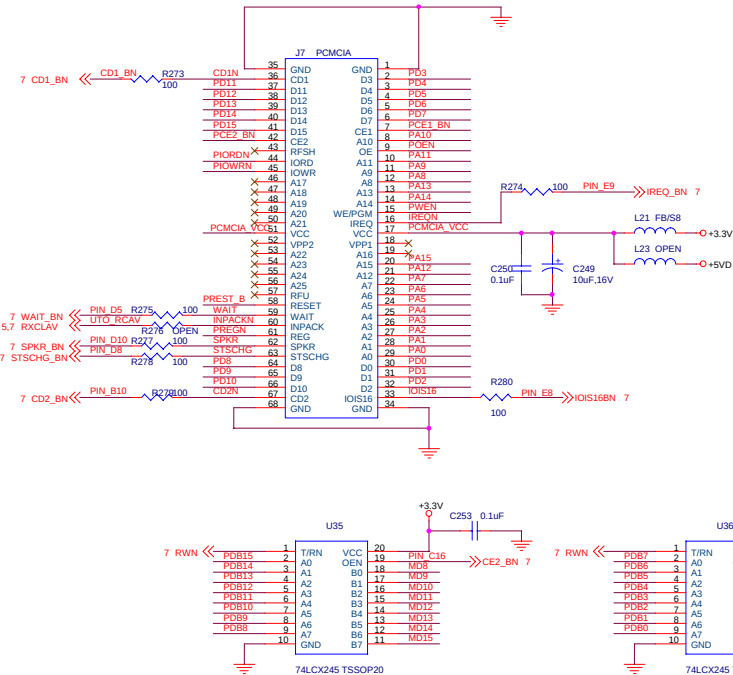
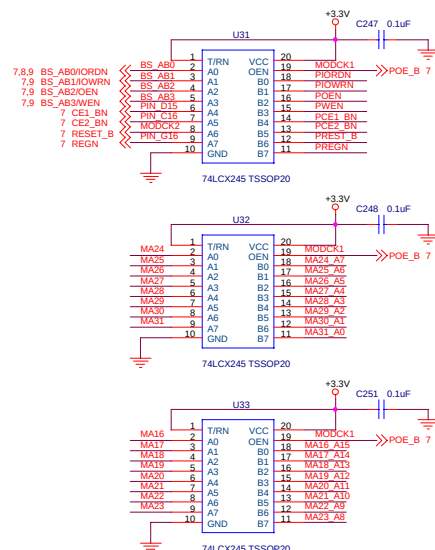
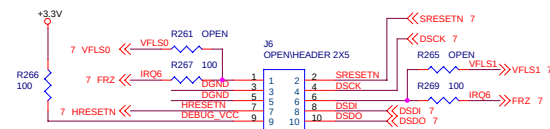
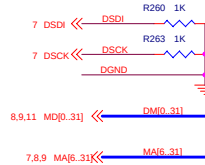






U30
74LCX125

Pin	Signal	Level / Connection
1	OE1	VCC +3.3V
2	IN1	MD9 (via R264)
3	IN2	+3.3V
4	OE2	+3.3V
5	IN3	MD10 (via R270)
6	IN4	+3.3V
7	OUT1	GND
14	OE3	+3.3V
13	IN5	+3.3V
12	IN6	MD5
11	IN7	+3.3V
10	OE4	+3.3V
9	IN8	+3.3V
8	OUT2	MD7



7 CON_RXD1 << R281 10K

7 CON_TXD1 << R282 10K

