

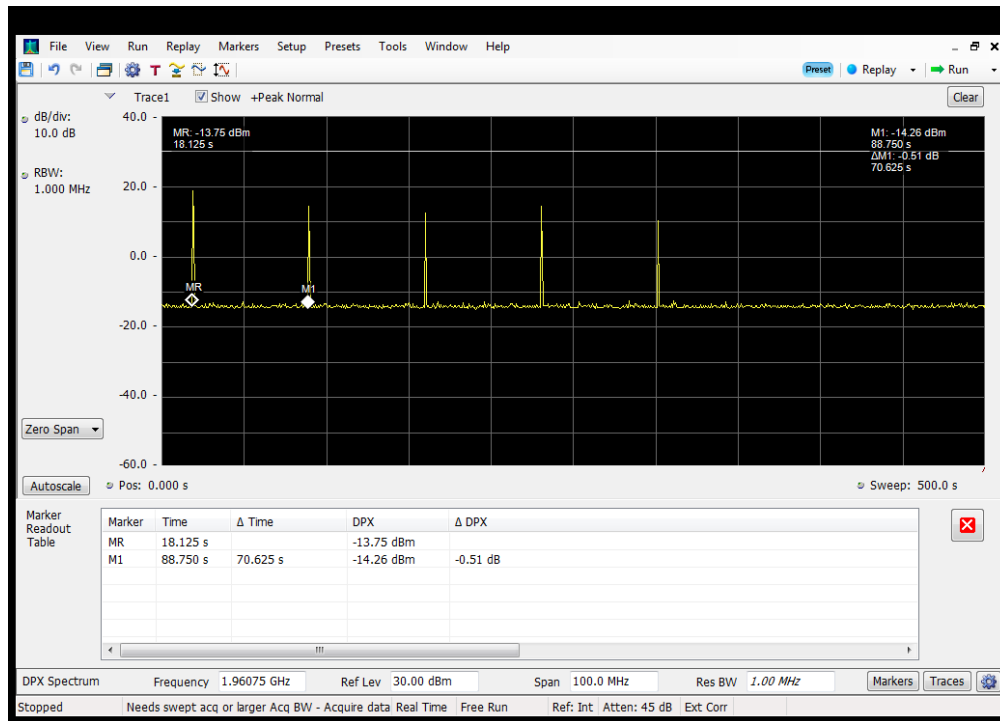


Annex I

Anti - Oscillation



of Restarts_DL_1930 - 1995 MHz

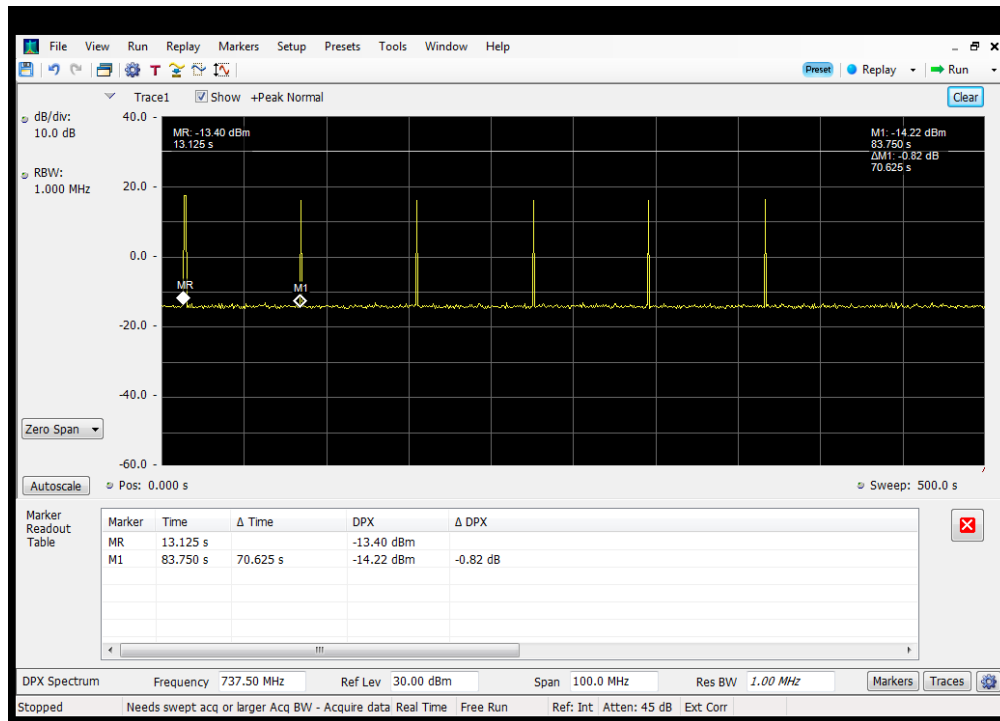


of Restarts_DL_2110 - 2155 MHz

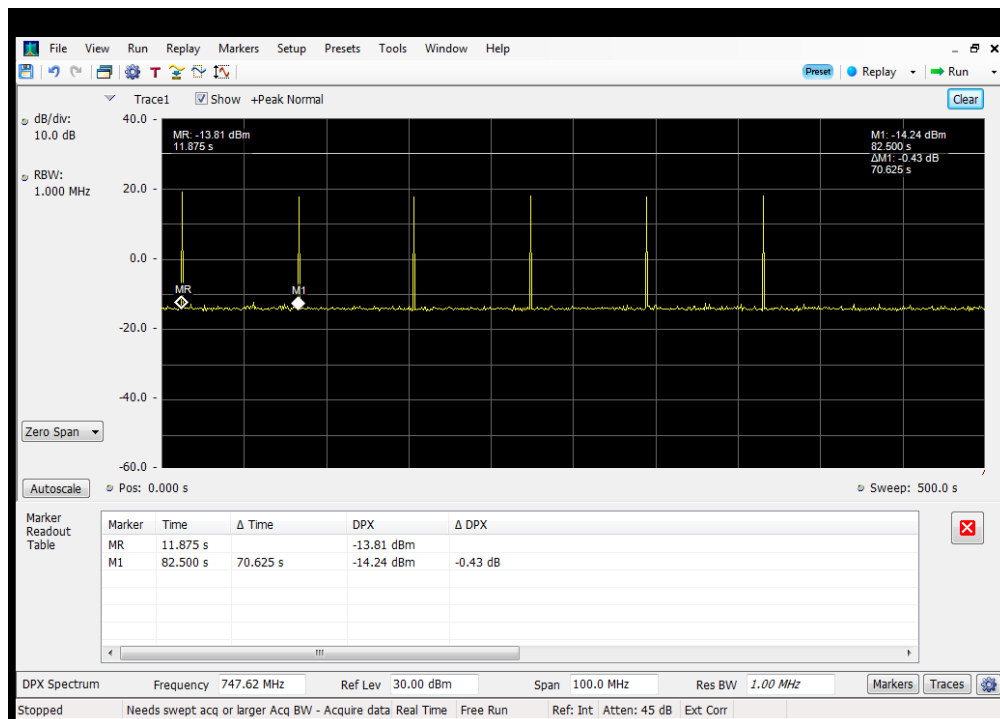




of Restarts_DL_728 - 746 MHz

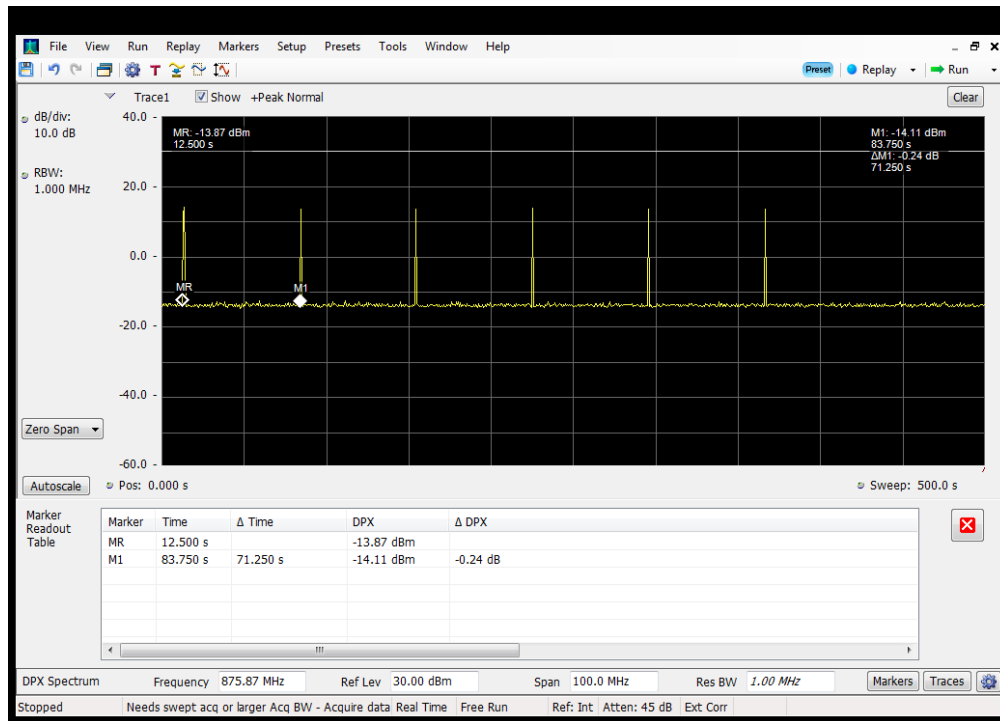


of Restarts_DL_746 - 757 MHz

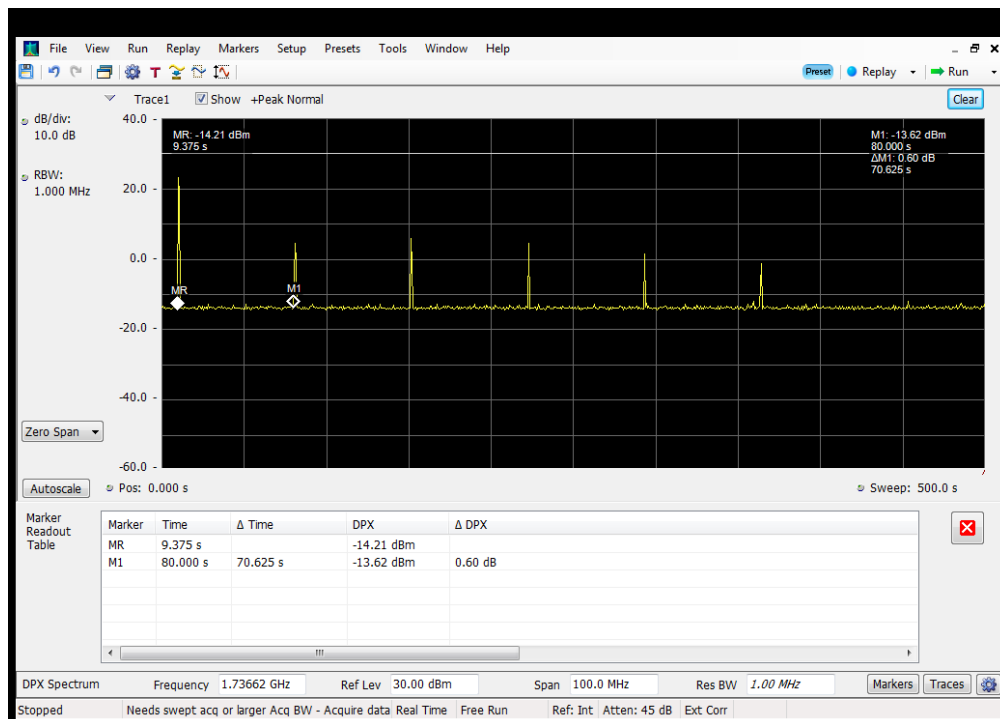




of Restarts_DL_869 - 894 MHz

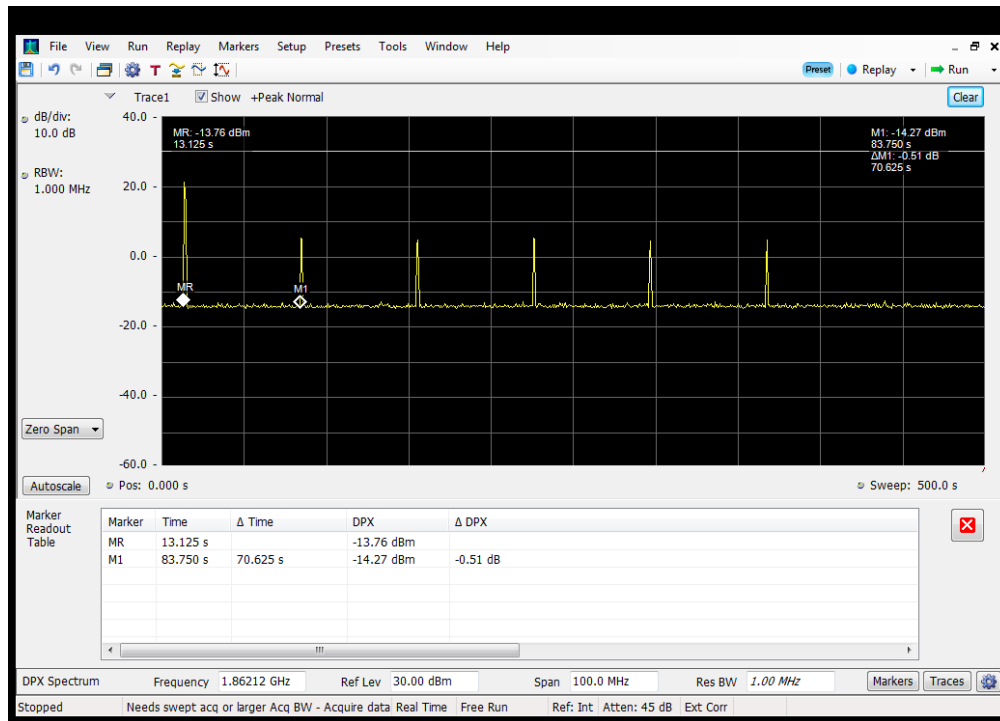


of Restarts_UL_1710 - 1755 MHz

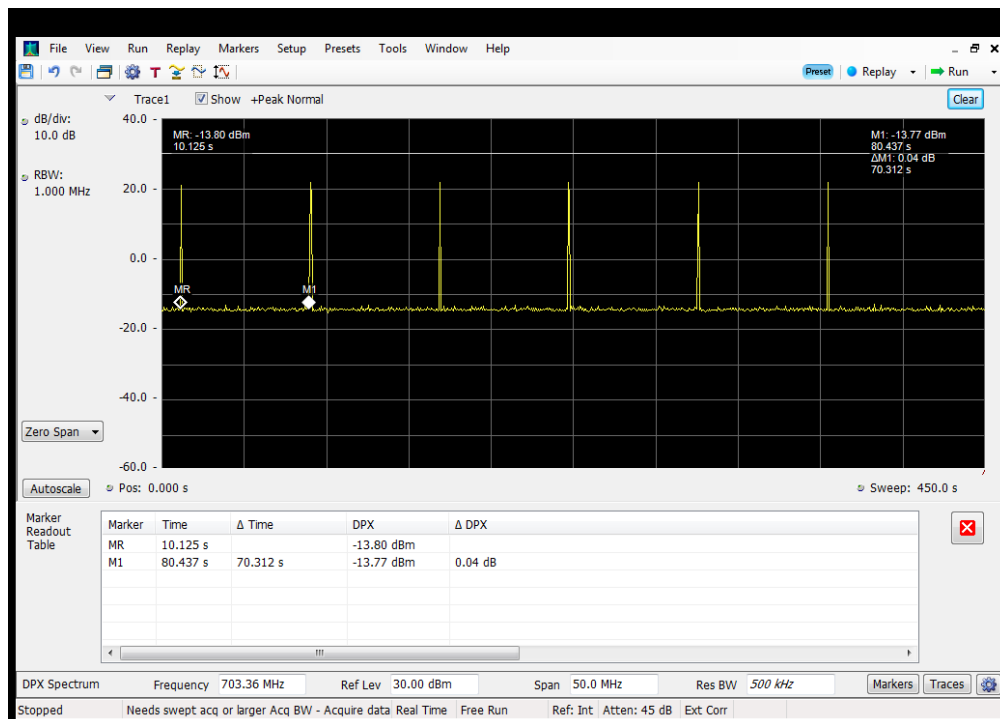




of Restarts_UL_1850 - 1915 MHz

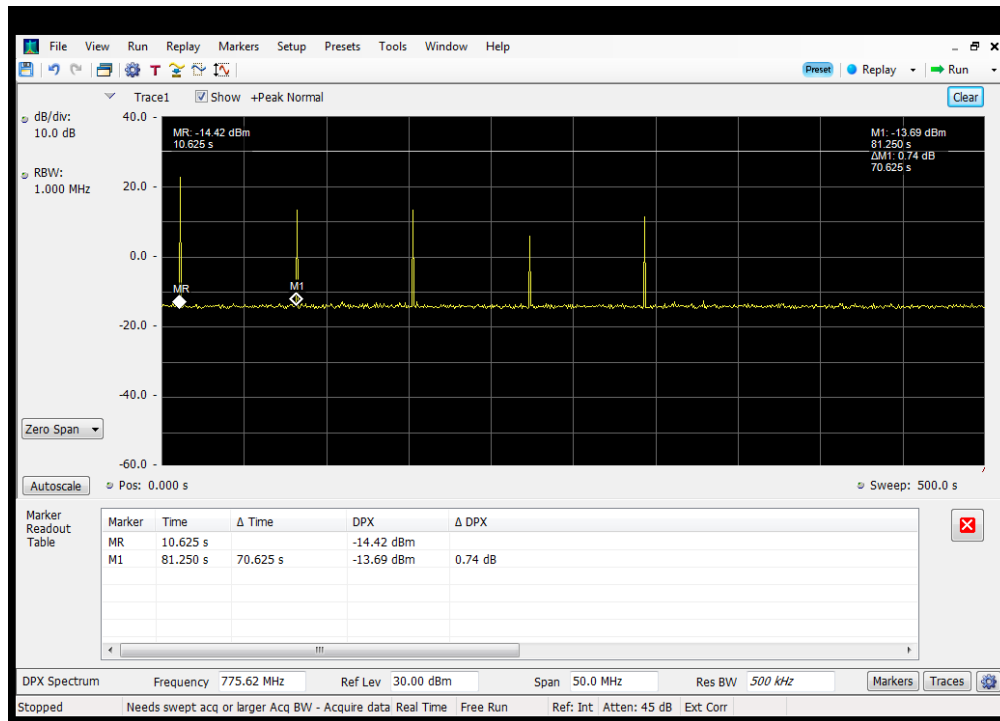


of Restarts_UL_698 - 716 MHz

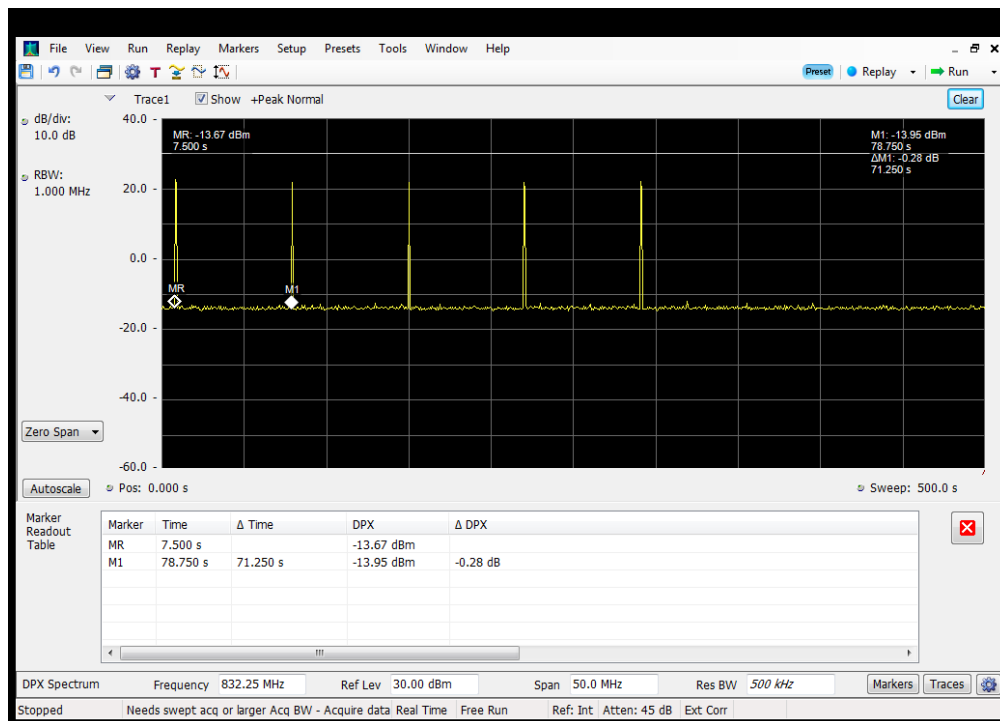




of Restarts_UL_776 - 787 MHz

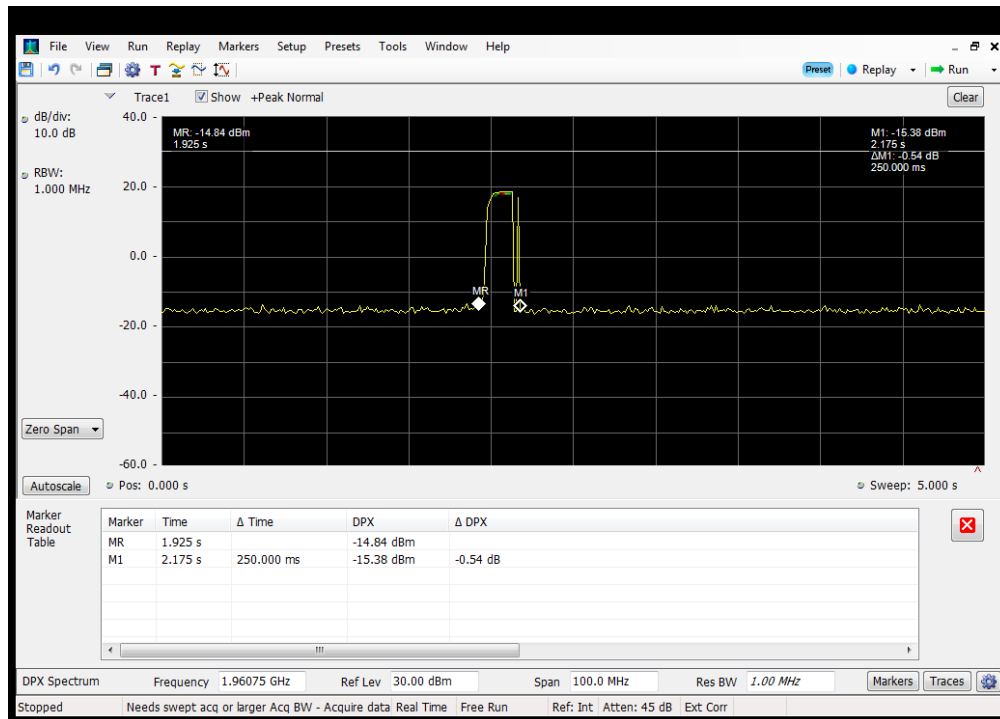


of Restarts_UL_824 - 849 MHz

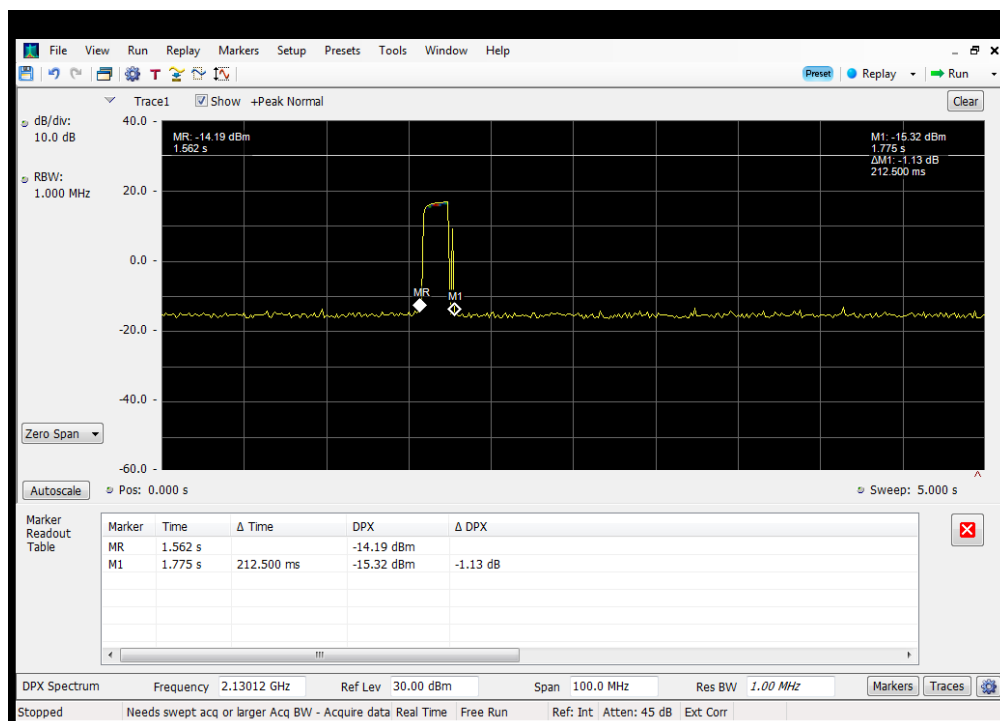




Osc Detection Time_DL_1930 - 1995 MHz

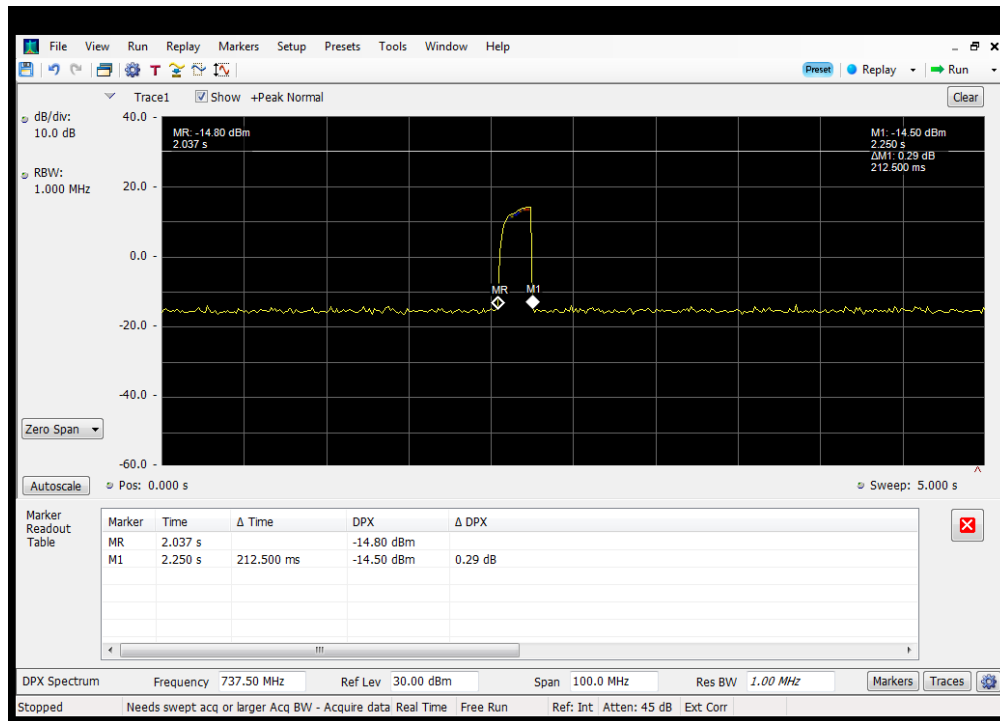


Osc Detection Time_DL_2110 - 2155 MHz

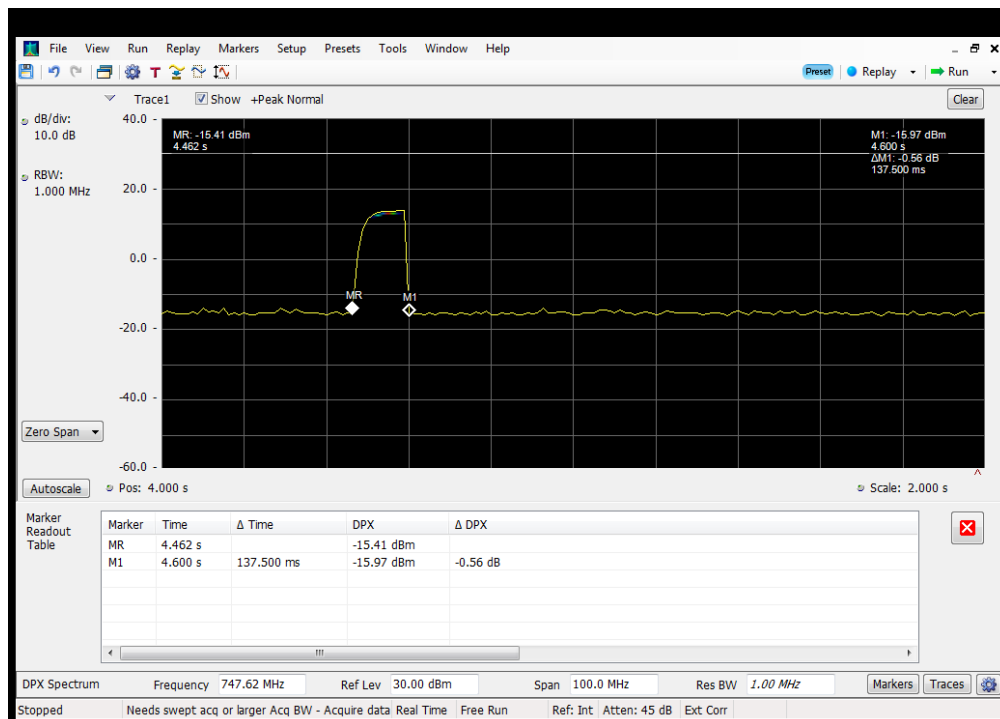




Osc Detection Time_DL_728 - 746 MHz

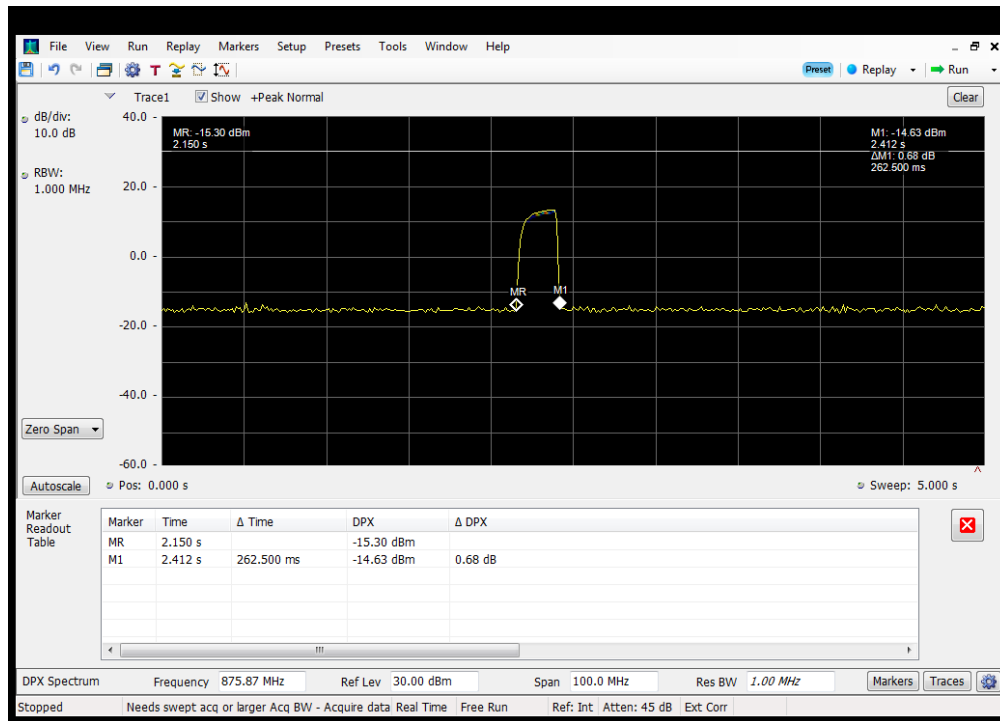


Osc Detection Time_DL_746 - 757 MHz

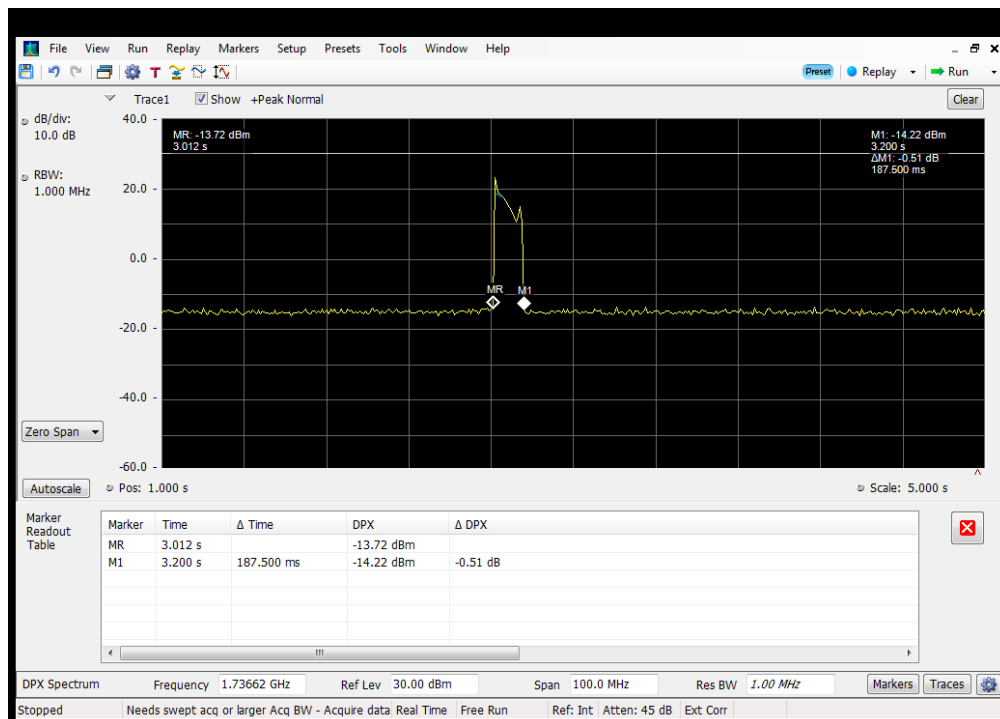




Osc Detection Time_DL_869 - 894 MHz

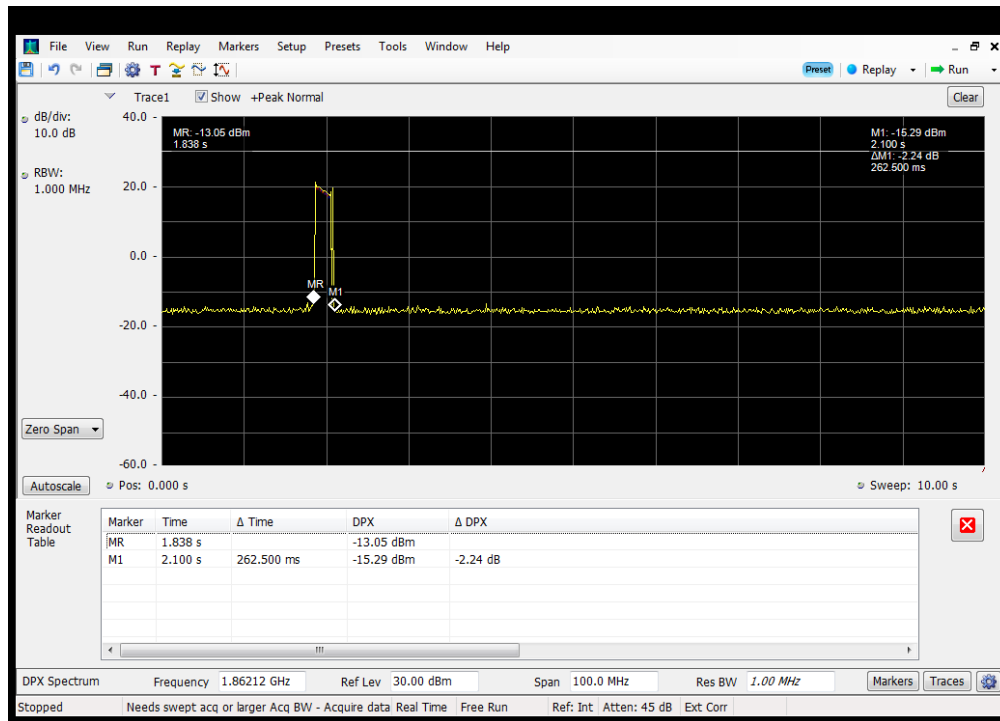


Osc Detection Time_UL_1710 - 1755 MHz

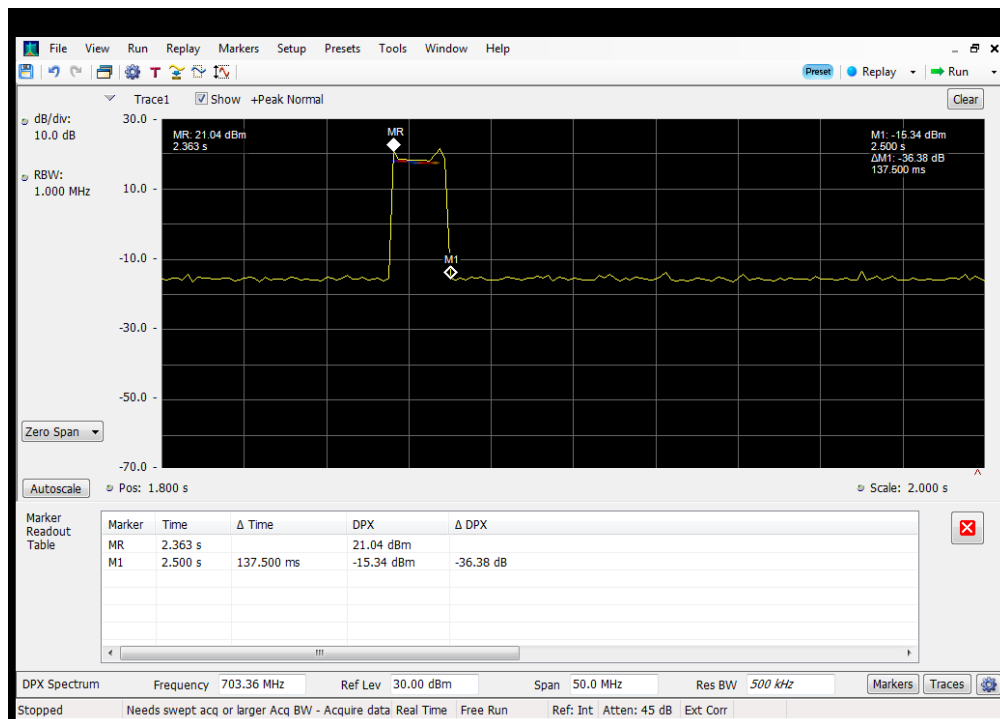




Osc Detection Time_UL_1850 - 1915 MHz

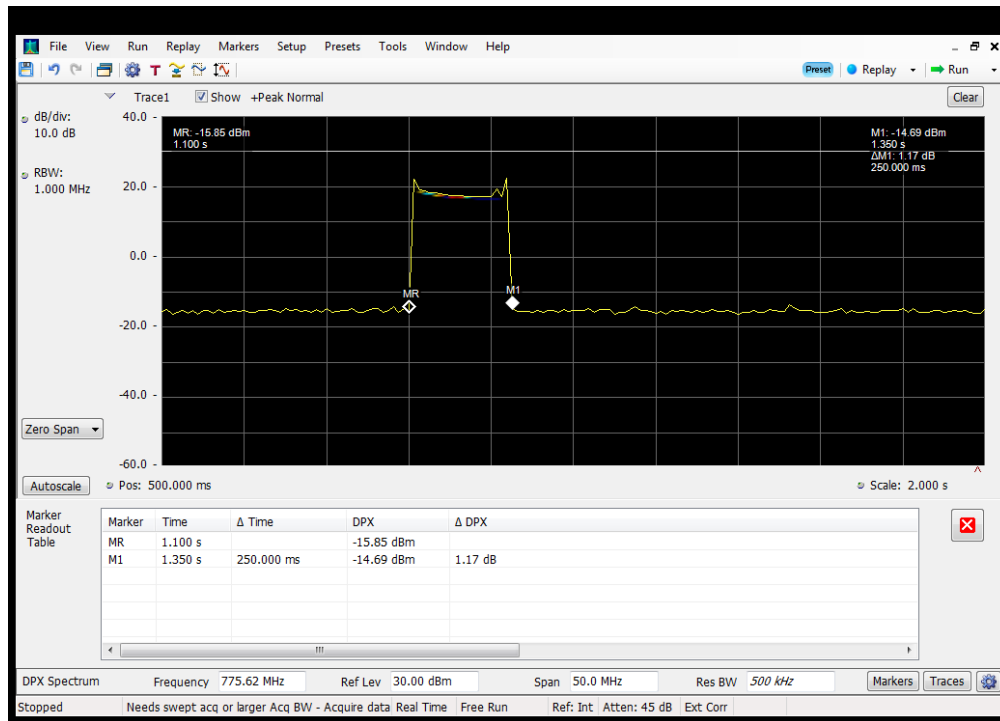


Osc Detection Time_UL_698 - 716 MHz

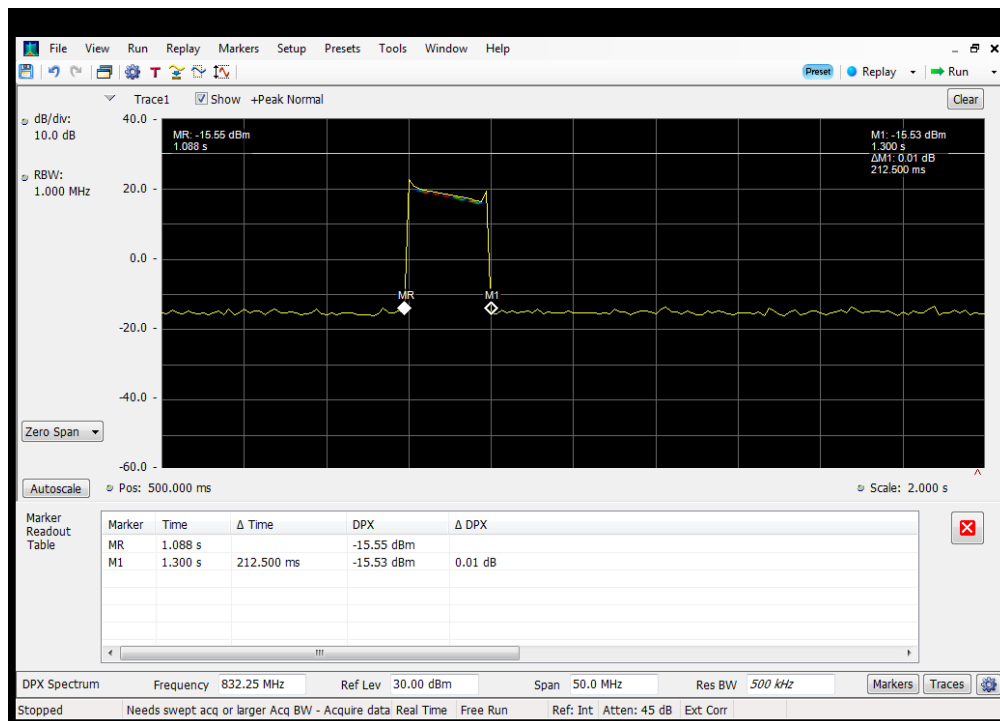




Osc Detection Time_UL_776 - 787 MHz

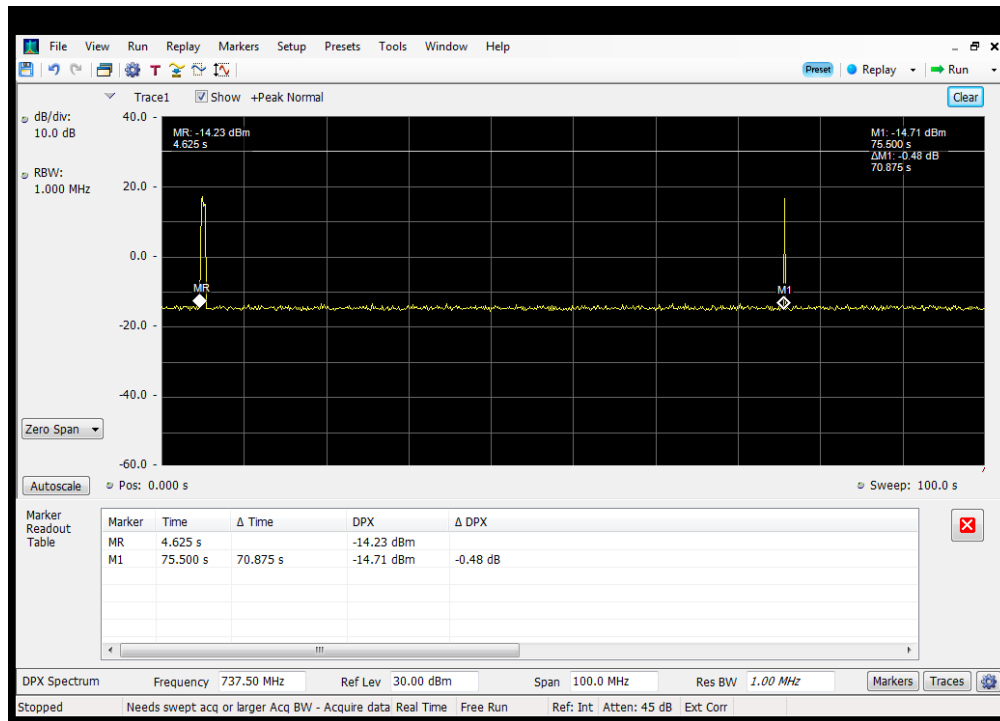


Osc Detection Time_UL_824 - 849 MHz

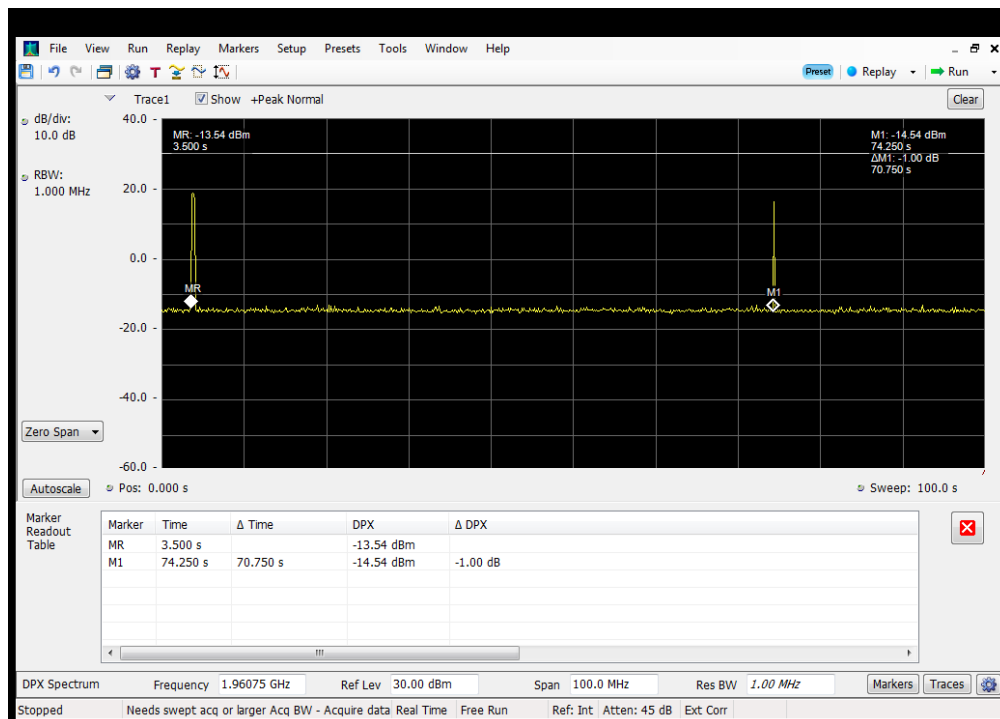




Osc Restart Timing_DL728 - 746 MHz

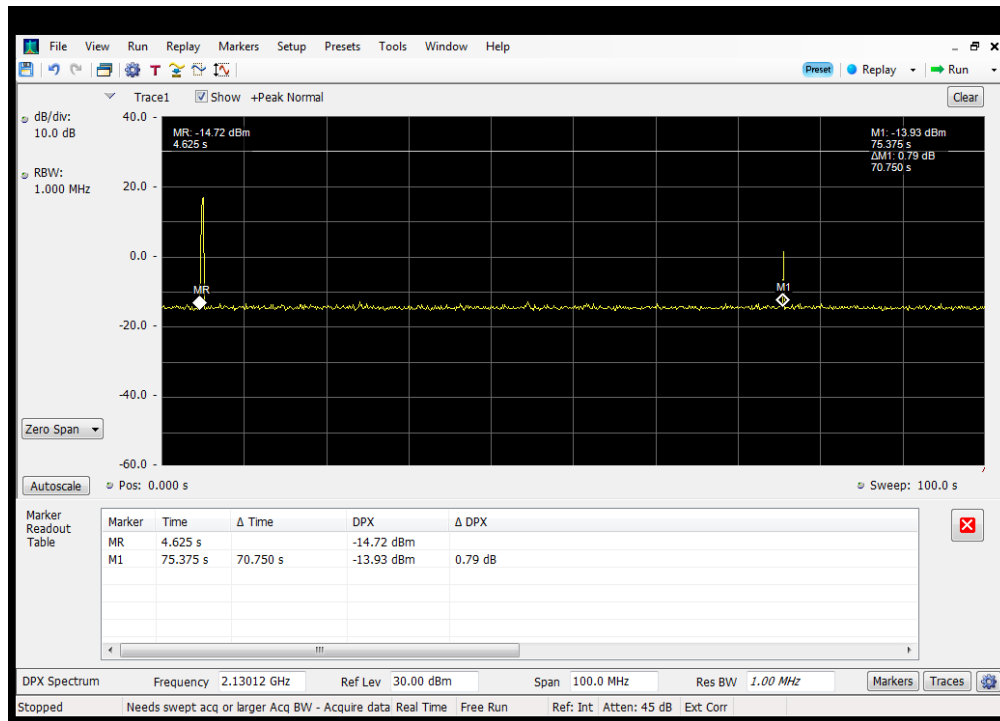


Osc Restart Timing_DL_1930 - 1995 MHz

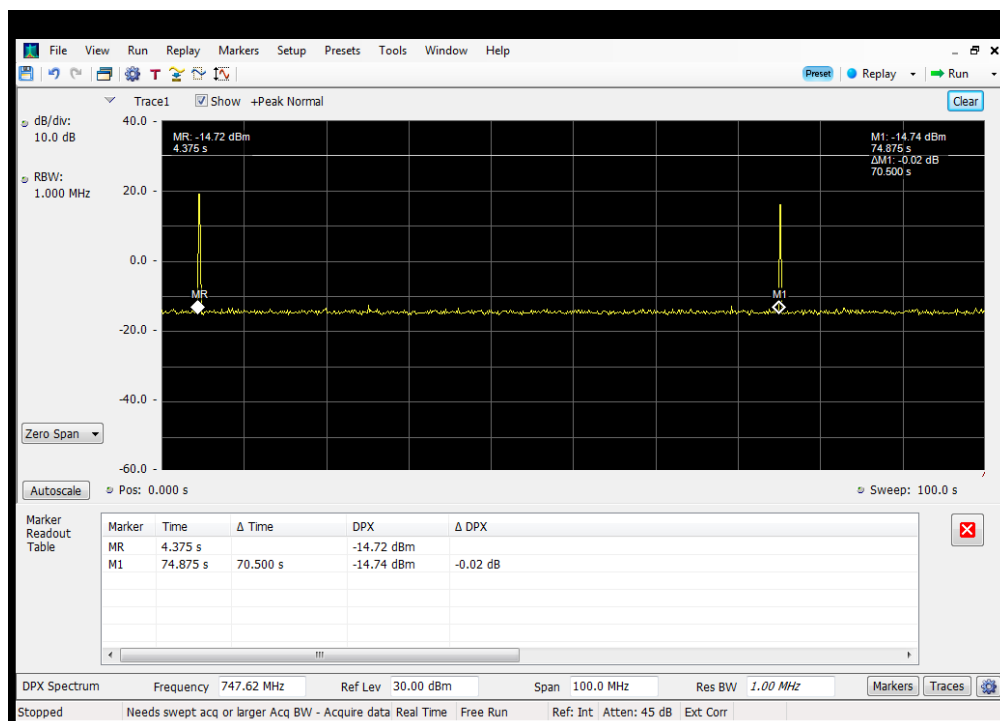




Osc Restart Timing_DL_2110 - 2155 MHz

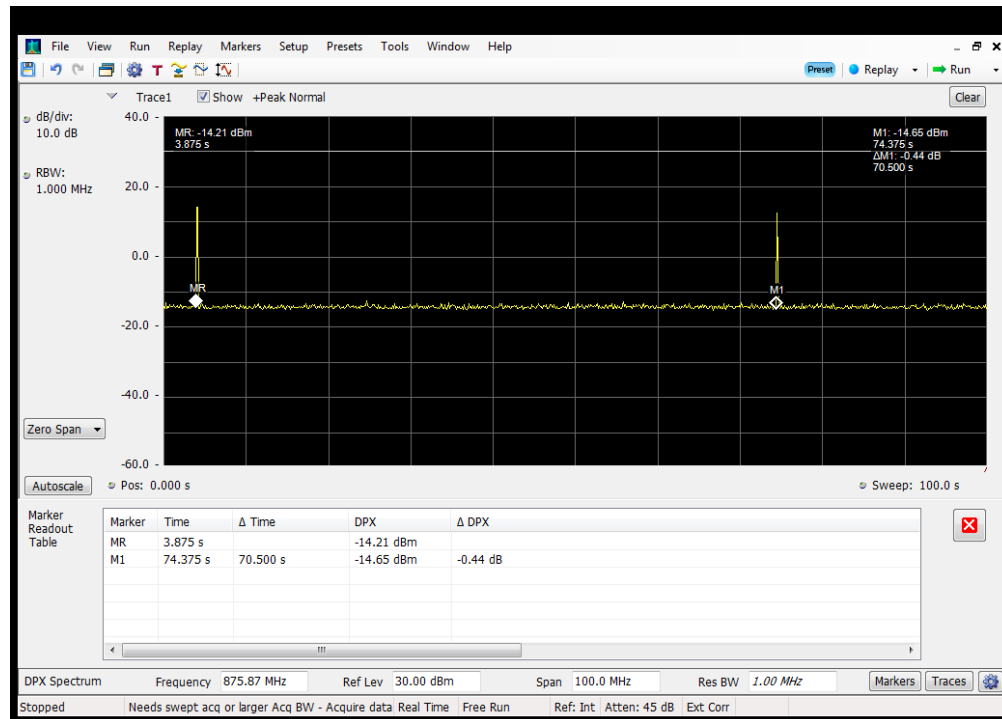


Osc Restart Timing_DL_746 - 757 MHz

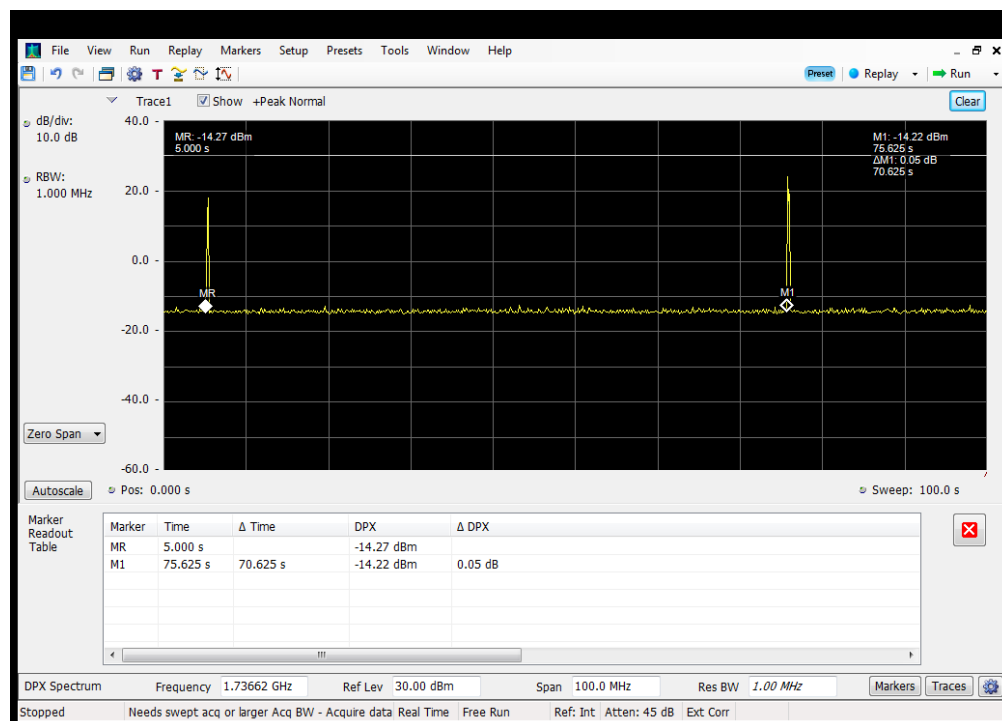




Osc Restart Timing_DL_869 - 894 MHz

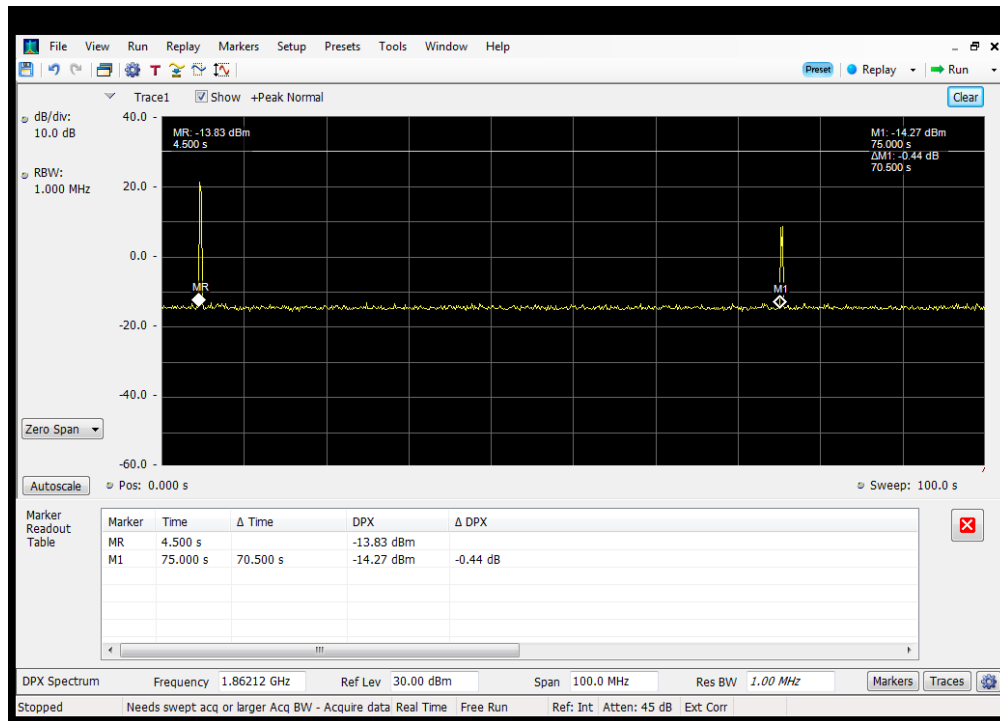


Osc Restart Timing_UL_1710 - 1755 MHz

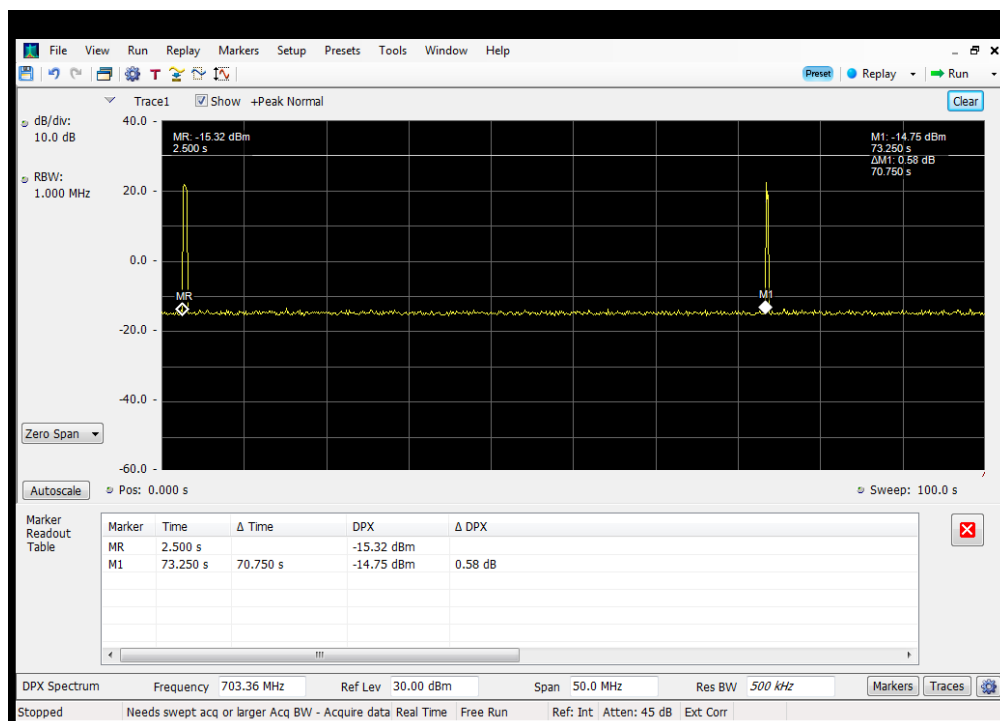




Osc Restart Timing_UL_1850 - 1915 MHz

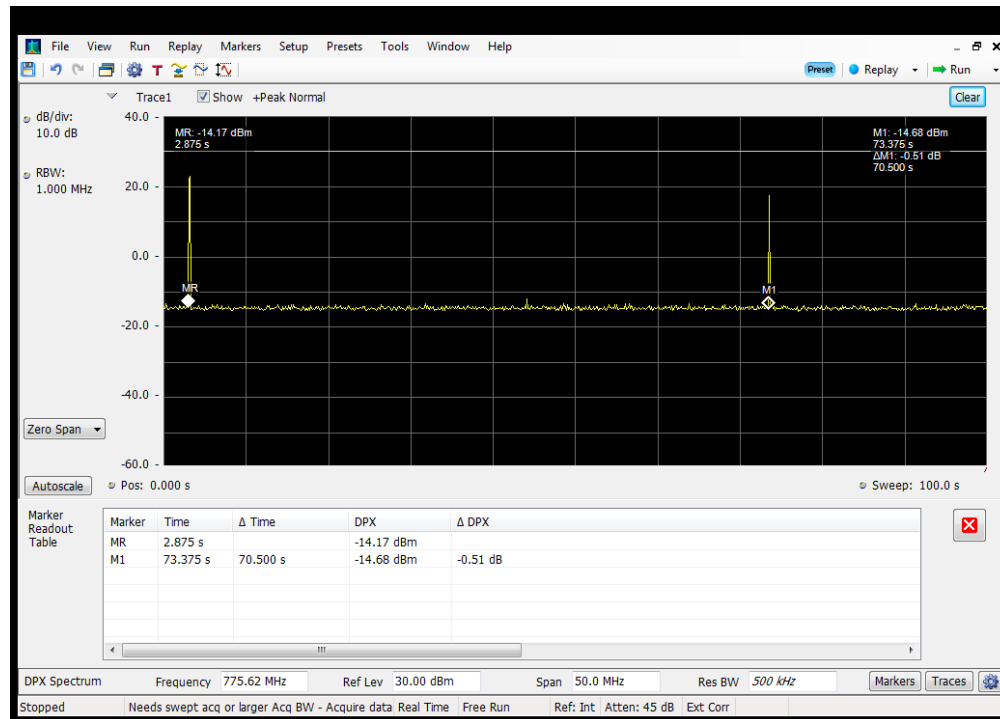


Osc Restart Timing_UL_698 - 716 MHz





Osc Restart Timing_UL_776 - 787 MHz



Osc Restart Timing_UL_824 - 849 MHz

