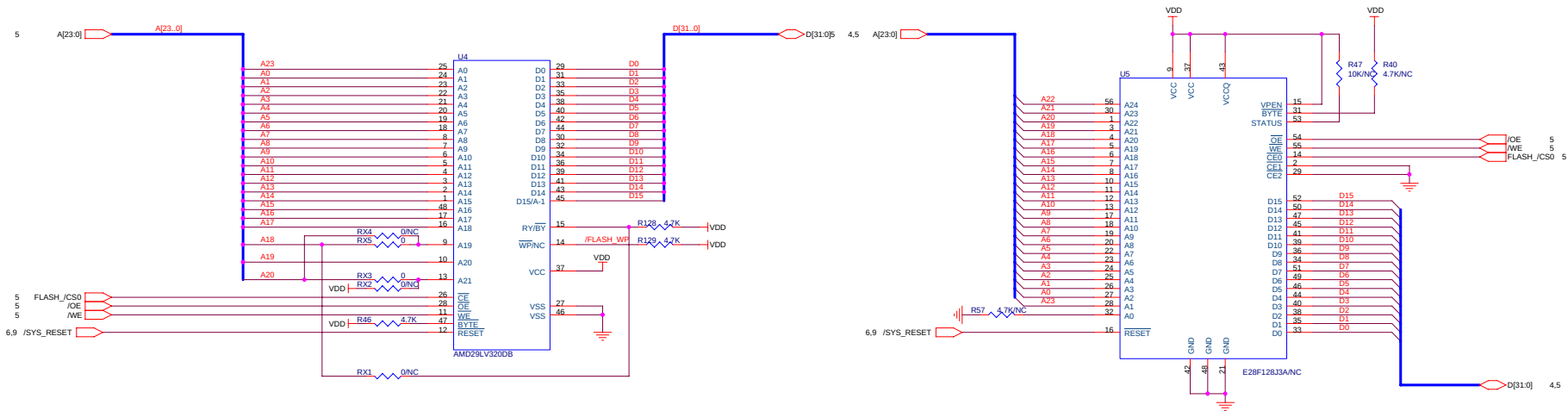


BOARD ID:052038

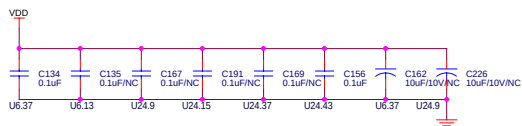
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Title WGR615VV2 CHANGE HISTORY			
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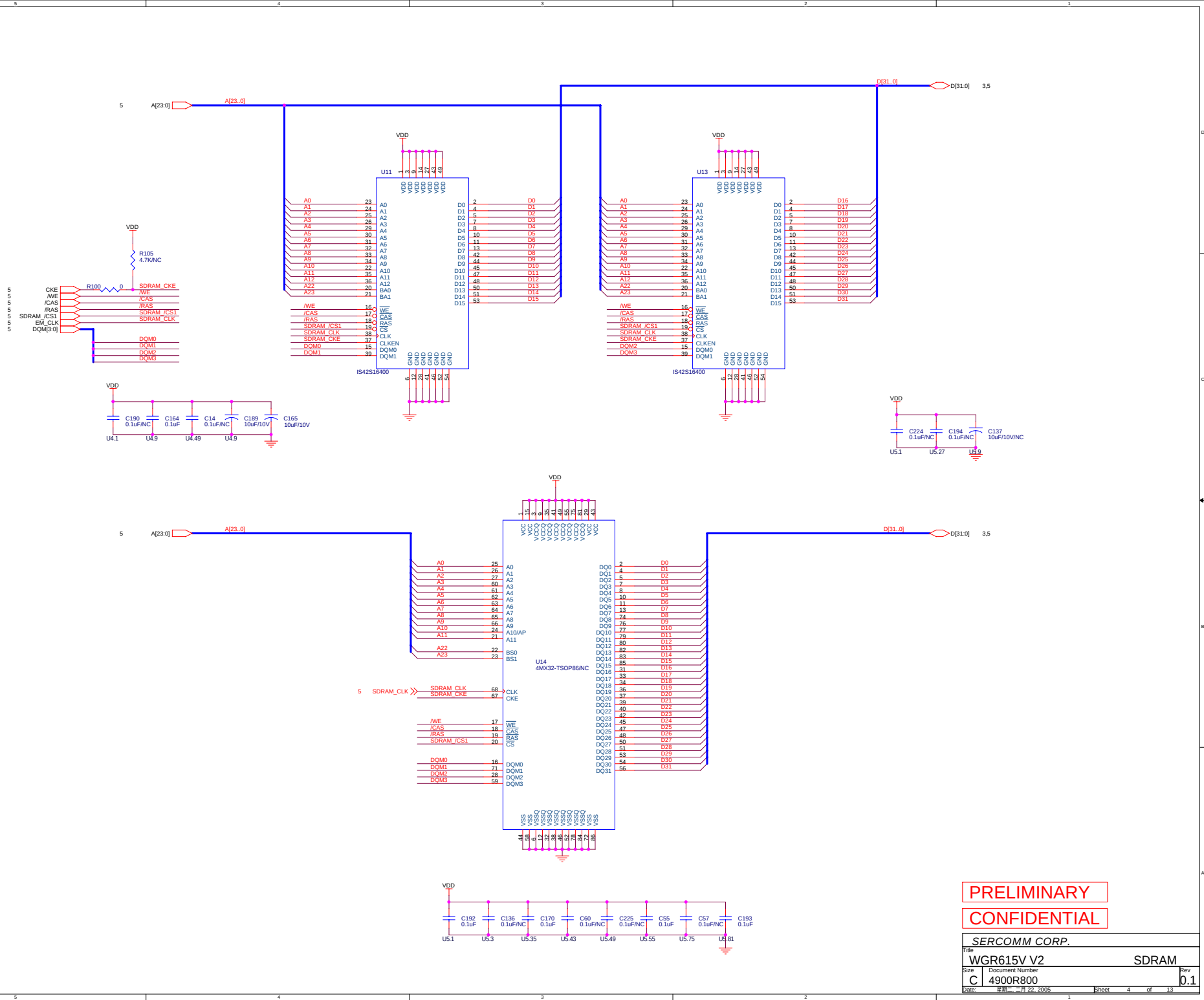


U6	AMD29LV640DB90	28F320C3TA100
RX4	NC	0 OHM
RX5	0 OHM	NC
RX3	0 OHM	NC
RX2	NC	0 OHM
RX1	NC	0 OHM
R46	4.7K OHM	0 OHM
R128	4.7K OHM	NC



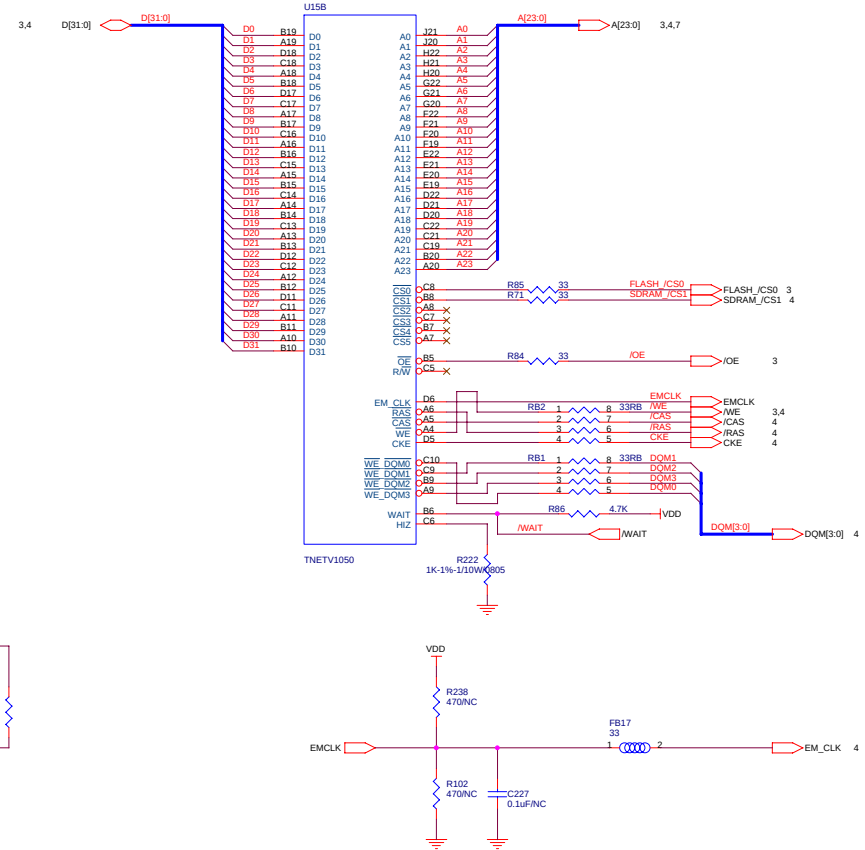
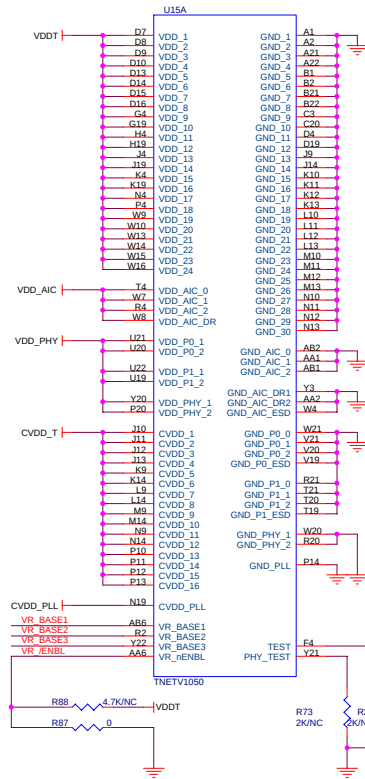
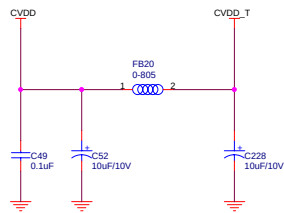
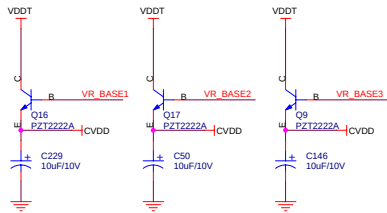
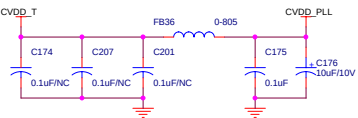
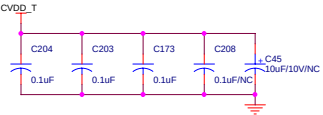
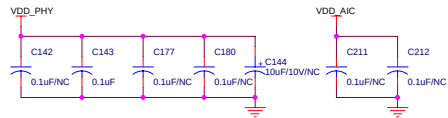
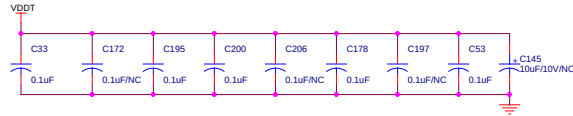
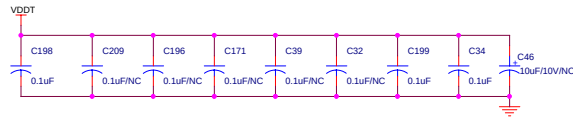
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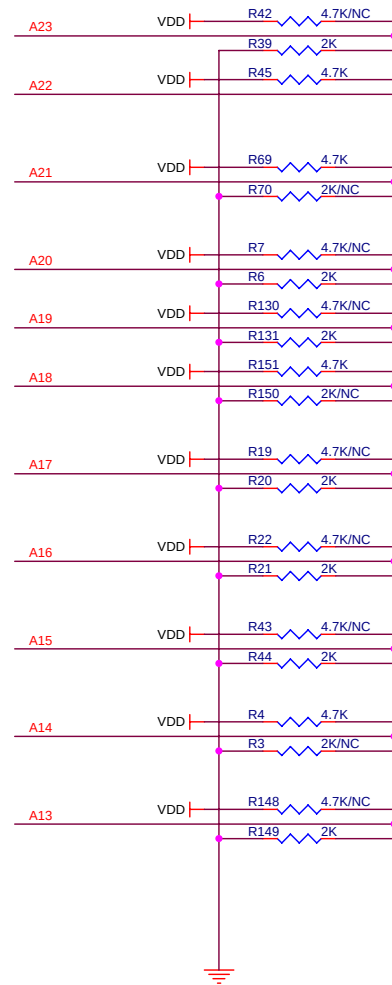
SERCOMM CORP.		
File	WGR615V V2	SDRAM
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BOOT CONFIGURATION OPTIONS



A23,A22 - FLASH WIDTH for CS0
11 - 32bit FLASH (default)
01 - 16bit FLASH

A21 - Endian Mode
1 - Big Endian (default)
0 - Little Endian

A20, A19, A18 - Boot Memory Location
111 - VLYNQ
110 - Serial EEPROM via SSP
101 - PLD_/CS5 (not valid)
100 - FLASH_/CS4
011 - SRAM_/CS3
010 - SDRAM_/CS1
001 - FLASH_/CS0 (default)
000 - Boot from internal 4K ROM

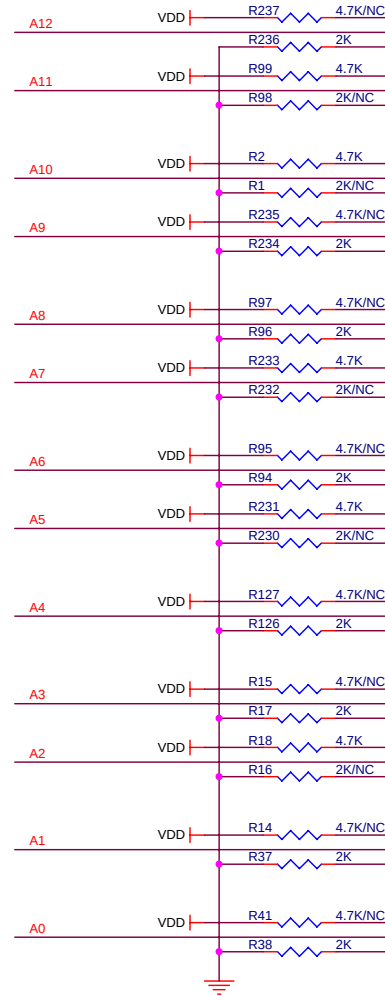
A17 - PLL Mode
1 - Bypass PLL (test mode)
0 - Use PLL (default)

A16 - Watch Dog Mode
1 - Watch Dog always Disabled
0 - Watch Dog may be Enabled (default)

A15 - Watch Dog Write Protect
1 - Watch Dog is write protected
0 - Watch Dog TIMER_ENABLE bit is active (default)

A14 - SDRAM Clock Mode
1 - SDRAM runs at full speed (default)
0 - SDRAM runs at half speed

A13 - SDRAM Initialization Mode
1 - Reduced SDRAM Initialization (test mode)
0 - Normal SDRAM Initialization (default)



A12,A11 - VBUSP Clock Input Mux Select
11 - Internal MIPS PLL clock output
10 - Alternate Clock I/O
01 - Reference Clock I/O (default)
00 - AIC 20 Clock I/O

A10,A9 - USB Clock Input Mux Select
11 - Internal MIPS PLL clock output
10 - Alternate Clock I/O (default)
01 - Reference Clock I/O
00 - AIC 20 Clock I/O

A8,A7 - Ethernet PHY Clock Input Mux Select
11 - Internal MIPS PLL clock output
10 - Alternate Clock I/O
01 - Reference Clock I/O (default)
00 - AIC 20 Clock I/O

A6,A5 - DSP Clock Input Mux Select
11 - Internal MIPS PLL clock output
10 - Alternate Clock I/O
01 - Reference Clock I/O (default)
00 - AIC 20 Clock I/O

A4 - USB Mode
1 - HOST
0 - Device (default)

A3,A2 - MIPS Clock Input Mux Select
11 - Internal MIPS PLL clock output
10 - Alternate Clock I/O
01 - Reference Clock I/O (default)
00 - AIC 20 Clock I/O

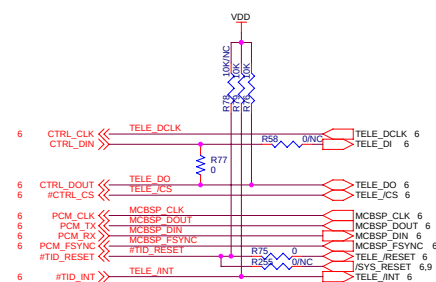
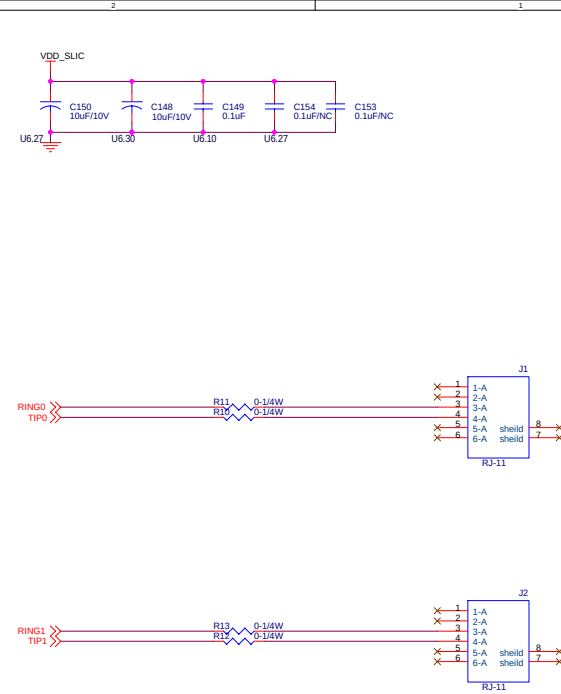
A1 - MIPS Clock Mode
1 - MIPS_CLK is asynchronous
0 - MIPS_CLK is synchronous (default)

A0 - Default Control
1 - Boot Config is default
0 - Boot Config is defined by A23:A0 (default)

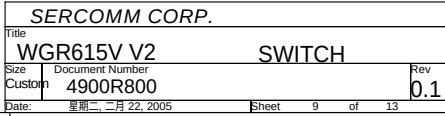
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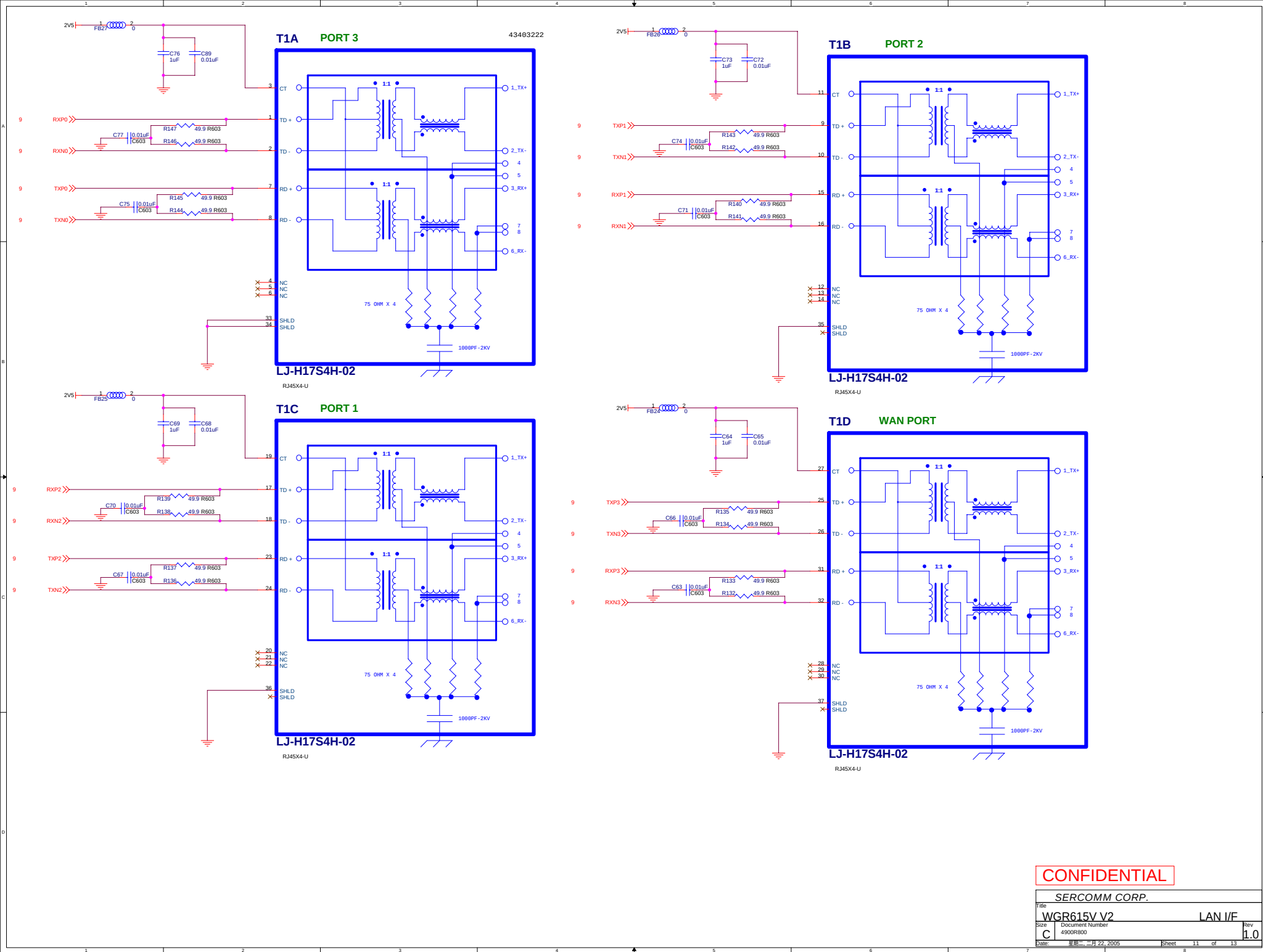
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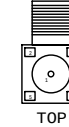
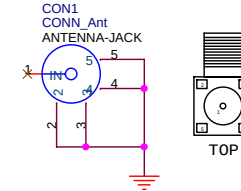
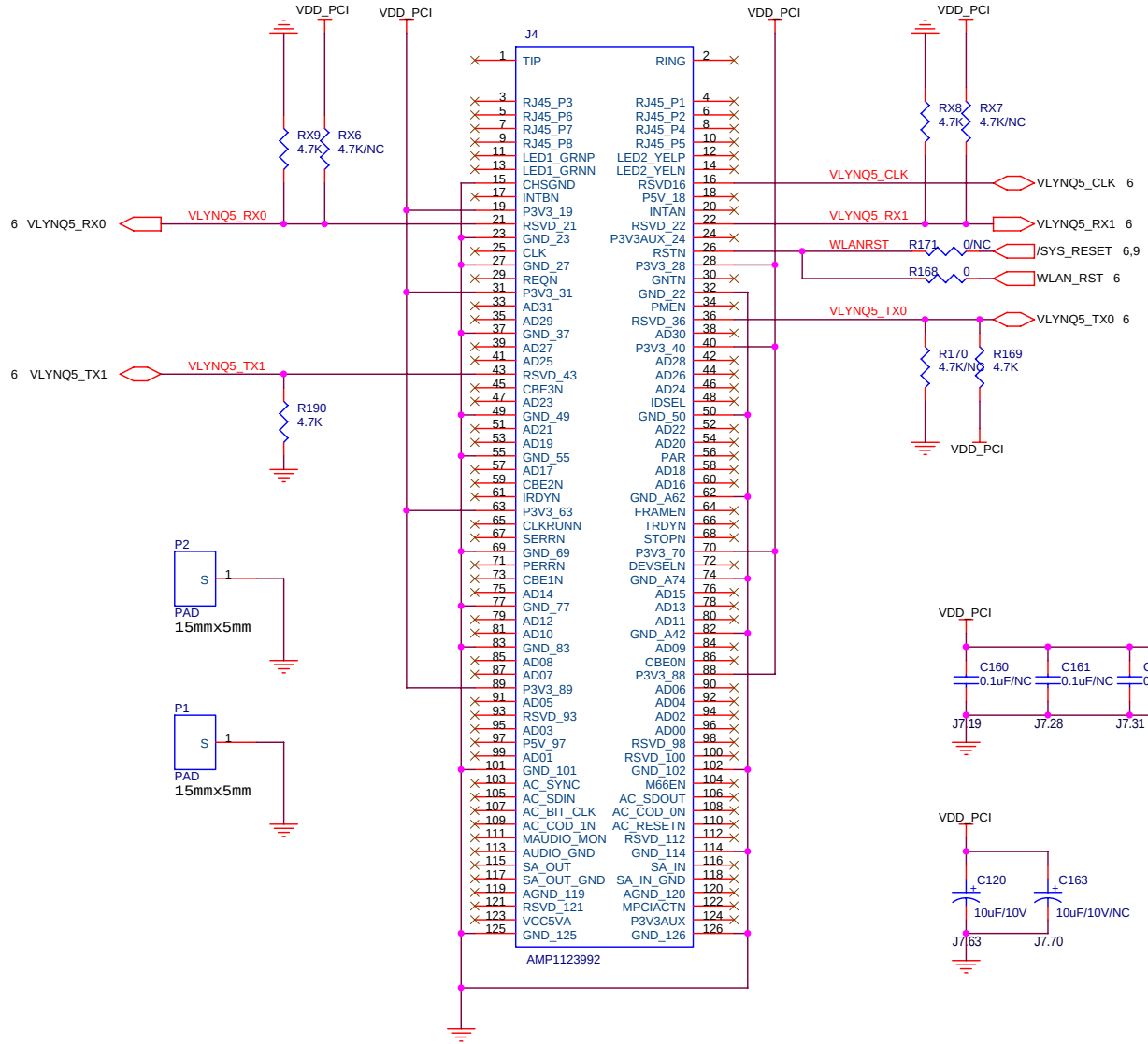




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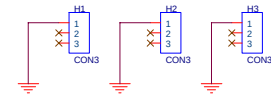
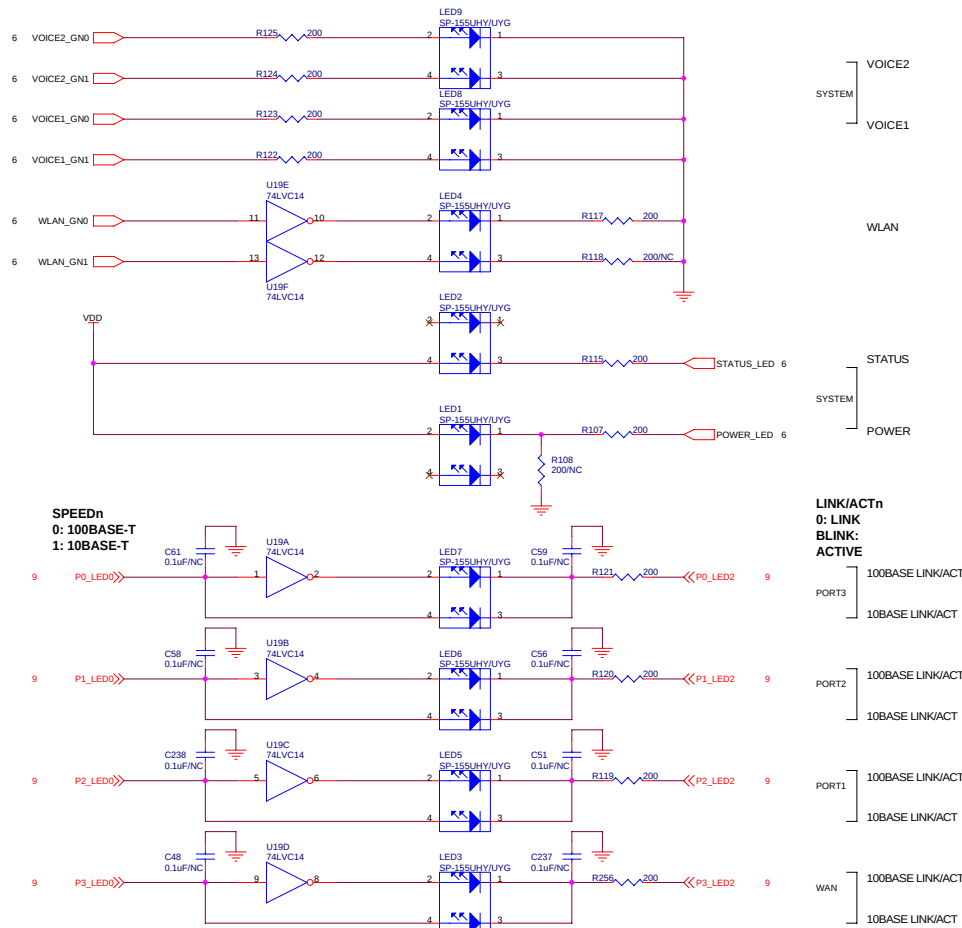
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VLYNQ CONNECTOR



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