

The block diagram illustrates the architecture of the AT91M55800A SoC. It features a central ARM7 processor core connected to various peripheral blocks. Power management is handled by a MAX6700 reset generator and a real-time clock. Data and control signals are managed through multiple DACs and ADCs, including a TI DAC2932 auxiliary DAC and a Tx DAC. The DSP (TI TMS320VC5416-160) is connected to the core via SPI, HPI, and I2C interfaces. Memory components include 8MByte FLASH, 1MByte SRAM, and an S71PL064 module. The SoC also includes a USART 1, a parallel bus, and a debug UART. External interfaces for a radio system (LTC1403A receiver ADC, serial link, IF converter, timing control, synth and demod control) and a data/fax serial interface are shown. The diagram is labeled 'Radio System Interface' on the left and 'Data / Fax Serial Interface' on the right.

The call processor (CP), an Atmel AT91M55800A, is the master system processor. It has control of the frame timing: the DSP and all other devices operate as slaves to the CP. The CP device includes not only the processor core, but also the following components in the same part:

- C7321-S-002 v1.6
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