

The block diagram illustrates the internal architecture of the VCO/PLL and Baseband IC, organized into several functional blocks:

- Power Amplifier:** Includes a TX pin, PWRCTR, PA_RAMP, and a 2.4GHz output stage.
- Receive LNA & IR Mixer:** Features RX, RXGAIN, and 90° phase shifters.
- VCO / PLL:** Contains a ϕ -DetL C.P., $\Delta\Sigma$ Frac-N PLL, and a 2.398-2.483 GHz output.
- Control Logic:** Manages RXEN, TXEN, PA_RAMP, and RXGAIN.
- BPF \ Limiter Discriminator \ Slicer:** Processes the RF signal through a BPF, limiter, discriminator, and slicer.
- 13.824MHz Xtal Oscillator:** Provides a stable reference frequency.
- Bias:** Manages VCC_BIAS and REXT.

External pins are numbered 1 through 32, with specific functions assigned to each, such as VCC_PA, TX, RX, RXGAIN, and RX_DATA.

[illegible]