

MP86 Circuit description

According to the circuit, the main core of MP86 is IC S5L840. It handles the MP3 decoding and control the accessory facilities, such as LCD. NAND flash K9F1G08U0M is used to store data. CODEC TLV320AIC23PW is used to decode digital signal to analog signal and transmit to speaker. On the other hand, analog signal from microphone is encoding to digital signal and enter IC S5L840 for further encoding. EL block of circuit diagram provides a high voltage source to drive the backlight. Power of circuit diagram is provide 2.8V voltage source to drive all IC.

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S5L840F

General Description

Features

Ordering Information

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Material Data Declaration Sheet

General Description

S5L840F is a single chip digital audio player IC supporting various compressed audio format on Flash Memory Media. S5L840F provides 2Mbits of embedded NOR flash memory and 76Kbytes of SRAM requiring no external

Features

- Supply Voltage Range
 - Supply Voltage (Core) : 1.8V
 - Supply Voltage (IO) : 3.0V
- X-tal Oscillator: 32.768 kHz
- 16bit RISC(CalmRISC16) & 24bit MAC with 4KB of Instruction Cache
 - 6KB of X Cache
 - 6KB of Y Cache
- 2Mbit NOR Flash, 76KB SRAM & 4KB Mask ROM
- IO DMA
- Supports SMC/MMC/SD/Memory Stick
- LCD Interface
- 2 Channels of IIS
- IIC / SPDIF Output / UART / SPI
- USB1.1 Device
- 5 channel 10bit ADC
- Real Timer Clock (RTC)
- General-Purpose Input/Output (GPIO)

Ordering Information

Device	Package	Operating Temperature
S5L840F	128-TQFP-1414 160-FBGA-1212	- 40 °C - + 85°C

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USB DEVICE CONTROLLER

OVERVIEW

Universal Serial Bus (USB) device controller is designed to provide a high performance full speed function controller solution with DMA interface. USB device controller allows bulk transfer with DMA, interrupt transfer and control transfer

USB device controller support :

- Full speed USB device controller compatible with the USB specification version 1.1
- DMA interface for bulk transfer
- Four endpoint with FIFO
 - EP0 : 16 bytes (Register)
 - EP1 : 64 bytes IN/OUT FIFO
 - EP2 : 64 X 2 bytes IN/OUT FIFO
 - EP3 : 64 X 2 bytes IN/OUT FIFO
- Integrated USB Transceiver

FEATURE

- Fully compliant with USB Specification Version 1.1
- Full speed (12Mbps) device
- Integrated USB Transceiver
- Supports control, interrupt, Isochronous and bulk transfer
- Four endpoints with FIFO
- Supports DMA interface for receive and transmit bulk endpoint. (EP1, EP2 and EP3)
- Support suspend and remote wakeup function.

BLOCK DIAGRAM

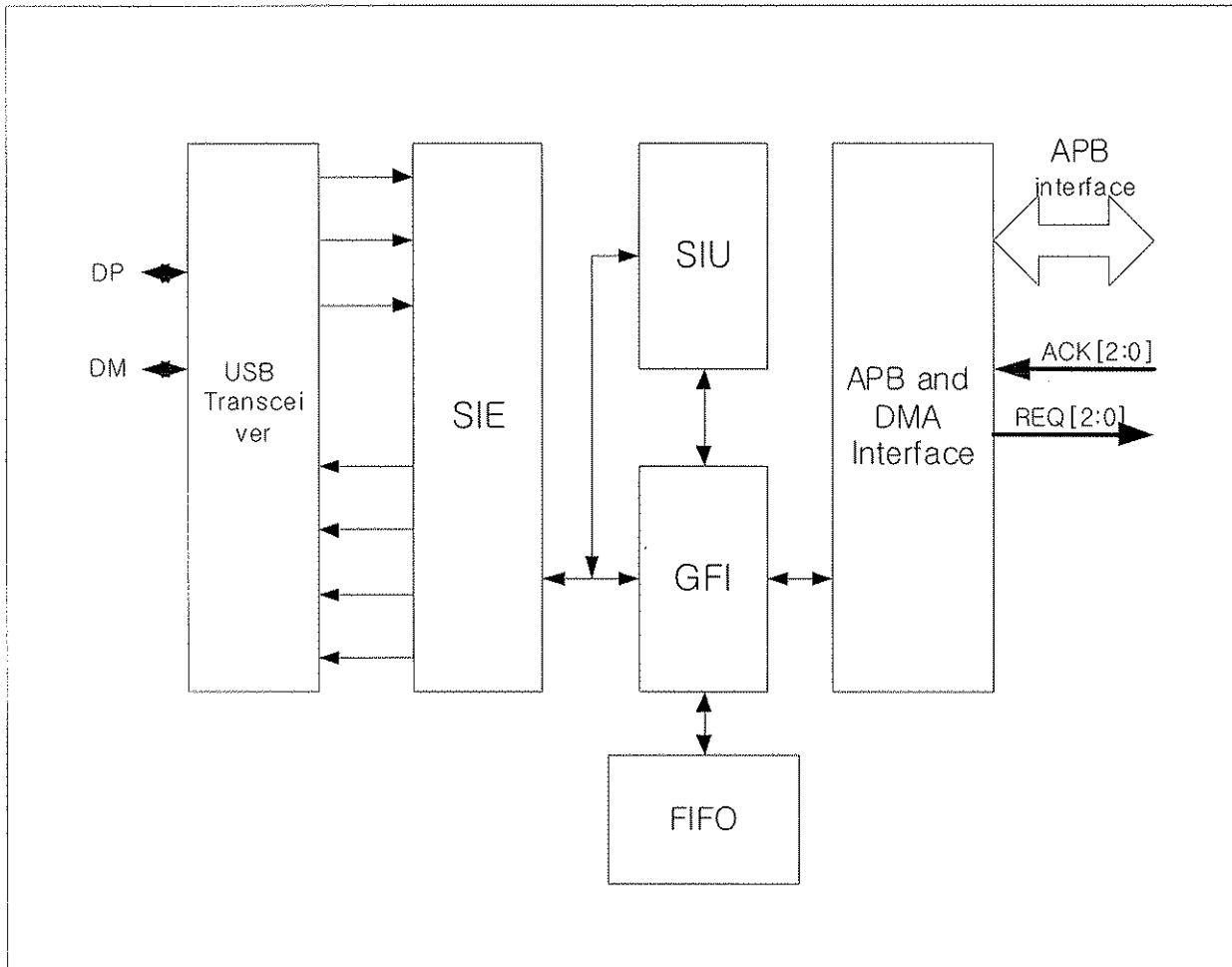


Figure -1. USB Device Controller Block Diagram

USB DEVICE CONTROLLER SPECIAL REGISTERS

This section describes detailed functionalities about register sets of USB device controller.

All special function register is byte-accessible.

Common indexed registers depend on INDEX register(INDEX_REG) value. For example if you want to write EP0 CSR register, you must write '0X00' on the INDEX_REG before writing IN_CSR1 register.