

MS-6526

Version 300

INTEL (R) Brookdale-G Chipset
Willamette/Northwood 478pin mPGA-B Processor Schematics

CPU:

Willamette/Northwood mPGA-478B Processor

System Brookdale-G Chipset:

**INTEL GMCH (North Bridge) +
INTEL ICH4 (South Bridge)**

On Board Chipset:

**BIOS -- FWH
AC'97 Codec -- ALC201A
LPC Super I/O -- W83627HF-AW
Clock Generation -- ICS950218AF
LAN -- Intel 562ET**

Expansion Slots:

PCI2.2 SLOT * 3

Title

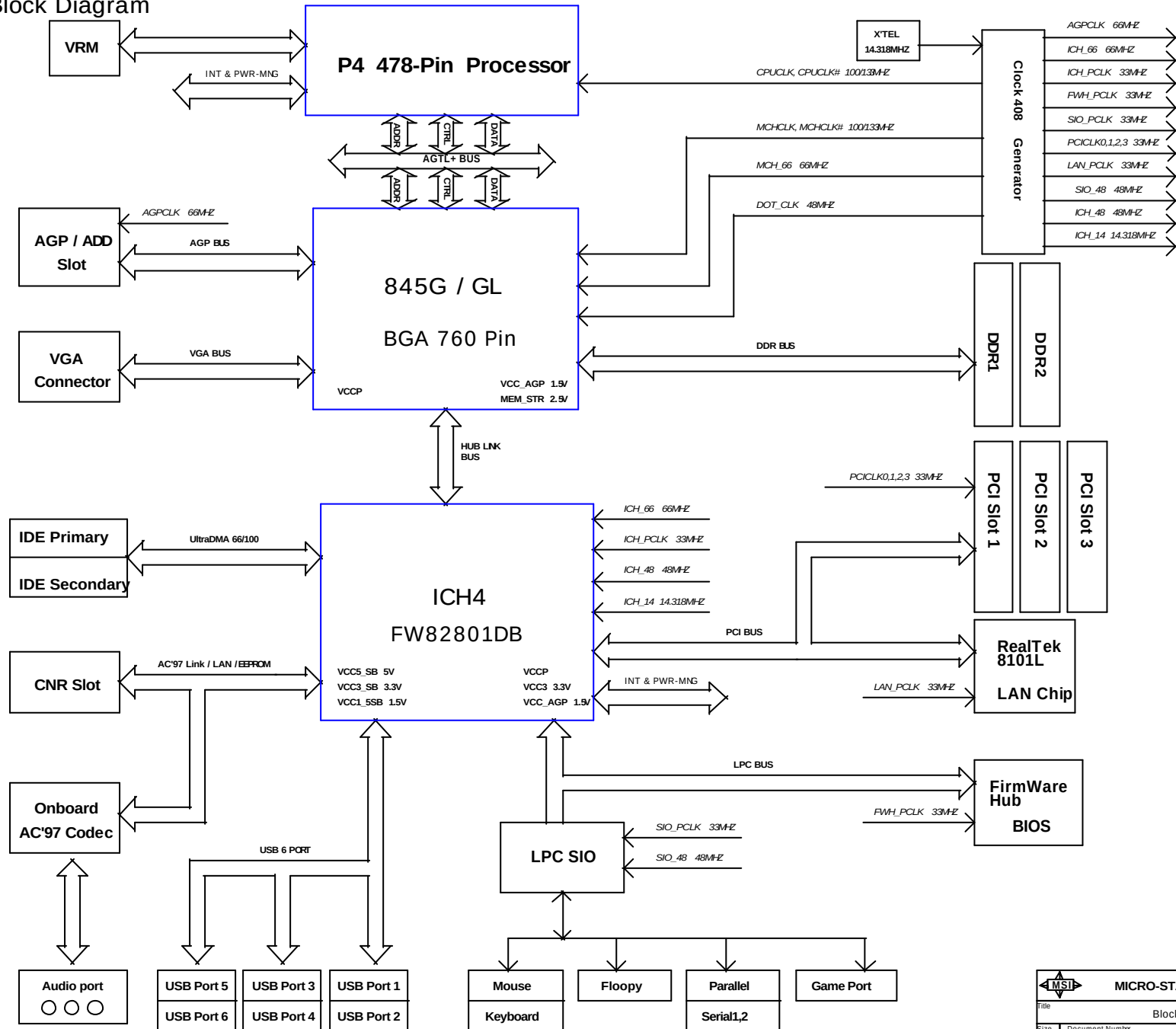
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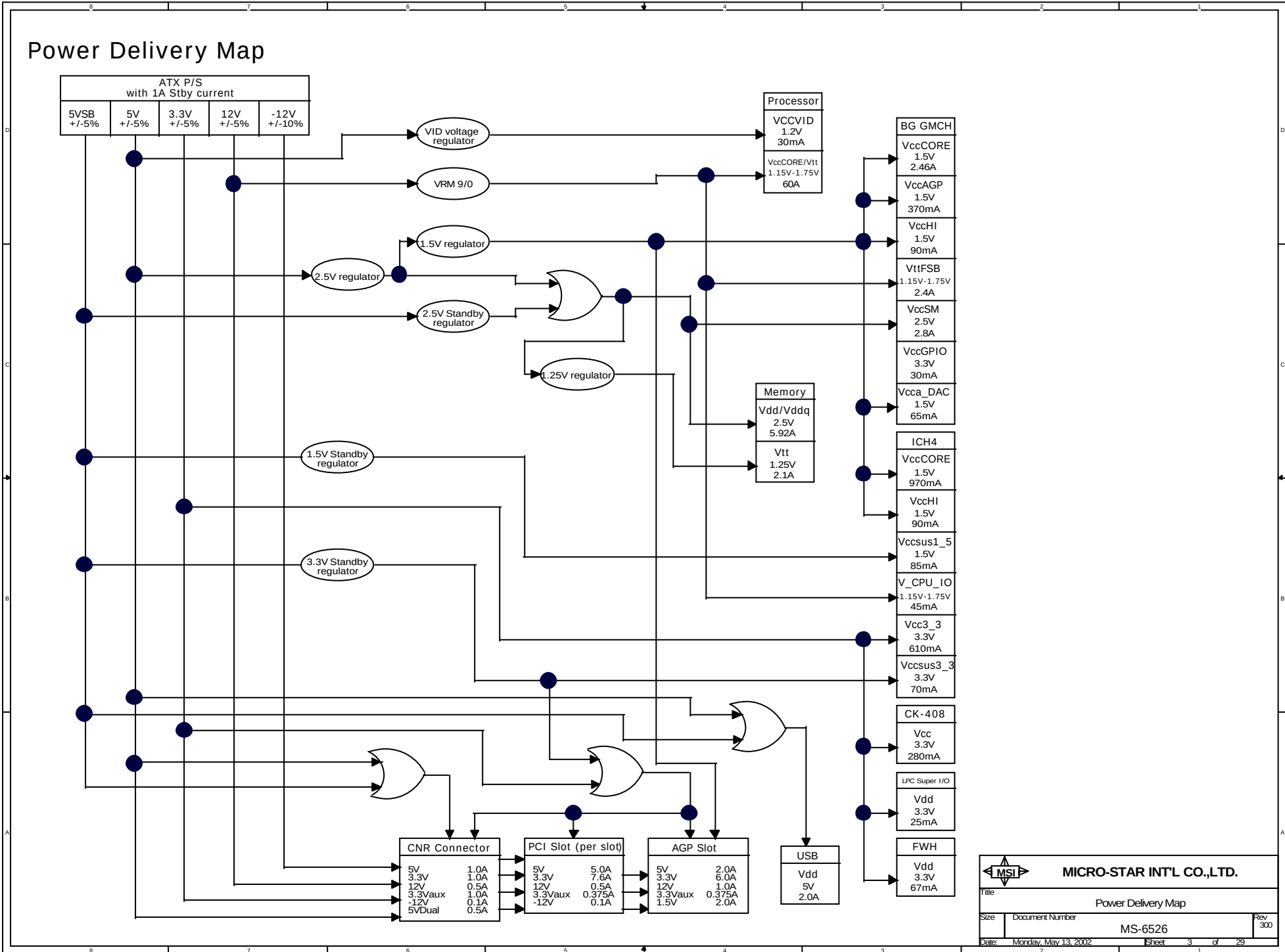
MODEL Config.	ORCAD Config.	Function	ERP Number
MS6526 STD	cfg6526-STD	STD	601-6526-08S
MS6526 Option:L	cfg6526-LAN	STD+Intel LAN	601-6526-09S
MS6526M1 STD	cfg6526M1-STD	STD+M1	
MS6526M1 Option:L	cfg6526M1-LAN	STD+M1+Intel LAN	

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Title Cover Sheet	
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Block Diagram



Power Delivery Map



General SPEC

ICH4

GPIO Pin	Type	Function
GPIO 0	I	REQ#A (multifunction pin)
GPIO 1	I	REQ#B (multifunction pin)
GPIO 2	I	Pull up through 8.2K ohms (PIRQE#)
GPIO 3	I	Pull up through 8.2K ohms (PIRQF#)
GPIO 4	I	Pull up through 8.2K ohms (PIRQG#)
GPIO 5	I	Pull up through 8.2K ohms (PIRQH#)
GPIO 6	I	Pull down through 10K ohms (unused)
GPIO 7	I	Pull down through 10K ohms (unused)
GPIO 8	I	Pull Up to 3.3VSBY through 4.7K ohms (SIO_PME)
GPIO 9	I	Not Implemented
GPIO 10	I	Not Implemented
GPIO 11	I	SMB_ALERT (multifuntn pin)
GPIO 12	I	EXTSMI# with Pull up 10K ohms to VCC3_SB
GPIO 13	I	Pull down through 10K ohms (unused)
GPIO 14~15	I	Not Implemented
GPIO 16	O	GNT#A (multifunction pin)
GPIO 17	O	GNT#B (multifunction pin)
GPIO 18*	O	No Connected
GPIO 19	O	No Connected
GPIO 20	O	No Connected
GPIO 21	O	No Connected
GPIO 22	OD	No Connected
GPIO 23	O	Pull Up to 3.3V through 8.2K ohms (BIOS protect)
GPIO 24	I/O	No Connected
GPIO 25	I/O	No Connected
GPIO 26	I/O	Not Implemented
GPIO 27	I/O	No Connected
GPIO 28	I/O	No Connected
GPIO 29~31	O	Not Implemented
GPIO 32	I/O	No Connected
GPIO 33	I/O	No Connected
GPIO 34	I/O	Primary IDE ATA66/100 detection (PD_DET)
GPIO 35	I/O	Secondary IDE ATA66/100 detection (SD_DET)
GPIO 36	I/O	No Connected
GPIO 37	I/O	No Connected
GPIO 38	I/O	No Connected
GPIO 39	I/O	No Connected
GPIO 40	I/O	No Connected
GPIO 41	I/O	No Connected
GPIO 42	I/O	No Connected
GPIO 43	I/O	No Connected
GPIO 44~47	I/O	Not Implemented

* GPIO18 will toggle at 1Hz frequency.

FWH

GPIO Pin	Type	Function
GPI 0	I	Pull down through 8.2K ohms (unused)
GPI 1	I	Pull down through 8.2K ohms (unused)
GPI 2	I	P1 customer defined
GPI 3	I	P1 customer defined
GPI 4	I	Pull down through 8.2K ohms (unused)

PCI Config.

DEVICE	ICH INT Pin	IDSEL	CLOCK	CLK GEN PIN OUT
PCI Slot 1	INTA# INTB# INTC# INTD#	AD16	PCICLK0	10 (PCI3/FS4)
PCI Slot 2	INTB# INTC# INTD# INTA#	AD17	PCICLK1	11 (PCI4)
PCI Slot 3	INTC# INTD# INTA# INTB#	AD18	PCICLK2	12 (PCI5)
PCI LAN	INTG# INTF#	AD29	LAN_PCLK	17 (PCI9)

*ICH4 reserved PCI address line AD22 for the PCI-to-ISA Bridge's IDSEL input.

DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	1010000B	DCLK0/DCLK 0# DCLK1/DCLK 1# DCLK2/DCLK 2#
DIMM 2	1010001B	DCLK3/DCLK 3# DCLK4/DCLK 4# DCLK5/DCLK 5#

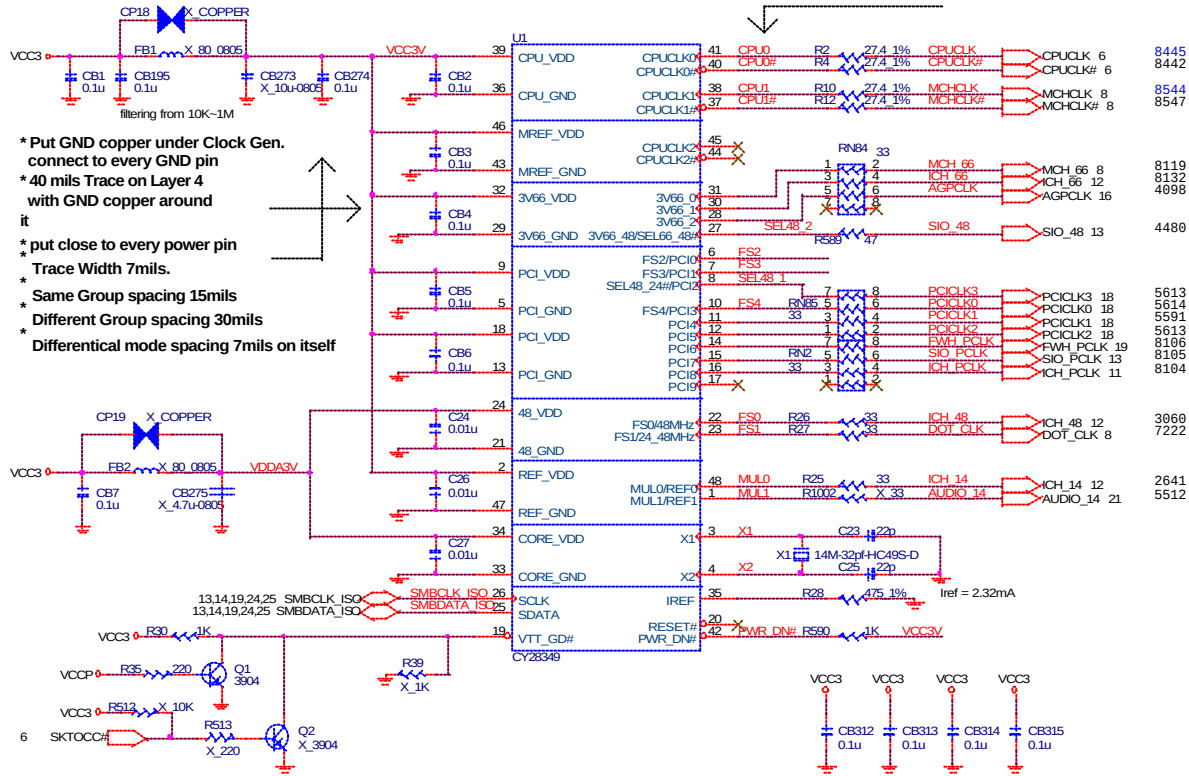


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Title			General SPEC
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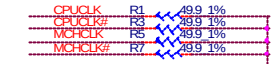
CLOCK GENERATOR BLOCK

*Trace < 0.5"



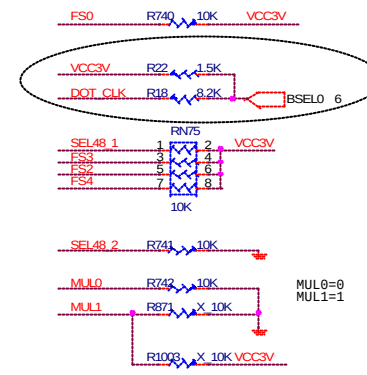
- * Put GND copper under Clock Gen. connect to every GND pin
- * 40 mils Trace on Layer 4 with GND copper around it
- * put close to every power pin
- * Trace Width 7mils.
- * Same Group spacing 15mils
- * Different Group spacing 30mils
- * Differential mode spacing 7mils on itself

Shut Source Termination Resistors



Trace less 0.2"
49.9ohm for 50ohm M/B impedance

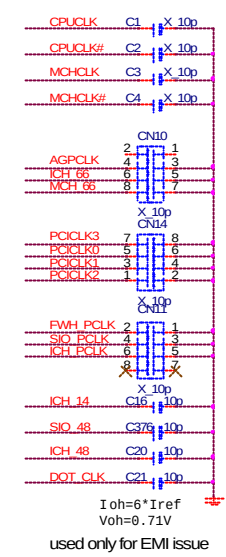
CLOCK STRAPPING RESISTORS



FS4	FS3	FS2	FS1	FS0	FSB (MHz)
1	1	1	0	1	100 MHz
1	1	1	1	1	133 MHz



Pull-Down Capacitors



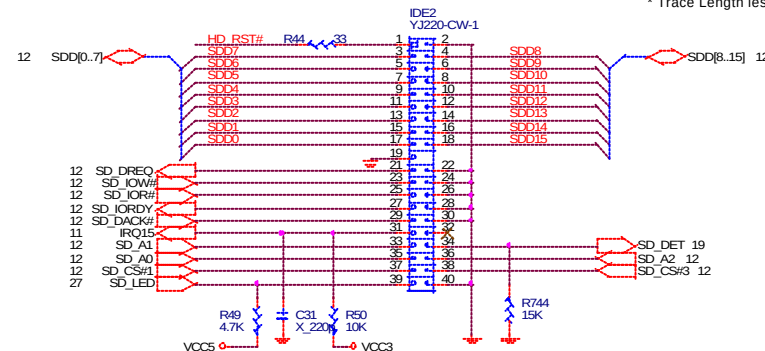
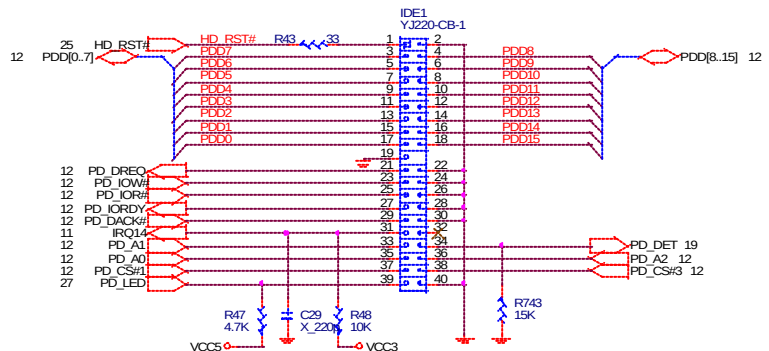
I_{oh}=6*I_{ref}
V_{oh}=0.71V
used only for EMI issue
Trace less 0.2"

PRIMARY IDE BLOCK

ATA100 IDE CONNECTORS

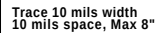
SECONDARY IDE BLOCK

- * Trace Width : 5mils
- * Trace Spacing : 7mils
- * Length(longest)-Length(shortest)<0.5"
- * Trace Length less than 5"



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Title Clock Gen & ATA100 IDE Connectors			
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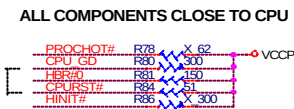
CPU SIGNAL BLOCK



CPU GTL REFERENCE VOLTAGE BLOCK



CPU STRAPPING RESISTORS



ALL COMPONENTS CLOSE TO CPU

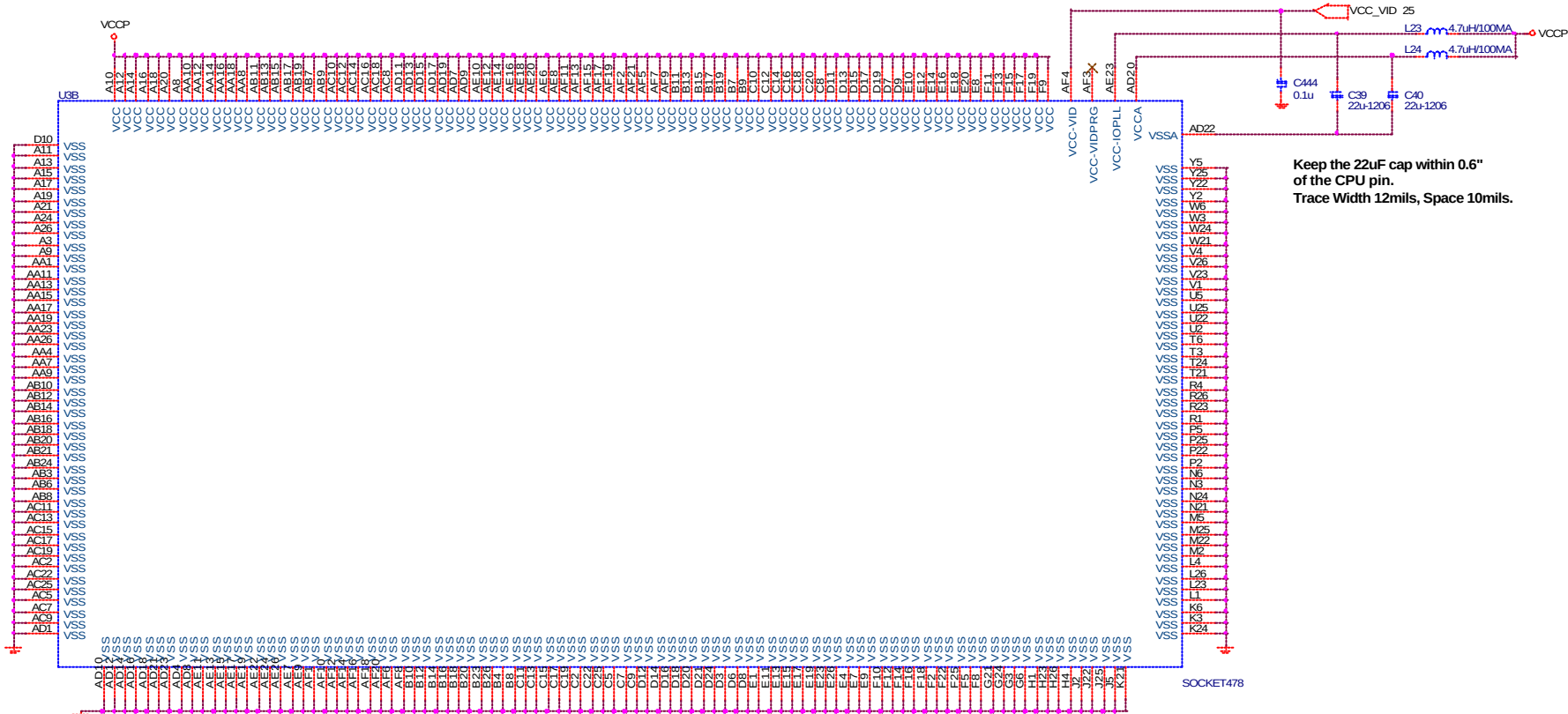


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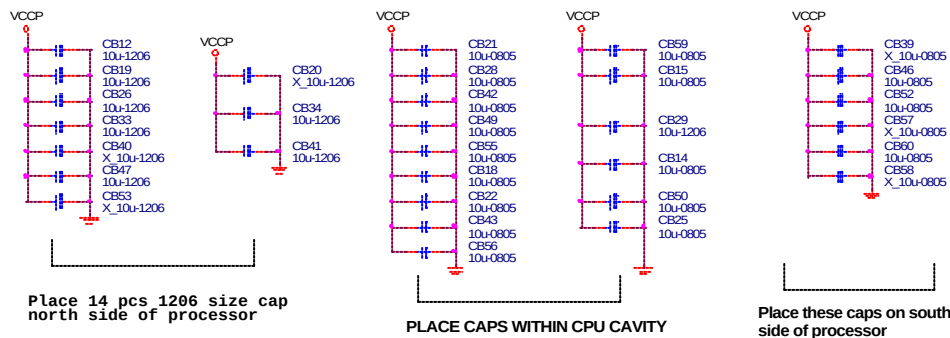
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CPU VOLTAGE BLOCK

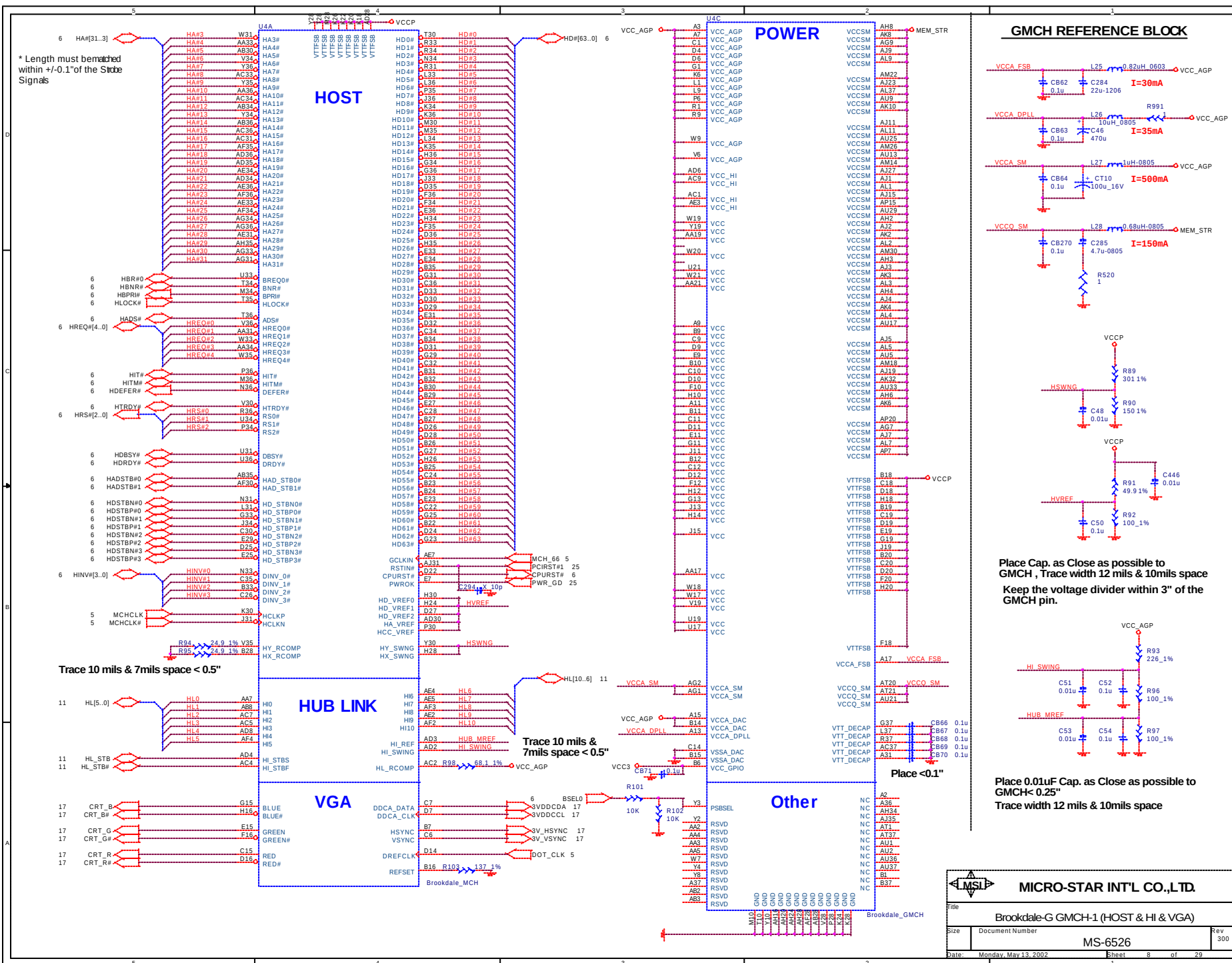


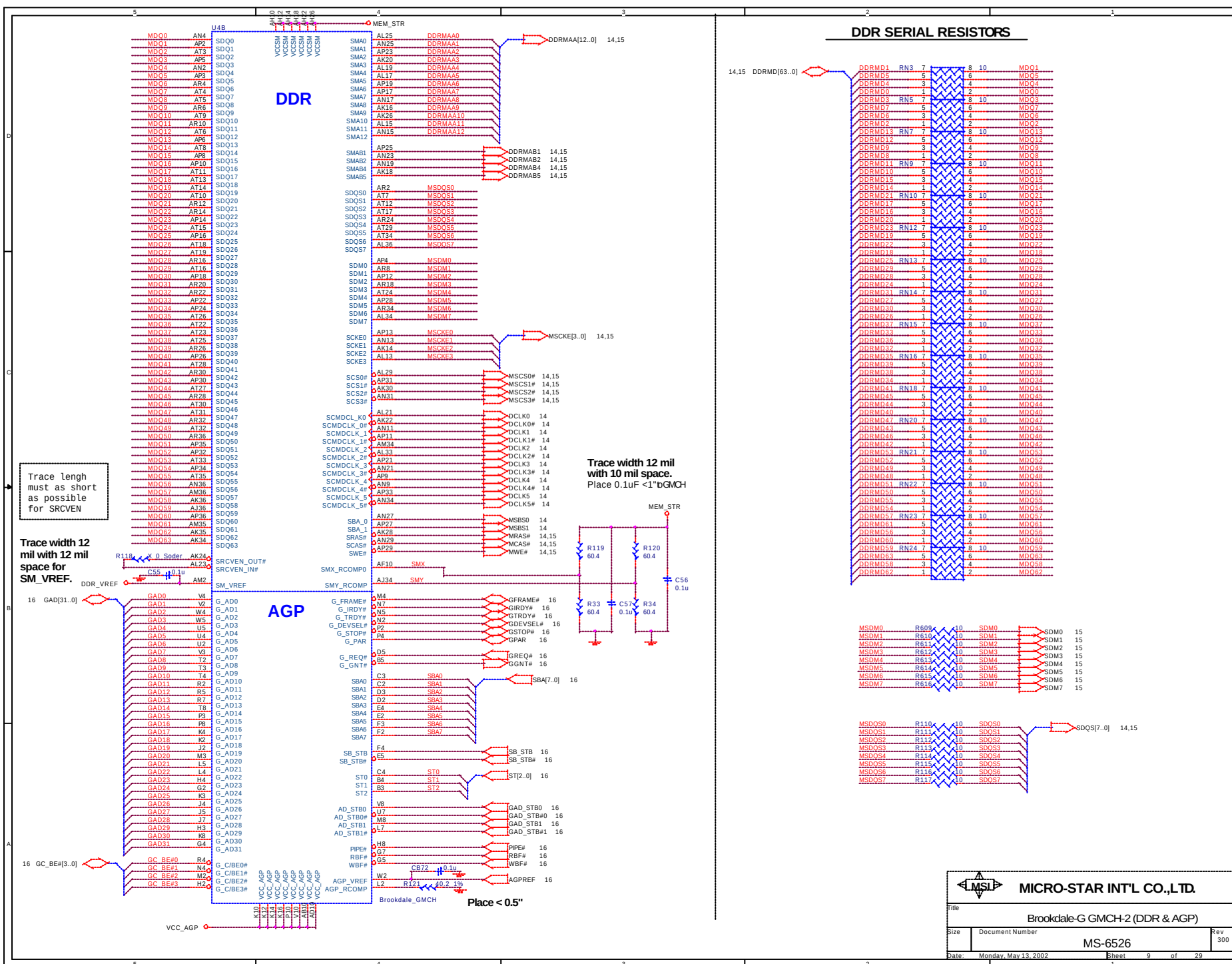
CPU DECOUPLING CAPACITORS

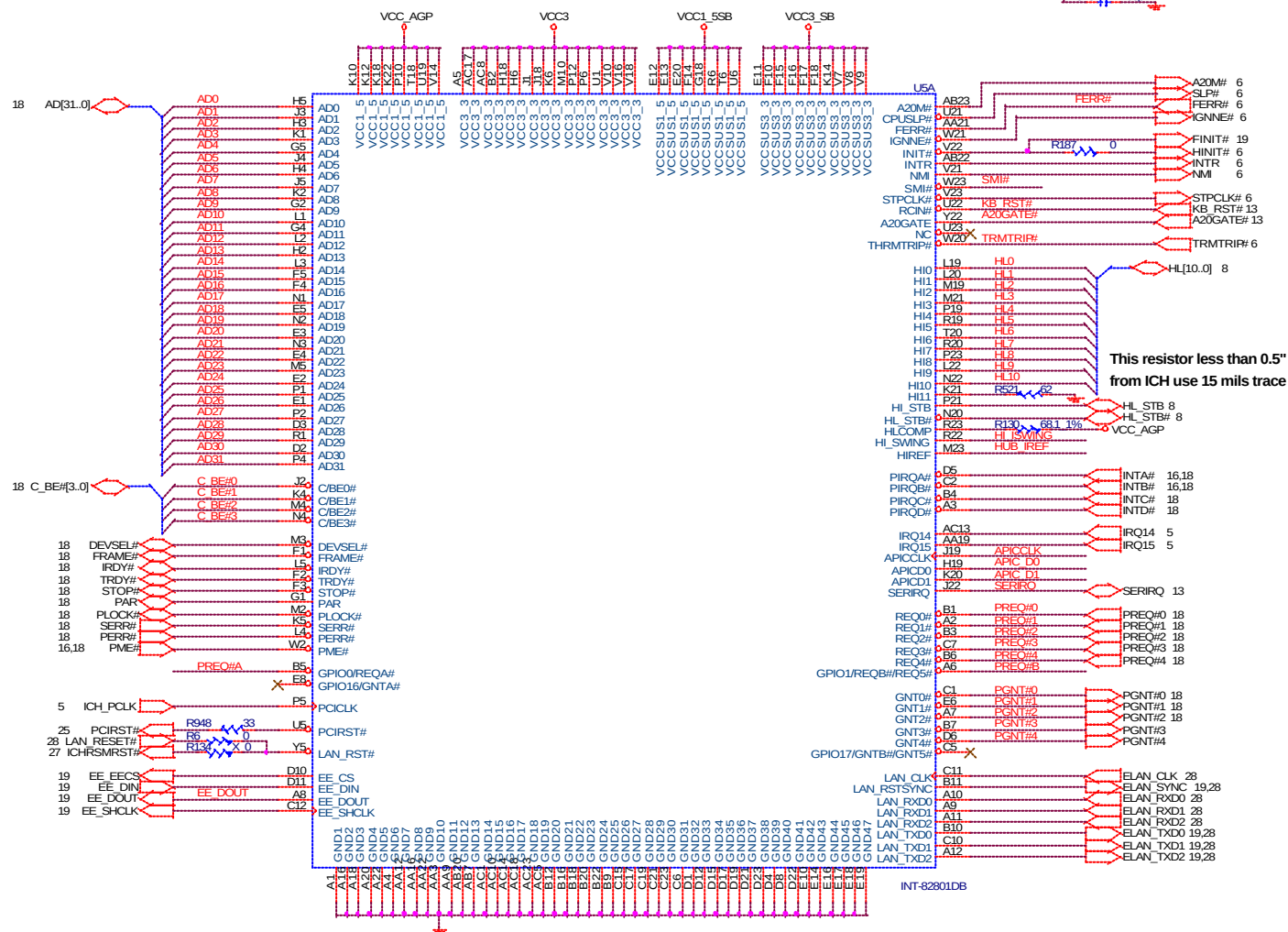


Within CPU Cavity Solder Side

MICRO-STAR INT'L CO.,LTD.			
Title mPGA478-B INTEL CPU Part2			
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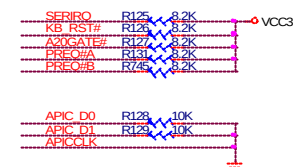




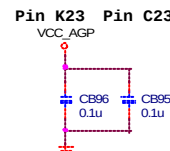
EE_DOUT R133 X_10K

Reserved pull-down resistor for ICH4 reserved function straps.

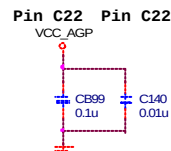
FERR# R123 62
TRMTRIP# R124 62
VCCP



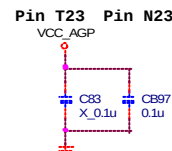
Place Cap. as Close as possible to ICH4 < 0.25"
Trace width use 12 mils and 10mils space



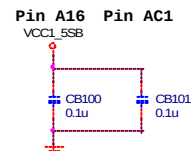
FOR Core Logic



FOR PLL



FOR Hub Interface

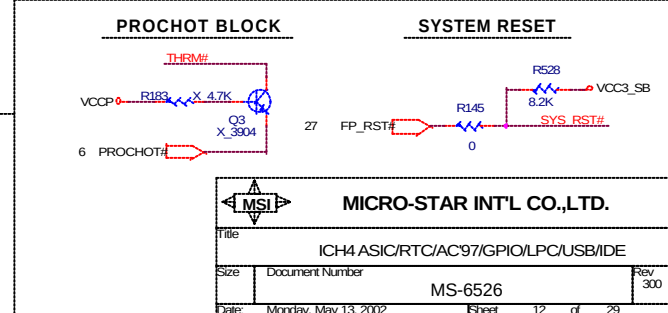
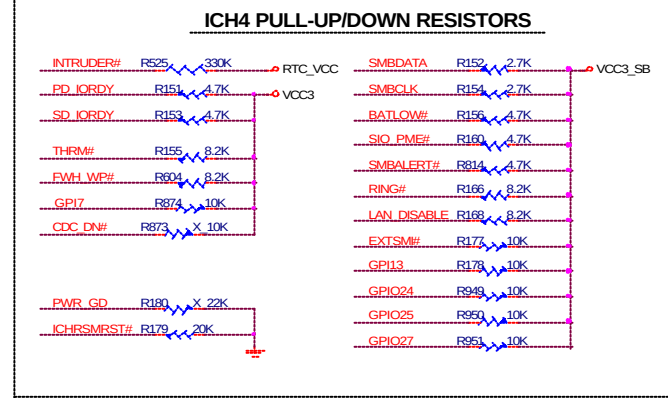
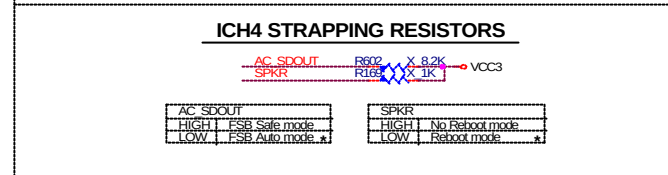
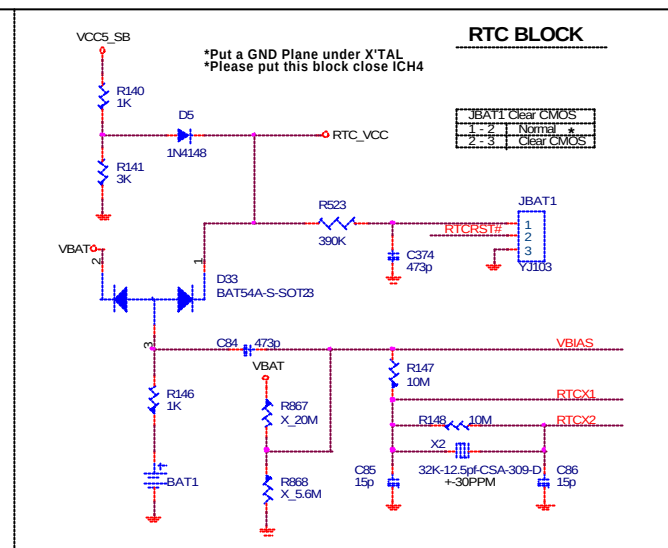
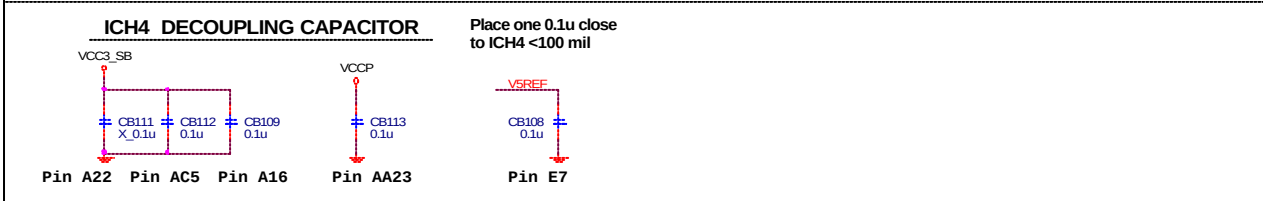
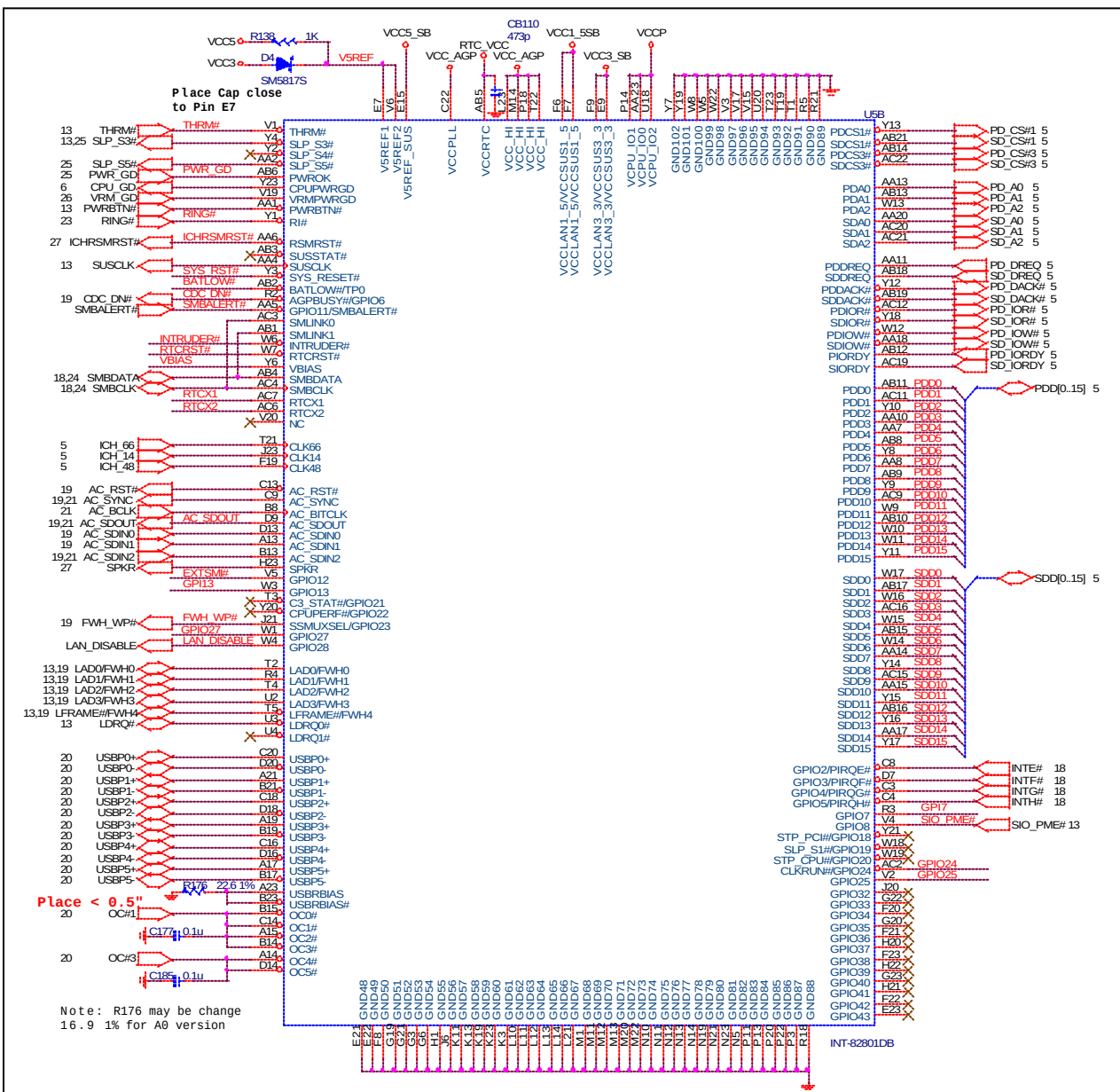


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ICH4 PCI & HI & LAN

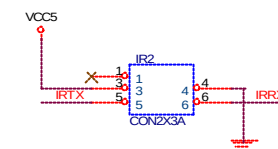
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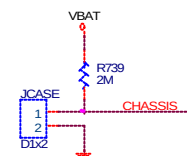
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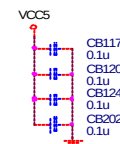
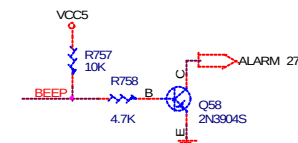
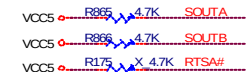


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[illegible]

SOUTA	L: Disable KBC	H: Enable KBC
SOUTB	L: 24MHz	H: 48MHz
RTSA#	L: CFAD=2E	H: CFAD=4E
DTRA#	L: PNP Default	H: PNP no Default

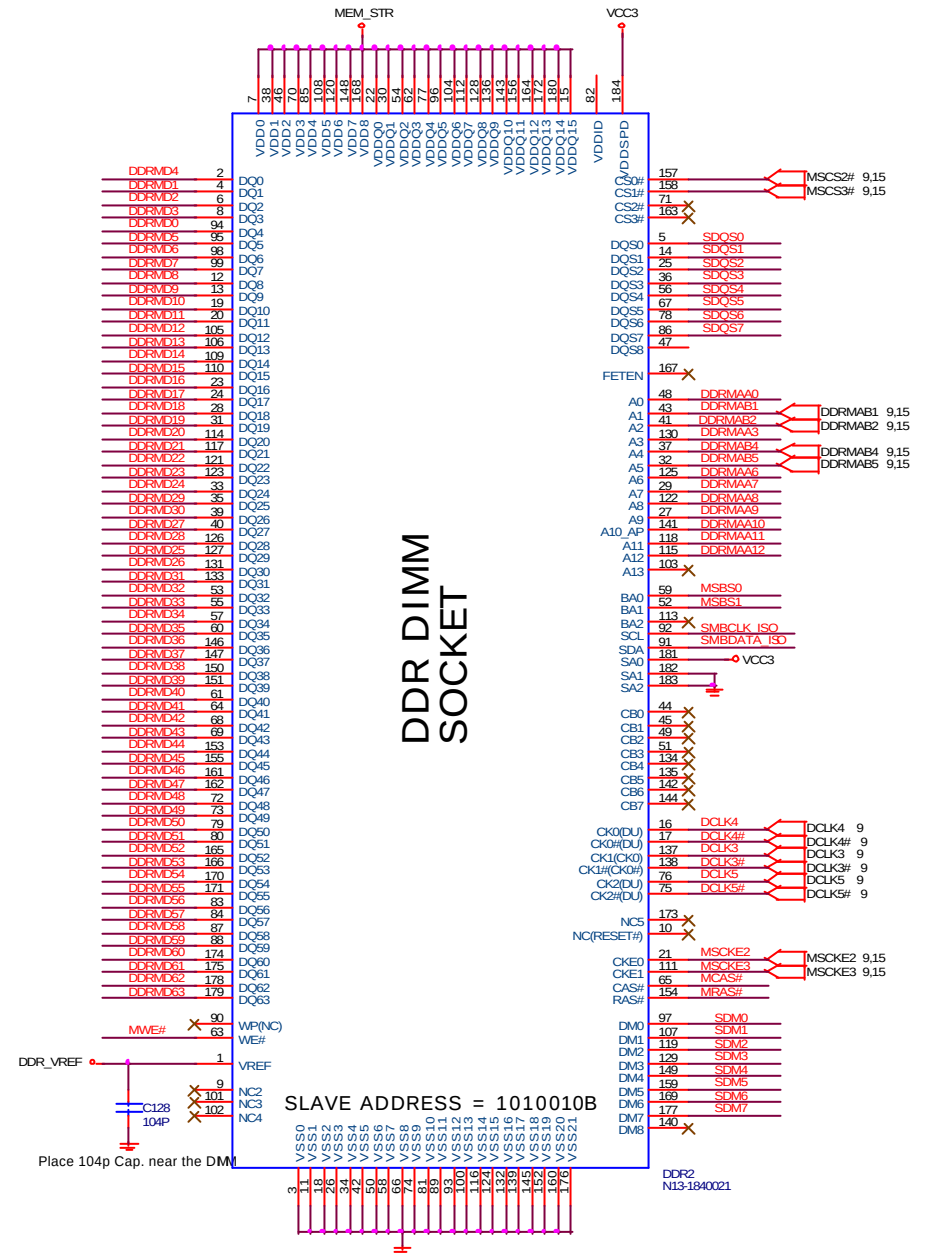
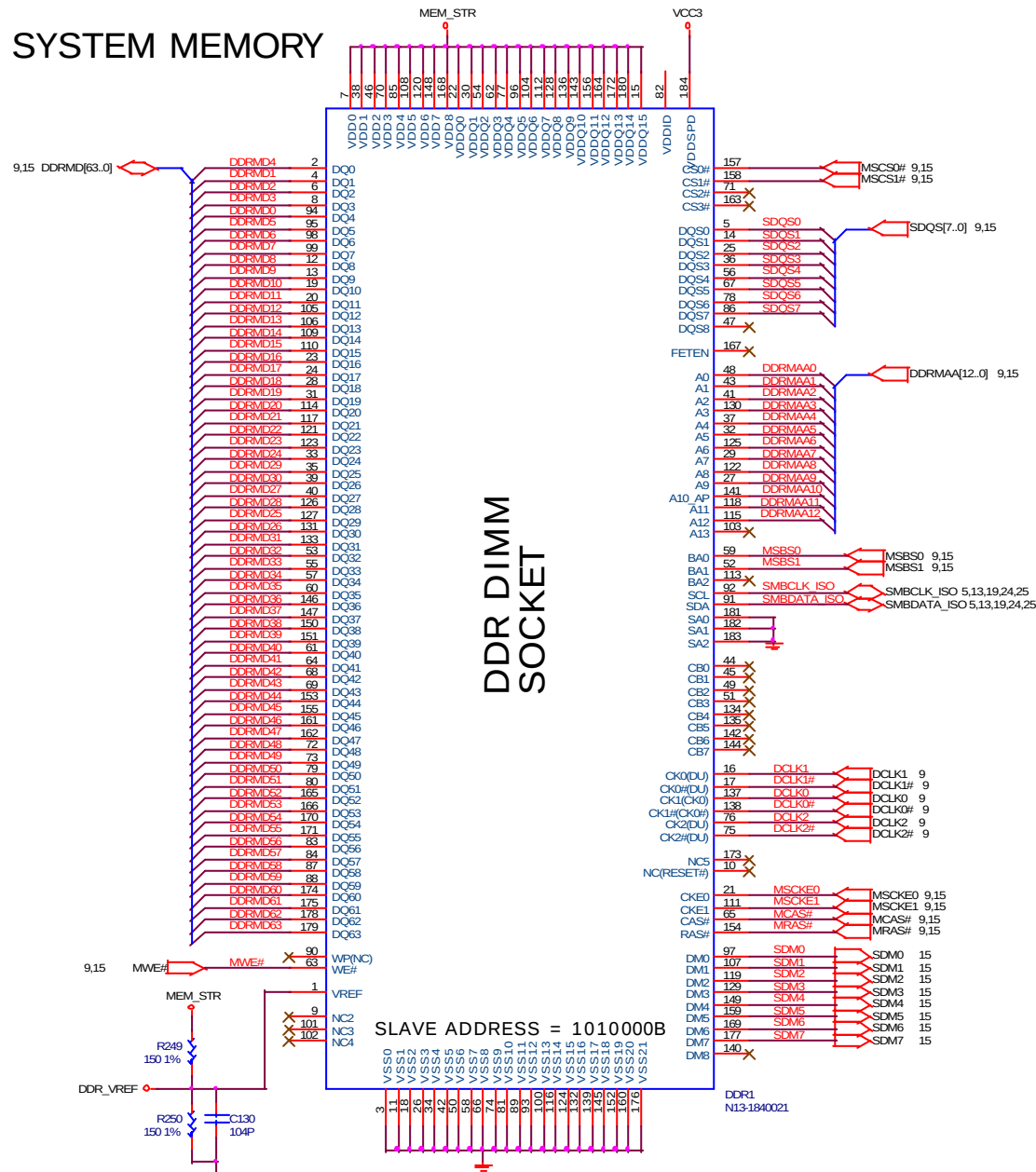


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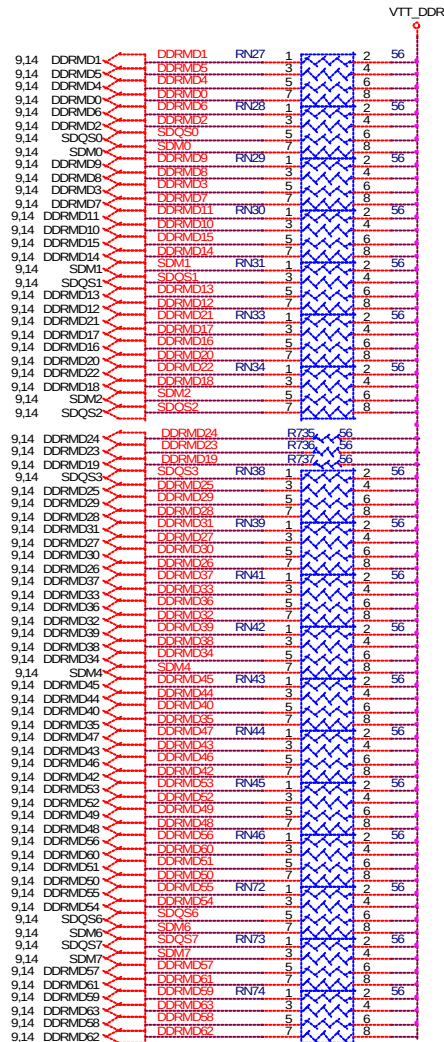
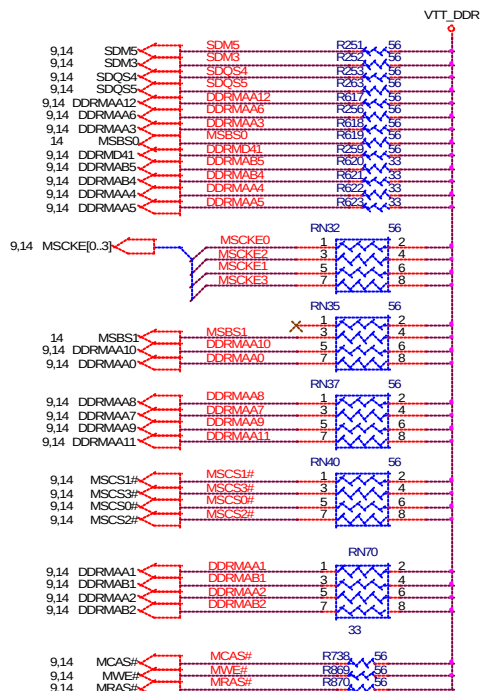
LPC IO & GAME PORT

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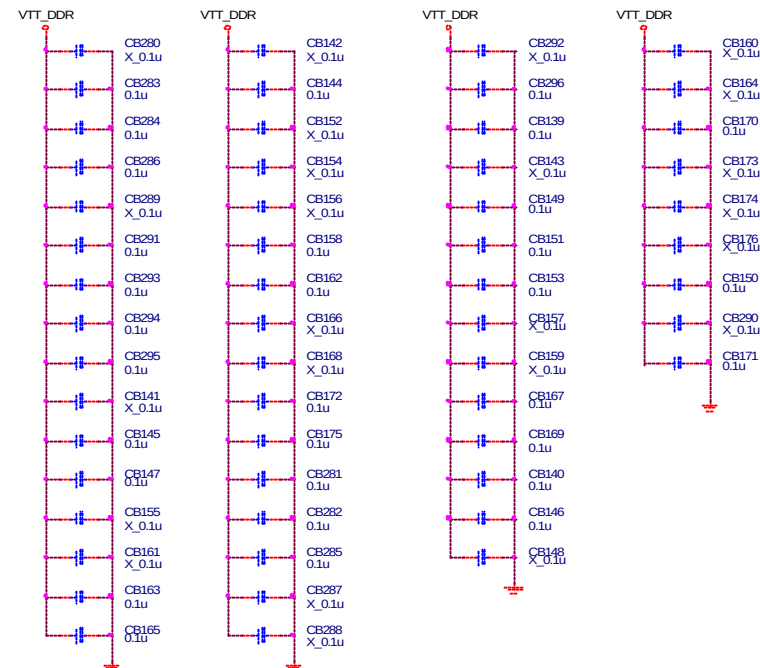
SYSTEM MEMORY



DDR TERMINATORS

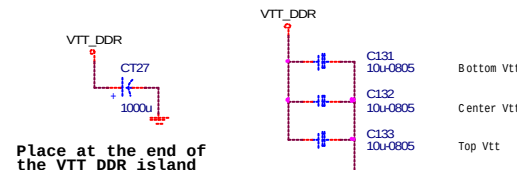


DDR Decoupling Caps



Total 110 signal, need 55 pcs decoupling.

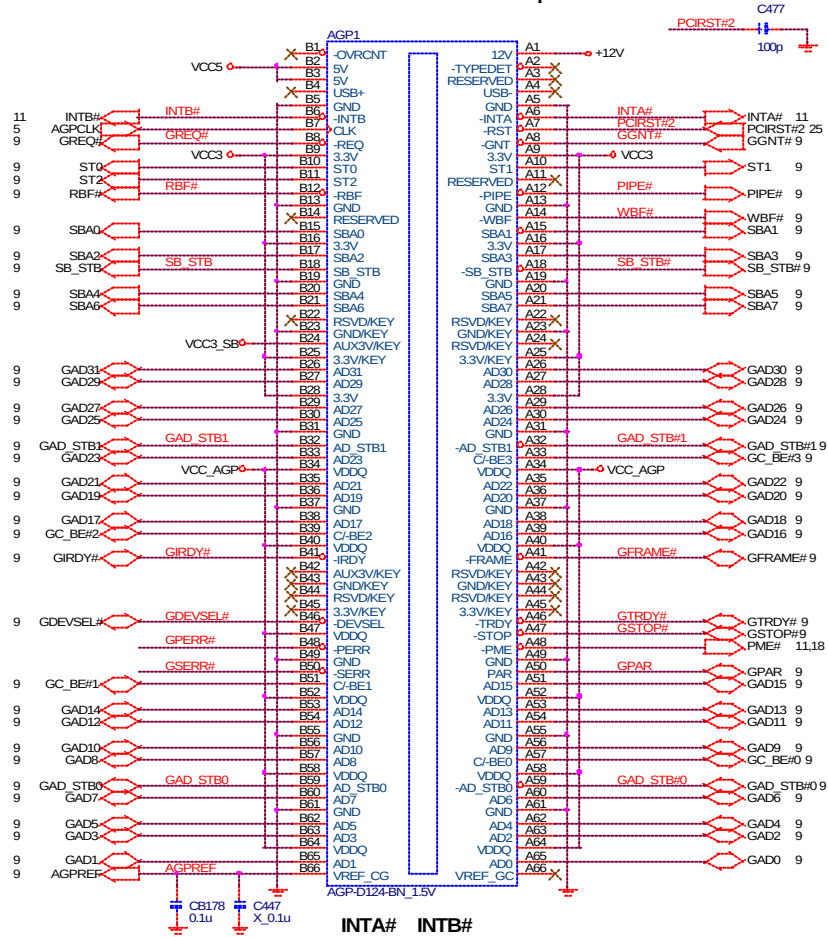
Place for VTT_DDR island



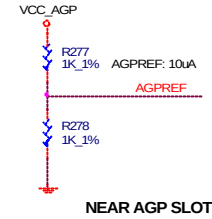
		MICRO-STAR INT'L CO.,LTD.	
Title			
DDR Terminator Resistor			
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AGP 1.5V 2X/4X SLOT(AGP VER:2.0 COMPLY)

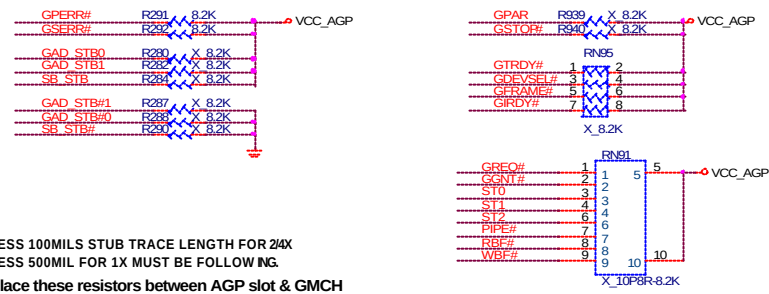
VCC5 = 60mils trace / 15 mils space



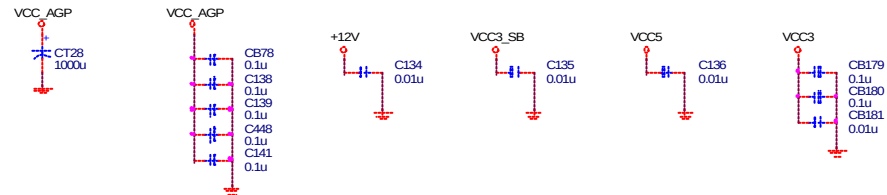
AGP SIGNAL REFERENCE CIRCUIT



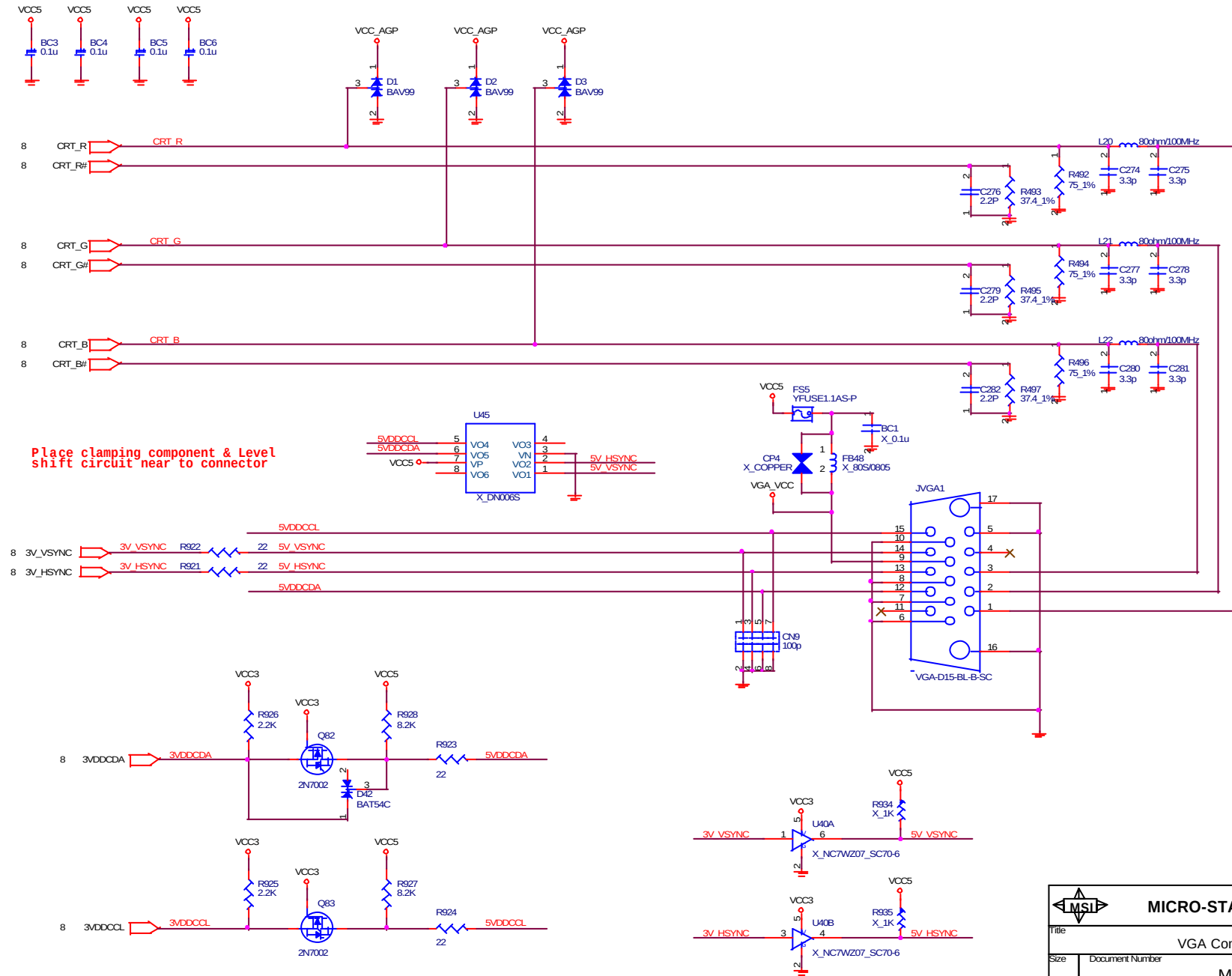
AGP TERMINATION RESISTORS



AGP SLOT DECOUPLING CAPACITORS

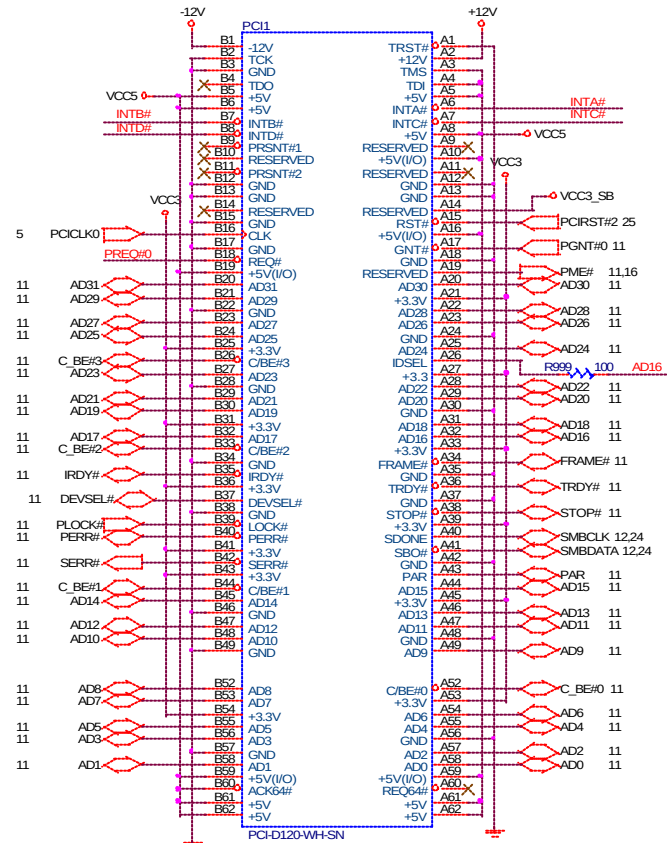


Video Connector

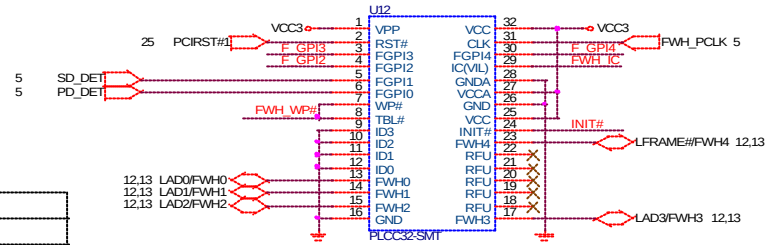


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Title		
VGA Connector		
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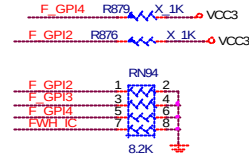
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



Firmware Hub (FWH)



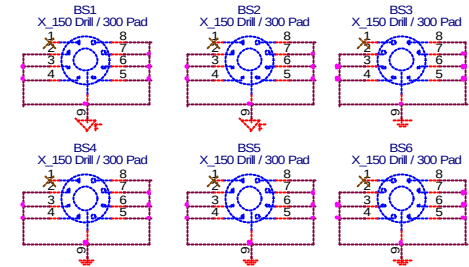
FWH RESISTORS



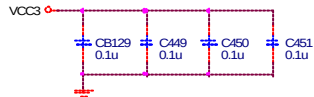
J6 Config.		
1 - 2	Normal	*
2 - 3	Configuration Mode	
OPEN	Recovery	

* Default

PCB Mounting Holes

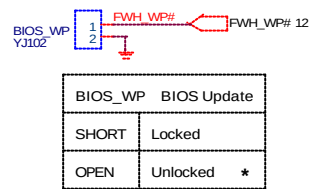


FWH DECOUPLING CAPACITORS



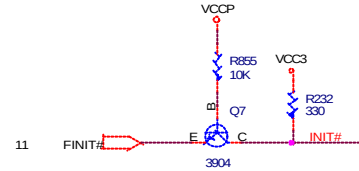
Place Cap. as Close to FWH< 350 mil

FWH write protect

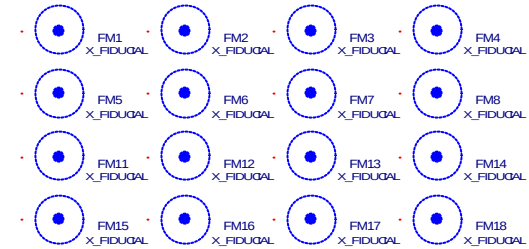


BIOS_WP	BIOS Update
SHORT	Locked
OPEN	Unlocked *

FWH INIT Signal Voltage Translation Block



PCB Fiducials



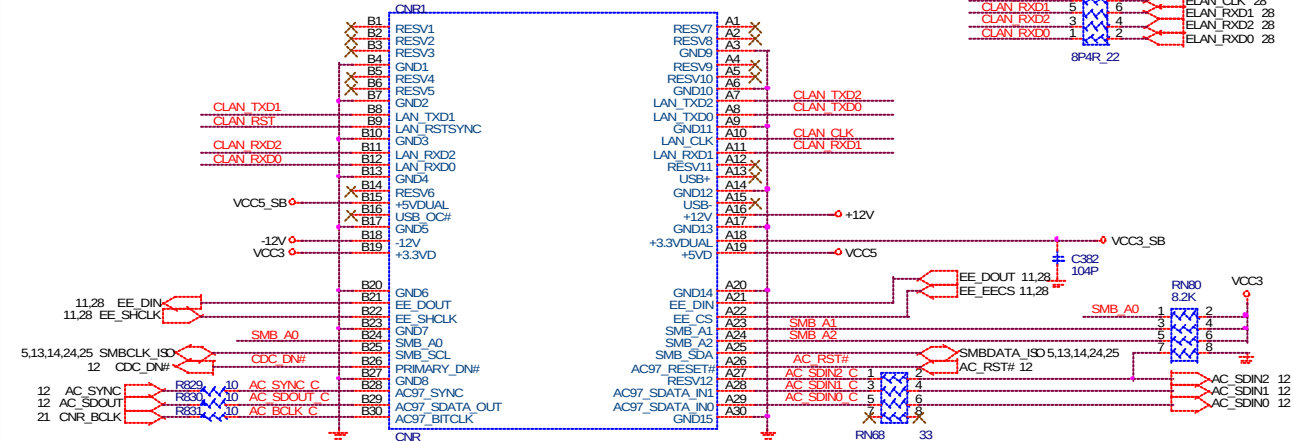
CNR RISER

* LAN Trace width : 5 mils

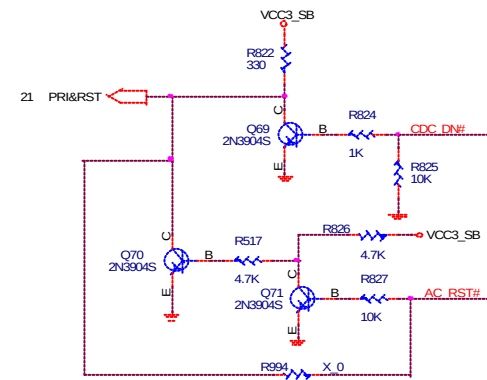
* AC'97 Trace Spacing : 10 mils

* Maxium trace length < 9.5"

* Equal to or up to 500 mils shorter than the ELAN_CLK trace



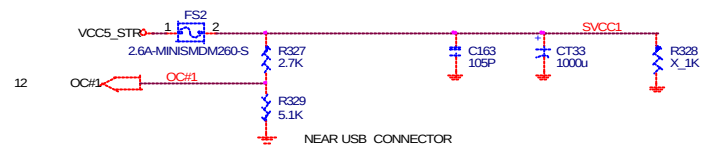
SIMULATION TRACE



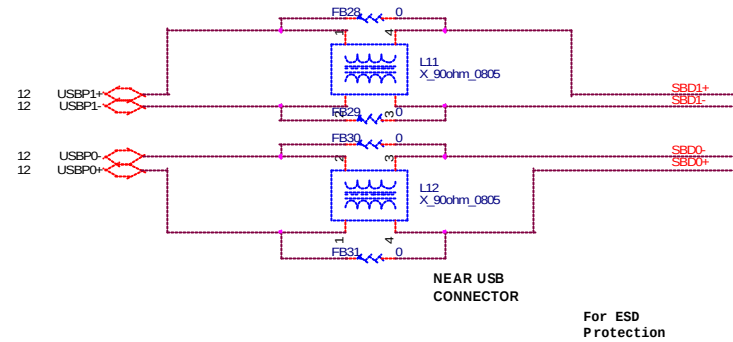
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FWH & CNR		
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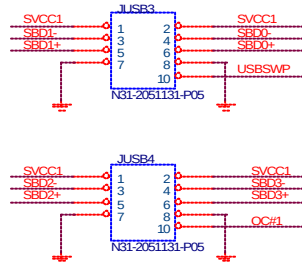
POWER CIRCUIT FOR USB PORT 0,1,2,3



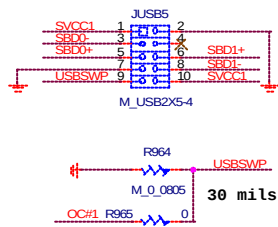
FRONT PANEL USB CONNECTOR FOR USB PORT 0,1



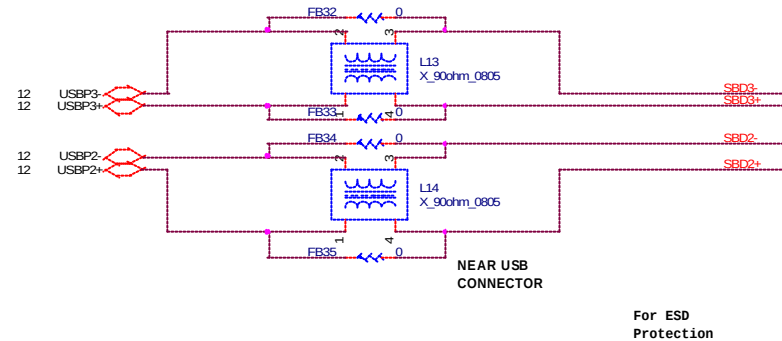
Intel Front USB Header



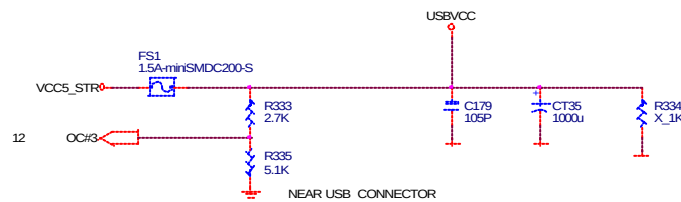
MSI Front USB Header



FRONT PANEL USB CONNECTOR FOR USB PORT 2,3

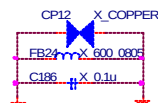
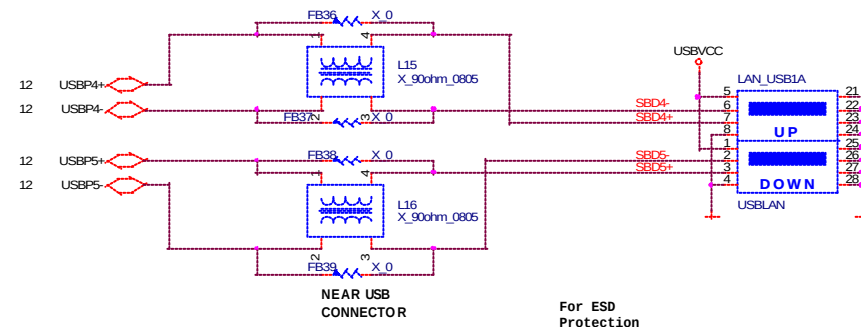


POWER CIRCUIT FOR USB PORT 4,5



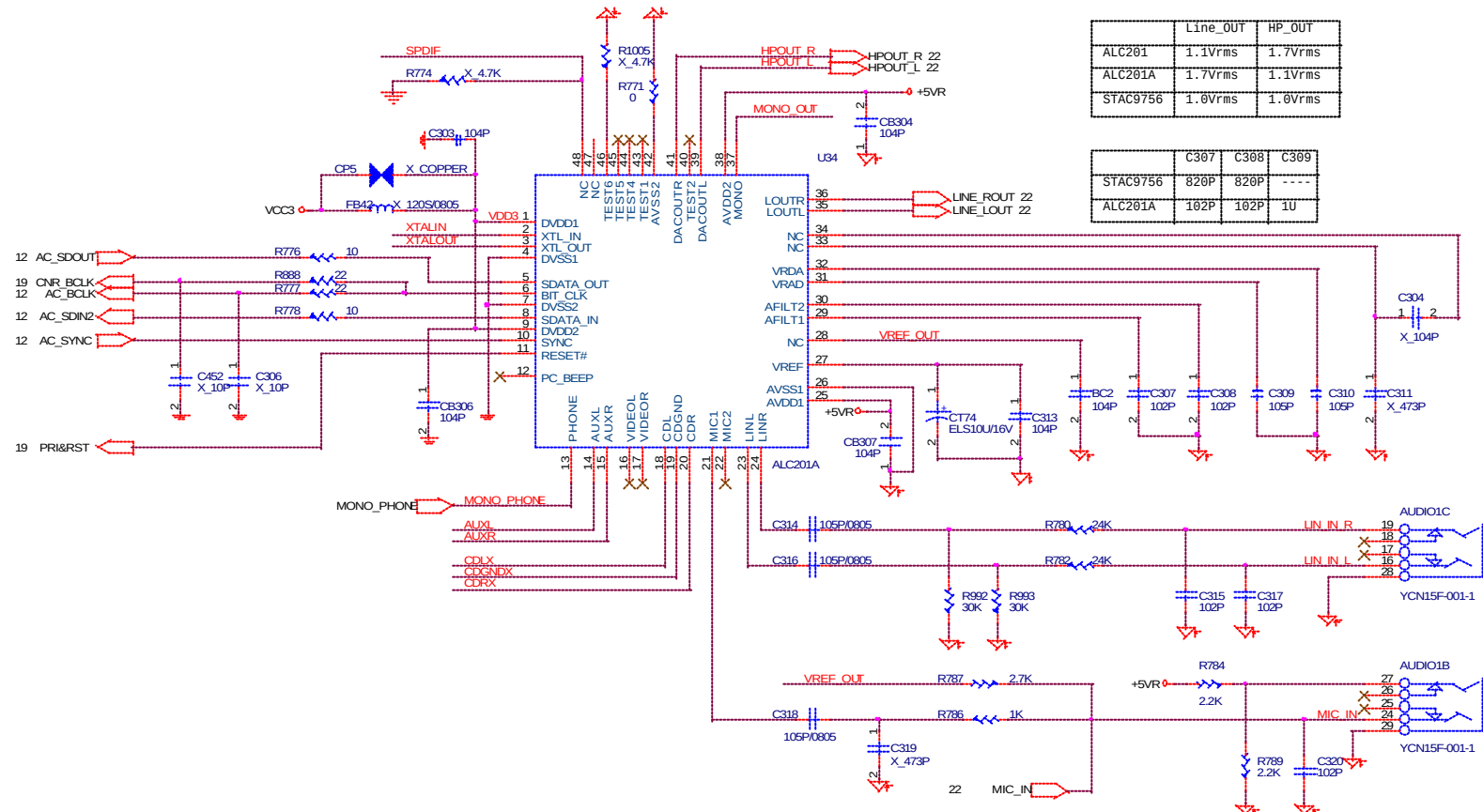
- * USB Trace width : 9 mils
- * USB Trace Spacing : 25 mils
- * Differential USB Signal Trace, Spacing : 18 mils
- * USB Power Trace must be 40mils width

REAR PANEL USB CONNECTOR FOR USB PORT 4,5

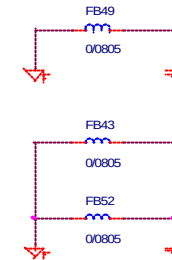
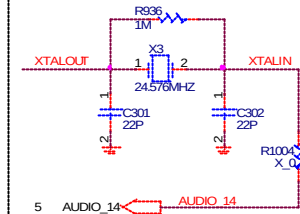


MICRO-STAR INT'L CO.,LTD.			
Title: USB CONNECTORS			
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ALC201A AC97 CODEC

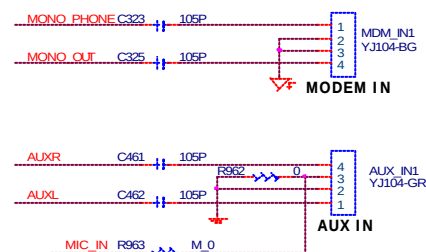
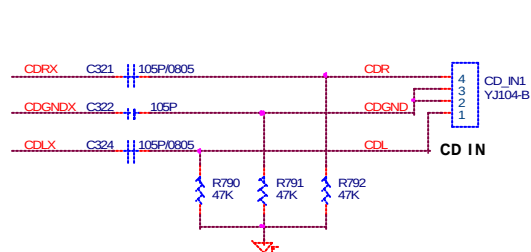


AUDIO CODE CRYSTAL CIRCUIT

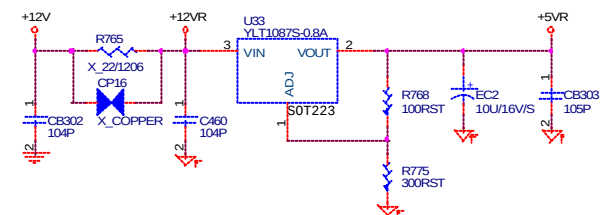
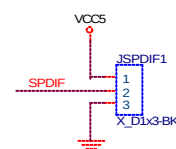


AUDIO CODE REGULATORS

AUDIO CODE CD / AUX / MODEM IN HEADERS



SPDIF HEADERS



MICRO-STAR INT'L CO.,LTD.

AC97 CODEC

MS-6526

Rev
300

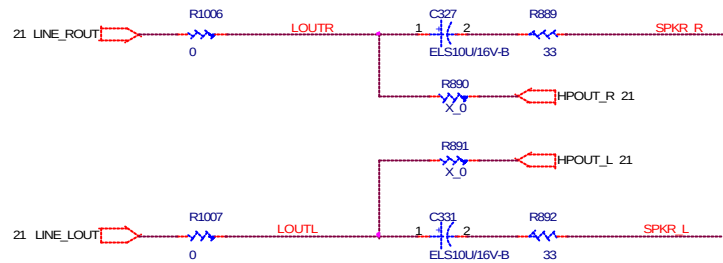
Date: Monday, May 13, 2002

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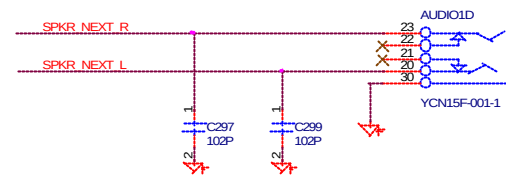
MS-0320

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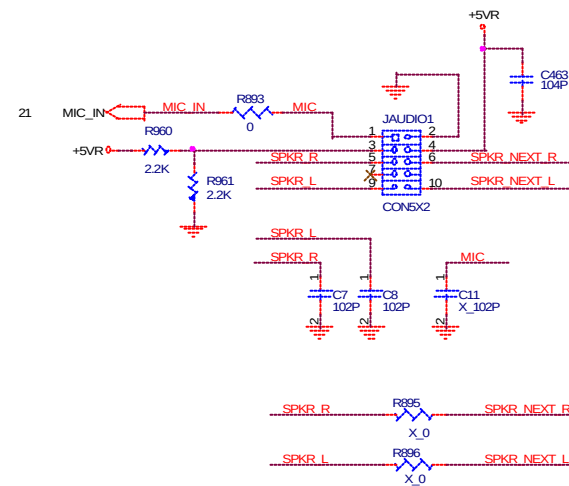
SPEAKER OUT CIRCUIT



SPEAKER OUT JACK



FOR Intel INTERNAL HEADER



MICRO-STAR INT'L CO.,LTD.

Title **AUDIO AMPLIFIER**

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SERIAL PORT 1

The schematic diagram illustrates the SERIAL PORT 1 circuit. It features a 75232-1 UART chip (U14) connected to a 12V supply. The chip is configured with VCC to +12V, V- to -12V, and V+ to +12V. The chip's pins are connected to various components, including two RS-485 transceivers, D9 (1N4148-S-LL34) and D10 (1N4148-S-LL34), and two capacitors, CB206 and CB207, for signal conditioning. The circuit also includes a 12V supply, a 12V supply, and a 12V supply. The circuit is labeled SERIAL PORT 1.

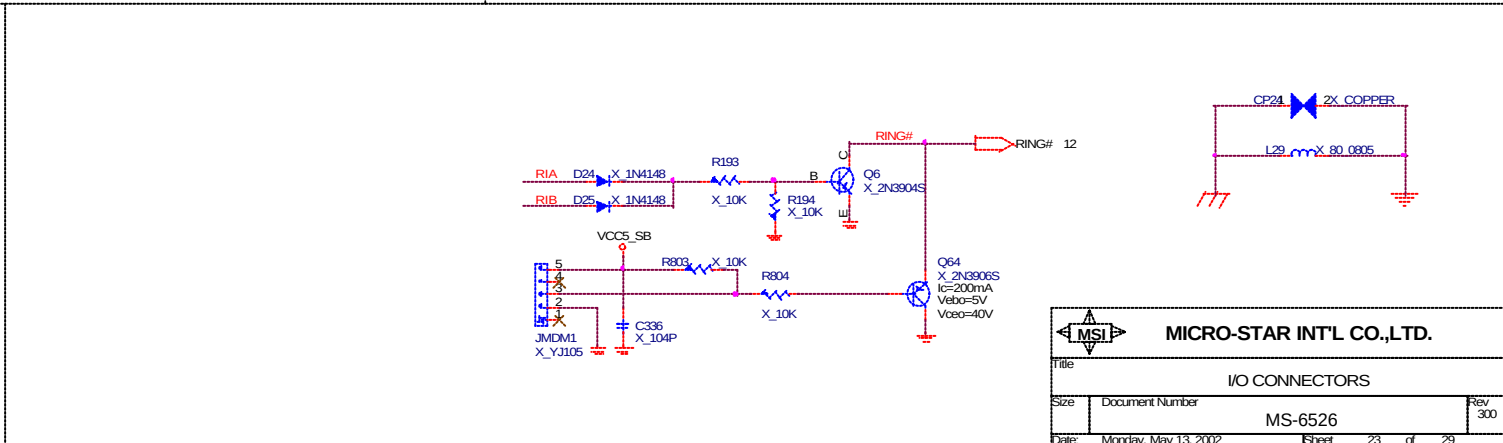
The schematic diagram illustrates the Parallel Port configuration. It shows the connection of LP signals to the LPT1A and LPT-D25-BK-BI connectors. The LP signals are connected to the LPT1A connector via a 1N4148S diode (D11) and a 2.2K resistor (R320). The LPT1A connector is connected to the LPT-D25-BK-BI connector via a 2.2K resistor (R320). The LPT-D25-BK-BI connector is connected to the LPT1A connector via a 2.2K resistor (R320). The LPT1A connector is connected to the LPT-D25-BK-BI connector via a 2.2K resistor (R320). The LPT1A connector is connected to the LPT-D25-BK-BI connector via a 2.2K resistor (R320).

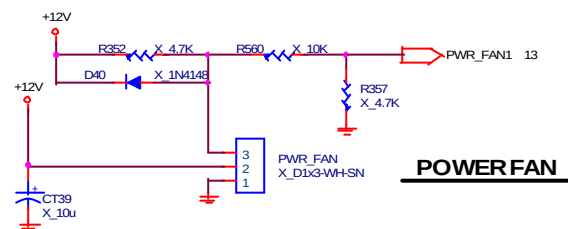
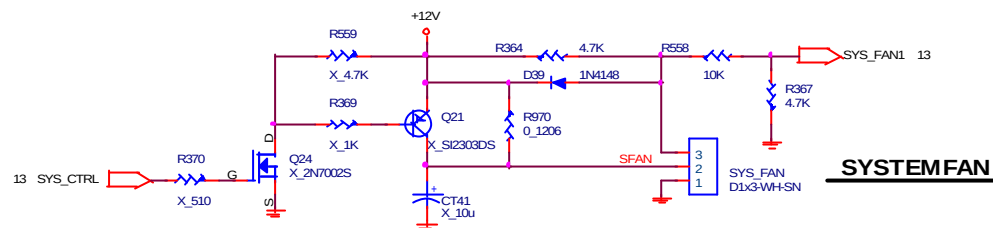
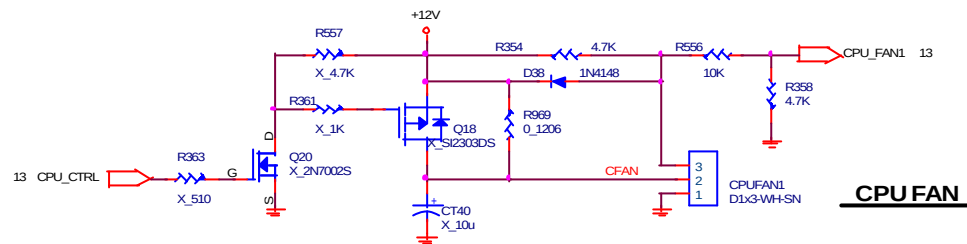
[illegible]

FLOPPY CONNECTOR

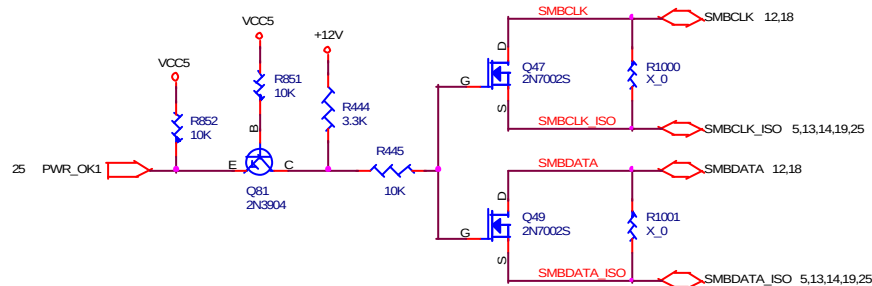
Pin	Signal	Direction
1	Ground	
2	DRV DEN0	Output
3	Ground	
4	INDEX#	Output
5	Ground	
6	DRV DEN1	Output
7	Ground	
8	INDEX#	Output
9	Ground	
10	MOT A#	Output
11	Ground	
12	DRV B#	Output
13	Ground	
14	DRV A#	Output
15	Ground	
16	MOT B#	Output
17	Ground	
18	DIR#	Output
19	Ground	
20	STEP#	Output
21	Ground	
22	WT DT#	Output
23	Ground	
24	WT EN#	Output
25	Ground	
26	TRACK0#	Output
27	Ground	
28	FDD WP#	Output
29	Ground	
30	RDATA#	Output
31	Ground	
32	HEAD#	Output
33	Ground	
34	DSKCHG#	Output

D2x17-1:31-BK



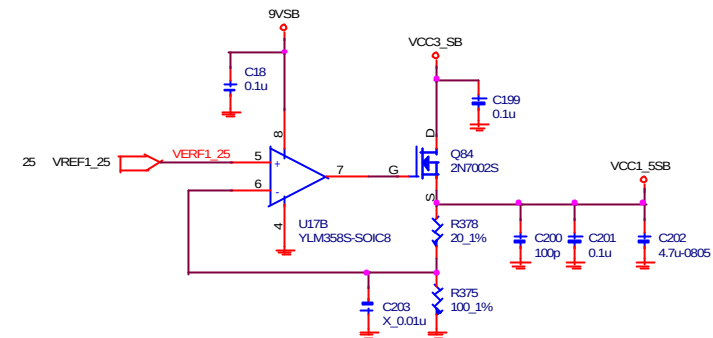


SMBus Isolation

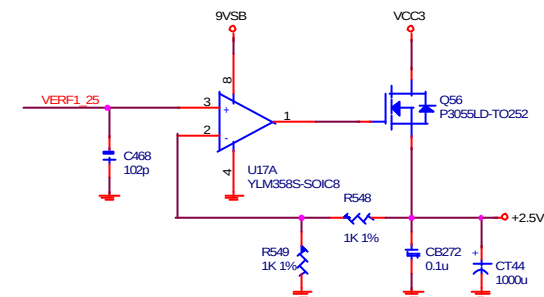


1.5V STANDBY POWER TRANSLATOR

(40mils trace/20 mils space)



AGP4X & GMCH 1.5V POWER TRANSLATOR



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SEL0	5VUSB
H	2 MOSFET
L	1 MOSFET

**S50# pin function(Hi level = 5V)
same as 5VUSB(Hi level = 12V)
5VUSB USE 2 MOSFET

Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC5_STR	Main	Standby	OV
MEM_STR	Main	Standby	OV

Near
302D

**INPUT 2 AND 3 MUST BE HI LEVEL WHEN USE
OUTPUT 1 AND 2 FOR GPIO FUNCTION

DDR VTT Power

1.25V/2.1A

SEL1	VRAM	VRAM_2.5
H	3.3VDUAL	2.5V
TRI-STATE	3.3VSB	2.5V
L	3.3VSTR	1.25V

FOR 3VSB OR 3VSTR SETTING BY SEL1

FOR 3VDUAL
SETTING BY
SEL1

** SETTING 3VSTR THEN VRAM_2.5
BECOME TO 1.25 VREF

Wide Trace

DDR 2.5V Power

2.5V/2.8A+5.92A

5V DUAL Power

CHARGE PUMP VOLTAGE OUTPUT

VCC_VID / VID_GOOD

Place MOSFET near CPU

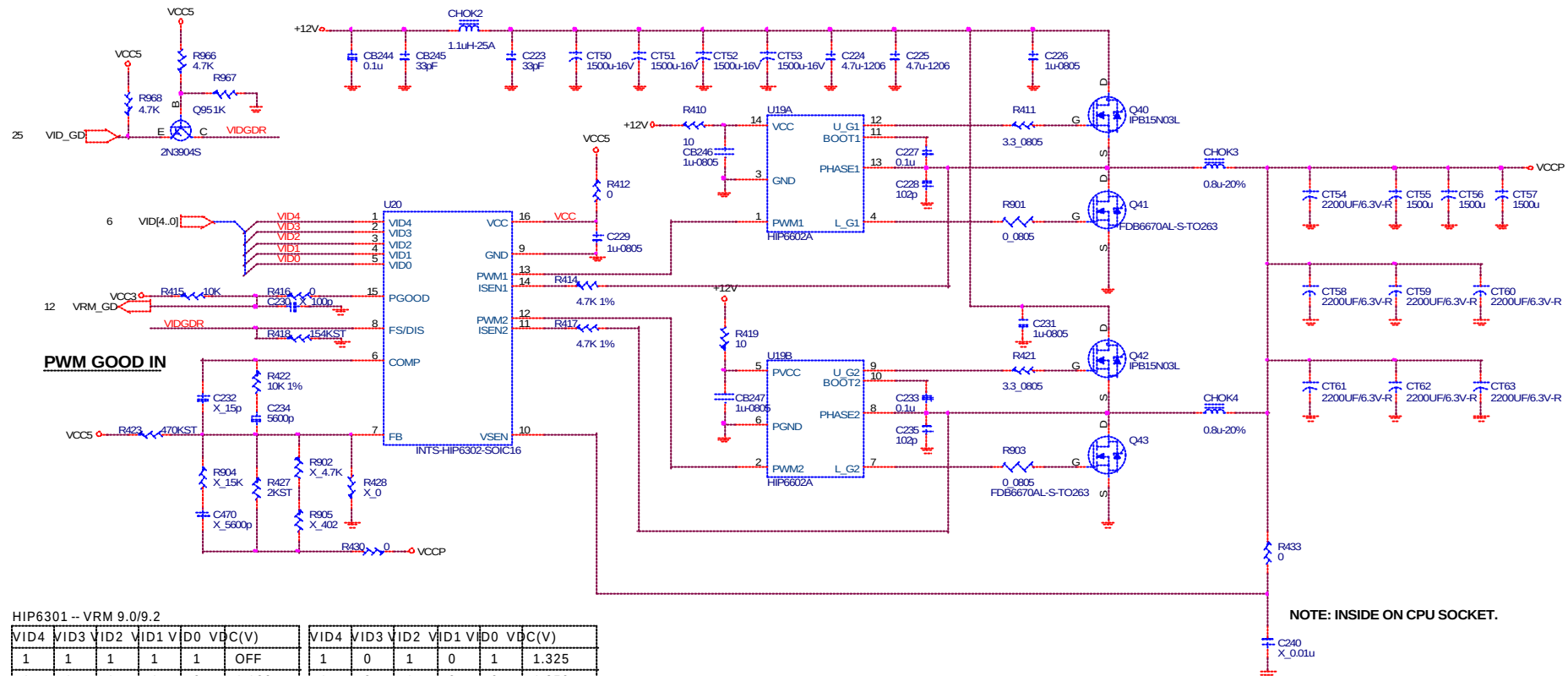
THIS PIN IS OPEN DRAIN OUTPUT

+2.5V
D30
1N4001-S-SM-1
MEM_STR



MICRO-STAR INT'L CO.,LTD.

Title ACPI CONTROLLER		
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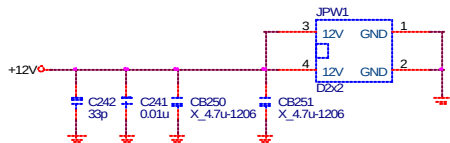


HIP6301 -- VRM 9.0/9.2

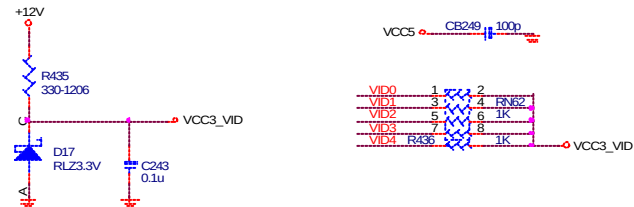
VID4	VID3	VID2	VID1	V	D0	VDC(V)
1	1	1	1	1	0	OFF
1	1	1	1	0	0	1.100
1	1	1	0	1	1	1.125
1	1	1	0	0	0	1.150
1	1	0	1	1	1	1.175
1	1	0	1	0	0	1.200
1	1	0	0	1	1	1.225
1	1	0	0	0	0	1.250
1	0	1	1	1	1	1.275
1	0	1	1	0	0	1.300

VID4	VID3	VID2	VID1	V	D0	VDC(V)
1	0	1	0	1	1	1.325
1	0	1	0	0	0	1.350
1	0	0	1	1	1	1.375
1	0	0	1	0	0	1.400
1	0	0	0	1	1	1.425
1	0	0	0	0	0	1.450
0	1	1	1	1	1	1.475
0	1	1	1	0	0	1.500
0	1	1	0	1	1	1.525
0	1	1	0	0	0	1.550

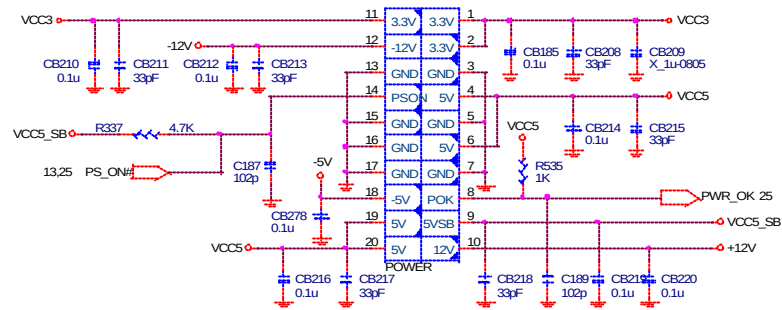
ATX12V POWER CONNECTOR



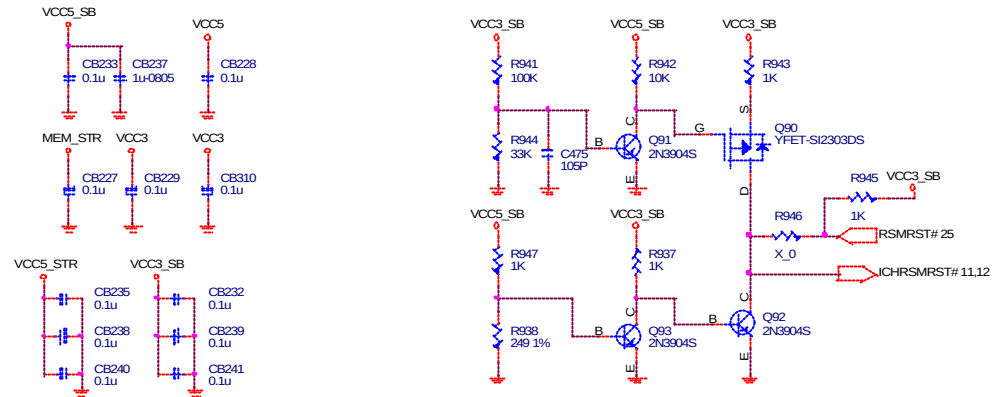
VID PULL-UP RESISTORS



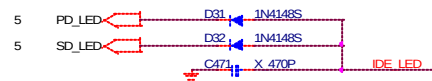
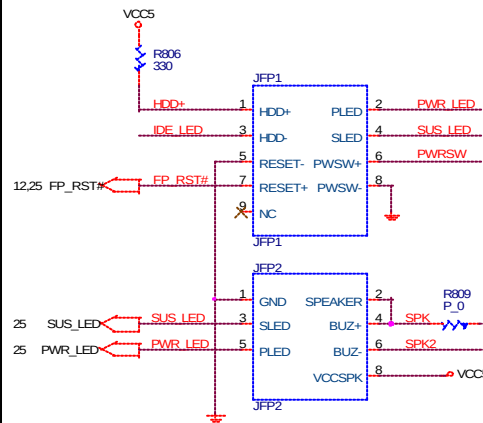
ATX CONNECTOR



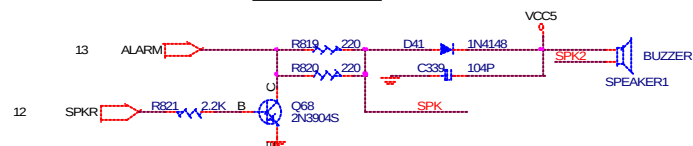
REGULATORS OUTPUT DECOUPLING CAPACITORS



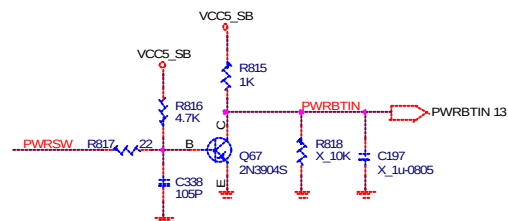
MSI/Intel Front Panel



SPEAKER



POWER BUTTON



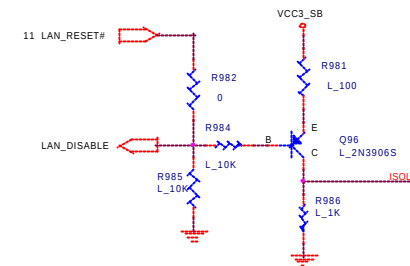
MICRO-STAR INT'L CO.,LTD.

Title	Front Panel & ATX Connector & FAN
-------	-----------------------------------

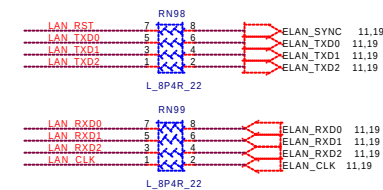
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LAN DISABLE

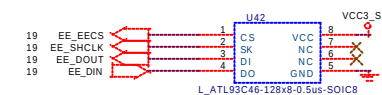


LAN OPTION RESISTORS



LAN EEPROM

Near ICH4

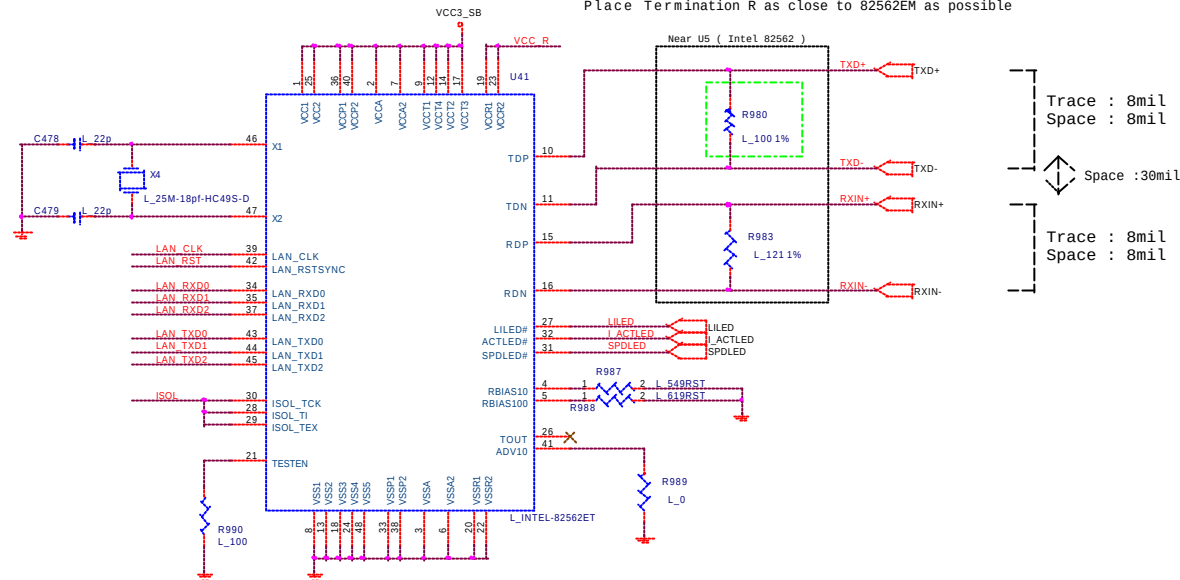


Remark:
82562EM with 93C66:M33-26N0103-A26
82562ET with 93C46:M33-1500203-A26 *

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Title			LAN INTEL 82562EMET	Rev 300
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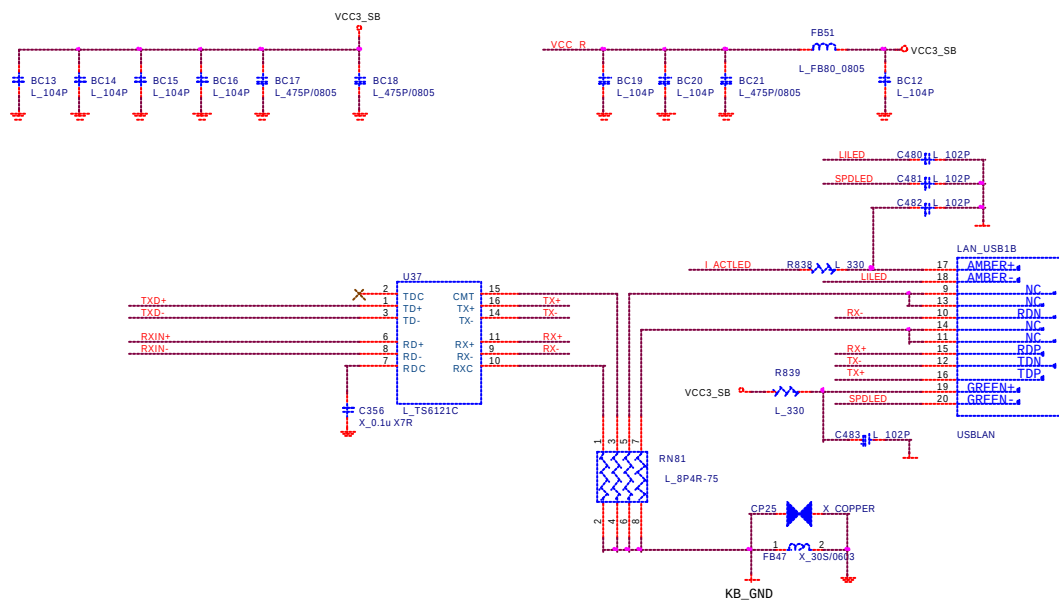
Place Termination R as close to 82562EM as possible

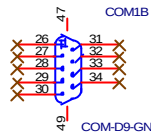
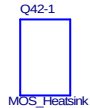
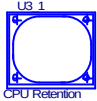
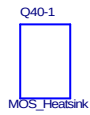
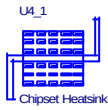
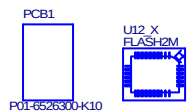


Trace : 8mil
Space : 8mil

Space : 30mil

Trace : 8mil
Space : 8mil

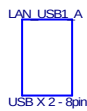
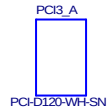




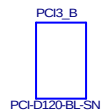
JBAT1 Clear CMOS	
1 - 2	Normal *
2 - 3	Clear CMOS

BIOS_WP	BIOS Update
SHORT	Locked
OPEN	Unlocked *

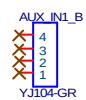
JLAN1	LAN SELECT
1-2	ENABLED
2-3	DISABLED



Option :M



Option :M



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Title			MANUAL PARTS
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