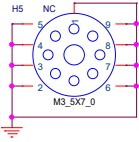
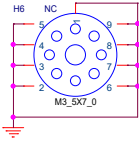
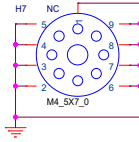
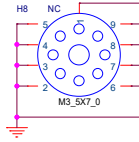
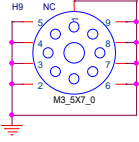
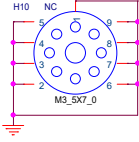
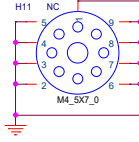
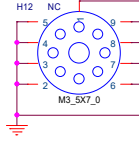
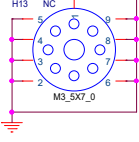
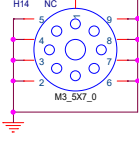
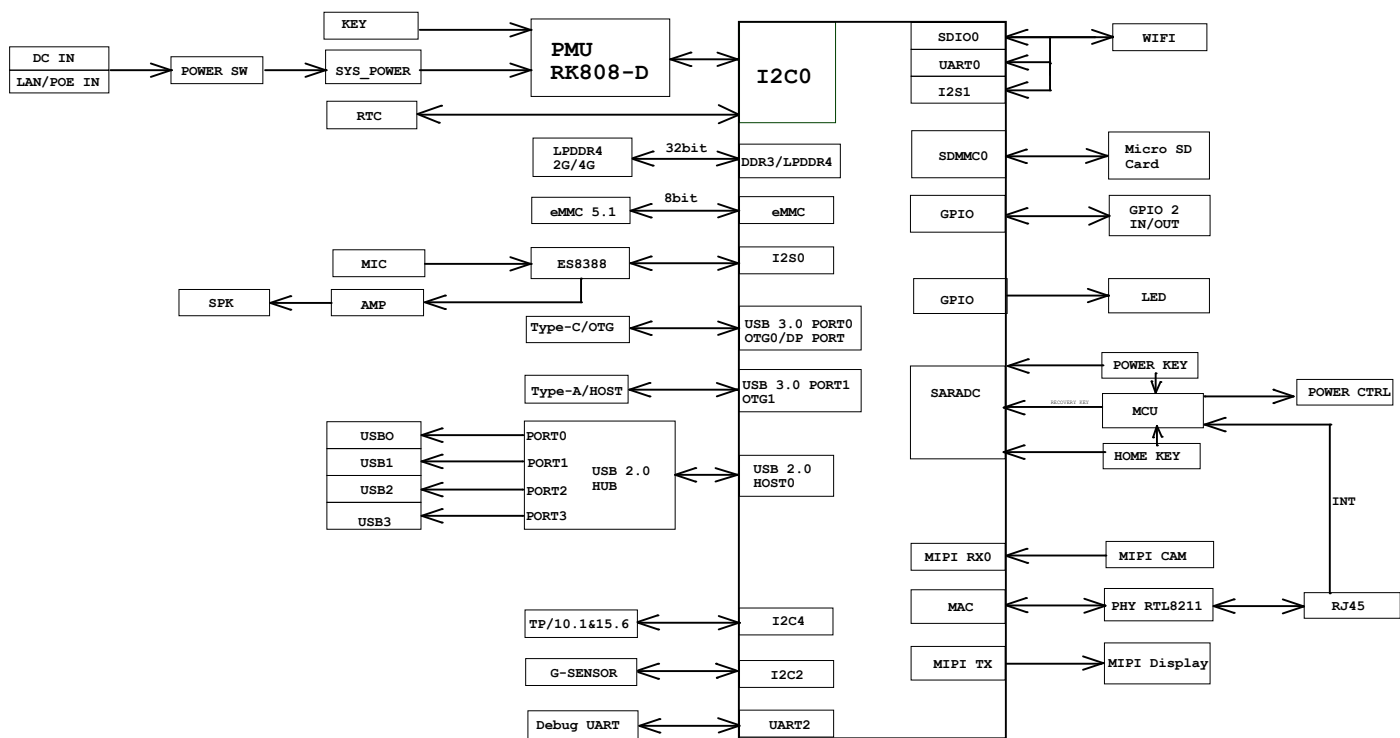


PCB MARK & LABEL

Heat Sink	
Optical Marks	T1 T2 T3 T4 T5 T6 MARK MARK MARK MARK MARK MARK MARK MARK MARK MARK MARK MARK
Label Outline	LOT Number ☐ H2 10mm X 10mm SR 105AC ☐ H1 20mm X 10mm
Silkscreen	PCB Name & Version E4723060 ☐ ENG Version A20xxx ☐ SMT DIP ROHS ☐ ELO3399 ☐ A20xxx
Mounting Hole	H5 NC  M3_5X7_0 H6 NC  M3_5X7_0 H7 NC  M4_5X7_0 H8 NC  M3_5X7_0 H9 NC  M3_5X7_0 H10 NC  M3_5X7_0 H11 NC  M4_5X7_0 H12 NC  M3_5X7_0 H13 NC  M3_5X7_0 H14 NC  M3_5X7_0

			
Project:	E473060		
File:	01.Msc		
Date:	Friday, March 25, 2022	Rev:	A0
Designed by:	ZhangboYanjin	Sheet:	1 of 32

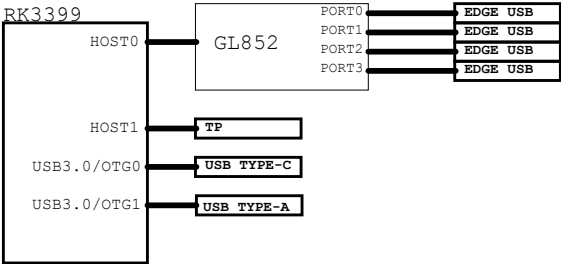
5	4	3	2	1															
Change List																			
<table><tr><td>Version</td><td>Date</td><td>Author</td><td>Change Note</td><td>Approved</td></tr><tr><td>V0.1</td><td>April 24, 2020</td><td>Zhangbo&Yangyin</td><td>First edition.</td><td>Zhouchangliang</td></tr><tr><td></td><td></td><td></td><td></td><td></td></tr></table>					Version	Date	Author	Change Note	Approved	V0.1	April 24, 2020	Zhangbo&Yangyin	First edition.	Zhouchangliang					
Version	Date	Author	Change Note	Approved															
V0.1	April 24, 2020	Zhangbo&Yangyin	First edition.	Zhouchangliang															
<table><tr><td colspan="2">Project: E473060</td></tr><tr><td colspan="2">File: 02.Change List</td></tr><tr><td>Date: Friday, March 25, 2022</td><td>Rev: A0</td></tr><tr><td>Designed by: Zhangbo&Yangyin</td><td>Sheet: 2 of 32</td></tr></table>					Project: E473060		File: 02.Change List		Date: Friday, March 25, 2022	Rev: A0	Designed by: Zhangbo&Yangyin	Sheet: 2 of 32							
Project: E473060																			
File: 02.Change List																			
Date: Friday, March 25, 2022	Rev: A0																		
Designed by: Zhangbo&Yangyin	Sheet: 2 of 32																		
5	4	3	2	1															



I2C MAP

Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
I2C0	GP101_B7/SP13_RXD/I2C0_SDA GP101_C0/SP13_TXD/I2C0_SCL	PMU102	I2C_SDA_PMIC I2C_SCL_PMIC	VCC_3V0	Rockchip RK808	0x1b	PMIC	100kHz,400KHz
					SY8377FNC	0x40	DC-DC Buck	100kHz,400KHz,3.4MHz
					SY8388FNC	0x41	DC-DC Buck	100kHz,400KHz,3.4MHz
					PT7C4337	0xd0,0xd1	RTC	100kHz
I2C1	GP104_A1/I2C1_SDA GP104_A2/I2C1_SCL	API05	I2C1_SDA_IV8 I2C1_SCL_IV8	VCC_IV8	ES8388/1.8V	0x10,0x11	Audio codec	100kHz
					FUSB360HPK/1.8V	0x44,0x46	USB-TypeC Mux	100kHz
					GL852	0x2C	USB HUB	100kHz
I2C2	GP102_A0/VOP_D0/CIF_D0/I2C2_SDA GP102_A1/VOP_D1/CIF_D1/I2C2_SCL	API02	I2C2_SDA_IV8 I2C2_SCL_IV8	VCC_IV8	MM8450Q/1.8V	0x1D,0x1E	G-SENSOR	100kHz,400KHz,
I2C3	GP104_C0/I2C3_SDA/UART2B_RX GP104_C1/I2C3_SCL/UART2B_TX	API04	I2C3_SDA I2C3_SCL	VCC_3V0	TP/3.3V	TD0	TP TOUCH	100kHz,400KHz,3.4MHz
I2C4	GP101_B3/I2C4_SDA GP101_B4/I2C4_SCL	PMU102	I2C4_SDA I2C4_SCL	VCC_3V0	SM201/3.0V	0xA0 0xE0	EEPROM	10kHz
I2C5	GP103_B2/MAC_RMR/I2C5_SDA GP103_B3/MAC_CLK/I2C5_SCL	API01	MAC USE					
I2C6	GP102_B1/SP12_RXD/CIF_HREF/I2C6_SDA GP102_B2/SP12_TXD/CIF_CLKIN/I2C6_SCL	API02	NOT USE					
I2C7	GP102_A7/VOP_D7/CIF_D7/I2C7_SDA GP102_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL	API02	I2C7_SDA_IV8 I2C7_SCL_IV8	VCC_IV8	MIP1_CSI /1.8V			100kHz

USB MAP

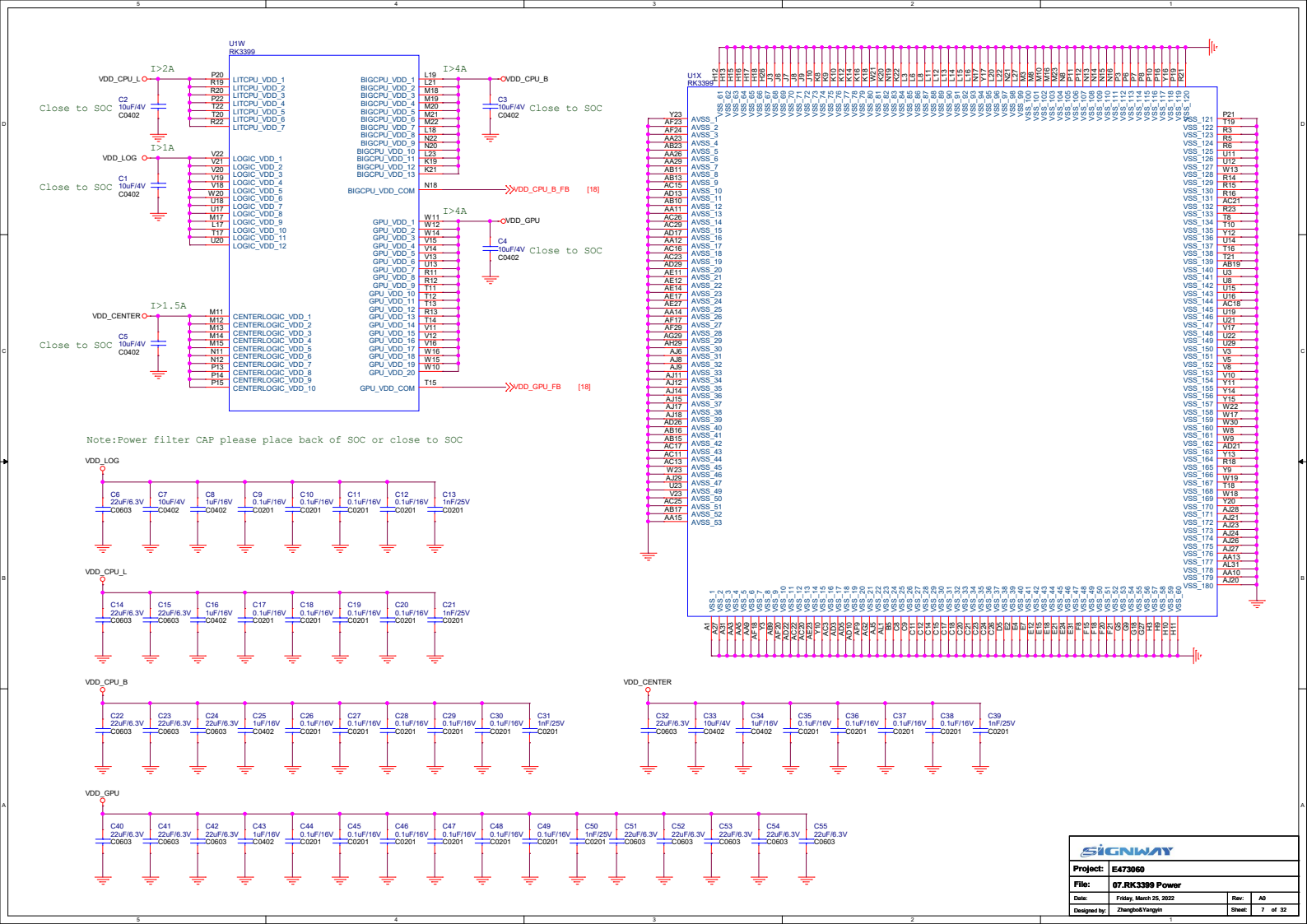


SIGNWAY			
Project: E473060			
File: 05I2C&USB Map			
Date: Friday, March 25, 2022	Rev: A0		
Designed by: ZhengshuYang	Sheet: 5 of 32		

Power Domain Map

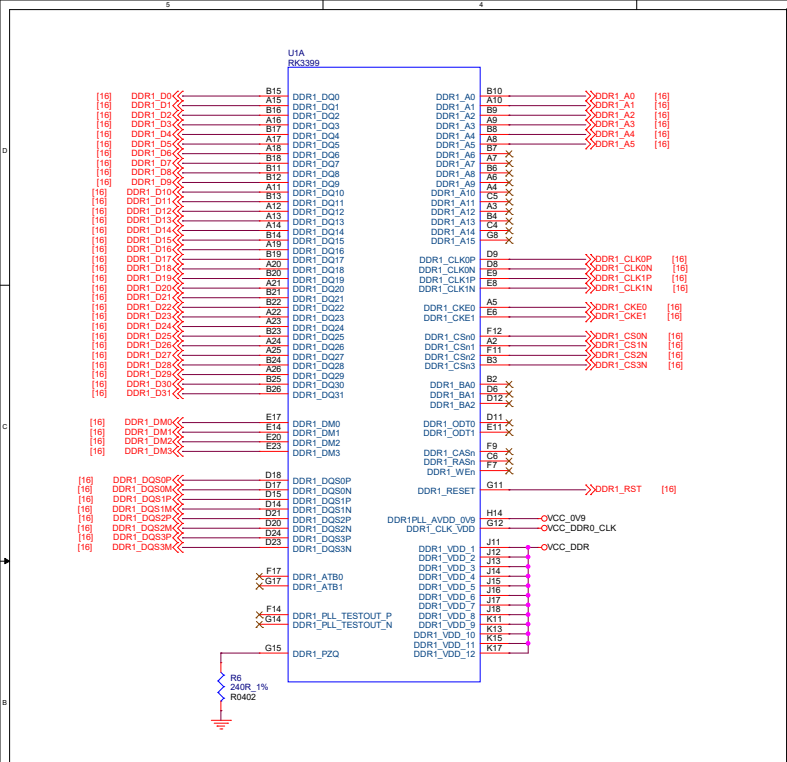
Part Port	Domain	Pin name in datasheet	I/O type	Power supply	Power source
Part C	PMUI01	pmui01_gpio0ab	1.8V only	VCCA_1V8	RK808-D VLD03
Part E	PMUI02/PART E	pmui830_gpiolabcd	3.0V	VCC_1V5	RK808-D Buck4 RK808-D VLD06
Part I	API01	gmac_gpio3abc	3.3V only	VCC_1V8 VCC3V3_LAN	RK808-D Buck4
Part L	API02	bt656_gpio2ab	1.8V	VCC_1V8	RK808-D VLD03
Part G	API03	wifi/bt_gpio2cd	1.8V only	VCC_1V8	RK808-D Buck4
Part K	API04	gpio1830_gpio4cd	1.8V 3.0V(Default)	VCC_1V5 VCC_3V0	RK808-D VLD06 RK808-D VLD08
Part J	API05/PART J	audio_gpio3d_gpio4a	VCC1V8_CODEC	VCC1V8_CODEC	RK808-D VLD01
Part F	SDMMC0	sdmmc_gpio4b	1.8V 3.0V(Default)	VCC_SDIO	RK808-D VLD04

			
Project:	E473060		
File:	06.Power Domain Map		
Date:	Friday, March 25, 2022	Rev:	A0
Designed by:	Zhanghui&Yangye	Sheet:	6 of 32

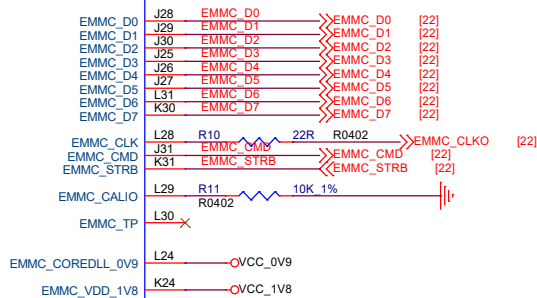


SIGNWAY			
Project: E473060			
File: 07 RK3399 Power			
Date: Friday, March 25, 2022	Rev: A0		
Designed by: Zhengshu Yang	Sheet: 7	of 32	



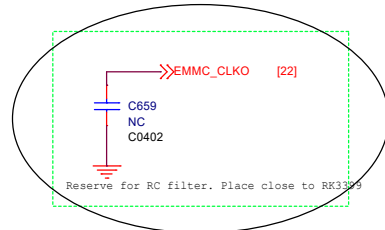
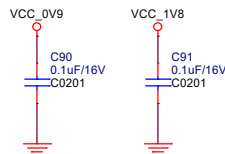


U1H
RK3399

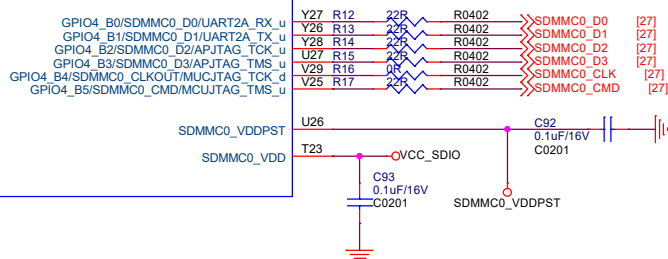


EMMC design rule:

- 1.Data[0:7], CMD and STRB signals routing parallel as a group, the skew between each other must be less than 100mils;
- 2.The Clock signal should be isolated with other signals by GND plane, the skew between data lines is less than 20ps;
- 3.Max trace length < 3.93 inches;
- 4.Trace impedance 50ohm+/-10%;
- 5.The distance between other signals follows the 3W rule;
- 6.R11 close to SOC;



U1F
RK3399

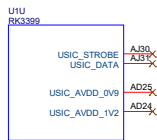


SDMMC design rule:

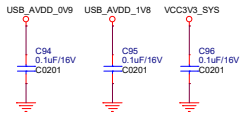
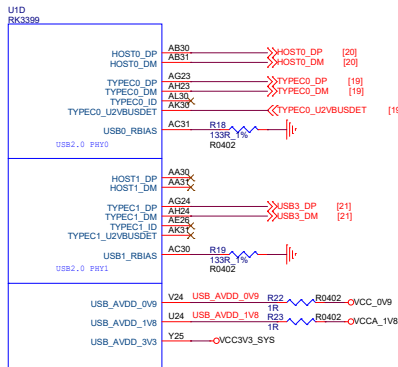
- 1.Data[0:7] and CMD signals routing parallel as a group, the skew between each other must be less than 100mils;
- 2.The Clock signal should be isolated with other signals by GND plane, the skew between data lines is less than 20ps;
- 3.Max trace length < 3.93 inches;
- 4.Trace impedance 50ohm+/-10%;
- 5.The distance between other signals follows the 3W rule;

SIGNWAY

Project:	E473060		
File:	10.RK3399 Flash&SDMMC Controler		
Date:	Friday, March 25, 2022	Rev:	A0
Designed by:	Zhangbo&Yangyin	Sheet:	10 of 32

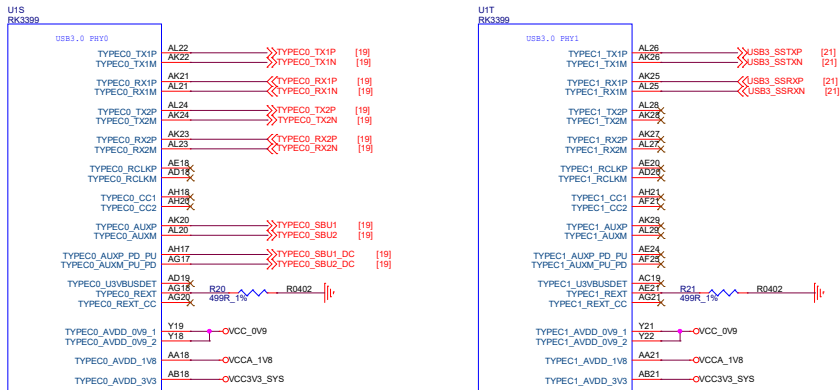


USB2.0



USB2.0 design rule:
1.Max intra-pair skew < 4 ps;
2.Max trace length < 6 inches;
3.Max allowed via < 4;
4.Trace impedance 90ohm+/-10%;
5.The distance between other signals follows the 3W rule;

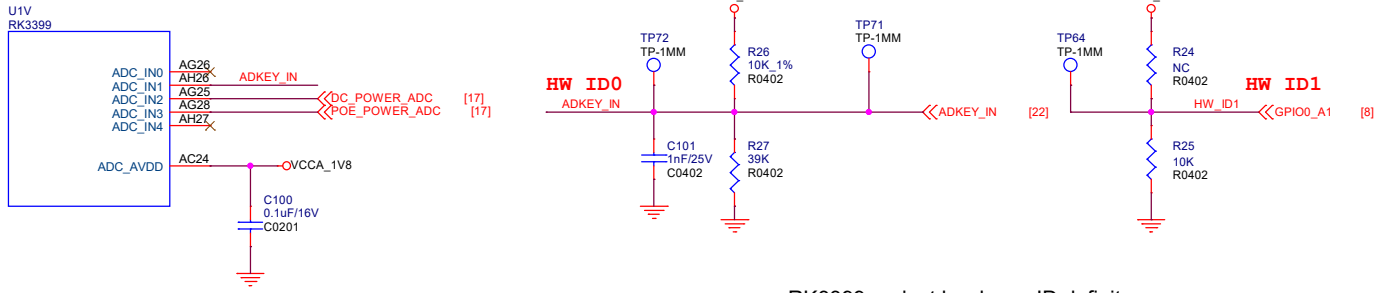
USB3.0



USB3.0 design rule:
1.Max intra-pair skew < 4 ps;
2.Max length skew between TX and RX < 1.6 ns;
3.Max trace length < 6 inches;
4.Max allowed via < 4;
5.Trace impedance 90ohm+/-10%;
6.The distance between other signals follows the 3W rule;

DP design rule:
1.Max intra-pair skew < 4 ps;
2.Max trace length < 6 inches;
3.Max allowed via < 4;
4.Trace impedance 90ohm+/-10%;
5.The distance between other signals follows the 3W rule;

SIGNWAY			
Project:	E473060		
File:	11.RK3399 USB/AUSIC Controller		
Date:	Friday, March 25, 2022	Rev:	A0
Designed by:	ZhanghuiYang	Sheet:	11 of 32

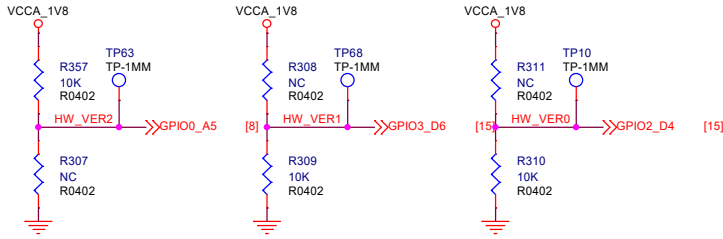


RK3399 project hardware ID definiton

ADC1 Function1: Hold on ZERO when AC plug in cold boot, enter Flash Image Mode.
 ADC1 Function2: Secondary definiton of product hardware ID.
 GPIO0_A1: Main definiton of of product hardware ID.

Seq.	GPIO0_A1	R27	ADC	HW ID	Date
01.	Low	NC	1.800V	E472673 (15.6)	March 02, 2020
02.	Low	91K	1.622V	E472828 (21.5)	
03.	Low	39K	1.433V	E473060 (10.1)	
04.	Low	22K	1.238V	E473261 (BACKPACK)	
05.	Low	13K	1.017V	E679524 (USB-C)	
06.	Low	9.1K	0.858V	TBD	
07.	Low	6.2K	0.689V	TBD	
08.	Low	3.9K	0.505V	TBD	
09.	High	NC	1.800V	TBD	
10.	High	91K	1.622V	TBD	
11.	High	39K	1.433V	TBD	
12.	High	22K	1.238V	TBD	
13.	High	13K	1.017V	TBD	
14.	High	9.1K	0.858V	TBD	
15.	High	6.2K	0.689V	TBD	
16.	High	3.9K	0.505V	TBD	

HW Version



E473060 Hardware Version

Seq.	GPIO0_A5	GPIO3_D6	GPIO2_D4	HW Version	Date
01.	0	0	0	V1 (EVT)	March 26, 2020
02.	0	0	1	V2	TBD
03.	0	1	0	V3	TBD
04.	0	1	1	V4	TBD
05.	1	0	0	V5	sep22.2021
06.	1	0	1	V6	TBD
07.	1	1	0	V7	TBD
08.	1	1	1	V8	TBD

SiGNWAY			
Project:	E473060		
File:	12.RK3399 SARADC/Key		
Date:	Friday, March 25, 2022	Rev:	A0
Designed by:	Zhanghui&Yangyin	Sheet:	12 of 32

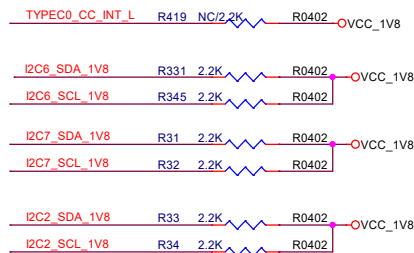
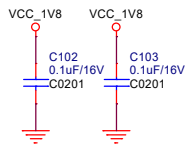
U1L
RK3399

GPI02_A0/VOP_D0/CIF_D0/I2C2_SDA_u
GPI02_A1/VOP_D1/CIF_D1/I2C2_SCL_u
GPI02_A2/VOP_D2/CIF_D2_d
GPI02_A3/VOP_D3/CIF_D3_d
GPI02_A4/VOP_D4/CIF_D4_d
GPI02_A5/VOP_D5/CIF_D5_d
GPI02_A6/VOP_D6/CIF_D6_d
GPI02_A7/VOP_D7/CIF_D7/I2C7_SDA_u
GPI02_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL_u
GPI02_B1/SPI2_RXD/CIF_HREF/I2C6_SDA_u
GPI02_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL_u
GPI02_B3/SPI2_CLK/VOP_DEN/CIF_CLKOUTA_u
GPI02_B4/SPI2_CSn0_u

APIO2_VDDPST
APIO2_VDD

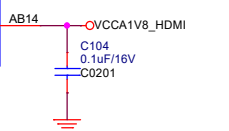
G31 << I2C2_SDA_1V8 [29]
H25 << I2C2_SCL_1V8 [29]
H30 << DVP_PWR [30]
F28 << Camera_RST_L [30]
H29 << EDGEUSB_EN3 [20]
F29 << TYPECO_CC_INT_L [19]
H27 << EDGEUSB_EN2 [20]
G30 << I2C7_SDA_1V8 [30]
H28 << I2C6_SDA_1V8 [30]
F30 << I2C7_SCL_1V8 [30]
H24 << I2C6_SCL_1V8 [30]
H31 << CIF_CLKO [30]
F31 << DVP_PDN0_H [30]

J24 -> VCC_1V8
K23 -> VCC_1V8



U1R
RK3399

MIPI_RX0_D0P
MIPI_RX0_D0N
MIPI_RX0_D1P
MIPI_RX0_D1N
MIPI_RX0_CLKP
MIPI_RX0_CLKN
MIPI_RX0_D2P
MIPI_RX0_D2N
MIPI_RX0_D3P
MIPI_RX0_D3N
MIPI_RX0_REXT
MIPI_RX0_AVDD_1V8



U1P
RK3399

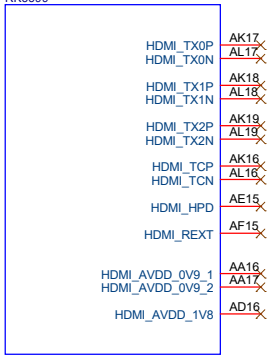
MIPI_TX1/RX1_D0P
MIPI_TX1/RX1_D0N
MIPI_TX1/RX1_D1P
MIPI_TX1/RX1_D1N
MIPI_TX1/RX1_CLKP
MIPI_TX1/RX1_CLKN
MIPI_TX1/RX1_D2P
MIPI_TX1/RX1_D2N
MIPI_TX1/RX1_D3P
MIPI_TX1/RX1_D3N
MIPI_TX1/RX1_REXT
MIPI_TX1/RX1_AVDD_1V8

AK6
AL6
AK7
AL7
AK8
AL8
AK9
AL9
AK10
AL10
AF11
AC10



Project:	E473060		
File:	13.RK3399 DVP Interface		
Date:	Friday, March 25, 2022	Rev:	A0
Designed by:	ZhanghuiYangin	Sheet:	13 of 32

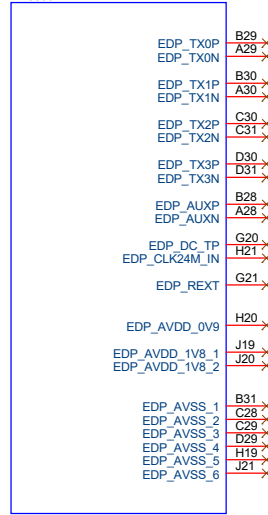
U1N
RK3399



HDMI design rule:

- 1.Max intra-pair skew < 4 ps;
- 2.Max length skew between clk and data < 80 ps;
- 3.Max trace length < 9.8 inchs;
- 4.Max allowed via < 4;
- 5.Trace impedance 100ohm+/-10%;
- 6.The distance between other signals follows the 3W rule;

U1M
RK3399



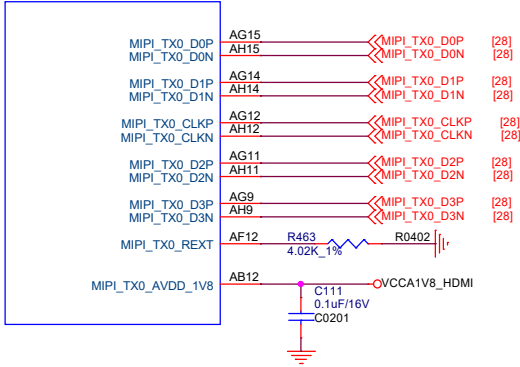
eDP design rule:

- 1.Max intra-pair skew < 4 ps;
- 2.Max trace length < 6 inchs;
- 3.Max allowed via < 4;
- 4.Trace impedance 90ohm+/-10%;
- 5.The distance between other signals follows the 3W rule;

MIPI design rule:

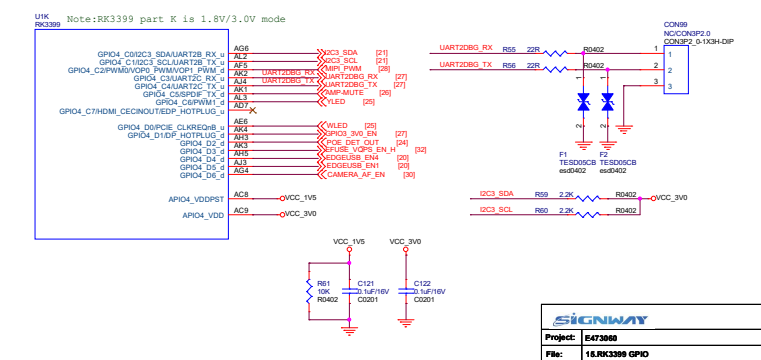
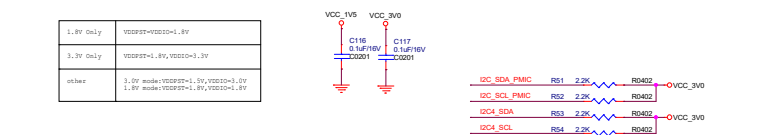
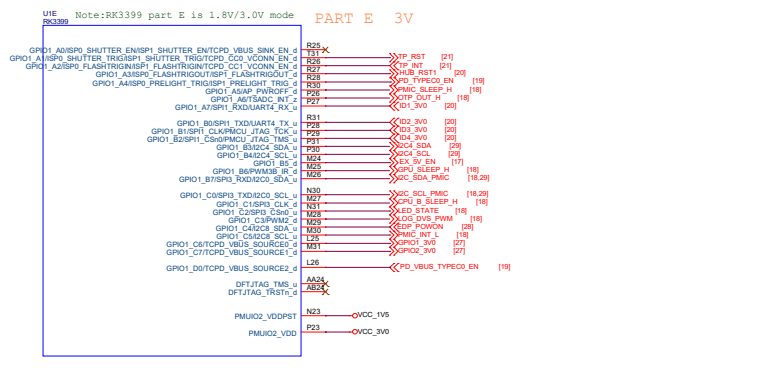
- 1.Max intra-pair skew < 4 ps;
- 2.Max length skew between clk and data < 7ps;
- 3.Max trace length < 7.2 inchs;
- 4.Max allowed via < 4;
- 5.Trace impedance 100ohm+/-10%;
- 6.The distance between other signals follows the 3W rule;

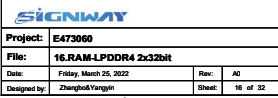
U1Q
RK3399



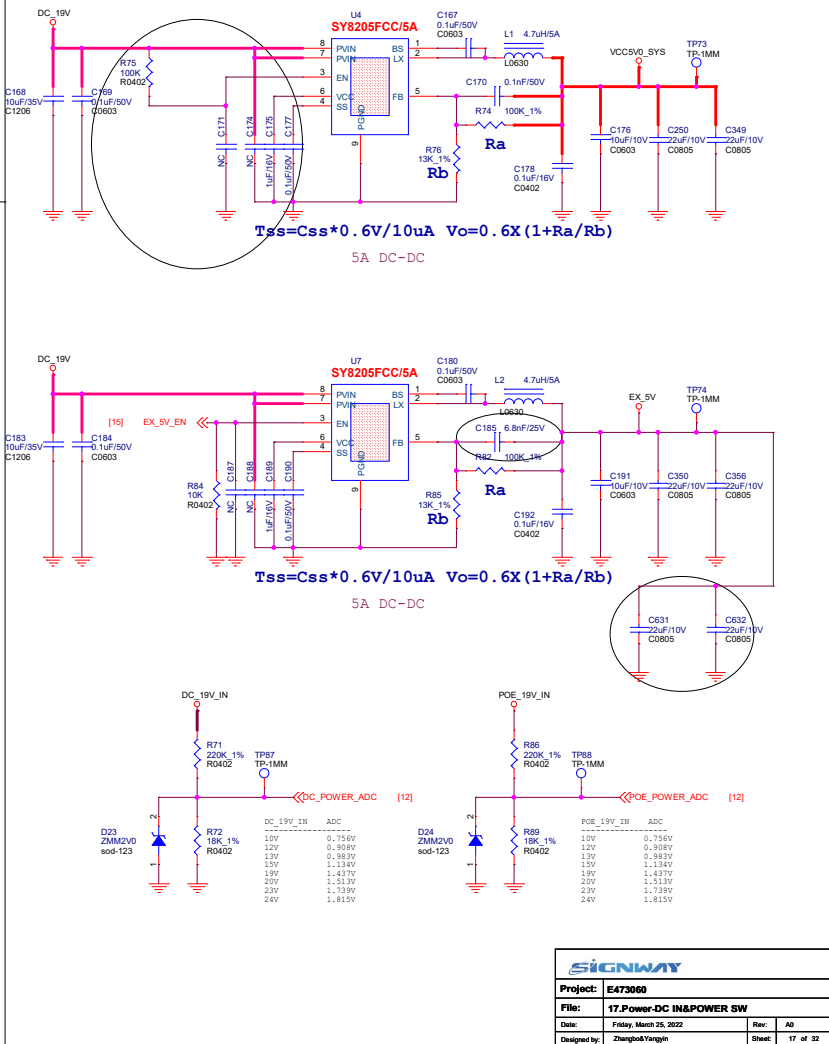
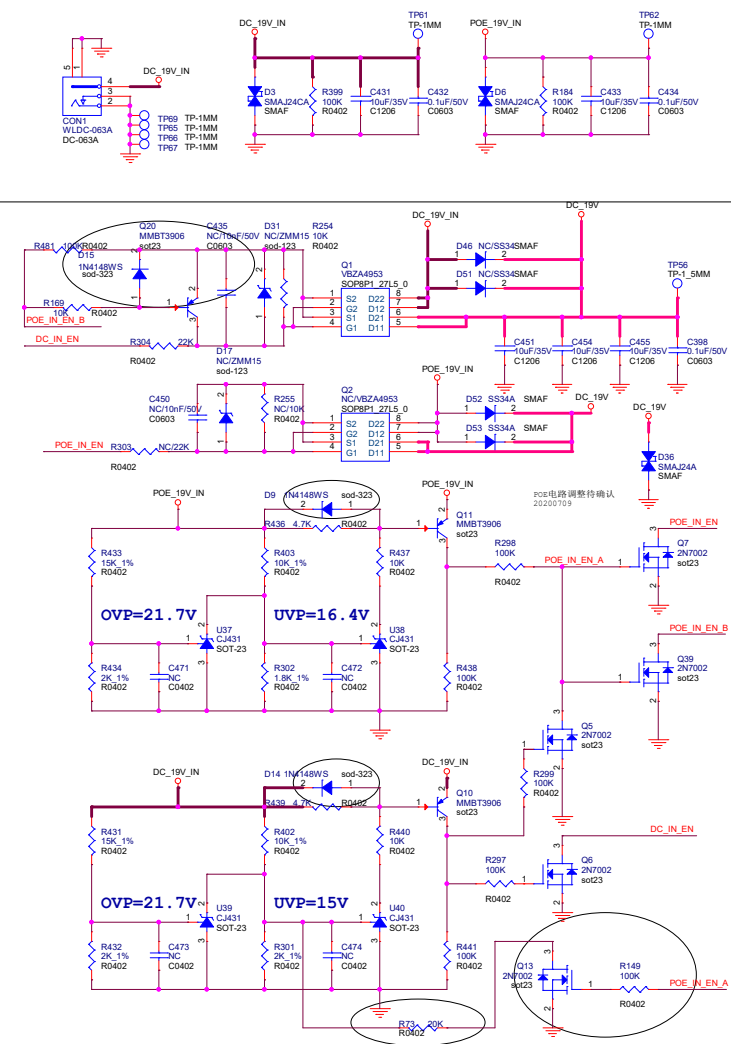
SIGNWAY

Project:	E473060		
File:	14.RK3399 Display Interface		
Date:	Friday, March 25, 2022	Rev:	A0
Designed by:	Zhanghui&Yangin	Sheet:	14 of 32

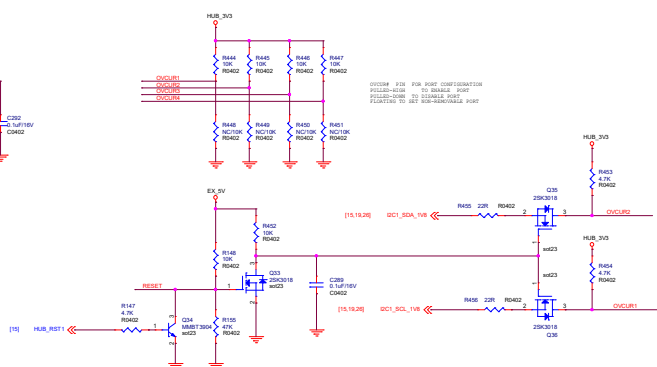
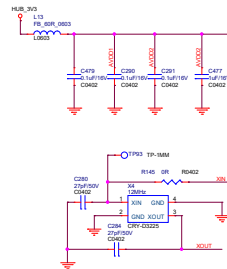
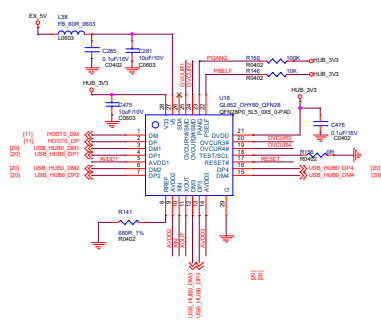




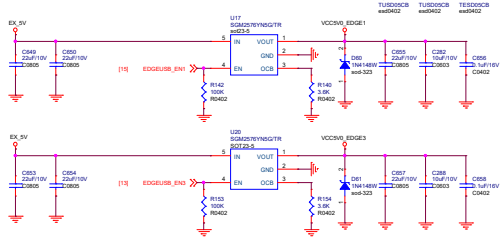
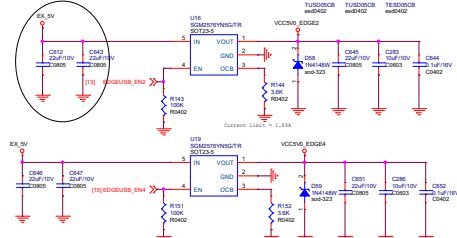
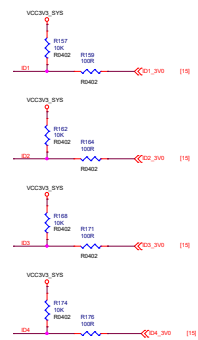
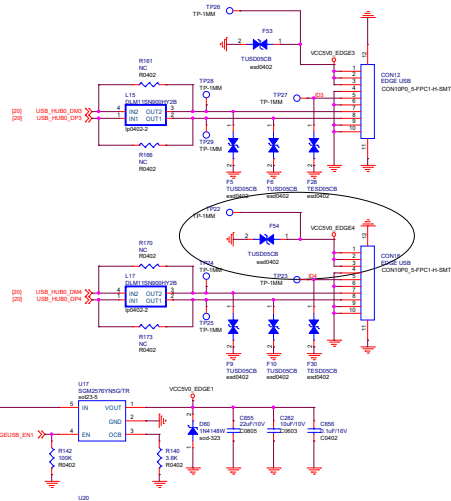
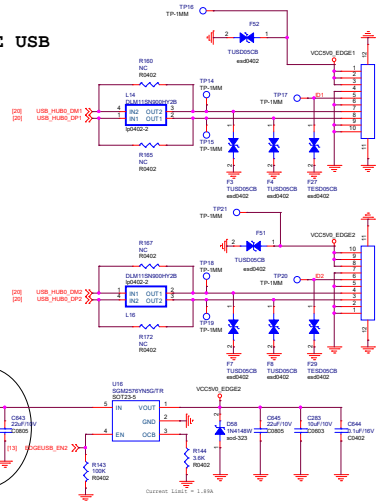
DC IN&SYSTEM Power



SMBUS ADDRESS : 0X2C



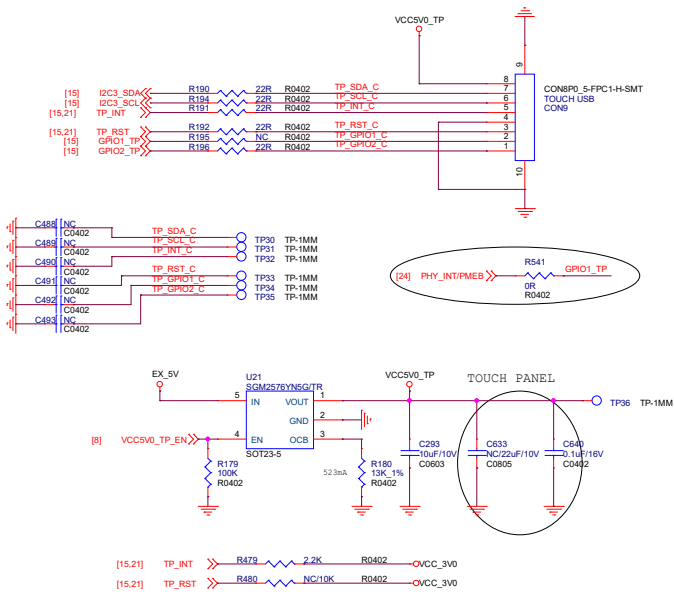
TP-1MM



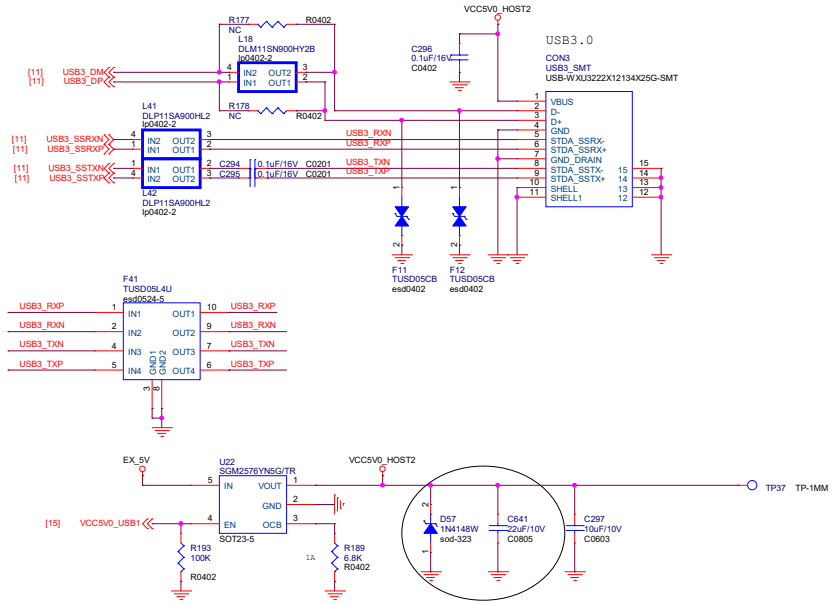
			
Project:		E473060	
File:		20.EDGE USB 4 PORT	
Date:	Friday, March 26, 2022	Rev:	40
Designed by:	ZhangQidongyan	Sheet:	26 of 32

Touch Panel

10.1" TOUCH

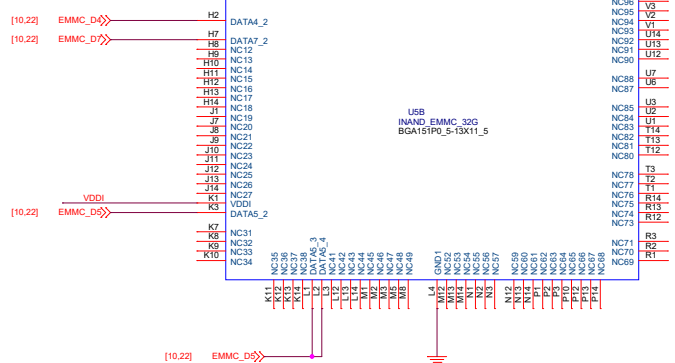
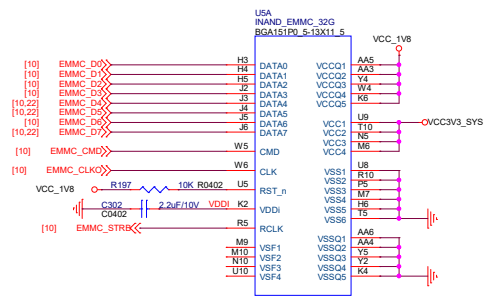


USB3.0 port



SIGNWAY			
Project: E473060			
File: 21.USB 3.0 HOST & TP			
Date: Friday, March 25, 2022	Rev: A0		
Designed by: Zhenghui Yang	Sheet: 21 of 32		

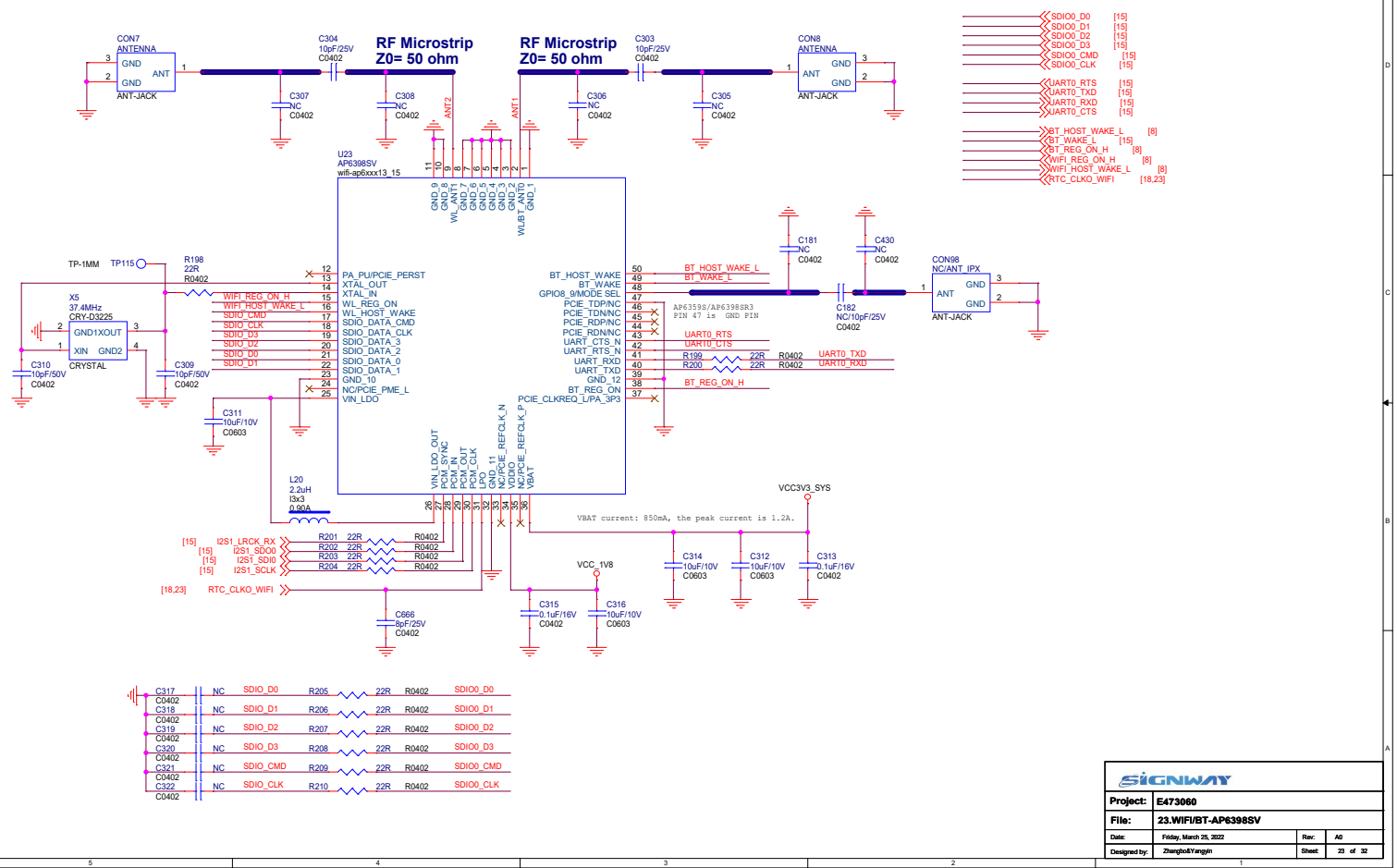
5	4	3	2	1
---	---	---	---	---

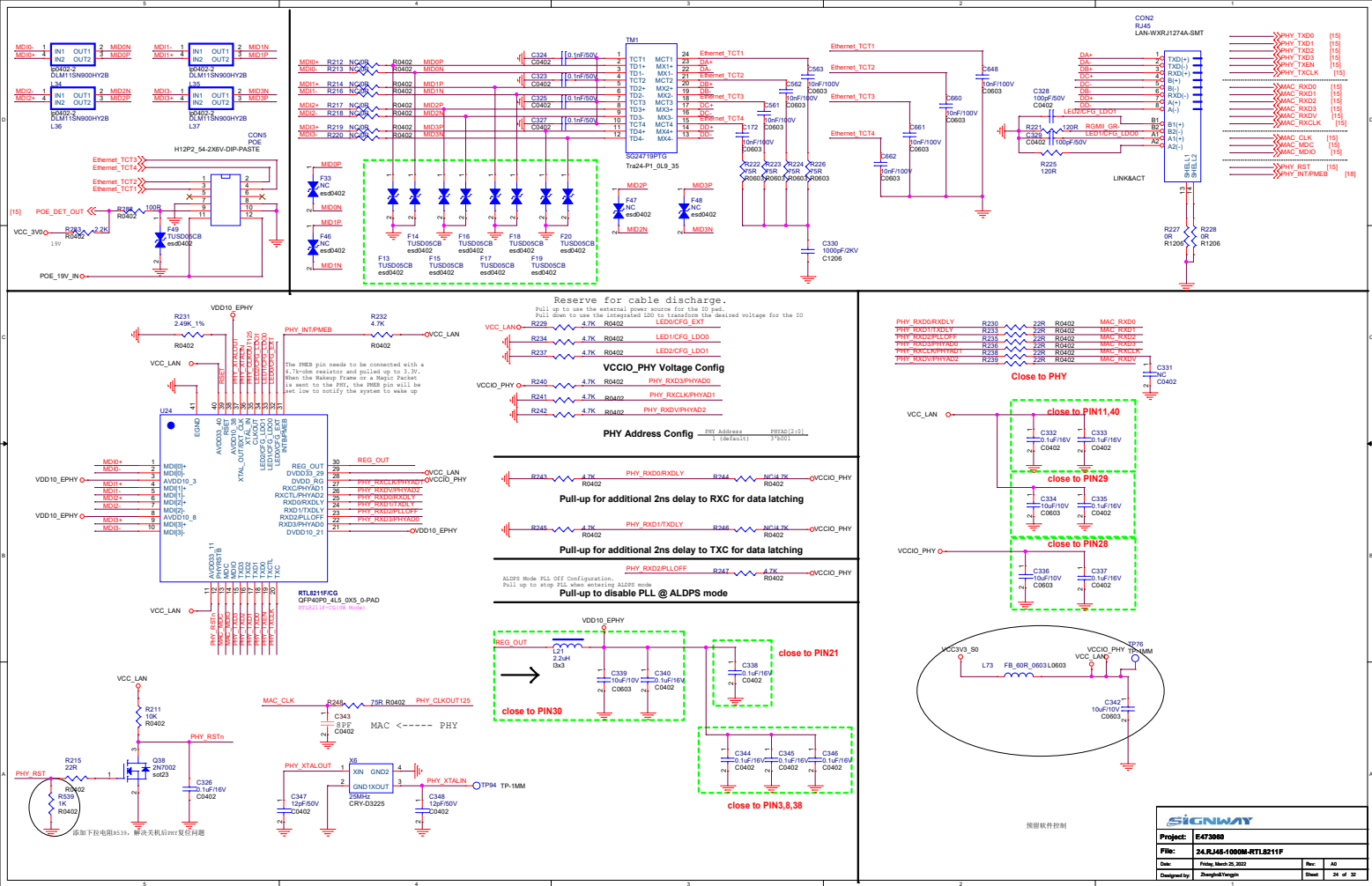


			
Project:	E473060		
File:	22.Memory-eMMC		
Date:	Friday, March 25, 2022	Rev:	A0
Designed by:	Zhangbo&Yangyin	Sheet:	22 of 32

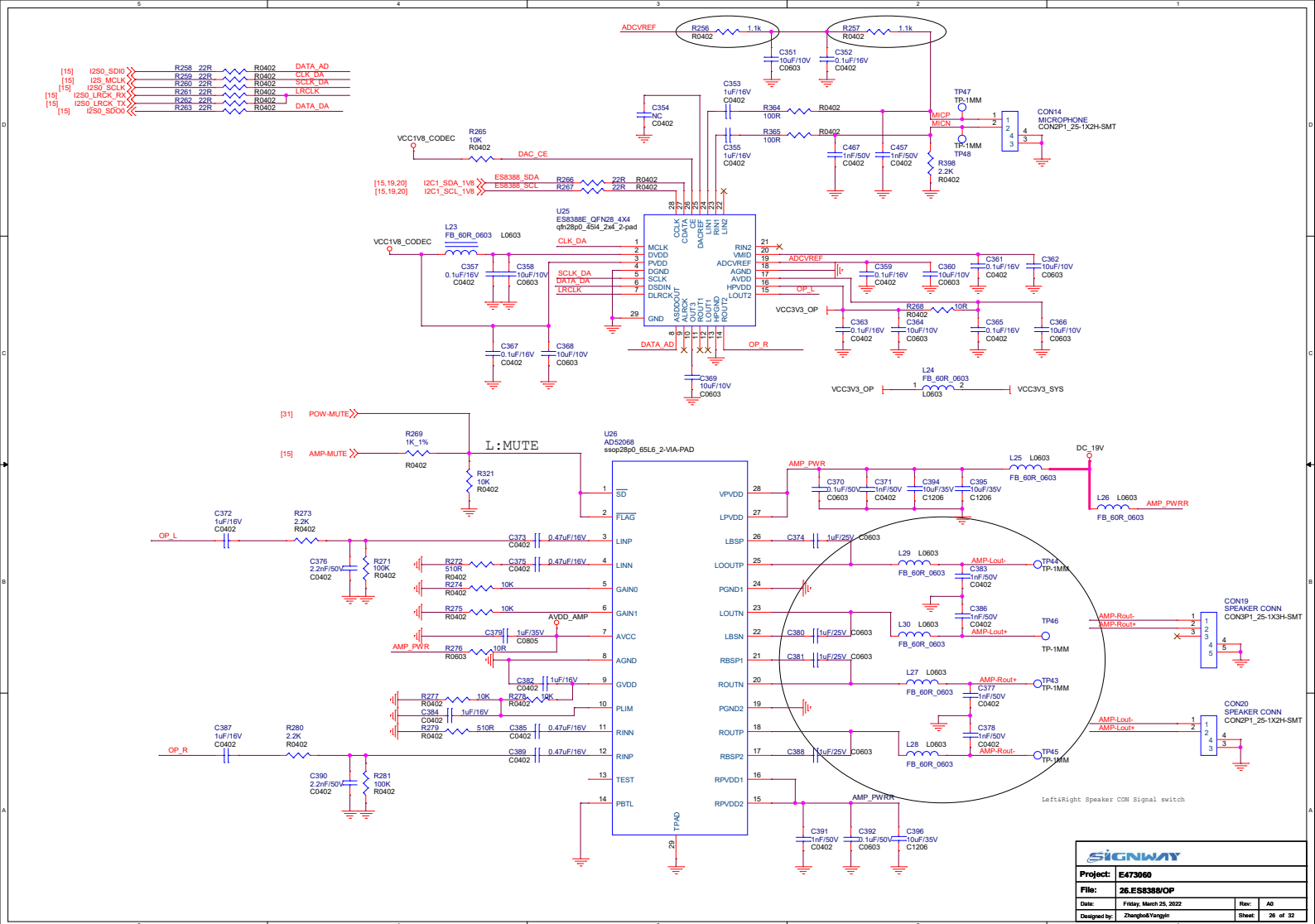
SDIO WIFI/BT MODULE-MIMO

Note:VBAT power supply range is 3.0V~4.8V.

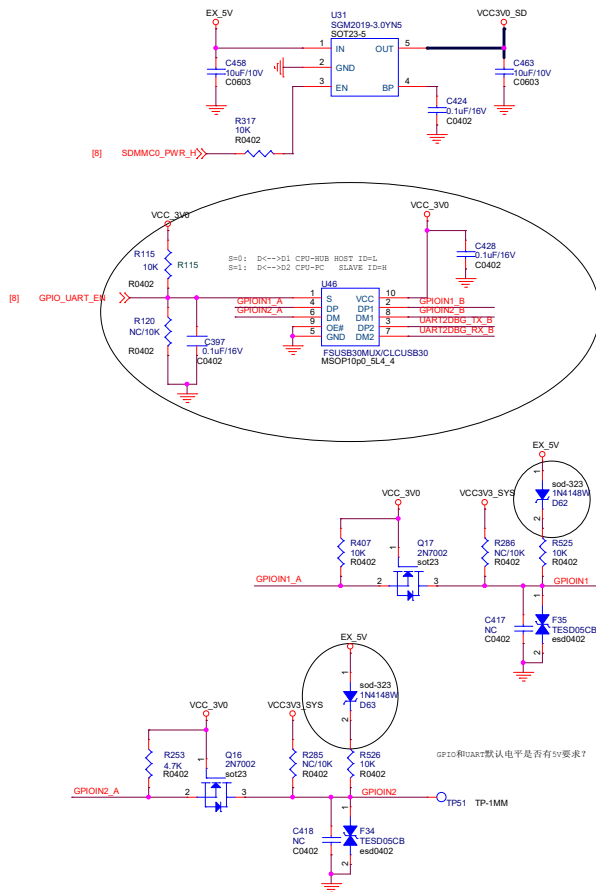




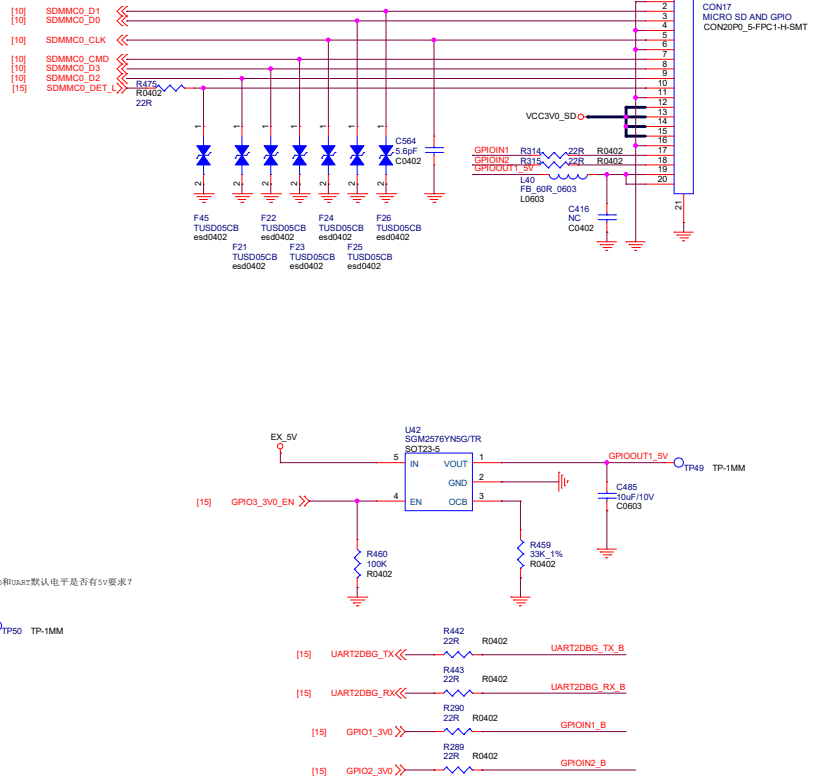
Project: E473080	
File: 24.RJ45-1000M-RTL8211F	
Date: Friday, March 25, 2022	Rev: A01
Designed by: Zhongfeng	Sheet: 24 of 32



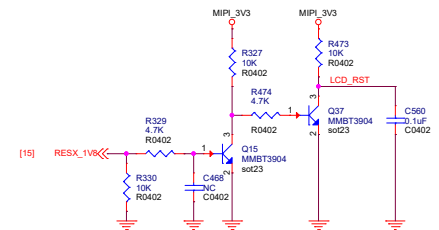
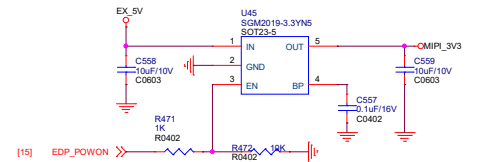
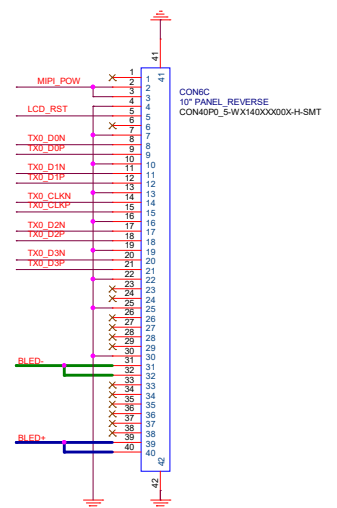
VCC3V0_SD power



TF CARD

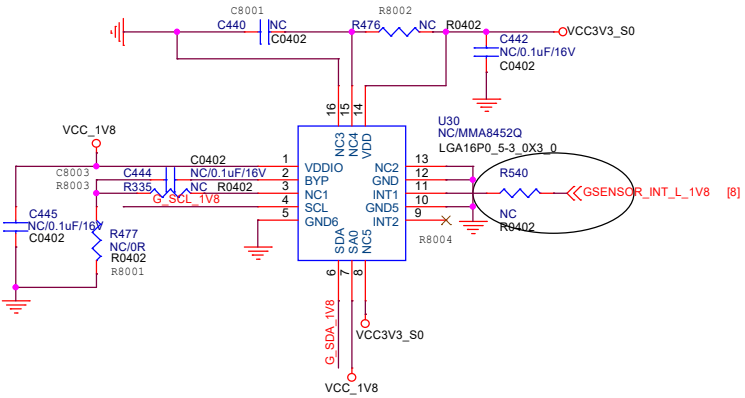


SIGWAY			
Project: EAT3060			
File: 27.TF Card/GPIO			
Date: Friday, March 25, 2022	Rev: A0		
Designed by: Zhengshu Yang	Sheet: 27 of 32		

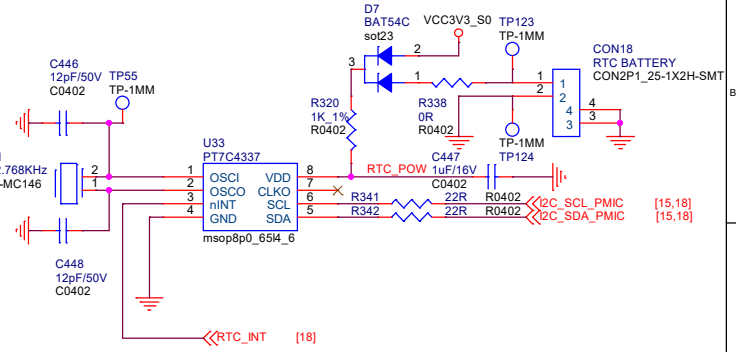
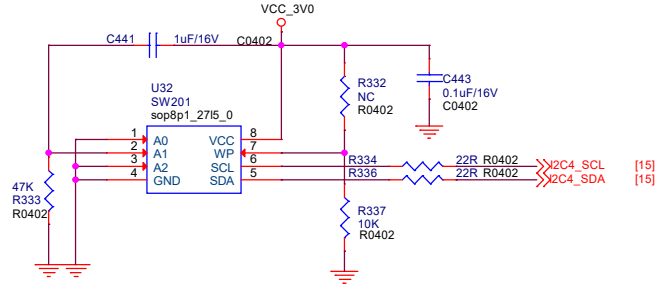
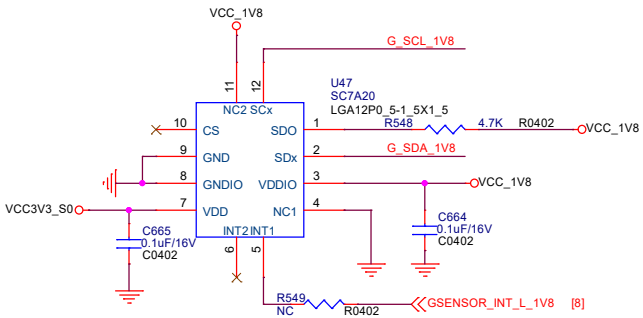


	LIS3DH	MMA8452Q	LSM303D
C8001	NC	NC	4.7uF
R8002	0ohm	NC	NC
R8001	NC	0ohm	NC
C8003	NC	0.1uF	0.22uF
R8003	NC	NC	OR
R8004	NC	NC	OR

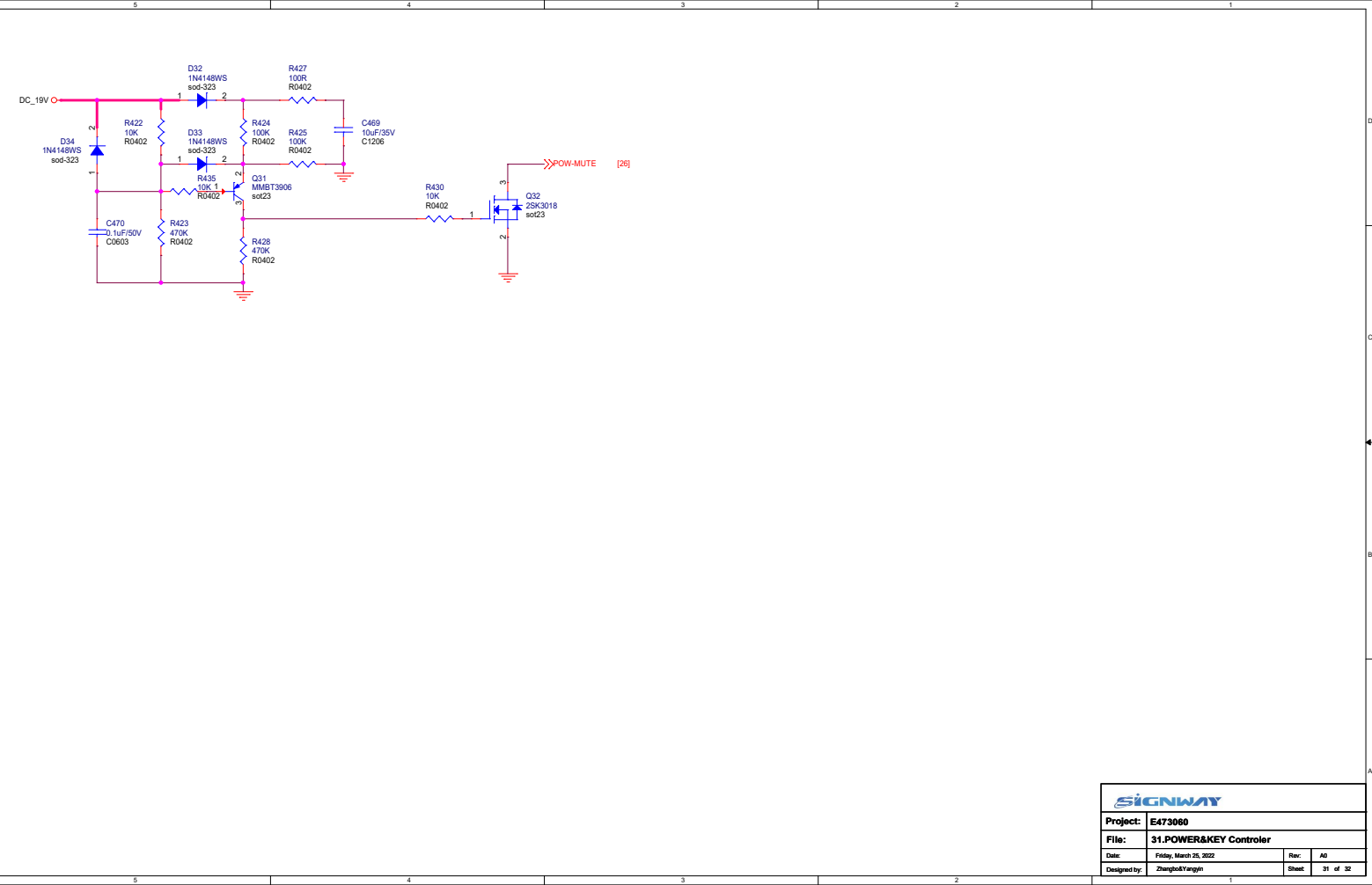
The MMA8452Q's standard slave address is a choice between the two sequential addresses 0011100 and 0011101. The selection is made by the high and low logic level of the SA0 (pin 7) input respectively. The slave addresses are factory programmed and alternate addresses are available at customer request



G_SCL_1V8 R339 22R R0402 I2C2_SCL_1V8 [13]
G_SDA_1V8 R340 22R R0402 I2C2_SDA_1V8 [13]



Project: E473060			
File: 29.G-sensor&RTC			
Date:	Friday, March 25, 2022	Rev:	A0
Designed by:	ZhanghuiYangyin	Sheet:	29 of 32

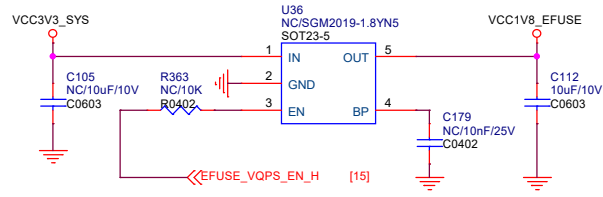


SIGNWAY

Project:	E473060		
File:	31.POWER&KEY Controller		
Date:	Friday, March 25, 2022	Rev:	A0
Designed by:	ZhangboKYanglin	Sheet:	31 of 32

eFUSE

Note: For eFUSE programming, can be removed if do not use eFUSE.



SIGNWAY			
Project:	E473060		
File:	32.eFUSE		
Date:	Friday, March 25, 2022	Rev:	A0
Designed by:	ZhanghuiYangin	Sheet:	32 of 32