

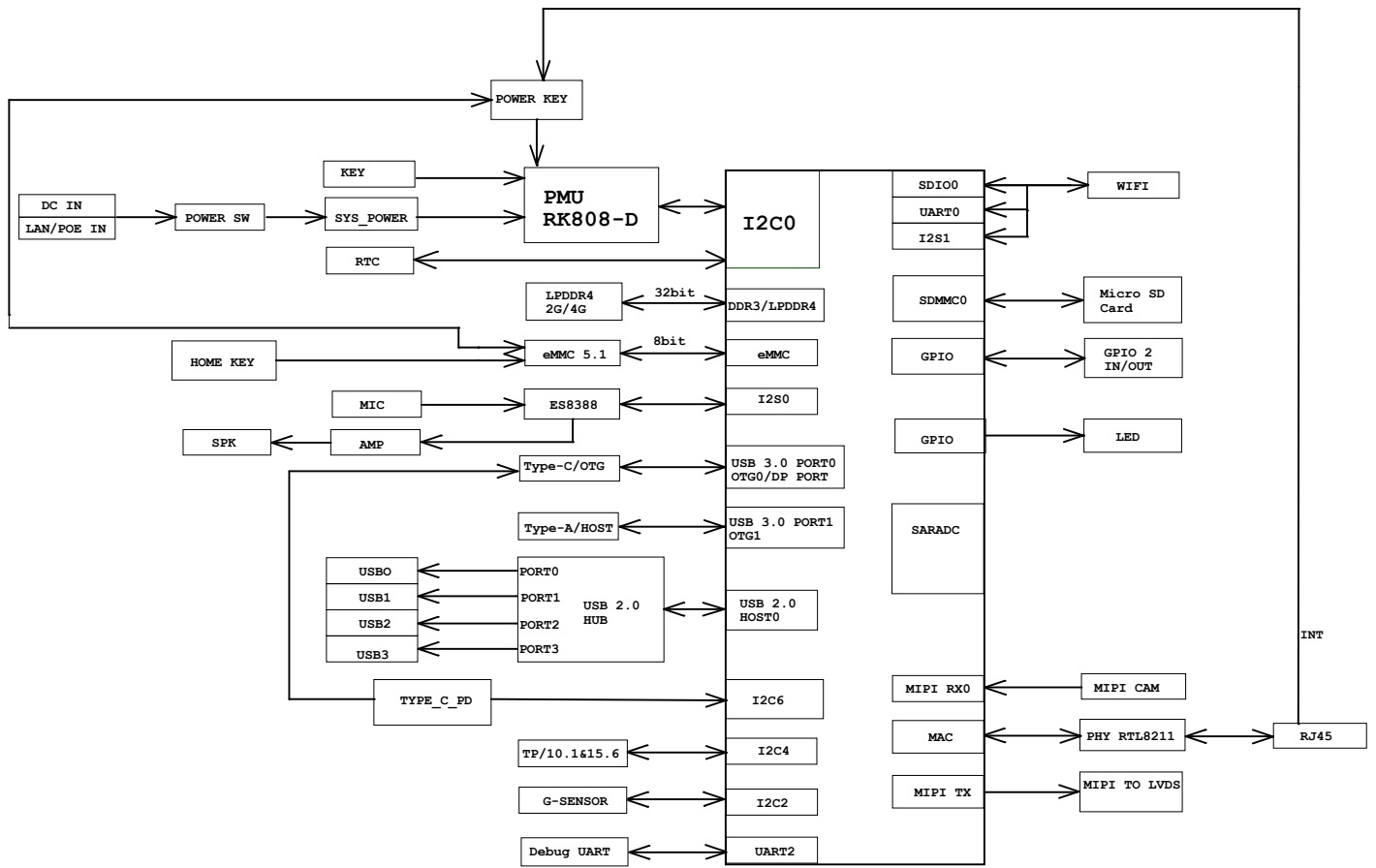
PCB MARK & LABEL

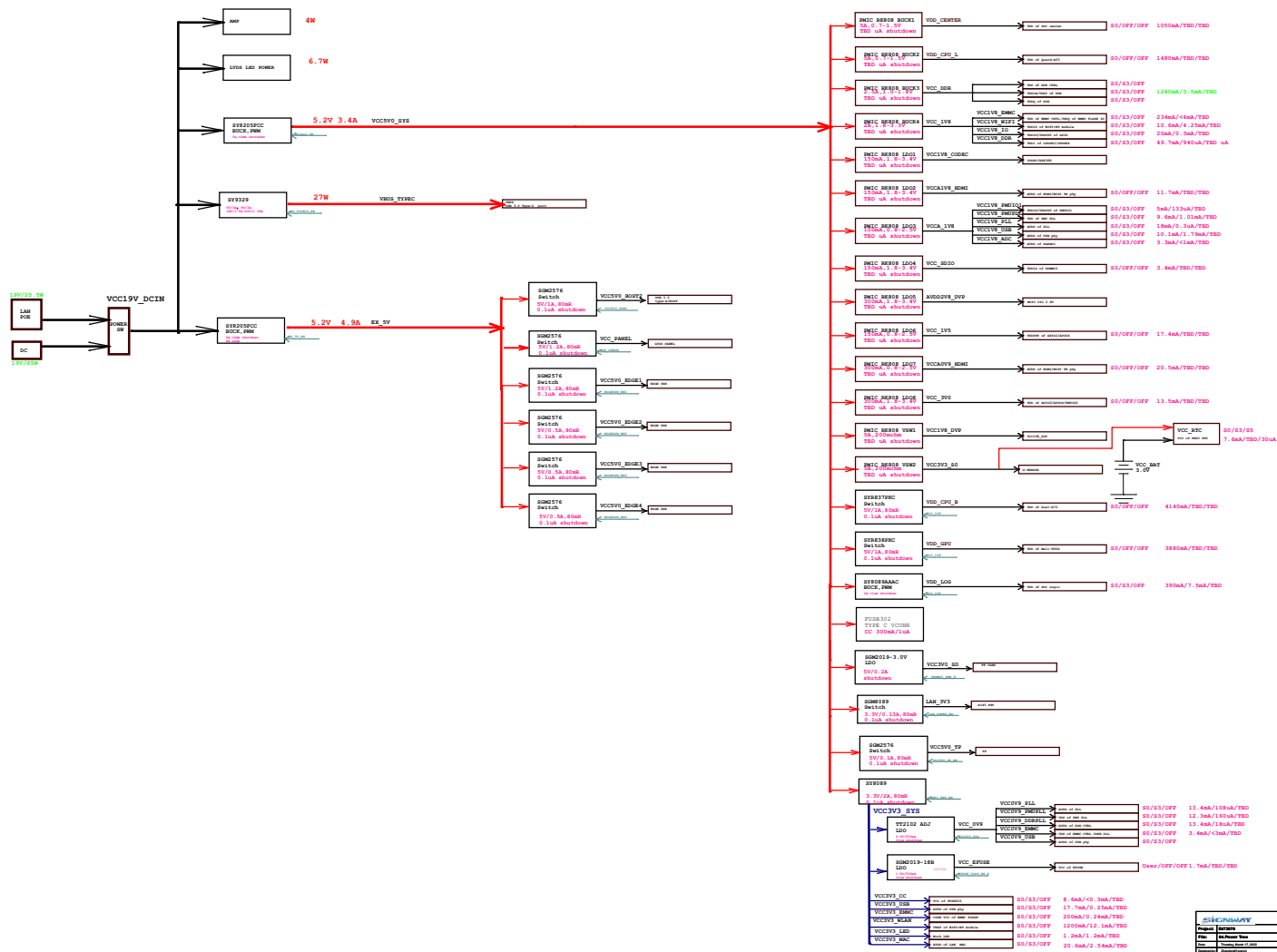
Heat Sink	
Optical Marks	T1 MARK T2 MARK T3 MARK T4 MARK T5 MARK T6 MARK MARK MARK MARK MARK MARK MARK MARK MARK
Label Outline	LOT Number H1 20mm X 10mm SN&MAC H2 10mm X 10mm
Silkscreen	PCB Name & Version ELO3399 ELO3399 ENG Version A20xxx A20xxx SMT DIP ROHS
Mounting Hole	H5 NC M3_5X7_0 H6 NC M3_5X7_0 H7 NC M4_5X7_0 H8 NC M3_5X7_0 H9 NC M3_5X7_0 H10 NC M3_5X7_0 H11 NC M4_5X7_0 H12 NC M3_5X7_0 H13 NC M3_5X7_0

SIGNWAY			
Project:	E472878		
File:	01.Mec		
Date:	Thursday, March 17, 2022	Rev:	A0
Designed by:	ZhangboKYanglin	Sheet:	1 of 32

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A1

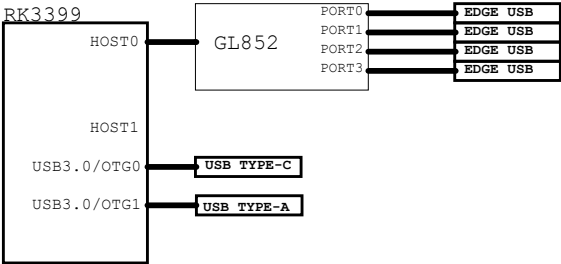




I2C MAP

Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
I2C0	GP101_B7/SP13_RXD/I2C0_SDA GP101_C0/SP13_TXD/I2C0_SCL	PMU102	I2C_SDA_PMIC I2C_SCL_PMIC	VCC_3V0	Rockchip RK808	0x1b	PMIC	100kHz,400KHz
					SY8377FNC	0x40	DC-DC Buck	100kHz,400KHz,3.4MHz
					SY8388FNC	0x41	DC-DC Buck	100kHz,400KHz,3.4MHz
					PT7C4337	0xd0,0xd1	RTC	100kHz
I2C1	GP104_A1/I2C1_SDA GP104_A2/I2C1_SCL	API05	I2C1_SDA_V18 I2C1_SCL_V18	VCC_V18	ESS388/1.8V	0x10,0x11	Audio codec	100kHz
					FUSB360HPK/1.8V	0x44,0x46	USB-TypeC Mux	100kHz
					GL852	0x2C	USB HUB	100kHz
					TC358775XBG	0x18,0x1F	LVDS Tx	100kHz
I2C2	GP102_A0/VOP_D0/CIF_D0/I2C2_SDA GP102_A1/VOP_D1/CIF_D1/I2C2_SCL	API02	I2C2_SDA_V18 I2C2_SCL_V18	VCC_V18	MMA8452Q/1.8V	0x1D,0x1E	G-SENSOR	100kHz,400KHz,
I2C3	GP104_C0/I2C3_SDA/UART2B_RX GP104_C1/I2C3_SCL/UART2B_TX	API04	I2C3_SDA I2C3_SCL	VCC_3V0	TP/3.3V	TD0	TP TOUCH	100kHz,400KHz,3.4MHz
I2C4	GP101_B3/I2C4_SDA GP101_B4/I2C4_SCL	PMU102	I2C4_SDA I2C4_SCL	VCC_3V0	SM201/3.0V	0xA0 0xE0	EEPROM	10kHz
I2C5	GP103_B2/MAC_RMII/I2C5_SDA GP103_B3/MAC_CLK/I2C5_SCL	API01	MAC USB					
I2C6	GP102_B1/SP12_RXD/CIF_HREF/I2C6_SDA GP102_B2/SP12_TXD/CIF_CLKIN/I2C6_SCL	API02	I2C6_SDA_V18 I2C6_SCL_V18	VCC_V18	SY9329	0XE2	PD	20kHz
I2C7	GP102_A7/VOP_D7/CIF_D7/I2C7_SDA GP102_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL	API02	I2C7_SDA_V18 I2C7_SCL_V18	VCC_V18	MIP1_CSI /1.8V			100kHz

USB MAP

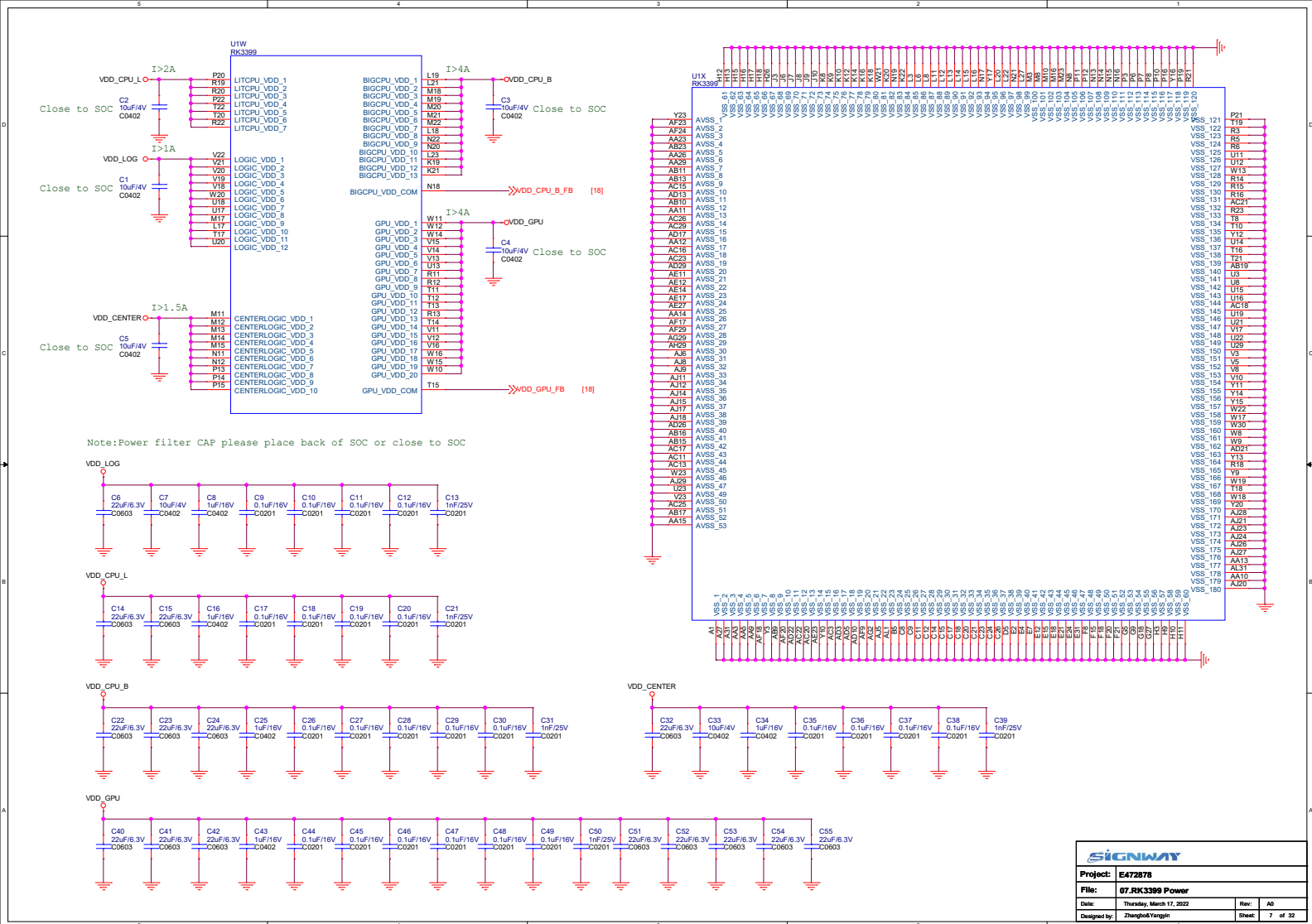


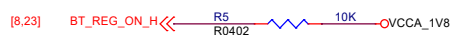
SIGNWAY			
Project:	E472878		
File:	05I2C&USB Map		
Date:	Thursday, March 17, 2022	Rev:	A0
Designed by:	ZhangshuYang	Sheet:	5 of 32

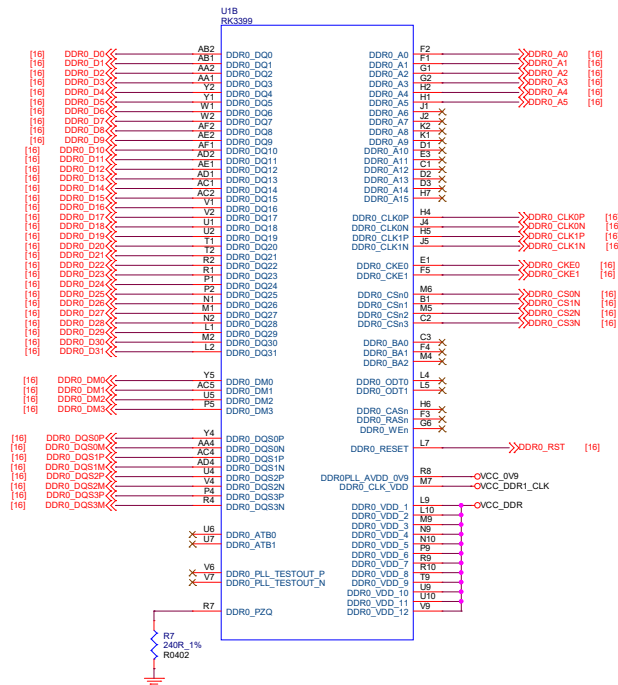
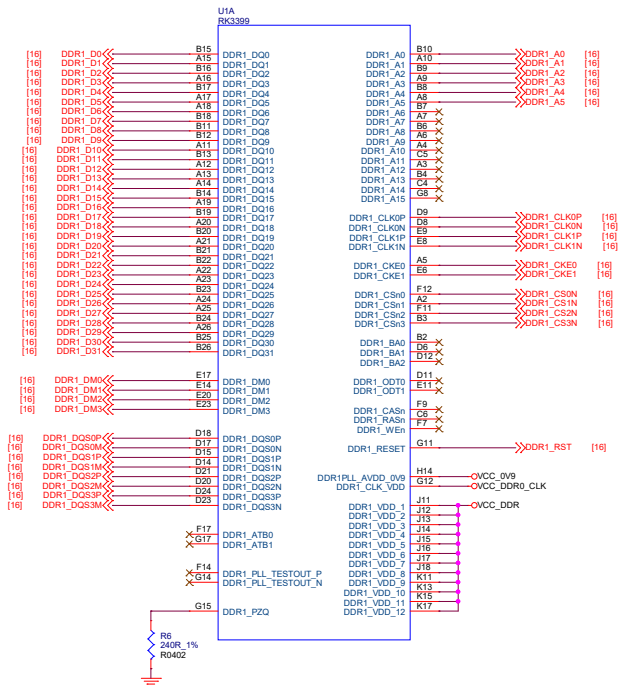
Power Domain Map

Part Port	Domain	Pin name in datasheet	I/O type	Power supply	Power source
Part C	PMUI01	pmui01_gpio0ab	1.8V only	VCCA_1V8	RK808-D VLD03
Part E	PMUI02/PART E	pmui830_gpiolabcd	3.0V	VCC_1V5	RK808-D Buck4 RK808-D VLD06
Part I	API01	gmac_gpio3abc	3.3V only	VCC_1V8 VCC3V3_LAN	RK808-D Buck4
Part L	API02	bt656_gpio2ab	1.8V	VCC_1V8	RK808-D VLD03
Part G	API03	wifi/bt_gpio2cd	1.8V only	VCC_1V8	RK808-D Buck4
Part K	API04	gpio1830_gpio4cd	1.8V 3.0V(Default)	VCC_1V5 VCC_3V0	RK808-D VLD06 RK808-D VLD08
Part J	API05/PART J	audio_gpio3d_gpio4a	VCC1V8_CODEC	VCC1V8_CODEC	RK808-D VLD01
Part F	SDMMC0	sdmmc_gpio4b	1.8V 3.0V(Default)	VCC_SDIO	RK808-D VLD04

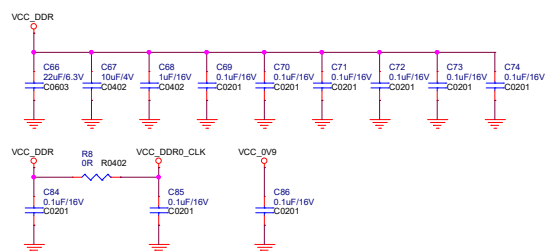
			
Project:	E472878		
File:	06.Power Domain Map		
Date:	Thursday, March 17, 2022	Rev:	A0
Designed by:	Zhanghui&Yangjin	Sheet:	6 of 32



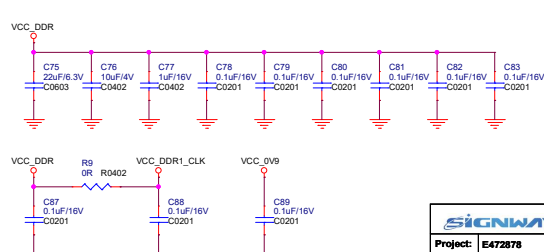




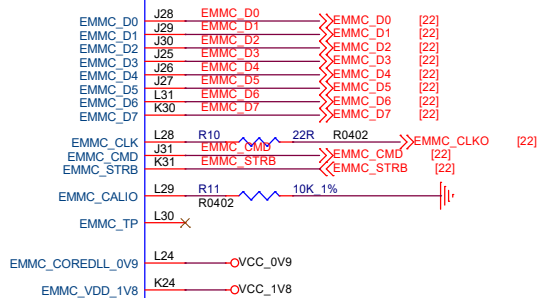
DDR FILTER Note:R10 cannot be deleted



DDR FILTER Note:R11 cannot be deleted

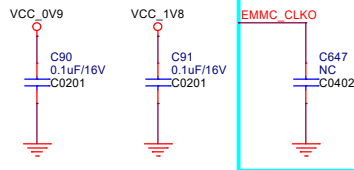


U1H
RK3399



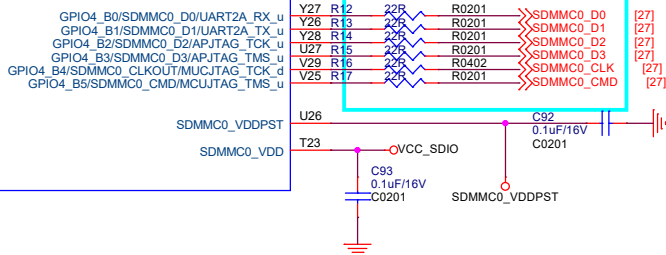
EMMC design rule:

- 1.Data[0:7], CMD and STRB signals routing parallel as a group, the skew between each other must be less than 100mils;
- 2.The Clock signal should be isolated with other signals by GND plane, the skew between data lines is less than 20ps;
- 3.Max trace length < 3.93 inches;
- 4.Trace impedance 50ohm+/-10%;
- 5.The distance between other signals follows the 3W rule;
- 6.R11 close to SOC;



修改点2-27
EMMC_CLK增加滤波电容，EMI认证200M频率超。
靠近R10 放置

U1F
RK3399



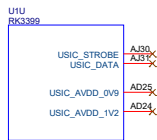
修改点2-19
SD卡电路布局优化，封装改0201

SDMMC design rule:

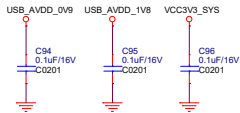
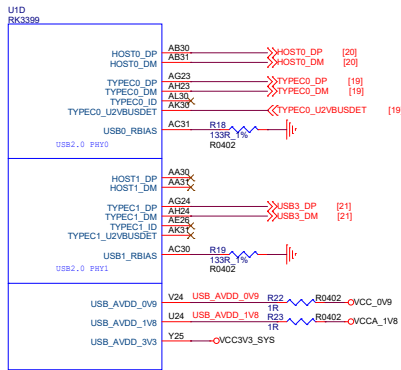
- 1.Data[0:7] and CMD signals routing parallel as a group, the skew between each other must be less than 100mils;
- 2.The Clock signal should be isolated with other signals by GND plane, the skew between data lines is less than 20ps;
- 3.Max trace length < 3.93 inches;
- 4.Trace impedance 50ohm+/-10%;
- 5.The distance between other signals follows the 3W rule;

SIGNWAY

Project:	E472878		
File:	10.RK3399 Flash&SDMMC Controler		
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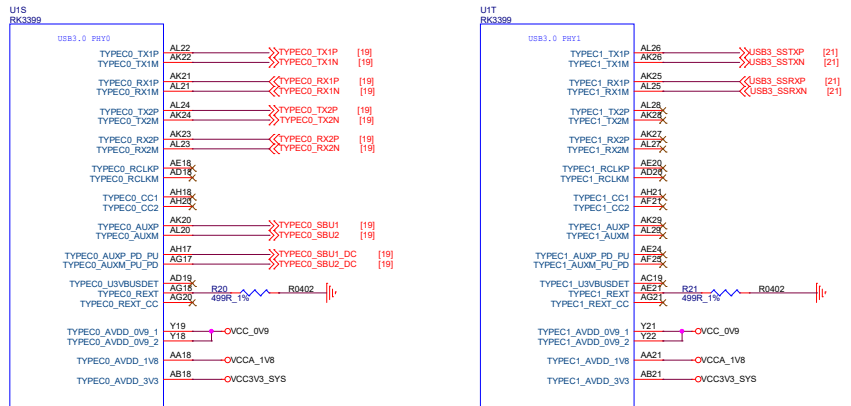


USB2.0



USB2.0 design rule:
1.Max intra-pair skew < 4 ps;
2.Max trace length < 6 inches;
3.Max allowed via < 4;
4.Trace impedance 90ohm+/-10%;
5.The distance between other signals follows the 3W rule;

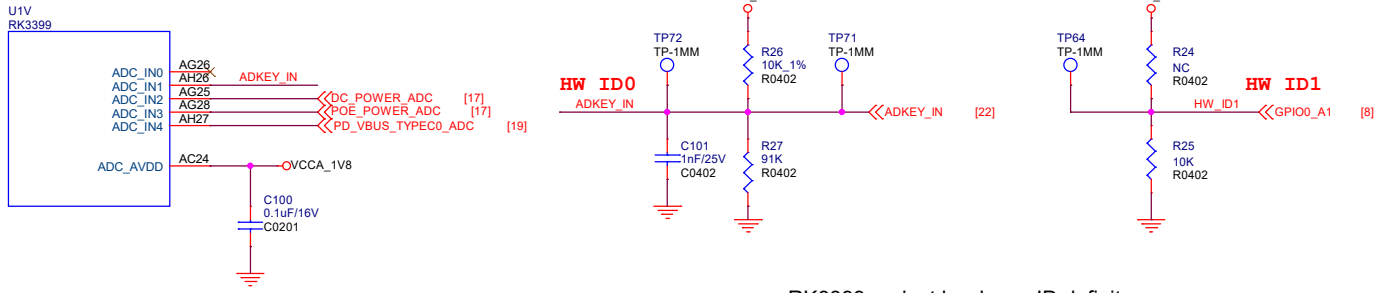
USB3.0



USB3.0 design rule:
1.Max intra-pair skew < 4 ps;
2.Max length skew between TX and RX < 1.6 ns;
3.Max trace length < 6 inches;
4.Max allowed via < 4;
5.Trace impedance 90ohm+/-10%;
6.The distance between other signals follows the 3W rule;

DP design rule:
1.Max intra-pair skew < 4 ps;
2.Max trace length < 6 inches;
3.Max allowed via < 4;
4.Trace impedance 90ohm+/-10%;
5.The distance between other signals follows the 3W rule;

SIGNWAY			
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File: 11.RK3399 USB3/USIC Controller			
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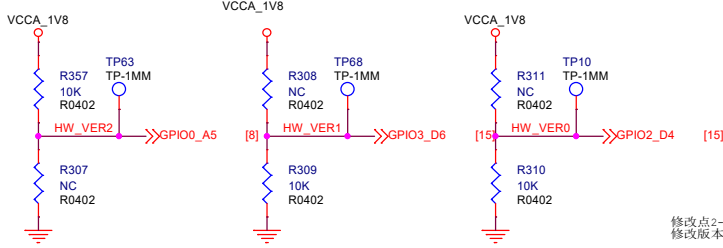


RK3399 project hardware ID definiton

ADC1 Function1: Hold on ZERO when AC plug in cold boot, enter Flash Image Mode.
 ADC1 Function2: Secondary definiton of product hardware ID.
 GPIO0_A1: Main definiton of of product hardware ID.

Seq.	GPIO0_A1	R27	ADC	HW ID	Date
01.	Low	NC	1.800V	E472673 (15.6)	March 02, 2020
02.	Low	91K	1.622V	E472828 (21.5)	
03.	Low	39K	1.433V	E473060 (10.1)	
04.	Low	22K	1.238V	E473261 (BACKPACK)	
05.	Low	13K	1.017V	E679524 (USB-c)	
06.	Low	9.1K	0.858V	TBD	
07.	Low	6.2K	0.689V	TBD	
08.	Low	3.9K	0.505V	TBD	
09.	High	NC	1.800V	TBD	
10.	High	91K	1.622V	TBD	
11.	High	39K	1.433V	TBD	
12.	High	22K	1.238V	TBD	
13.	High	13K	1.017V	TBD	
14.	High	9.1K	0.858V	TBD	
15.	High	6.2K	0.689V	TBD	
16.	High	3.9K	0.505V	TBD	

HW Version



修改点2-17
修改版本号

E472673 Hardware Version

Seq.	GPIO0_A5	GPIO3_D6	GPIO2_D4	HW Version	Date
01.	0	0	0	V1 (EVT)	March 26, 2020
02.	0	0	1	V2	TBD
03.	0	1	0	V3	TBD
04.	0	1	1	V4	TBD
05.	1	0	0	V5	20210816
06.	1	0	1	V6	TBD
07.	1	1	0	V7	TBD
08.	1	1	1	V8	TBD

SIGNWAY			
Project:	E472878		
File:	12.RK3399 SARADC/Key		
Date:	Thursday, March 17, 2022	Rev:	A0
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U1N
RK3399

HDMI_TX0P AK17
HDMI_TX0N AL17
HDMI_TX1P AK18
HDMI_TX1N AL18
HDMI_TX2P AK19
HDMI_TX2N AL19
HDMI_T0P AK16
HDMI_T0N AL16
HDMI_HPD AE15
HDMI_REXT AF15
HDMI_AVDD_0V9_1 AA16
HDMI_AVDD_0V9_2 AA17
HDMI_AVDD_1V8 AD16

HDMI design rule:

- 1.Max intra-pair skew < 4 ps;
- 2.Max length skew between clk and data < 80 ps;
- 3.Max trace length < 9.8 inchs;
- 4.Max allowed via < 4;
- 5.Trace impedance 100ohm+/-10%;
- 6.The distance between other signals follows the 3W rule;

U1M
RK3399

EDP_TX0P B29
EDP_TX0N A29
EDP_TX1P B30
EDP_TX1N A30
EDP_TX2P C30
EDP_TX2N C31
EDP_TX3P D30
EDP_TX3N D31
EDP_AUXP B28
EDP_AUXN A28
EDP_DC_TP G20
EDP_CLK24M_IN H21
EDP_REXT G21
EDP_AVDD_0V9 H20
EDP_AVDD_1V8_1 J19
EDP_AVDD_1V8_2 J20
EDP_AVSS_1 B31
EDP_AVSS_2 C28
EDP_AVSS_3 C29
EDP_AVSS_4 D28
EDP_AVSS_5 H19
EDP_AVSS_6 J21

eDP design rule:

- 1.Max intra-pair skew < 4 ps;
- 2.Max trace length < 6 inchs;
- 3.Max allowed via < 4;
- 4.Trace impedance 90ohm+/-10%;
- 5.The distance between other signals follows the 3W rule;

MIPI design rule:

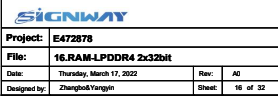
- 1.Max intra-pair skew < 4 ps;
- 2.Max length skew between clk and data < 7ps;
- 3.Max trace length < 7.2 inchs;
- 4.Max allowed via < 4;
- 5.Trace impedance 100ohm+/-10%;
- 6.The distance between other signals follows the 3W rule;

U1Q
RK3399

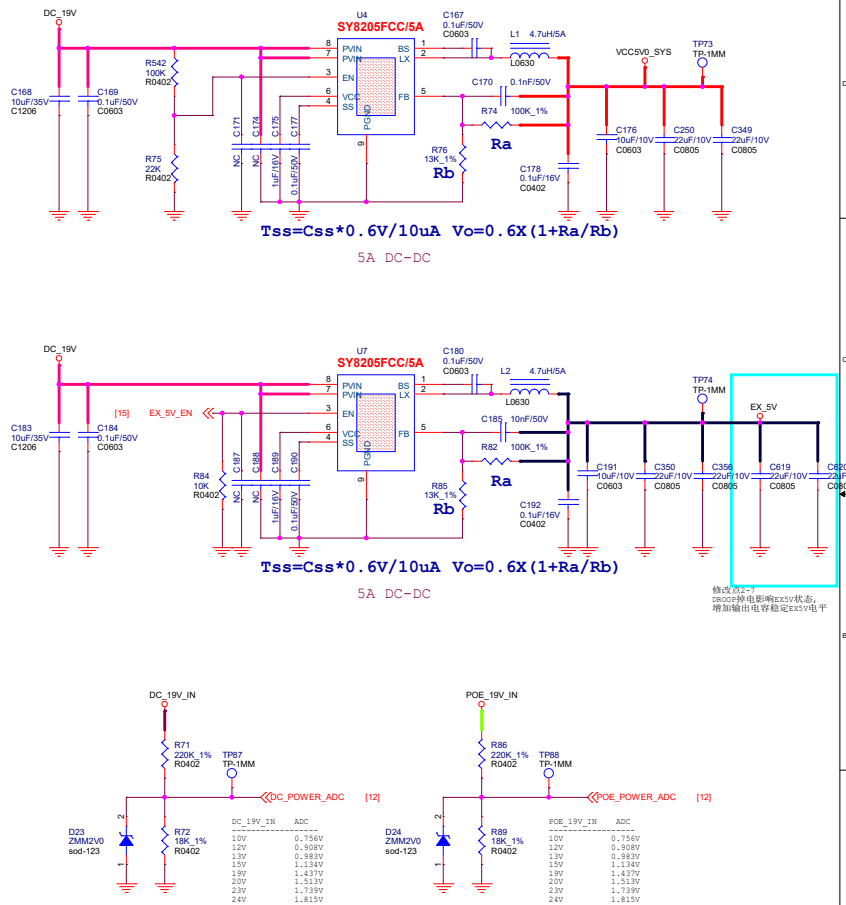
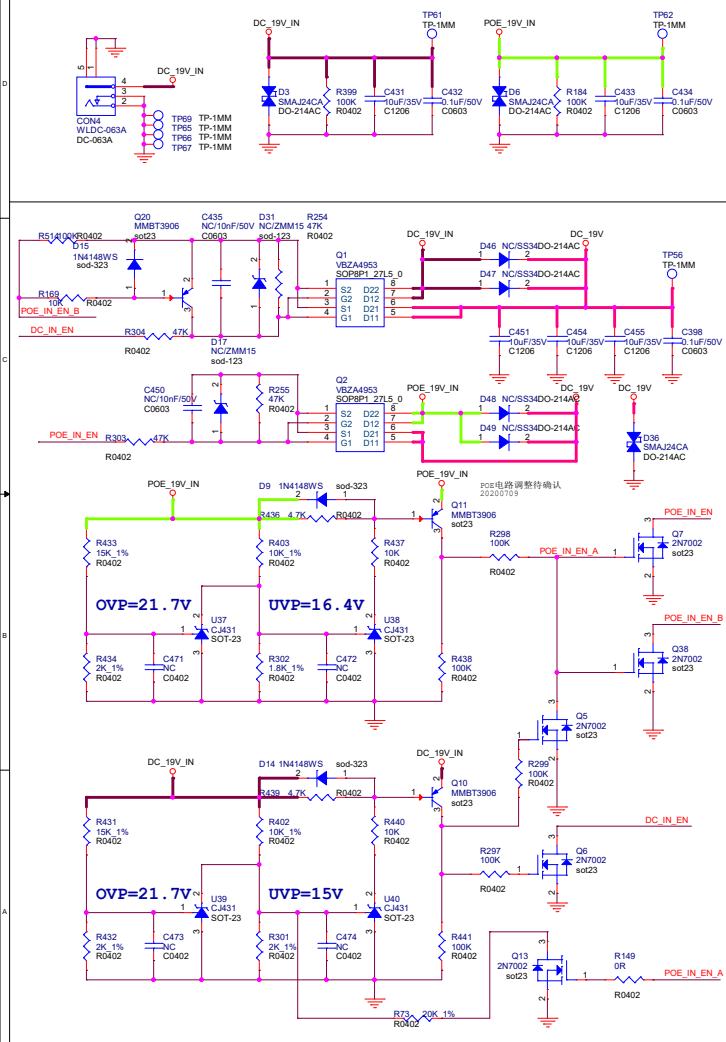
MIPI_TX0_D0P AG15
MIPI_TX0_D0N AH15
MIPI_TX0_D1P AG14
MIPI_TX0_D1N AH14
MIPI_TX0_CLKP AG12
MIPI_TX0_CLKN AH12
MIPI_TX0_D2P AG11
MIPI_TX0_D2N AH11
MIPI_TX0_D3P AG9
MIPI_TX0_D3N AH9
MIPI_TX0_REXT AF12
MIPI_TX0_AVDD_1V8 AB12
R463 4.02K_1%
R0402
C111 0.1uF/16V
C0201
VCCA1V8_HDMI

SIGNWAY

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File:	14.RK3399 Display Interface		
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DC IN&SYSTEM Power



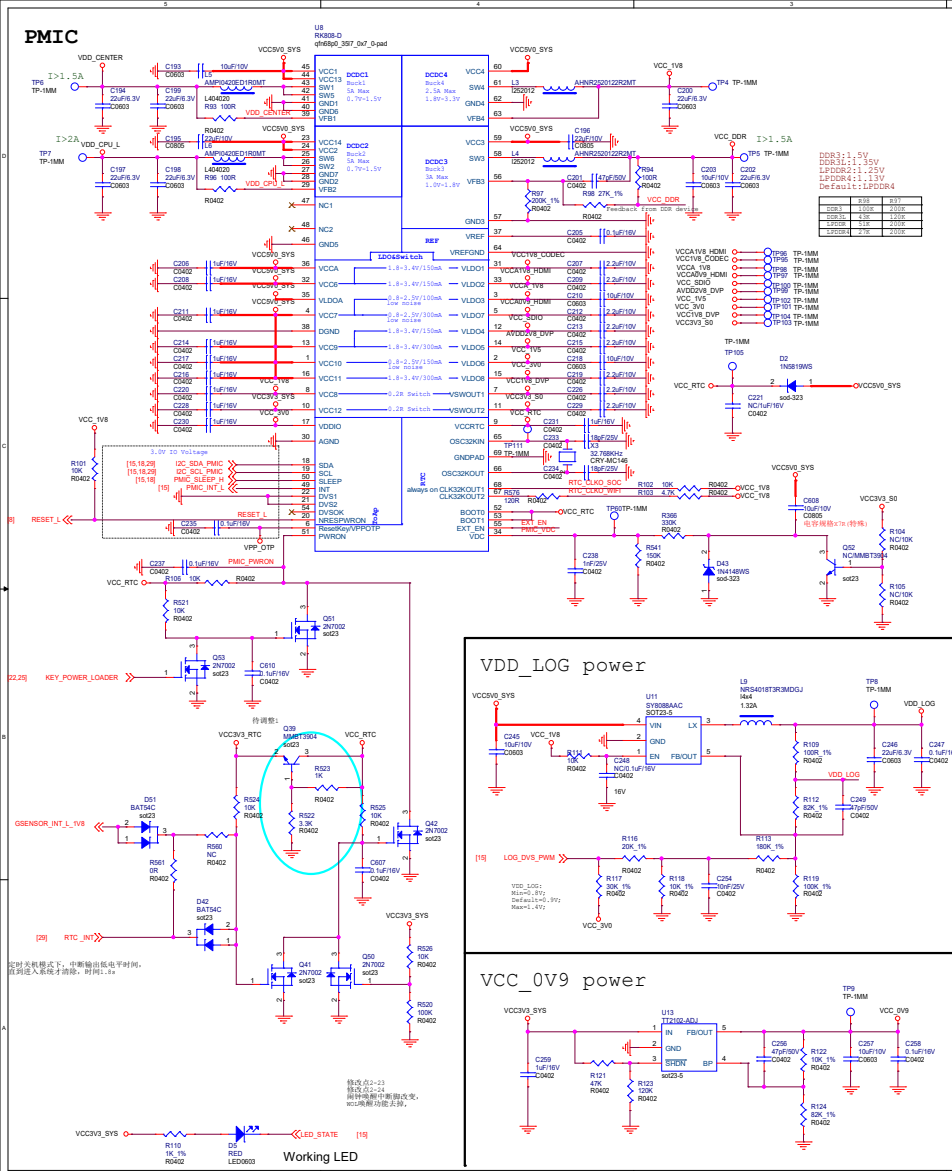
[12]

D24
ZMM2V0
sod-123

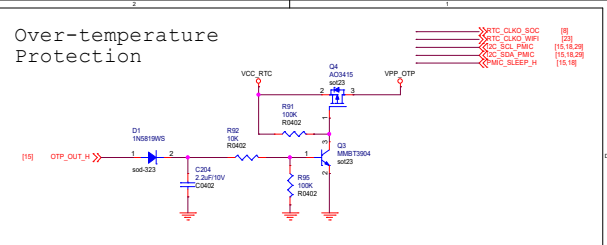
R89
18K_1%
R0402

PCE 19V_IN
10V
12V
13V
15V
19V
20V
23V

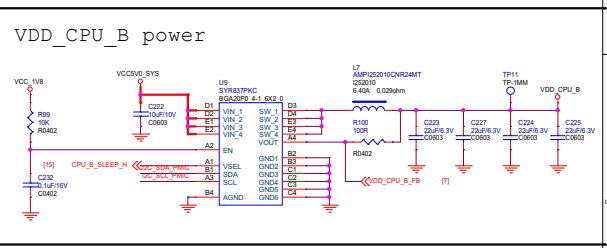
PMIC



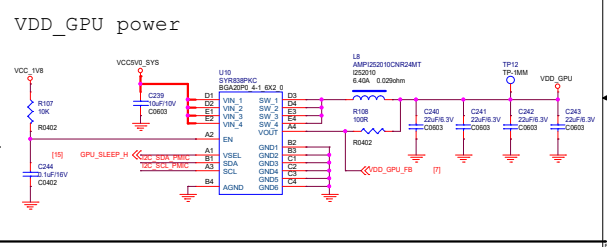
Over-temperature
Protection



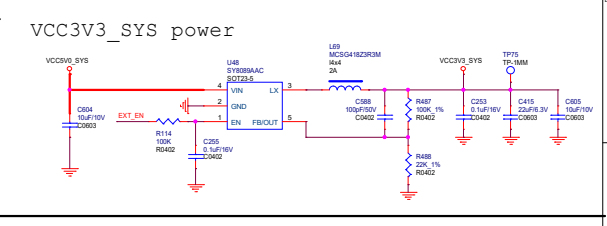
VDD CPU B power



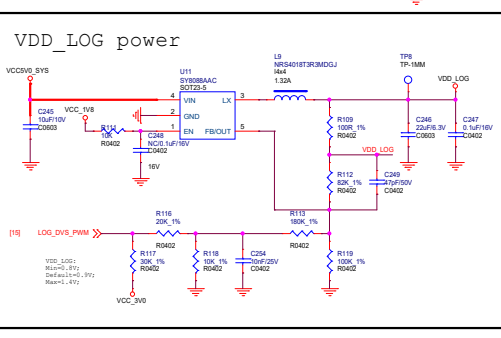
VDD GPU power



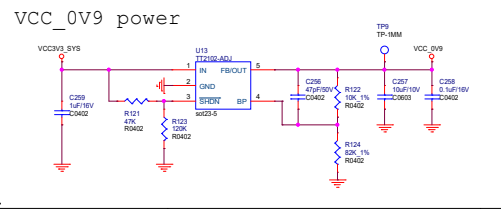
```
VCC3V3 SYS power
```



VDD LOG power

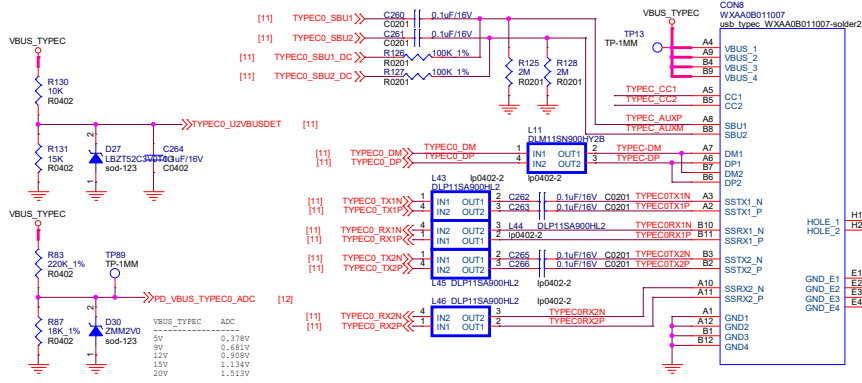


```
VCC 0V9 power
```

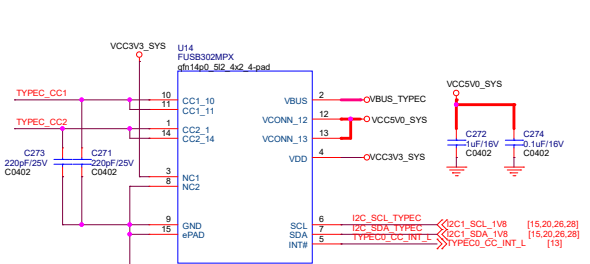


			
Project:	E472878		
File:	18.Power-PMIC RK808-D		
Date:	Thursday, March 17, 2022	Rev:	AD
Designed by:	ZhangboYiyanjin	Sheet:	18 of 32

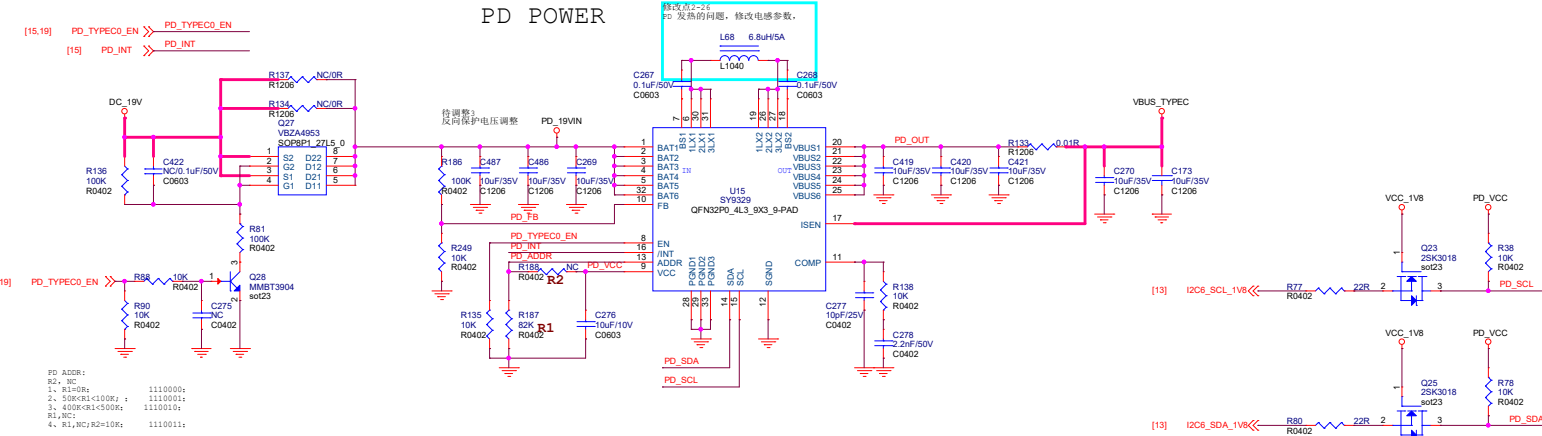
USB Type-C port



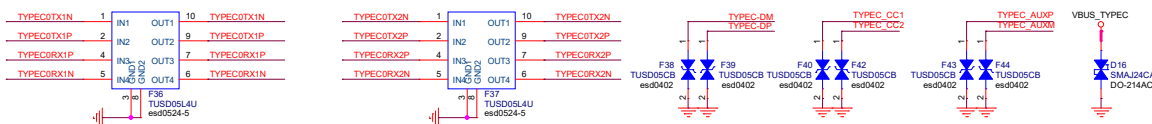
CC CTRL



PD POWER

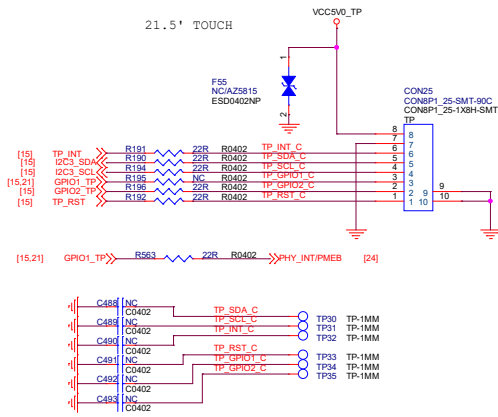


ESD

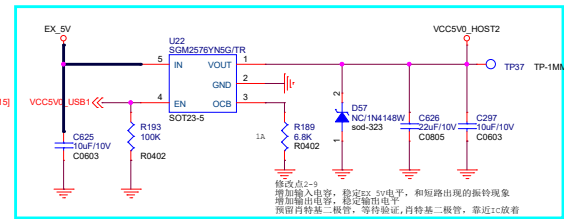
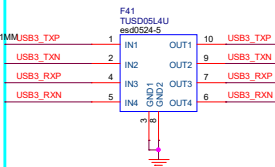
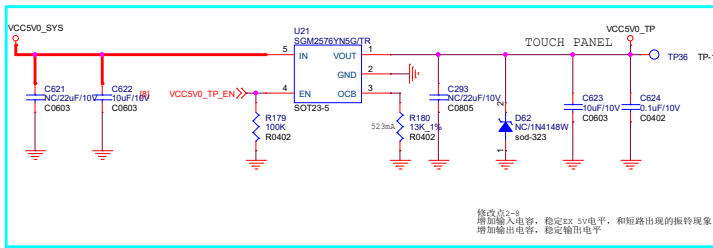
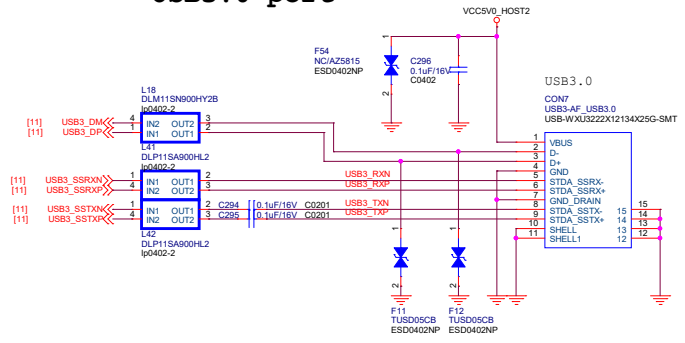


			
Project:	E472878		
File:	19.TYPE-C		
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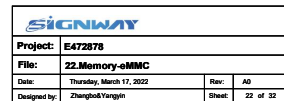
Touch Panel

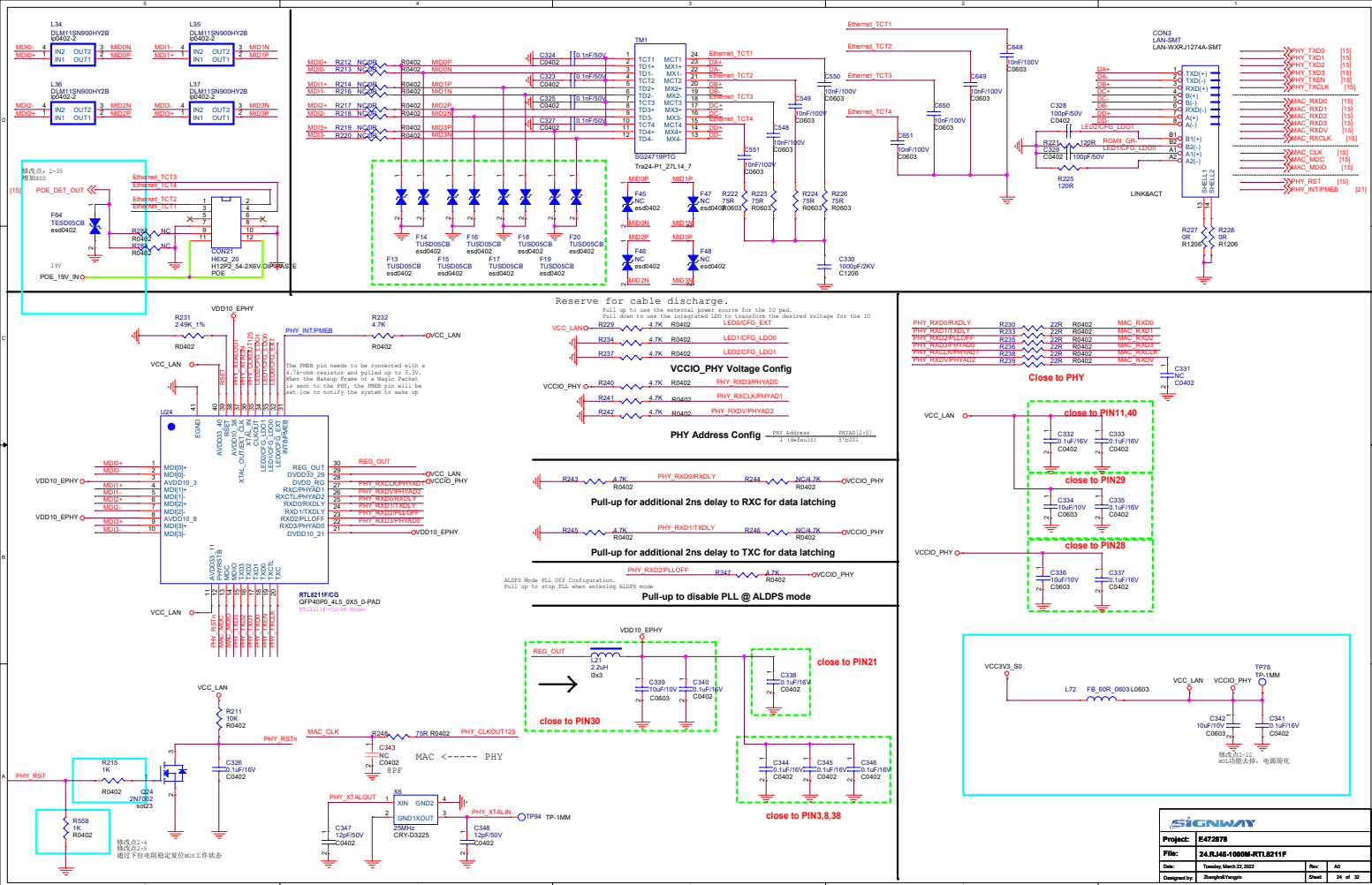


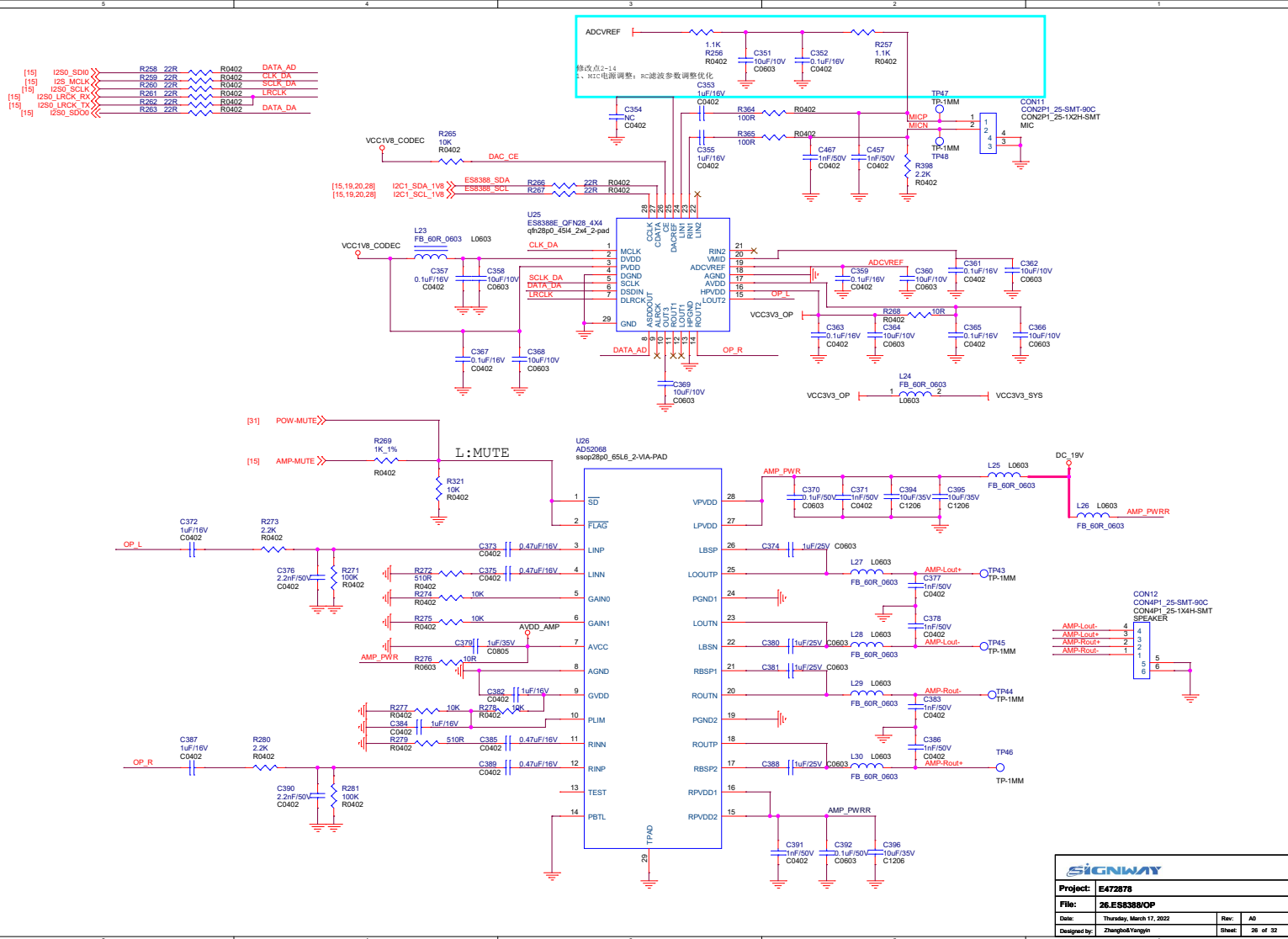
USB3.0 port



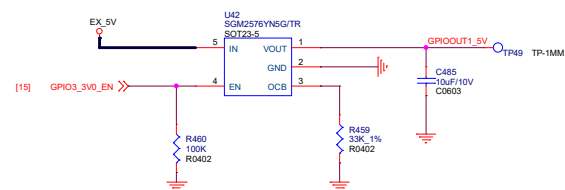
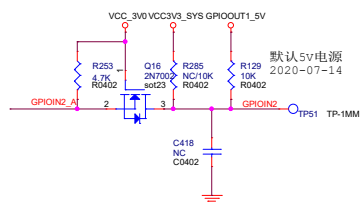
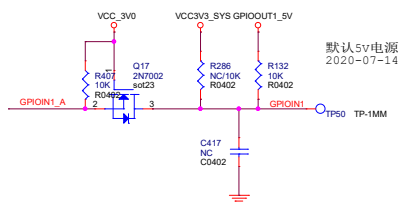
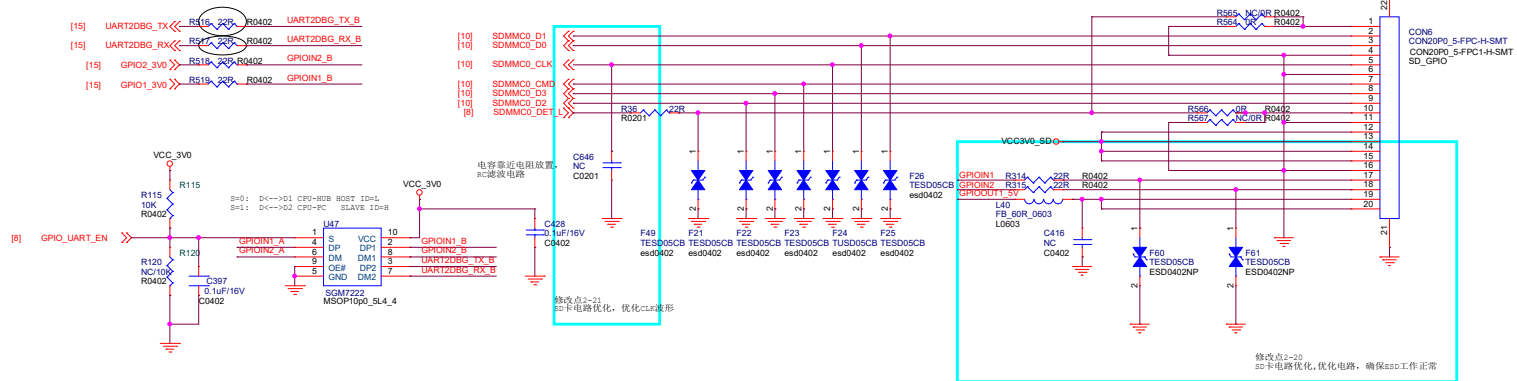
SIGNWAY			
Project: E472878			
File: 21.USB 3.0.HOST & TP			
Date: Thursday, March 17, 2022	Rev: A0		
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[illegible]

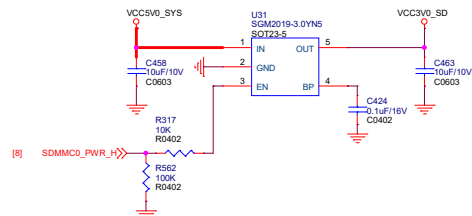




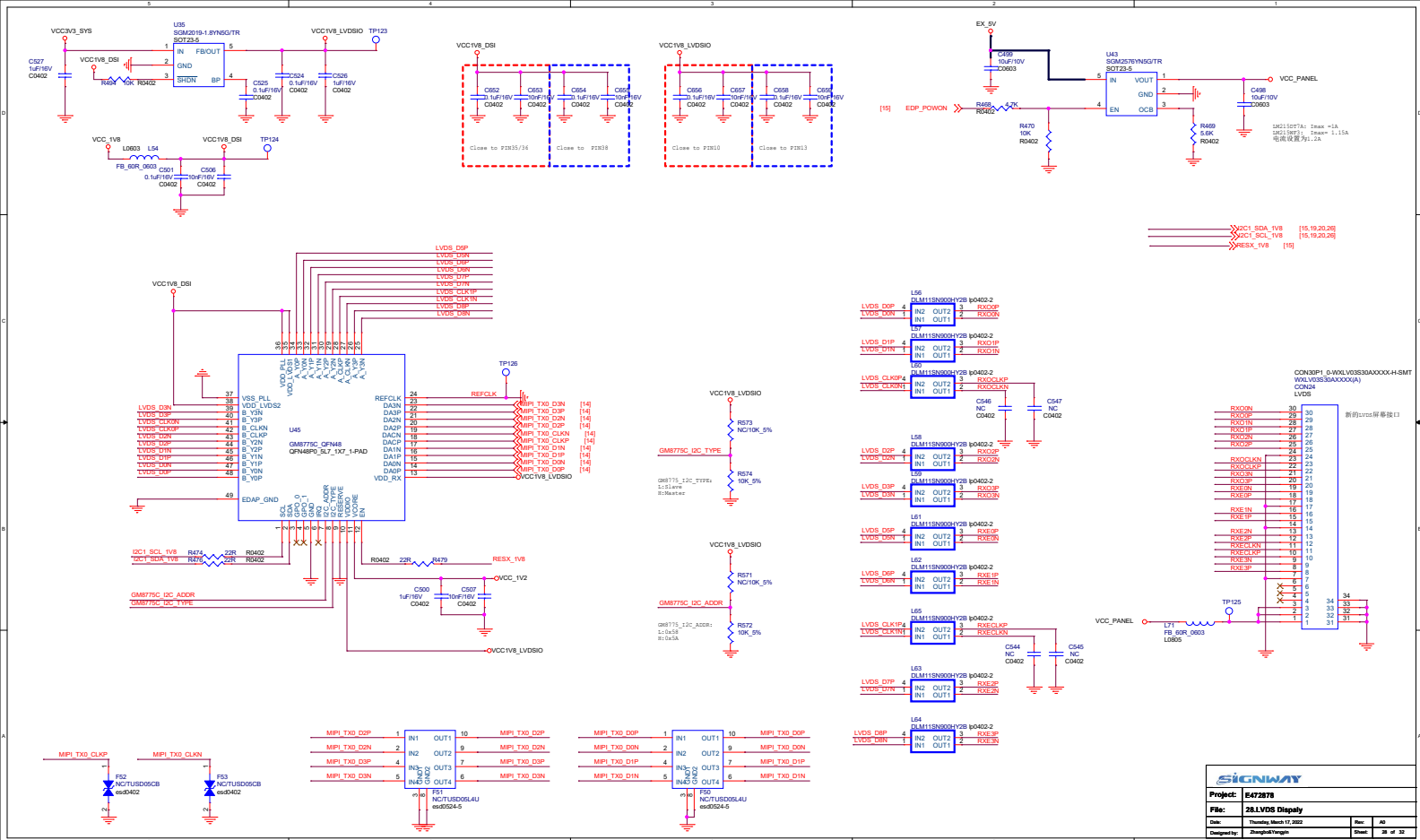
TF CARD



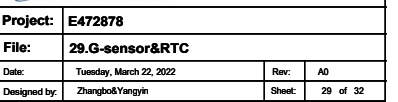
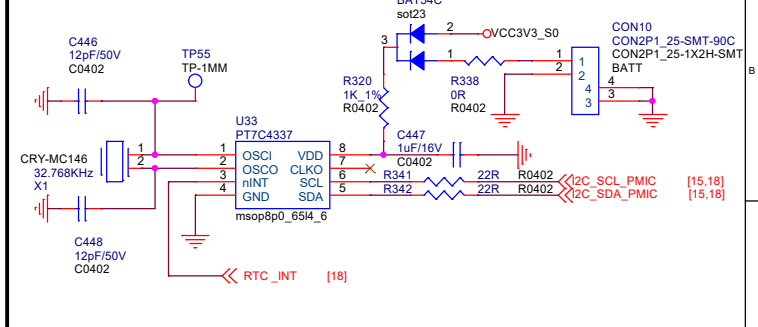
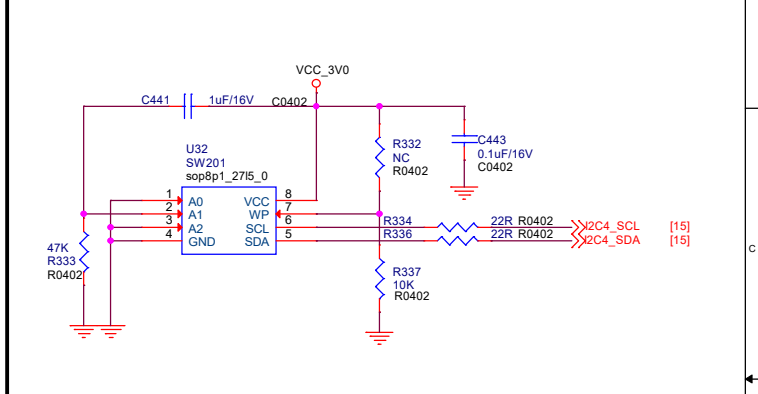
VCC3V0_SD power

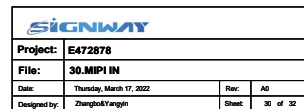


			
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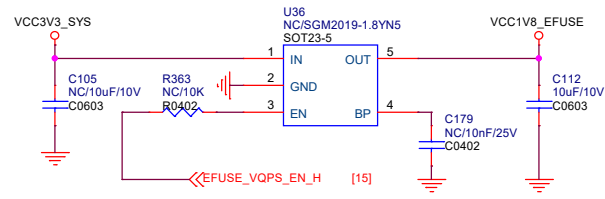
The MMA8452Q's standard slave address is a choice between the two sequential addresses 0011100 and 0011101. The selection is made by the high and low logic level of the SA0 (pin 7) input respectively. The slave addresses are factory programmed and alternate addresses are available at customer request.





eFUSE

Note: For eFUSE programming, can be removed if do not use eFUSE.



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