



FE910C04

Hardware Design Guide

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1 Applicability Table

Table 1: Applicability Table

Products
FE910C04-WW
FE910C04-WWD

2 Introduction

2.1 Scope

This document introduces the Telit FE910C04 module and presents possible and recommended hardware solutions for the development of a product based on the FE910C04 module. All the features and solutions described in this document are applicable to all FE910C04 variants, where “FE910C04” refers to the variants listed in the applicability table.

Note: FE910C04 refers to all modules listed in the Applicability Table.

This document covers all the basic functions of a wireless module; it cannot include every hardware solution or every product that can be designed. Where the suggested hardware configurations are not to be considered mandatory, the information provided should be used as a guide and starting point to successfully develop the product with the Telit FE910C04 module.

Note: The integration of the LTE/5G FE910C04 cellular module within a user application must be done according to the design rules described in this manual.

2.2 Audience

This document is intended for system integrators that are using the Telit FE910C04 module in their products.

2.3 Contact Information, Support

For technical support and general questions, e-mail:

- TS-EMEA@telit.com
- TS-AMERICAS@telit.com
- TS-APAC@telit.com
- TS-SRD@telit.com
- TS-ONEEDGE@telit.com

Alternatively, use: <https://www.telit.com/contact-us/>

For Product information and technical documents, visit: <https://www.telit.com>

2.4 Conventions

Note: Provide advice and suggestions that may be useful when integrating the module.

Danger: This information MUST be followed, or catastrophic equipment failure or personal injury may occur.

Warning: Alerts the user on important steps about the module integration.

All dates are in ISO 8601 format, that is YYYY-MM-DD.

2.5 Terms and Conditions

Refer to <https://www.telit.com/hardware-terms-conditions/>.

2.6 Disclaimer

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3 General Product Description

3.1 Overview

The FE910C04 is an industrial-grade, LTE Cat4 / 5G RedCap module series ideal for IoT applications that need 5G mid-speed data and voice transmission. The embedded GNSS receiver makes the FE910C04 ideal for all-in-one tracking use cases in which more precise, faster-refreshing, satellite-based positioning and navigation must complement cellular-based positioning.

FE910C04 is available in hardware variants as listed in Applicability Table. For differences in the designated RF band sets – refer to Section 3.2.Bands Variants.

Note: (EN) The integration of the FE910C04 cellular module within user application shall be done according to the design rules described in this manual.

(IT) L'integrazione del modulo cellulare FE910C04 all'interno dell'applicazione dell'utente dovrà rispettare le indicazioni progettuali descritte in questo manuale.

(DE) Die Integration des FE910C04 Mobilfunk-Moduls in ein Gerät muß gemäß der in diesem Dokument beschriebenen Konstruktionsregeln erfolgen.

(SL) Integracija FE910C04 modula v uporabniški aplikaciji bo morala upoštevati projektna navodila, opisana v tem priročniku.

(SP) La utilización del modulo FE910C04 debe ser conforme a los usos para los cuales ha sido diseñado descritos en este manual del usuario.

(FR) L'intégration du module cellulaire FE910C04 dans l'application de l'utilisateur sera faite selon les règles de conception décrites dans ce manuel.

(HE) ייעשה המשתמש יישום בתוך FE910C04 הסלולרי המודול של השילוב זה במדריך המתוארים התכנון לכללי בהתאם.

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3.2 Product Variants and Frequency Bands

The operating frequencies in 5G and LTE modes conform to 3GPP specifications. Following table summarizes all region variants within the FE910C04 family, showing the band sets supported in each variant.

Table 2: Product Variants and their Frequency Bands

Product	LTE Cat4	5G FR1 RedCap	GNSS	Region
FE910C04-WW FE910C04-WWD	B1, B2, B3, B4, B5, B7, B8, B12, B13, B14, B17, B18, B19, B20, B25, B26, B28, B30, B34, B38, B39, B40, B41, B42, B43, B48, B66, B70, B71, B106	n1, n2, n3, n5, n7, n8, n12, n13, n14, n18, n20, n25, n26, n28, n30, n38, n40, n41, n48, n66, n70, n71, n77, n78, n79	L1/L5	Worldwide

For details information about frequencies and bands, refer to the [RF Section](#).

Note: Cellular technologies and frequency bands that are enabled may vary based on the firmware version and firmware configuration used.

3.3 Target Market

FE910C04 can be used for rugged industrial applications where tamper-resistance, confidentiality, integrity, and authenticity of end-user information are essential. Target applications may include:

- Video surveillance / security
- Routers/Gateways
- EV Charging infrastructure
- Machine and agricultural telematics

3.4 Main Features

The FE910C04 series of cellular modules features a 5G NR Redcap, LTE and multi-RAT modules together with an on-chip powerful application processor and a rich set of interfaces.

The main functions and features are listed below:

Table 3: Main Features

Function	Features
Modem	3GPP Release 17 NR RedCap, SA Sub6 20MHz • Peak data rates (NR): 223Mbps DL / 123Mbps UL Release 16 LTE standalone only and Cat4 support • Peak data rates (LTE): 200*Mbps DL / 105*Mbps UL *For Peak data rates, 256QAM needs network support Support for SIM profile switching. Regional variants with optimal choice of RF bands for worldwide coverage of countries and MNOs State-of-the-art GNSS solution with GPS/GLONSS/BeiDou/Galileo/QZSS receiver
Two USIM ports – dual voltage	• Class B and Class C support • Hot swap support • Clock rates up to 5 MHz
Application processor	Application processor to run customer application code • ARM Cortex-A7 up to 1.7 GHz 2Gbit NAND Flash + 2Gbit LPDDR2 533 MHz MCP
Interfaces	Rich set of interfaces, including:

Function	Features
	• USB2.0 • UART • I2C • I2S • USIM x2 • SGMII – 1.25Gbps • PCIe Gen 2.0 x 1-lane • SDIO • GPIOs • Antenna ports
Form factor	Form factor (28.2x28.2mm), accommodating the multiple RF bands in each region variant
Environment and quality requirements	The entire module is designed and qualified by Telit for satisfying the environment and quality requirements.
Single supply module	The module generates all its internal supply voltages.
RTC	No dedicated RTC supply, RTC is supplied by VBATT
Operating temperature	Range -40 °C to +85 °C (conditions as defined in Section 3.7.1 Temperature Range)

3.5 Block Diagram

Figure below shows an overview of the internal architecture of the FE910C04 module. It includes the following sub-functions:

- Application processor and Modem subsystem with their external interfaces. These two functions are contained in a single SOC.
- RF front end and antenna ports.
- Rich IO interfaces. Depending on which FE910C04 software features are enabled, some of its exported interfaces due to multiplexing may be used internally and therefore may not be usable by the application.

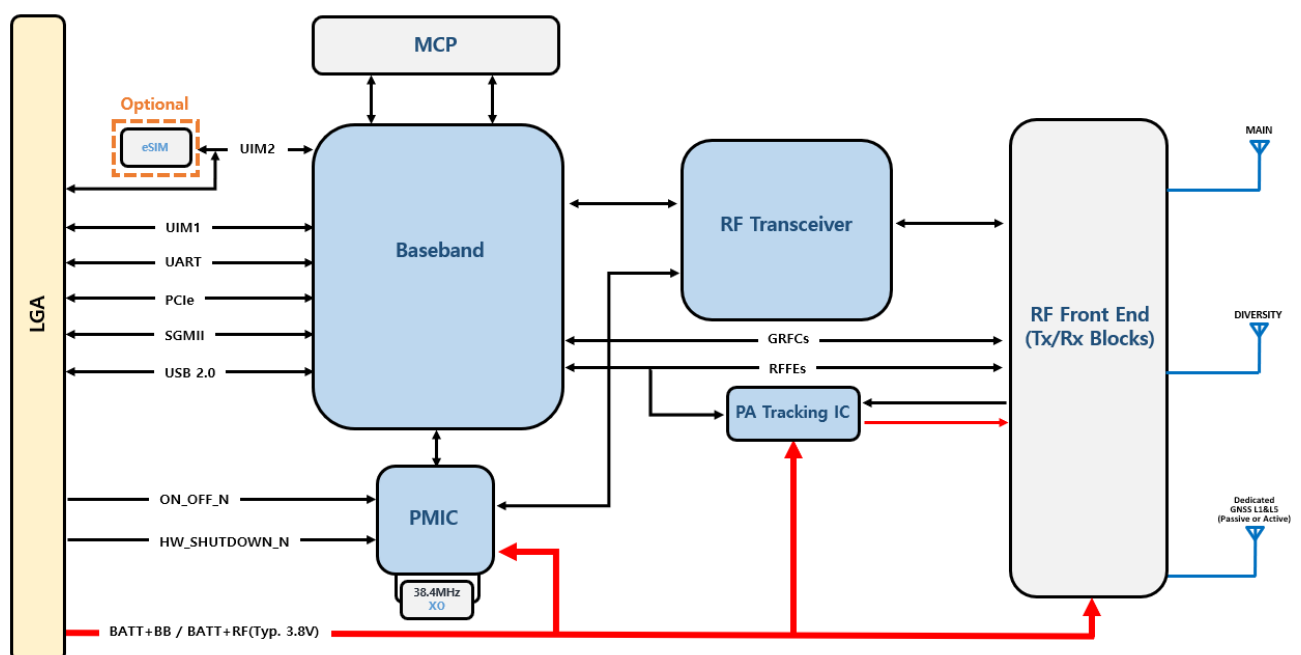


Figure 1: Block Diagram

3.6 Mechanical Specifications

3.6.1 Dimensions

The overall dimensions of FE910C04 are:

- Length: 28.2 mm
- Width: 28.2 mm
- Thickness: 2.4 mm

3.6.2 Weight

The nominal weight of the FE910C04 is 5.0 grams.

3.7 Environmental Requirements

3.7.1 Temperature Range

Table 4: Temperature Range

Mode	Temperature	Note
Operating Temperature Range	-20°C ~ +55°C	The module is fully functional(*) in all the temperature range and it fully meets the 3GPP specifications.
	-40°C ~ +85°C	The module is fully functional (*) in all the temperature range, might slightly deviate from the 3GPP specifications.
Storage and non-operating Temperature Range	-40°C ~ +90°C	The module is not powered and not connected to power supply

Note: (*) Functional: if applicable, the module is able to make and receive voice calls, data calls, send and receive SMS and data traffic.

Note: RED compliance from -30°C to +75°C

3.7.2 RoHS Compliance

As a part of the Telit corporate policy of environmental protection, the FE910C04 products comply with the RoHS (Restriction of Hazardous Substances) directive of the European Union (EU directive 2011/65/EU).

4 Pins Allocation

4.1 Pin-out

Table 5: Pin-out Information

Pin	Signal	I/O	Function	Type	Comment
USB HS 2.0 Communication Port					
B15	USB_D+	I/O	USB 2.0 differential Data (+)		
C15	USB_D-	I/O	USB 2.0 differential Data (-)		
A13	USB_VBUS	AI	Power sense for the internal USB transceiver	Power	
A14	USB_ID	AI	USB ID		
Asynchronous UART					
N15	C103/TXD	I	Serial data input (TXD) from DTE	1.8V	Connect to the TXD line.
M15	C104/RXD	O	Serial data output to DTE	1.8V	Connect to the RXD line.
P15	C106/CTS	O	Output for Clear to send signal (CTS) to DTE	1.8V	Connect to the CTS line.
L14	C105/RTS	I	Input for Request to send signal (RTS) from DTE	1.8V	Connect to the RTS line.
M14	C108/DTR	I	Input for Data Terminal Ready (DTR) from DTE	1.8V	
N14	C109/DCD	O	Output for Data Carrier Detect (DCD) to DTE	1.8V	
P14	C107/DSR	O	Output for Data Set Ready (DSR) to DTE	1.8V	
R14	C125/RING	O	Output for Ring Indication (RI) to DTE	1.8V	
Bluetooth UART					
F3	TXD1	I	Bluetooth UART Transmit	1.8V	Connect to the TXD line.
H3	RXD1	O	Bluetooth UART Receive	1.8V	Connect to the RXD line.
J3	CTS1	O	Bluetooth UART Clear to Send	1.8V	Connect to the CTS line.
K4	RTS1	I	Bluetooth UART Request to Send	1.8V	Connect to the RTS line.
COEX UART					
M8	WCI_TX	O	Wireless coexistence interface TXD	1.8V	
M9	WCI_RX	I	Wireless coexistence interface RXD	1.8V	
Debug UART					
D15	DEBUG_UART_TXD	O	Debug UART transmit	1.8V	
E15	DEBUG_UART_RXD	I	Debug UART receive	1.8V	
SIM Card Interface 1					
A6	SIMCLK1	O	External SIM 1 signal – Clock	1.8/2.95V	
A7	SIMRST1	O	External SIM 1 signal – Reset	1.8/2.95V	

Pin	Signal	I/O	Function	Type	Comment
A5	SIMIO1	I/O	External SIM 1 signal - Data I/O	1.8/2.95V	Internal PU (20 KΩ)
A4	SIMIN1	I	External SIM 1 signal - Presence	1.8V	Internal PU (100 KΩ)
A3	SIMVCC1	-	External SIM 1 signal – Power supply for SIM 1	1.8/2.95V	
SIM Card Interface 2					
C1	SIMCLK2	O	External SIM 2 signal – Clock	1.8/2.95V	
D1	SIMRST2	O	External SIM 2 signal – Reset	1.8/2.95V	
C2	SIMIO2	I/O	External SIM 2 signal – Data I/O	1.8/2.95V	Internal PU (20 KΩ)
G4	SIMIN2	I	External SIM 2 signal – Presence	1.8V	Internal PU (100 KΩ)
D2	SIMVCC2	-	External SIM 2 signal – Power supply for SIM 2	1.8/2.95V	
Digital Voice Interface (DVI)					
B9	DVI_WAO	O	Digital Voice interface (WAO master output)	1.8V	
B6	DVI_RX	I	Digital Voice interface (Rx)	1.8V	
B7	DVI_TX	O	Digital Voice interface (Tx)	1.8V	
B8	DVI_CLK	O	Digital Voice interface (CLK master output)	1.8V	
B12	REF_CLK	O	Reference clock for external Codec (Audio Master clock)	1.8V	
General Purpose Digital I/O					
C8	GPIO_1	I/O	GPIO_1 / STAT_LED	1.8V	Default STAT_LED
C9	GPIO_2	I/O	GPIO_2	1.8V	
C10	GPIO_3	I/O	GPIO_3	1.8V	
C11	GPIO_4	I/O	GPIO_4	1.8V	
B14	GPIO_5	I/O	GPIO_5	1.8V	
C12	GPIO_6	I/O	GPIO_6	1.8V	
C13	GPIO_7	I/O	GPIO_7	1.8V	
K15	GPIO_8	I/O	GPIO_8 / SW_RDY	1.8V	Default SW_RDY
L15	GPIO_9	I/O	GPIO_9	1.8V	
G15	GPIO_10	I/O	GPIO_10	1.8V	
RF Section					
K1	Ant_Main	I/O	Primary antenna	RF	50 Ω impedance
F1	Ant_Div	I/O	Secondary antenna	RF	50 Ω impedance
GNSS Section					
R9	ANT_GNSS	I	GNSS antenna	RF	50 Ω impedance
R7	GNSS_LNA_EN	O	Enables the external regulator for GNSS LNA	1.8V	

Pin	Signal	I/O	Function	Type	Comment
N9	GNSS_SYNC	O	GNSS 1PPS signal	1.8V	
SGMII Interface					
D5	SGMII_TX_P	AO	SGMII transmit – plus	PHY	
D6	SGMII_TX_N	AO	SGMII transmit – minus	PHY	
E4	SGMII_RX_P	AI	SGMII receive – plus	PHY	
F4	SGMII_RX_N	AI	SGMII receive – minus	PHY	
C7	ETH_INT_N	I	Interrupt from Ethernet PHY	1.8V	Active low. Connect an external pull-up resistor.
D9	ETH_MDC	O	MAC to PHY Clock	1.8V	
A8	ETH_MDIO	I/O	MAC to PHY Data	1.8V	
A9	ETH_RST_N	O	Reset to Ethernet PHY	1.8V	Active low Connect an external pull-up resistor.
A10	ETH_PWR_EN	O	External power IC enable control pin for Ethernet PHY	1.8V	
D8	WOL_INT_N	I	Wake on LAN Interrupt	1.8V	Active low Connect an external pull-up resistor.
PCIe Interface					
H15	PCIe_TX_P	O	PCIe receive - plus	Analog	
J15	PCIe_TX_N	O	PCIe receive - minus	Analog	
J14	PCIe_RX_P	I	PCIe receive - plus	Analog	
K14	PCIe_RX_N	I	PCIe receive - minus	Analog	
D10	PCIe_REFCLK_P	I/O	PCIe differential reference clock - plus	Analog	
D11	PCIe_REFCLK_N	I/O	PCIe differential reference clock - Minus	Analog	
D13	PCIe_CLK_REQ_N	I/O	PCIe reference clock request signal	1.8V	Internal PU (4.7 KΩ)
D14	PCIe_WAKE_N	I/O	PCIe wake up	1.8V	Internal PU (4.7 KΩ)
C14	PCIe_RST_N	I/O	PCIe reset	1.8V	
SDIO(WiFi) Interface					
N13	WiFi_SD_CMD	O	Wi-Fi SD Command	1.8V	
L13	WiFi_SD_CLK	O	Wi-Fi SD Clock	1.8V	
J13	WiFi_SD_DATA0	I/O	Wi-Fi SD Serial Data 0	1.8V	
M13	WiFi_SD_DATA1	I/O	Wi-Fi SD Serial Data 1	1.8V	

Pin	Signal	I/O	Function	Type	Comment
K13	WiFi_SD_DATA2	I/O	Wi-Fi SD Serial Data 2	1.8V	
H13	WiFi_SD_DATA3	I/O	Wi-Fi SD Serial Data 3	1.8V	
L12	WiFi_SDRST	O	Wi-Fi Reset / Power enable control	1.8V	
M11	WiFi_SLEEP_CLK	O	Wi-Fi Sleep clock output(32.768KHz)	1.8V	
M10	RFCLK2	O	Wi-Fi clock output(38.4MHz)	1.8V	
L4	WOW	I	Wake On WLAN	1.8V	Active Low
Miscellaneous Functions					
R12	ON_OFF_N	I	Power ON / Power OFF		Active low
R13	HW_SHUTDOWN_N	I	Unconditional Shutdown input		Active low
R11	VAUX/PWRMON	O	Supply output for external accessories / Power ON monitor	1.8V	
E13	VIO_1V8	O	IO voltage for internal ICs	1.8V	This power rail is always on while FE910C04 is working.
F14	USB_BOOT	I	Forced USB BOOT – emergency download	1.8V	
P12	USB_PCl_e_SW	I	PCle / USB interface boot switch OPEN(Internal Pull-Up) : USB LOW : PCIe	1.8V	Internal PU (1 KΩ)
M7	DPR	I	Dynamic Power Reduction	1.8V	
J4	WLAN_TX_ENABLE_N79	I	Input to N79. N79 puts its LNA in isolation mode when this signal is high and frequency.	1.8V	
M5	N79_TX_ENABLE_WLAN	O	Output from N79. Wi-Fi puts its LNA in isolation mode when this signal is high and frequency.	1.8V	
B1	ADC_IN1	AI	Analog/Digital Converter Input 1	Analog	
H4	ADC_IN2	AI	Analog/Digital Converter Input 2	Analog	
D7	ADC_IN3	AI	Analog/Digital Converter Input 3	Analog	
I2C Interface					
B11	I2C_SCL	I/O	I2C clock	1.8V	Internal PU (2.2 KΩ)
B10	I2C_SDA	I/O	I2C Data	1.8V	Internal PU (2.2 KΩ)
Bluetooth I2S					
B2	I2S_TX	O	Bluetooth I2S Data Output	1.8V	
B3	I2S_RX	I	Bluetooth I2S Data Input	1.8V	
B4	I2S_WS	I/O	Bluetooth I2S word select	1.8V	
B5	I2S_CLK	I/O	Bluetooth I2S clock	1.8V	

Pin	Signal	I/O	Function	Type	Comment
Power Supply					
M1	VBATT	-	Main Power Supply (Digital Section)	Power	
M2	VBATT	-	Main Power Supply (Digital Section)	Power	
N1	VBATT_PA	-	Main Power Supply (RF Section)	Power	
N2	VBATT_PA	-	Main Power Supply (RF Section)	Power	
P1	VBATT_PA	-	Main Power Supply (RF Section)	Power	
P2	VBATT_PA	-	Main Power Supply (RF Section)	Power	
A2	GND	-	Ground	Power	
B13	GND	-	Ground	Power	
D4	GND	-	Ground	Power	
E1	GND	-	Ground	Power	
E2	GND	-	Ground	Power	
E14	GND	-	Ground	Power	
F2	GND	-	Ground	Power	
G1	GND	-	Ground	Power	
G2	GND	-	Ground	Power	
G7	GND	-	Ground	Power	
G8	GND	-	Ground	Power	
G9	GND	-	Ground	Power	
H1	GND	-	Ground	Power	
H2	GND	-	Ground	Power	
H7	GND	-	Ground	Power	
H8	GND	-	Ground	Power	
H9	GND	-	Ground	Power	
J1	GND	-	Ground	Power	
J2	GND	-	Ground	Power	
J7	GND	-	Ground	Power	
J8	GND	-	Ground	Power	
J9	GND	-	Ground	Power	
K2	GND	-	Ground	Power	
L1	GND	-	Ground	Power	
L2	GND	-	Ground	Power	
M3	GND	-	Ground	Power	
M4	GND	-	Ground	Power	
M12	GND	-	Ground	Power	
N3	GND	-	Ground	Power	
N4	GND	-	Ground	Power	
N5	GND	-	Ground	Power	
N6	GND	-	Ground	Power	
P3	GND	-	Ground	Power	

Pin	Signal	I/O	Function	Type	Comment
P4	GND	-	Ground	Power	
P5	GND	-	Ground	Power	
P6	GND	-	Ground	Power	
P8	GND	-	Ground	Power	
P9	GND	-	Ground	Power	
P10	GND	-	Ground	Power	
P13	GND	-	Ground	Power	
R2	GND	-	Ground	Power	
R3	GND	-	Ground	Power	
R5	GND	-	Ground	Power	
R6	GND	-	Ground	Power	
R8	GND	-	Ground	Power	
R10	GND	-	Ground	Power	
RESERVED					
A11	Reserved	-	Reserved		
A12	Reserved	-	Reserved		
C3	Reserved	-	Reserved		
C4	Reserved	-	Reserved		
C5	Reserved	-	Reserved		
C6	Reserved	-	Reserved		
D3	Reserved	-	Reserved		
D12	Reserved	-	Reserved		
E3	Reserved	-	Reserved		
E12	Reserved	-	Reserved		
F12	Reserved	-	Reserved		
F13	Reserved	-	Reserved		
F15	Reserved	-	Reserved		
G3	Reserved	-	Reserved		
G12	Reserved	-	Reserved		
G13	Reserved	-	Reserved		
G14	Reserved	-	Reserved		
H12	Reserved	-	Reserved		
H14	Reserved	-	Reserved		
J12	Reserved	-	Reserved		
K12	Reserved	-	Reserved		
M6	Reserved	-	Reserved		
N7	Reserved	-	Reserved		
N8	Reserved	-	Reserved		
N10	Reserved	-	Reserved		
N11	Reserved	-	Reserved		

Pin	Signal	I/O	Function	Type	Comment
N12	Reserved	-	Reserved		
P7	Reserved	-	Reserved		
P11	Reserved	-	Reserved		
R4	Reserved	-	Reserved		
K3	Reserved	-	Reserved		
L3	Reserved	-	Reserved		

Note: When the UART signals are used as the communication port between the host and the modem, the RTS must be connected to GND (on the module side) if flow control is not used.
If the UART port is not used, all UART signals can be left disconnected

Note: The following pins are unique for the FE910C04 and may not be supported on other (former or future) xE910 family modules. Special care must be taken when designing the application board if future compatibility is required.
PCIe • I2S • Ethernet interface control pin • USB_PCl_e_Switch, Bluetooth UART • SDIO(WiFi) Interface control pin • USB BOOT

Warning: Reserved pins must not be connected.

4.2 Signals that Must Be Connected

Table 6 lists the FE910C04 signals that must be connected even if not used by the end application:

Table 6: FE910C04 signals that must be connected

PAD	Signal	Notes
M1, M2, N1, N2, P1, P2	VBATT & VBATT_PA	
A2, B13, D4, E1, E2, E14, F2, G1, G2, G7, G8, G9, H1, H2, H7, H8, H9, J1, J2, J7, J8, J9, K2, L1, L2, M3, M4, M12, N3, N4, N5, N6, P3, P4, P5, P6, P8, P9, P10, P13, R2, R3, R5, R6, R8, R10	GND	
R12	ON/OFF	Main power on / off signal
R13	HW_SHUTDOWN_N	Unconditional Shutdown
F14	USB_BOOT	Forced USB BOOT – emergency download If not used, connect to a Test Point
P12	USB_PCl_e_SW	PCIe / USB interface boot switch

PAD	Signal	Notes
		OPEN(Internal Pull-Up) : USB LOW : PCIe
B15	USB_D+	If not used, connect to a Test Point or an USB connector
C15	USB_D-	If not used, connect to a Test Point or an USB connector
A13	USB_VBUS	If not used, connect to a Test Point or an USB connector
N15	C103/TXD	If not used, connect to a Test Point
M15	C104/RXD	If not used, connect to a Test Point
L14	C105/RTS	If flow control is not used, connect to GND
P15	C106/CTS	If not used, connect to a Test Point
D15	DEBUG_UART_TXD	If not used, connect to a Test Point
E15	DEBUG_UART_RXD	If not used, connect to a Test Point
C8	GPIO_1/STAT_LED	If not used, connect to a Test Point
K1	Antenna	MAIN antenna
F1	ANT_DIV	DVI antenna
R9	ANT_GNSS	GNSS antenna
C4, C5, C6, C7, D3, E3, G3, P11	Reserved	Connect to a Test Point for Telit internal use

4.3 LGA Pads Layout

Top View

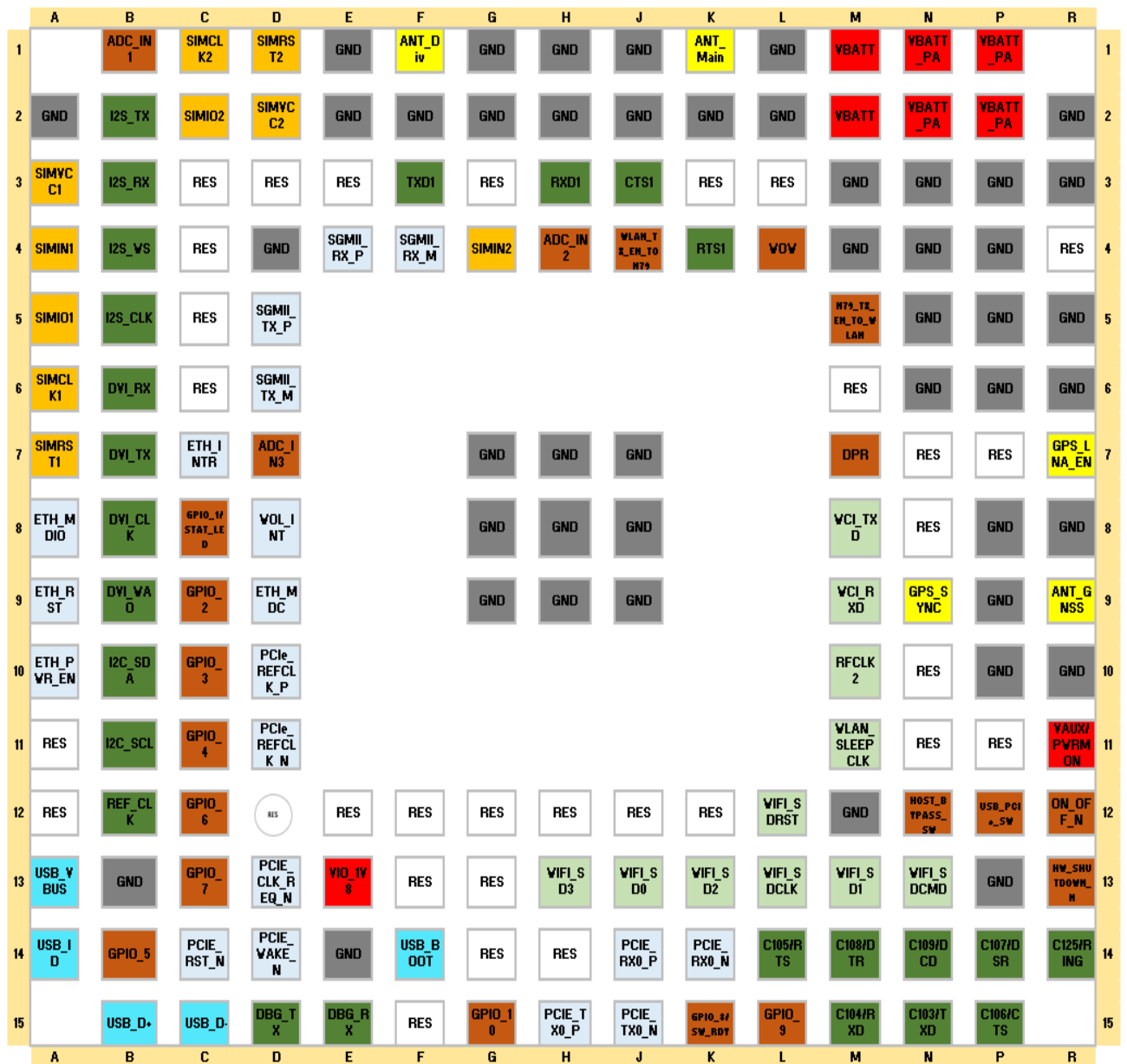
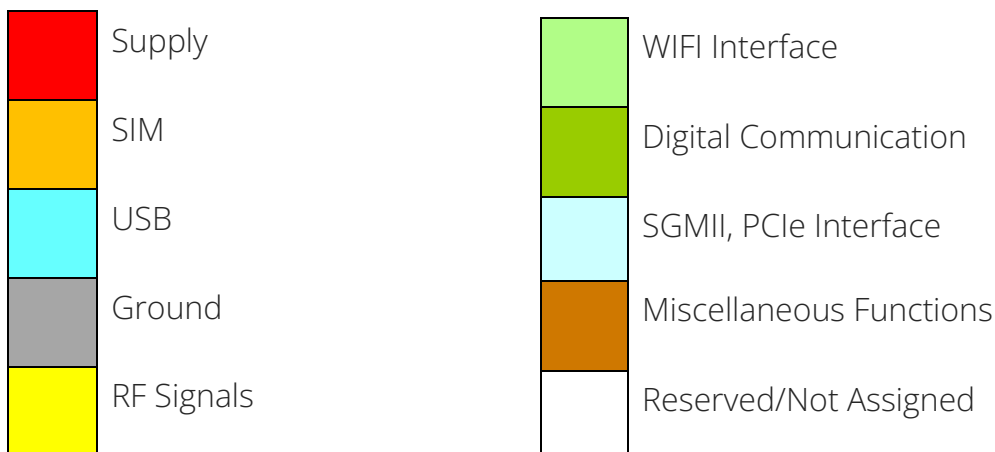


Figure 2: LGA Pads Layout (Top View)



5 Power Supply

The power supply circuitry and the board layout are a very important part of the full product design and they strongly reflect on the product's overall performance, so the requirements and the guidelines that will follow should be read carefully for a proper design.

5.1 Power Supply Requirements

The external power supply must be connected to VBATT and VBATT_PA pads and must fulfil the following requirements:

Table 7: Power Supply Requirements

Power Supply	Value
Nominal Supply Voltage	3.8 V
Operating Voltage Range	3.3 V - 4.2 V
Max ripple on module input supply	30 mV
Peak current consumption*	3.8V @ 2A

Note:

- The Operating Voltage Range MUST never be exceeded; the application's power supply section must be designed with care to avoid an excessive voltage drop
- If the voltage drop exceeds the limits, it may cause an unintentional module power off.
- The voltage must be at least VBATTmin to power the module.
- The exceeding voltage and drop in MUST never be exceeded.
- For PTCRB approval on the final products the power supply is required to be within the "Normal Operating Voltage Range".
- * The peak current must be higher than the average current due to TDD bands and power class 2.

5.2 Power Consumption

5.2.1 Idle Mode

Table 8: Idle Mode

Mode	Average (Typical)	Mode Description
Switched off		
Switched off	60.0 uA	Module supplied but switched Off (RTC On)
IDLE mode (Standby Mode; No Call in Progress)		
AT+CFUN=1	20 mA	Module full functionality with power saving disabled (USB is connected to the host)
AT+CFUN=4	12 mA	TX and RX disabled; the module is not registered on the network (Flight mode) (USB is disconnected)
Variant - WW		
LTE DRX	3.93mA	Paging cycle #32 frames (0.32sec DRX cycle)

Mode	Average (Typical)	Mode Description
AT+CFUN=5	3.50mA	Paging cycle #64 frames (0.64sec DRX cycle)
	3.28mA	Paging cycle #128 frames (1.28sec DRX cycle)
	3.17mA	Paging cycle #256 frames (2.56sec DRX cycle)
5G NR DRX AT+CFUN=5	3.77mA	Paging cycle #32 frames (0.32sec DRX cycle)
	3.20mA	Paging cycle #64 frames (0.64sec DRX cycle)
	2.93mA	Paging cycle #128 frames (1.28sec DRX cycle)
	2.76mA	Paging cycle #256 frames (2.56sec DRX cycle)

5.2.2 Connected Mode

Table 9: Connected Mode

Mode	Average (Typical)	Mode Description
LTE Cat4		
Max Power	800mA	LTE FDD 10 MHz, RB=12, Tx = Max power
0 dBm	140mA	
5G NR		
Max Power	750mA	5G Sub6 FDD 20 MHz, Inner_Full(50@20), Tx = Max power
0 dBm	130mA	
Operative Mode (GPS/GNSS)		
GNSS Acquisition	54.11mA	LTE connection is idle, USB connected
GNSS Tracking	56.25mA	

Note:

- Worst/best case current values depend on network configuration, not under module control.
- The electrical design for the power supply must ensure a peak current output of at least 2.0 A.
- The support of specific network wireless technology depends on the product variant configuration.
- The power supply must be designed to withstand current peaks without large voltage drops. This means that both the electrical design and the board layout must be designed for this current flow.
- If the voltage drops during the peaks, the current absorption is too high. The device may even shut down due to a drop in the supply voltage.

5.3 General Design Rule

The main guidelines for the Power Supply Design include three different design steps:

- The electrical design of the power supply
- The thermal design
- The PCB layout

5.3.1 Electrical Design Guidelines

The electrical design of the power supply strongly depends on the power source where this power is drained. We will distinguish them into three categories:

- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)
- Battery

5.3.1.1 +5V Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, so there's not a big difference between the input source and the desired output and a linear regulator can be used. A switching power supply will not be suitable due to the low drop out requirements.
- When using a linear regulator, a proper heat sink shall be provided to dissipate the power generated.
- A Bypass low ESR capacitor of adequate capacity must be provided to cut the current absorption peaks close to the Module, a 100 μ F capacitor is usually suitable.
- Make sure the low ESR capacitor on the power supply output is rated at least 10V.
- A protection diode must be placed near the power input to protect the FE910C04 module from power polarity inversion.

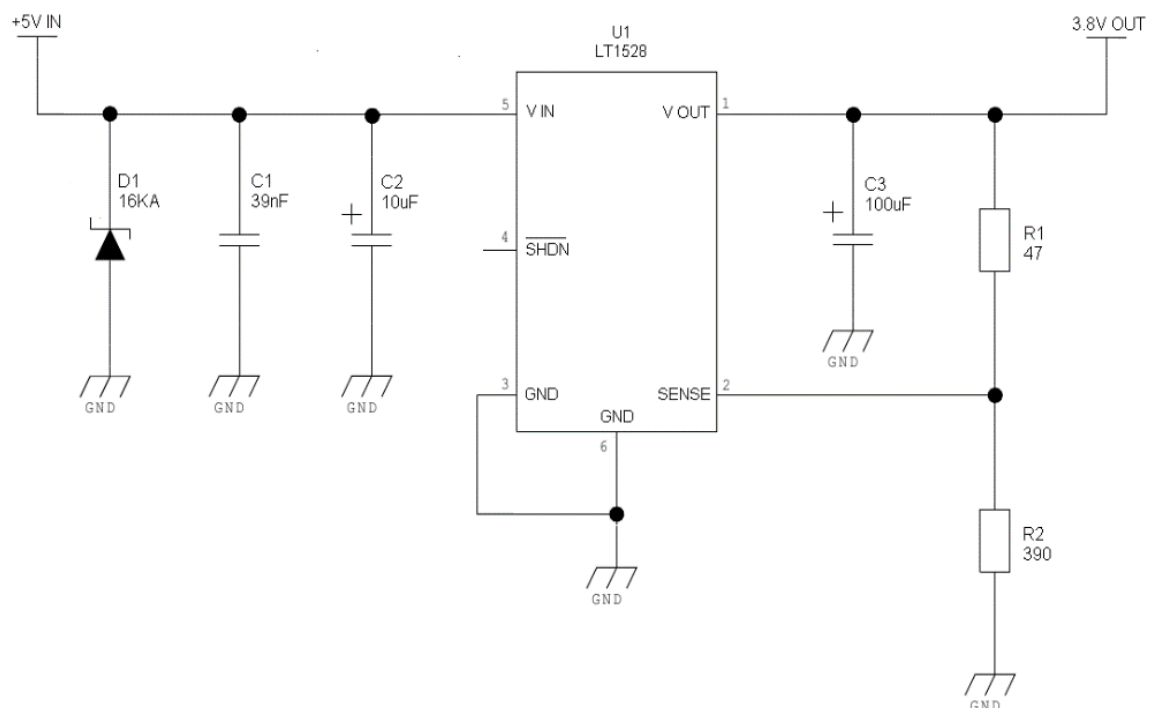


Figure 3: An Example of Linear Regulator with 5V Input

5.3.1.2 +12V Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, so due to the big difference between the input source and the desired output, a linear regulator is not suitable and shall not be used. A switching power supply will be preferable because of its better efficiency.

- When using a switching regulator, a 500kHz or more, switching frequency regulator is preferable because of its smaller inductor size and its faster transient response. This allows the regulator to respond quickly to the current peak absorption.
- In any case, the frequency and Switching design selection are related to the application to be developed since the switching frequency could also generate EMC interferences.
- For the car PB battery, the input voltage can rise to 15.8V and this should be kept in mind when choosing components: all components in the power supply must withstand this voltage.
- A Bypass low ESR capacitor of adequate capacity must be provided to cut the current absorption peaks, a 100μF capacitor is usually suitable.
- Make sure the low ESR capacitor on the power supply output is rated at least 10V.
- For Car applications, a spike protection diode should be inserted close to the power input, to clean the supply from the spikes.

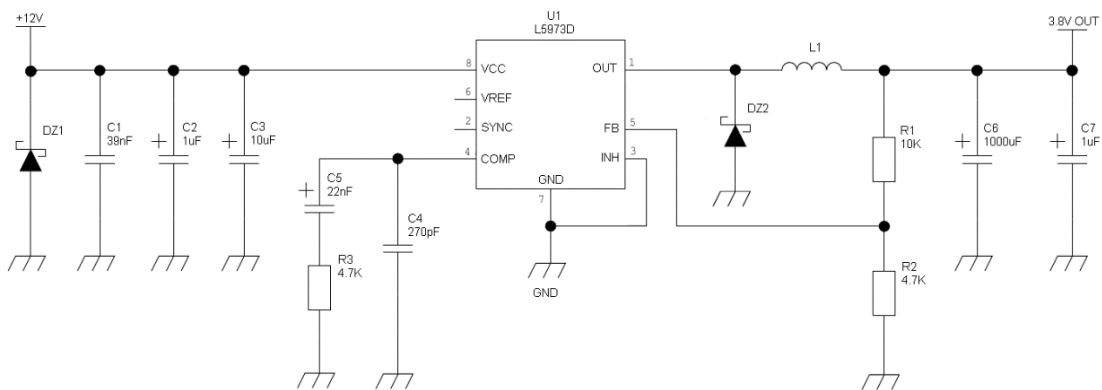


Figure 4: An Example of Switching Regulator with 12V Input

5.3.1.3 Battery Source Power Supply Design Guidelines

- The desired nominal output for the power supply is 3.8V and the maximum voltage allowed is 4.2V, so a single 3.7V Li-Ion cell battery type is suitable to supply power to the Telit FE910C04 module.
- A Bypass low ESR capacitor of adequate capacity must be provided to cut the current absorption peaks, a 100μF tantalum capacitor is usually suitable
- Make sure the low ESR capacitor (usually a tantalum one) is rated at least 10V.
- A protection diode should be inserted close to the power input to protect the FE910C04 module from power polarity inversion. Otherwise, the battery connector should be done in a way to avoid polarity inversions when connecting the battery.
- The battery must be rated to supply peaks of current up to 0.6 A for LTE.

Note: DON'T USE any Ni-Cd, Ni-MH, and Pb battery types directly connected with FE910C04. Their use can lead to overvoltage on the FE910C04 and damage it. USE ONLY Li-Ion battery types.

5.3.2 Thermal Design Guidelines

The thermal design for the power supply heat sink should be done with the following specifications:

- Considering the very low current during Idle, especially if the Power Saving function is enabled, it is possible to consider from the thermal point of view that the device absorbs significant current only during an Active Call or Data session.
- For the heat generated by the FE910C04 module, consider it to be 2W.
- The FE910C04 supports different RATs: 4G, and 5G Sub-6.
- Based on the Radio Access Technology, the FE910C04 modem might exhibit high current consumption, thus proper thermal designs are essential to dissipate heat well.
- The FE910C04 is designed to conduct the heat flow from the module IC's towards the bottom of the PCB across GND metal layers
- The generated heat is mostly conducted to the grounding plane under the FE910C04 module. The application board should be properly designed to dissipate this heat.
- The design of the application board must ensure that the area under the FE910C04 module is as large as possible. Make sure the FE910C04 is mounted on the large ground area of application board and provides plenty of ground vias to dissipate heat.

Note:

- Make PCB design to have the best connection of GND pads to large surfaces of copper.
- Note: The average consumption during transmission depends on the power level at which the device is requested to transmit over the network. Therefore, the average current consumption varies significantly.

5.3.3 Power Supply PCB Layout Guidelines

As seen in the guidelines for electrical design, the power supply shall have a low ESR capacitor on the output to cut the current peaks on the input, to protect the supply from spikes. The placement of this component is crucial for the correct working of the circuitry. A misplaced component can be useless or can even decrease the power supply performances.

- The Bypass low ESR capacitor must be placed close to the Telit FE910C04 power input pads or, in the case the power supply is a switching type it can be placed close to the inductor to cut the ripple, provided the PCB trace from the capacitor to the FE910C04 is wide enough to ensure a voltage drop less connection even during a 2 A current peak.
- The protection diode must be placed close to the input connector where the power source is drained.
- The PCB's traces from the input connector to the power regulator IC must be wide enough to ensure no voltage drops occurs when a 2 A current peak is absorbed.
- The PCB traces to the FE910C04 and the Bypass capacitor must be wide enough to ensure no significant voltage drops occurs. This is for the same reason as the previous point. Try to keep this trace as short as possible.



- To reduce the EMI due to switching, it is important to keep the mesh involved very small; therefore the input capacitor, the output diode (if not embodied in the IC) and the regulator, shall form a very small loop. This is done to reduce the radiated field (noise) at the switching frequency (100-500 kHz usually).
- A dedicated ground for the Switching regulator separated by the common ground plane is suggested.
- The placement of the power supply on the board should be done in such a way as to guarantee that the high current return paths in the ground plane are not overlapped with any noise-sensitive circuitry, such as the microphone amplifier/buffer or earphone amplifier.
- The power supply input cables should be kept separate from noise-sensitive lines such as microphone/earphone cables.
- The insertion of an EMI filter on VBATT pins is suggested in those designs where the antenna is placed close to the battery or supply lines. A ferrite bead-like Murata BLM18EG101TN1 or Taiyo Yuden P/N FBMH1608HM101 can be used for this purpose.

The below figure shows the recommended circuit:

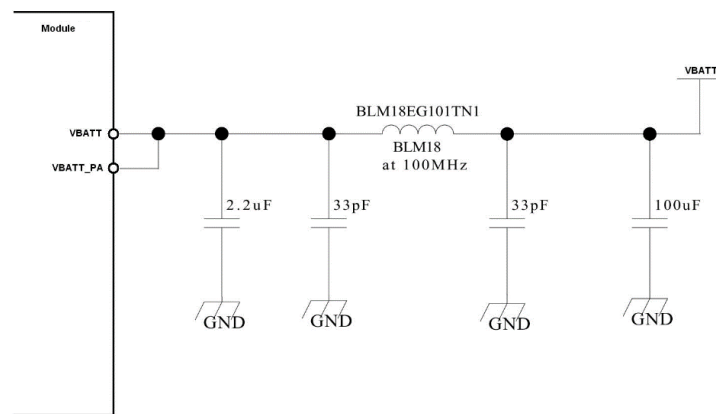


Figure 5: Recommended Circuit

5.3.4 Bypass Capacitor on Power Supplies

When a sudden voltage step to or cut from the power supplies is asserted, the steep transition causes some reactions such as overshoot and undershoot. This abrupt voltage transition can affect the device causing it to fail or to malfunction.

Bypass capacitors are needed to alleviate this behaviour. The behaviour may appear for different applications. Customers must pay special attention to this issue when they design their application board.

The length and width of the power lines must be considered carefully, and the capacitance of the capacitors must be selected accordingly.

The capacitor will also avoid power supplies ripple and the switching noise caused.

In particular, a suitable bypass capacitor must be mounted on the following lines on the application board:

- VBATT & VBATT_PA (M1, M2, N1, N2, P1, P2)
- USB_VBUS (Pad A13)

Recommended values are:

- 100uF for both VBATT and VBATT_RF together
- 4.7uF for USB_VBUS

However, customers should consider that the capacitance mainly depends on the conditions of their application board.

Generally, more capacitance is required when the power line is longer.

5.4 VAUX Power Output

A regulated power supply output is provided to supply small devices from the module, like level translators, audio codecs, sensors, and others.

Pad R11 can be used also as PWRMON (module powered ON indication) function because is always active when the module is powered ON and cannot be set to a LOW level by any AT command.

The host can only detect deep sleep mode by monitoring of VAUX/PWRMON output pin since there is no pin dedicated to the PSM status indicator.

The operating range characteristics of the supply are:

Table 10: Operating Range Characteristics of the Supply

Item	Min	Typical	Max
Output voltage	1.75V	1.80V	1.85V
Output current	-	-	100mA
Output bypass capacitor (inside the module)		1uF	

Note: If power saving configuration is enabled by AT+CPSMS Command, VAUX during deep sleep mode period is OFF.

5.5 RTC Supply

The RTC within the FE910C04 module does not have a dedicated RTC supply pin.

The RTC block is supplied by the VBATT supply.

If the battery is removed, the RTC is not maintained so if it is necessary to maintain an — internal RTC , VBATT must be supplied continuously.

RTC is functional when FE910C04 is in PSM or OFF state and VBATT pin is supplied.

RTC settings are erased if the VBATT supply is temporarily disconnected.

6 Digital Section

FE910C04 has four main operation states:

- **OFF state:** VBATT is applied and only RTC is running. Baseband is switched OFF and the only change possible is the ON state.
- **ON state:** baseband is fully switched on and FE910C04 is ready to accept AT commands. The FE910C04 can be idle or connected.
- **Sleep mode state:** main baseband processor is intermittently switched ON and AT commands can be processed with some latency. FE910C04 is idle with low current consumption.
- **Deep sleep mode state:** PSM defined in 3GPP Release 12. Baseband is switched OFF most of the time.

6.1 Logic Levels

Unless otherwise specified, all the interface circuits of the FE910C04 are 1.8V CMOS logic. Only few specific interfaces (such as USIM) are capable of dual voltage I/O.

The following tables show the logic level specifications used in the FE910C04 interface circuits.

6.1.1 1.8V Standard GPIOs

Table 11: Operating Range – Interface Levels (1.8V CMOS)

Pad	Parameter	Min	TYP	Max	Unit	Comment
V _{IH}	Input high level	VCC * 0.7	1.8	VCC + 0.3	[V]	
V _{IL}	Input low level	-0.3		0.3 * VCC	[V]	
V _{OH}	Output high level	VCC - 0.45		VCC	[V]	
V _{OL}	Output low level	0		0.45	[V]	
I _{IL}	Low-level input leakage current	-1		-	[uA]	No pull-up
I _{IH}	High-level input leakage current	-		10	[uA]	No pull-down
R _{PU}	Pull-up resistance	20	-	60	[kΩ]	
R _{PD}	Pull-down resistance	20	-	60	[kΩ]	

6.1.2 1.8V SIM Card Pads

Table 12: Operating Range – SIM Pads Working at 1.8V

Pad	Parameter	Min	TYP	Max	Unit	Comment
VCC	Supply Voltage	1.65	1.8	1.95	[V]	
V _{IH}	Input high level	VCC * 0.7	-	VCC + 0.3	[V]	
V _{IL}	Input low level	-0.3	-	VCC * 0.2	[V]	
V _{OH}	Output high level	0.8 * VCC	-	VCC	[V]	
V _{OL}	Output low level	0	-	0.4	[V]	
I _{IL}	Low-level input leakage current		-	1000	[uA]	No pull-up
I _{IH}	High-level input leakage current	-20	-	20	[uA]	No pull-down

Pad	Parameter	Min	TYP	Max	Unit	Comment
R _{PU}	Pull-up resistance	10	-	100	[kΩ]	
R _{PD}	Pull-down resistance	10	-	100	[kΩ]	

6.1.3 2.95 V SIM Card Pads

Table 13: Operating Range – For SIM Pads Operating at 2.95 V

Pad	Parameter	Min	TYP	Max	Unit	Comment
VCC	Supply voltage	2.7	2.95	3.05	[V]	
V _{IH}	Input high level	0.7 * VCC	-	VCC + 0.3	[V]	
V _{IL}	Input low level	-0.3	-	0.2 * VCC	[V]	
V _{OH}	Output high level	0.8 * VCC	-	VCC	[V]	
V _{OL}	Output low level	0		0.4	[V]	
I _{IL}	Low-level input leakage current		-	1000	[uA]	No pull-up
I _{IH}	High-level input leakage current	-20	-	20	[uA]	No pull-down
R _{PU}	Pull-up resistance	10	-	100	[kΩ]	
R _{PD}	Pull-down resistance	10	-	100	[kΩ]	

6.2 Power On

To turn on the FE910C04 module, the ON_OFF_N pad must be asserted low for more than 0.3 seconds and less than 1 seconds, and then released.

The maximum current that can be drained from the ON/OFF_N pad is 0.12 mA. This pin is pulled up internally; customers should expect to see VBATT at the output.

Figure 6 illustrates a simple circuit to power on the module using an inverted buffer output.

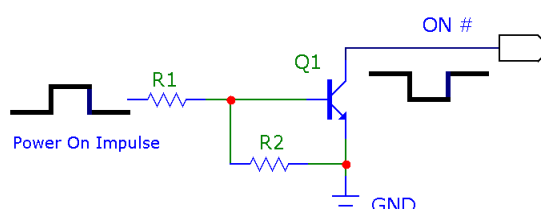


Figure 6: Power-on Circuit; illustrates a simple circuit to power on the module using an inverted buffer output.

Note:

- Do not use any pull up resistor on the ON_OFF_N line, it is internally pulled up. Using pull up resistor may bring to latch up problems on the FE910C04 power regulator and improper power on/off of the module. The line ON_OFF_N must be connected only in open collector or open drain configuration.
- To avoid back powering it is recommended to prevent any HIGH logic level signal from being applied to the digital pins of FE910C04 when the module is powered off or during an ON-OFF transition.
- To check if the device has just powered on, the hardware line PWRMON should be monitored.

After turning on the FE910C04 module, a predefined internal boot sequence performs the HW and SW initialization of the module, which takes some time to complete. During this process, the FE910C04 is not accessible.

As shown in Figure 7, the FE910C04 becomes operational at least 50 seconds after ON_OFF is asserted.

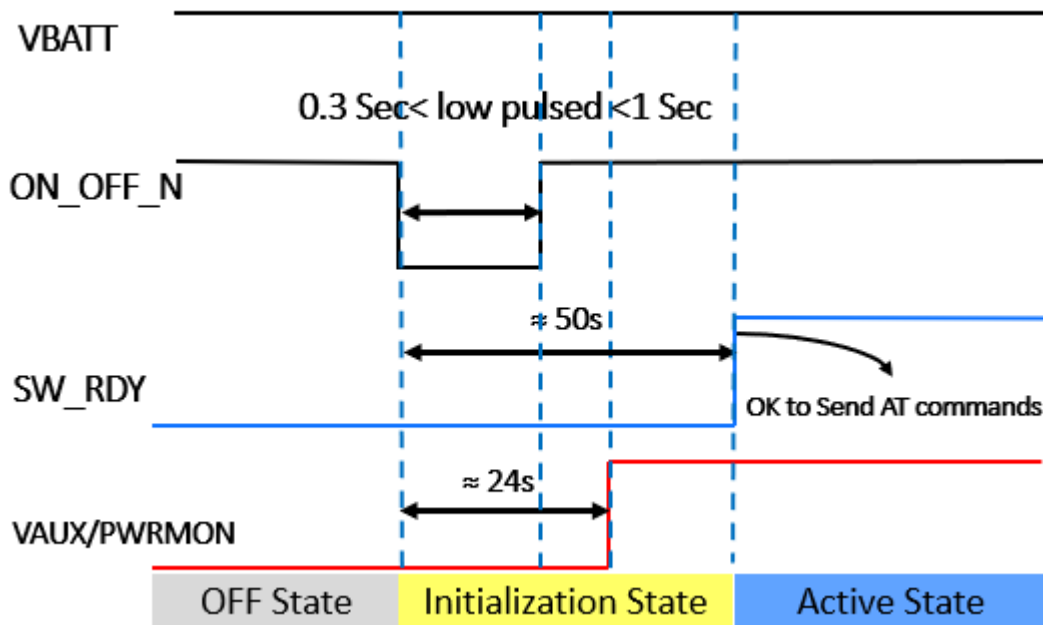


Figure 7: Power ON Sequence

Note:

- During the Initialization state, AT commands are not available. The DTE host must wait for the Activation state prior to communicating with the FE910C04.
- To check whether the FE910C04 is fully operational, monitor the SW_RDY hardware line. When SW_RDY goes high, the module is fully operational and is ready to accept AT commands.
- During the SW initialization of the FE910C04, the SW configures all pads and interfaces in the desired status. When PWRMON goes high, this indicates that the initialization of all I/O pads is completed.
- Active low signals are labeled with a name that ends with "#" or with "_N"

A flow chart showing the proper Power-On procedure is displayed below:

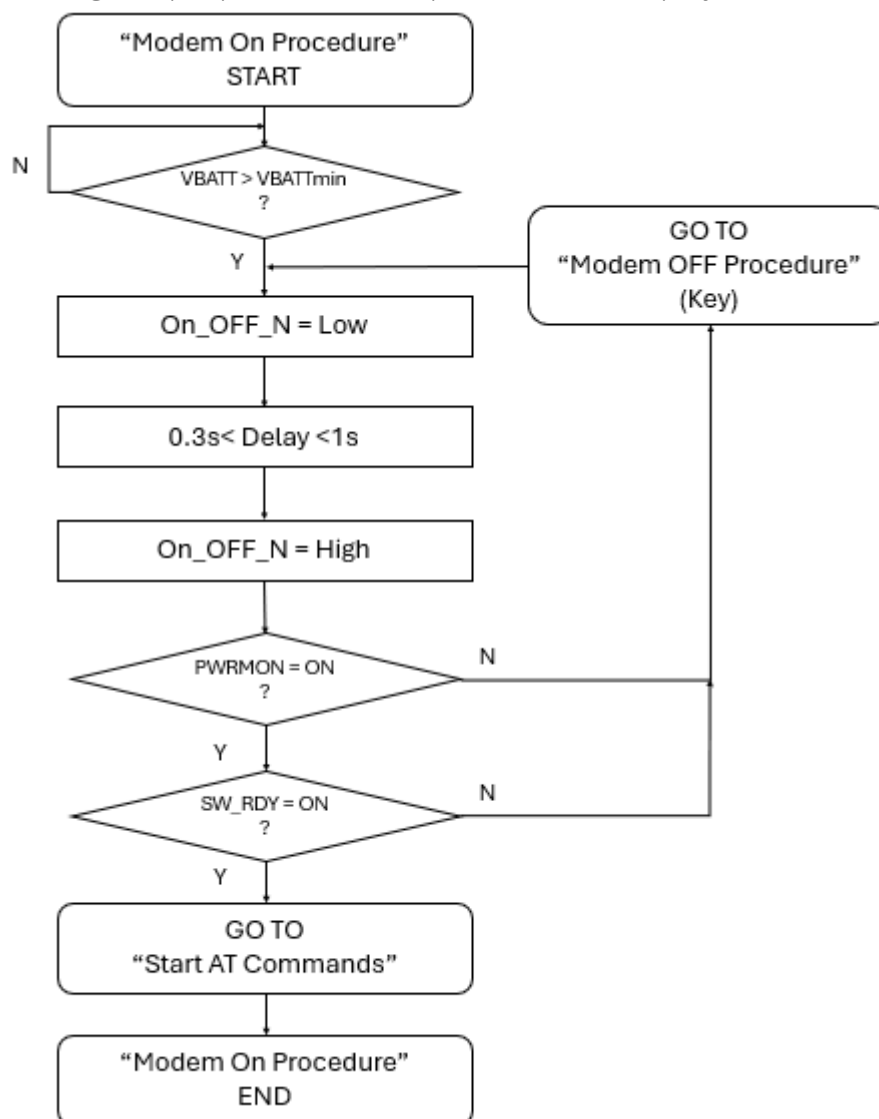


Figure 8: Power On Procedure Flow Chart

A flow chart showing the AT commands managing procedure is displayed below:

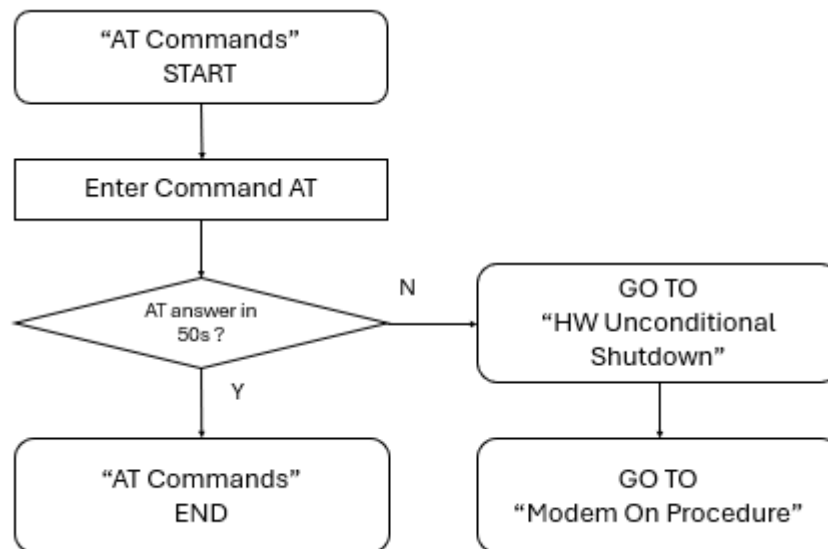


Figure 9: AT commands Managing Procedure Flow Chart

Note: To avoid a back-powering effect it is recommended to prevent any HIGH logic level signal from being applied to the digital pins of the FE910C04 when the module is powered off or during an ON-OFF transition.

6.3 Power Off

Turning off the device can be done in the following different ways:

- Shutdown by software using AT#SHDN software command
- Hardware shutdown using ON_OFF_N Pad
- Unconditional shutdown using HW_SHUTDOWN_N

When the device is shut down by a software command or a hardware shutdown, it sends a detach disconnection request to the network, informing the network that the device will no longer be reachable.

Note:

- To check if the device has turned off, monitor the PWRMON hardware line. When PWRMON goes low, this indicates that the device is turned off.
- To avoid a back-powering effect it is recommended to prevent any HIGH logic level signal from being applied to the digital pins of the FE910C04 when the module is powered off or during an ON-OFF transition.

Warning: Not following the recommended shut-down procedures might damage the device and consequently void the warranty.

6.4 Shutdown by Software Command

The FE910C04 module can be shut down via a software command.

When a shutdown command is sent, the FE910C04 enters the Finalization state and at the end of the finalization process shuts down PWRMON.

The duration of the Finalization state may vary depending on the current situation of the module, so it is not possible to define a value.

Usually, it will take more than 15 seconds from sending a shutdown command until a complete shutdown is achieved. The DTE host should monitor the PWRMON status to observe the actual power-off.

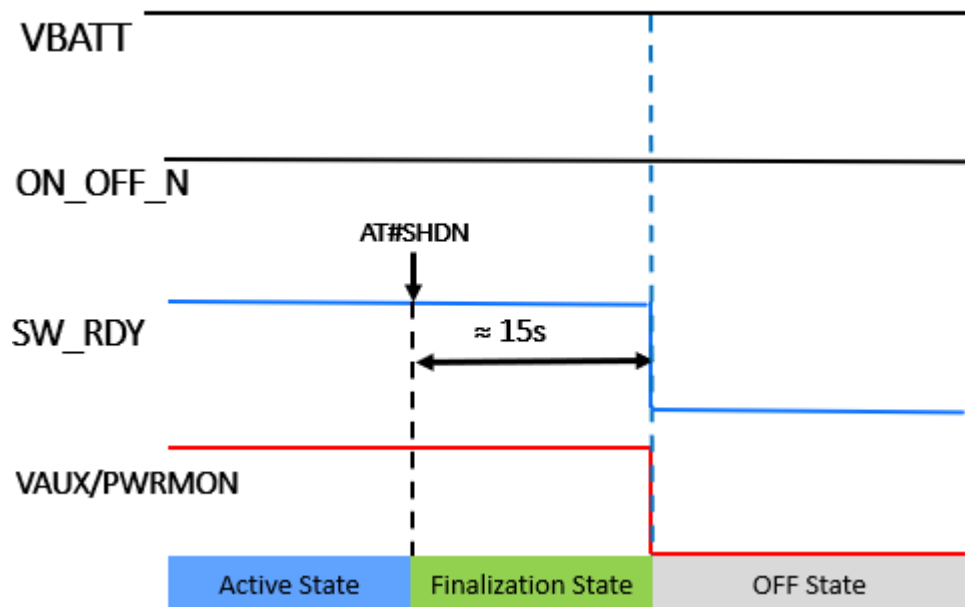


Figure 10: Shutdown by Software Command

6.5 Hardware Shutdown

To turn off the FE910C04 module, the ON_OFF_N pad must be asserted low for more than 2 seconds, and then released. Use the same circuitry and timing for power-on. When the hold time of ON_OFF_N is more than 2 seconds, the FE910C04 enters the Finalization state and finally shuts down PWRMON.

The duration of the Finalization may vary depending on the current situation of the module, so it is not possible to define a value. Usually, it will take more than 3 seconds issuing a shutdown command until a complete shutdown is achieved. The DTE host should monitor the PWRMON status to observe the actual power-off.

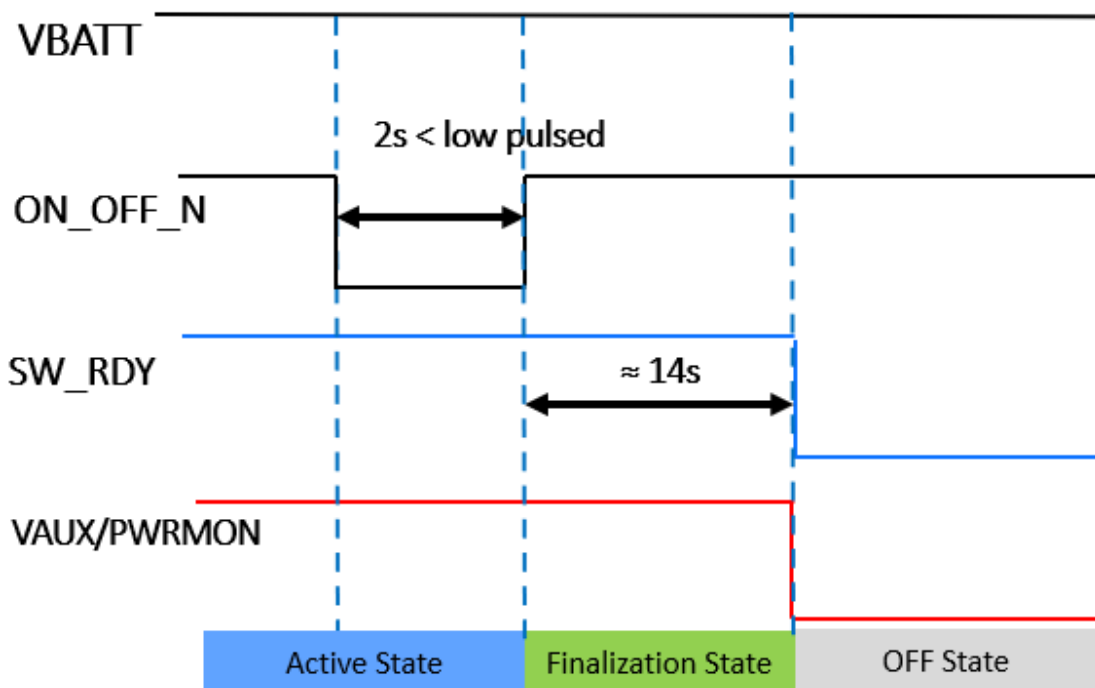


Figure 11: Hardware Shutdown

6.6 Unconditional Shutdown

HW_SHUTDOWN* is used to unconditionally shut down the FE910C04. Whenever this signal is pulled low, the FE910C04 is reset. When the device is reset it stops any operation. After the release of the line, the FE910C04 is unconditionally shut down, without performing any disconnection from the network where it is registered. This behaviour is not a proper shutdown because any cellular device is requested to issue a detach request on turn off. The HW_SHUTDOWN* is internally controlled on start-up to always achieve a proper power-on reset sequence, so there's no need to control this pin at start-up.

To unconditionally shut down the FE910C04, the pad HW_SHUTDOWN* must be tied low for at least 200 milliseconds and then released.

The signal is internally pulled up so that the pin can be left floating if not used.

If used, then it must always be connected with an open collector transistor, to allow the internal circuitry to perform the power on reset and under voltage lockout functions.

The use of the HW_SHUTDOWN* pin is valid only when FE910C04 has VAUX/PWRMON output HI.

Pin Description

Table 14: HW_SHUTDOWN* Signal

Signal	Function	I/O	PAD
HW_SHUTDOWN*	Unconditional Shutdown of the Module	I	R13

Warning: The hardware unconditional Shutdown must not be used during normal device operation as it does not disconnect the device from the network. It shall be kept as an emergency exit procedure.

A typical circuit is the following:

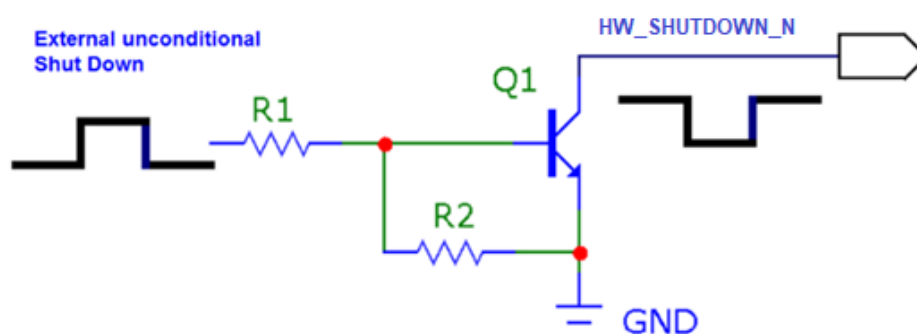


Figure 12: Circuit for Unconditional Hardware Shutdown

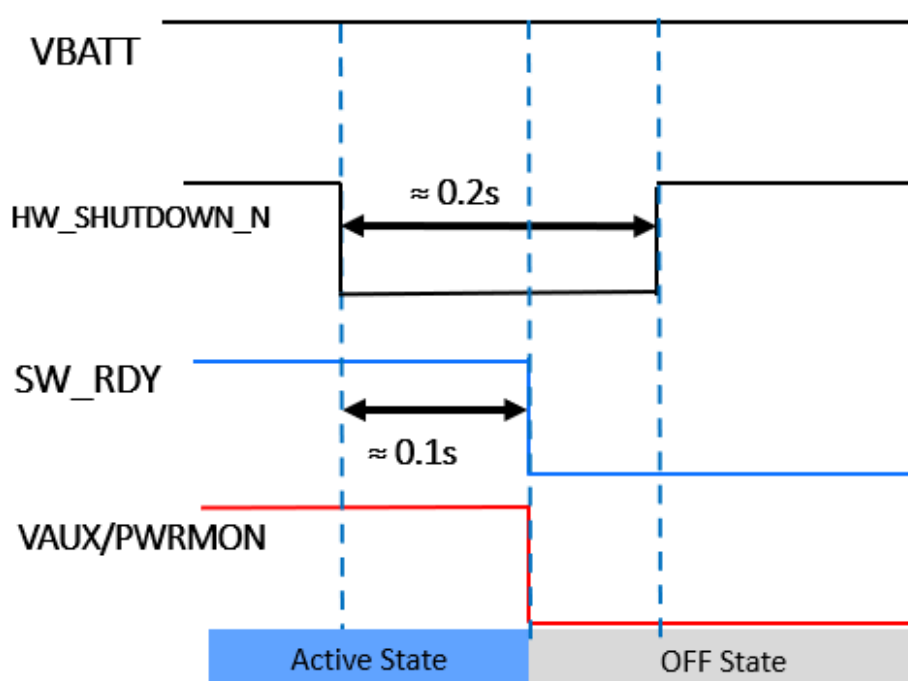


Figure 13: Power down timing using HW_SHUTDOWN_N

In the following flow chart the proper restart procedure is described:

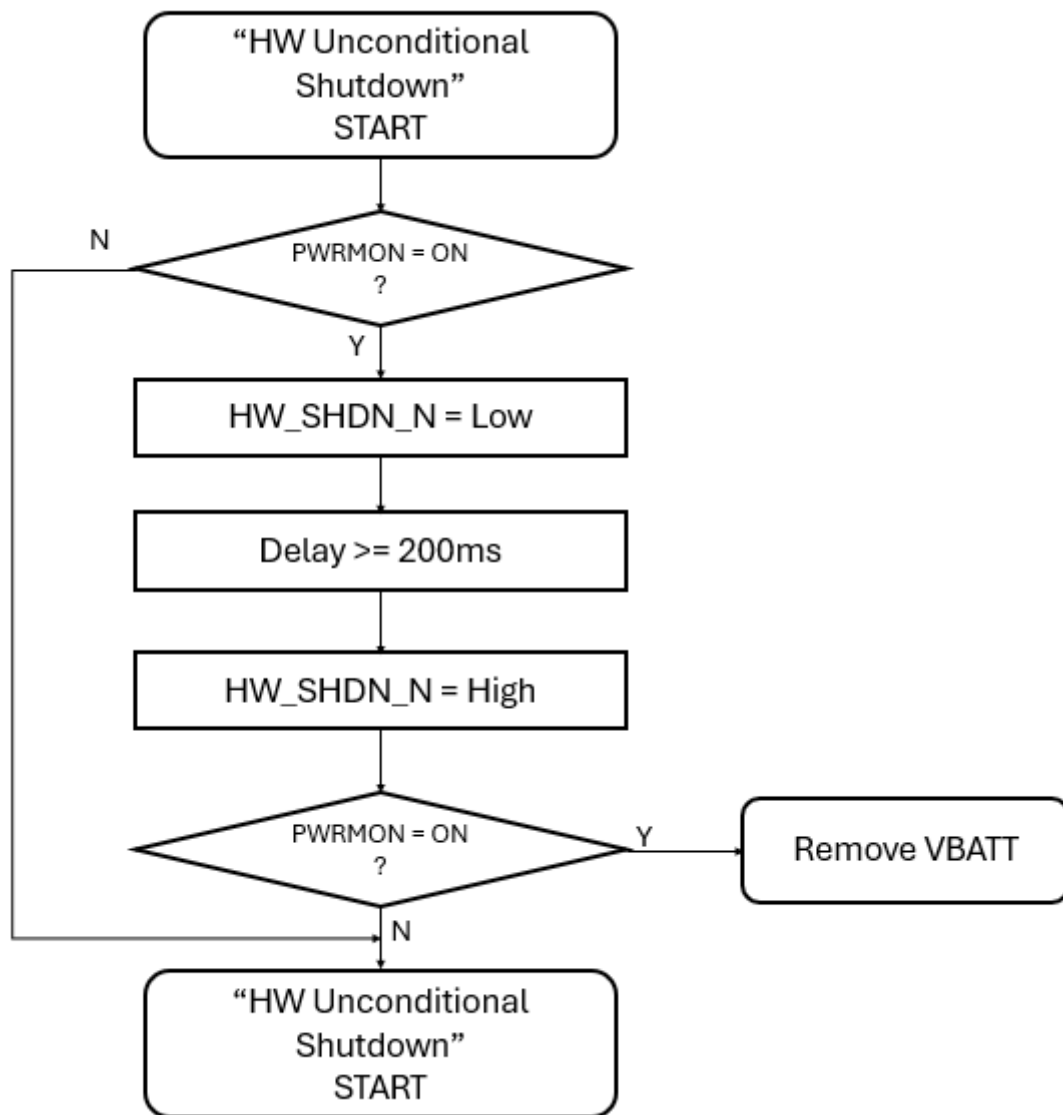


Figure 14: Power down timing using HW_SHUTDOWN_N Procedure Flow Chart

Note:

- To avoid a back-powering effect it is recommended to prevent any HIGH logic level signal from being applied to the digital pins when the module is powered off or during an ON-OFF transition.
- Do not use any pull-up resistor on the HW_SHUTDOWN* line or any totem pole digital output. Using a pull-up resistor may bring latch-up problems on power regulator and improper functioning of the module. To correctly restart the module, refer to the [Power ON](#) section.
- The unconditional hardware shutdown must always be implemented on the boards and should be used only as an emergency exit procedure.

6.7 Fast Power Down[TBD]

The procedure to power off FE910C04 described in the [Power Off](#) section normally takes more than 14 second to detach from the network and make FE910C04 internal filesystem properly closed.

In case of unwanted supply voltage loss, the system can be switched off without any risk of filesystem data corruption by implementing the Fast Shut Down feature.

The fast Shut Down feature permits the reduction of the current consumption and the time-to-power off to minimum values.

Note: Refer to FE910 AT command reference guide (Fast power down - #FASTSHDN) to set up detailed AT command.

6.7.1 Fast Shut Down by Hardware

The Fast Power Down can be triggered by the configuration of any GPIO. HI, level to LOW-level transition of GPIO commands fast power down.

Example circuit:

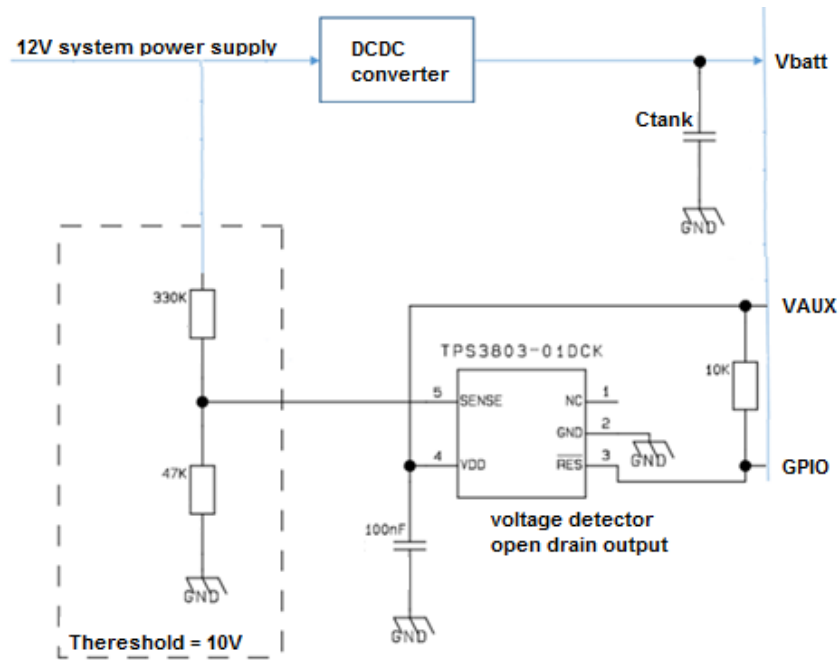


Figure 15: Example Circuit

Note: Consider voltage drop under max current conditions when defining the voltage detector threshold to avoid an unwanted shutdown.

The capacitor is rated with the following formula:

$$C = I \frac{\Delta t}{\Delta V}$$

Note: Make the same plot during system verification to check timings and voltage levels.

6.7.2 Fast Shut Down by Software

The Fast Power Down can be triggered by AT command.

6.8 Communication Ports

6.8.1 USB

The FE910C04 module includes a Universal Serial Bus (USB) transceiver, which operates at USB high-speed (480Mbps/sec). It can also operate with USB full-speed hosts (12Mbps/sec).

It is compliant with the USB 2.0 specification and can be used for control and data transfers, as well as for diagnostic monitoring and firmware update.

The USB port is typically the main interface between the FE910C04 module and OEM hardware.

Note: The USB_D+ and USB_D- signals have a clock rate of 480Mbps/sec. The signal traces must be routed carefully. Minimize trace lengths, number of vias, and capacitive loading. The impedance value should be as close as possible to 90 Ohms differential.

Table 15: USB Interface Signals

Signal	Pad No.	Usage
USB_VBUS	A13	Power and cable detection for the internal USB transceiver. Acceptable input voltage range 2.5V – 5.5V @ max 5 mA consumption
USB_D-	C15	Minus (-) line of the differential, bi-directional USB signal to/from the peripheral device
USB_D+	B15	Plus (+) line of the differential, bi-directional USB signal to/from the peripheral device
USB_ID	A14	Used for USB OTG to determine host or client mode.

Note: USB_VBUS input power is used internally to detect the USB port and start the enumeration process.

It is a power supply pin with a maximum consumption of 5 mA. Do not use pull up or a voltage divider for sourcing this supply

Note: Even if USB communication is not used, it is still highly recommended to place an optional USB connector on the application board.

At least USB signal test points are required as USB physical communication is needed in the case of SW update.

Note: USB OTG feature is supported by default.

If the USB_ID pin asserted to 'low', USB OTG is enabled. Please note that FE910C04 doesn't supply 5V power to OTG devices. therefore, an external 5V power is required on an application board to provide 5V power to OTG devices.

6.8.1.1 USB Layout Guidelines

- If third-party components are required for signal improvement, place them closer to the USB connector.

- There are relatively fast edge rates, so must be routed away from sensitive circuits and signals (RF, audio, and XO).
- Maintain good isolation between the USB connector and RF antennas (especially 2.4 GHz).
- Route differential pairs in the inner layers with a solid GND reference to have good impedance control and to minimize discontinuities.
- Keep isolation between the Tx pair, Rx pair, and DP/DM to avoid crosstalk.

Table 16: USB requirement

Type of guidance	Guideline	Requirement
General	Data rate	480 Mbps
	Impedance	90 ohms differential
	Bus length	Max 150 mm
Length matching	Intra-pair length match	2 mm
Spacing	Lane to other signals	3 x line width

6.8.2 UART

The serial port is typically a secondary interface between the FE910C04 module and OEM hardware. The following serial ports are available on the module:

- Main UART interface supports 115200 bps baud rate. This interface is used for AT command communication. It supports RTS and CTS hardware flow control.
- Debug UART interface supports 115200 bps baud rate. (Console log)
- Bluetooth UART interface supports 115200 bps baud rate. (Bluetooth communication)
- COEX UART interface is used for WWAN/WLAN coexistence.

Table 17: Main UART

Pin	Signal	I/O	Function	Type	Comment
Asynchronous UART					
N15	C103/TXD	I	Serial data input (TXD) from DTE	1.8V	Connect to the TXD line.
M15	C104/RXD	O	Serial data output to DTE	1.8V	Connect to the RXD line.
P15	C106/CTS	O	Output for Clear to send signal (CTS) to DTE	1.8V	Connect to the CTS line.
L14	C105/RTS	I	Input for Request to send signal (RTS) from DTE	1.8V	Connect to the RTS line.
M14	C108/DTR	I	Input for Data Terminal Ready (DTR) from DTE	1.8V	
N14	C109/DCD	O	Output for Data Carrier Detect (DCD) to DTE	1.8V	
P14	C107/DSR	O	Output for Data Set Ready (DSR) to DTE	1.8V	
R14	C125/RING	O	Output for Ring Indication (RI) to DTE	1.8V	

Table 18: Debug UART

Pin	Signal	I/O	Function	Type	Comment
Debug UART					

Pin	Signal	I/O	Function	Type	Comment
D15	DEBUG_UART_TXD	O	Debug UART transmit	1.8V	
E15	DEBUG_UART_RXD	I	Debug UART receive	1.8V	

Table 19: Bluetooth UART

Pin	Signal	I/O	Function	Type	Comment
Bluetooth UART					
F3	TXD1	I	Bluetooth UART Transmit	1.8V	Connect to the TXD line.
H3	RXD1	O	Bluetooth UART Receive	1.8V	Connect to the RXD line.
J3	CTS1	O	Bluetooth UART Clear to Send	1.8V	Connect to the CTS line.
K4	RTS1	I	Bluetooth UART Request to Send	1.8V	Connect to the RTS line.

Table 20: COEX UART

Pin	Signal	I/O	Function	Type	Comment
COEX UART					
M8	WCI_TX	O	Wireless coexistence interface TXD	1.8V	
M9	WCI_RX	I	Wireless coexistence interface RXD	1.8V	

Note: DCD, DTR, DSR, RI signals that are not used for UART functions can be configured as GPIO using AT commands.

Note: To avoid a back-powering effect, it is recommended to prevent any HIGH logic level signal from being applied to the module's digital pins when it is powered OFF or during an ON/OFF transition.

Note: The Debug UART is used as the SW main debug console. It is required to place test points on this interface even if not used.

Note: The DTR pin is used to control the UART and system sleep. Pulling the DTR pin down prevents the UART and the entire module from entering low power mode. DTR can be left floating if no used (DTR is internally pulled high).

Note: For minimum implementations, only the TXD and RXD lines need be connected. The other lines can be left open provided a software flow control is implemented.

Note: The FE910C04 supports BT/Wi-Fi and is only compatible with Qualcomm's QCA6174A-1(Wi-Fi 5) and WCN685x(Wi-Fi 6/6E) chipsets.

FE910C04 provides 1.8 V UART interfaces. Use a level shifter if the application is equipped with a 3.3 V UART interface.

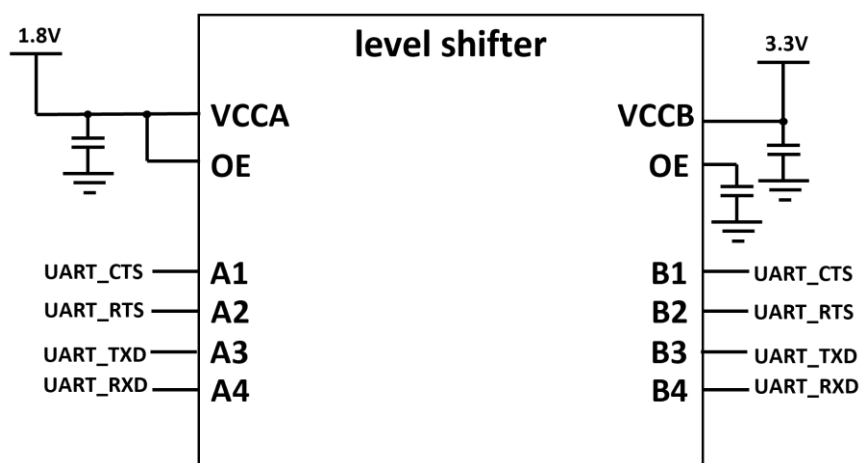


Figure 16: Level Shifter Schematic Example for UART

6.8.2.1 RS232 Level Translation

To interface the FE910C04 with a PC COM port or an RS232 (EIA/TIA-232) application, a level translator is required. This level translator must perform the following actions:

- Invert the electrical signal in both directions
- Change the level from 0/1.8 V to ± 15 V

The RS232 UART 16450, 16550, 16650 and 16750 chipsets accept signals with lower levels on the RS232 side (EIA/TIA-562), allowing a lower voltage-multiplying ratio on the level translator. Note that the negative signal voltage must be less than 0 V and hence some sort of level translation is always required.

The easiest way to translate the levels and invert the signal is by using a single chip-level translator. There are a multitude of them, differing in the number of drivers and receivers and in the levels (make sure to get a true RS232 level translator, not a RS485 or other standards).

By convention, the driver is the level translator from the 0 – 1.8 V UART to the RS232 level. The receiver is the translator from the RS232 level to 0 – 1.8 V UART. To translate the whole set of control lines of the UART, the following is required:

- 2 drivers
- 2 receivers

Warning: The digital input lines, operating at 1.8 V CMOS levels, have an absolute maximum input voltage of 2.0 V. The level translator IC outputs on the module side (i.e. FE910 inputs) will cause damage to

the module inputs if the level translator is powered with +3.8 V power. So, the level translator IC must be powered by a dedicated +1.8 V power supply.

As an example, RS232 level adaption circuitry could use a MAXIM transceiver (MAX218). In this case, the chipset is capable of translating directly from 1.8 V to the RS232 levels (example on 4 signals only).

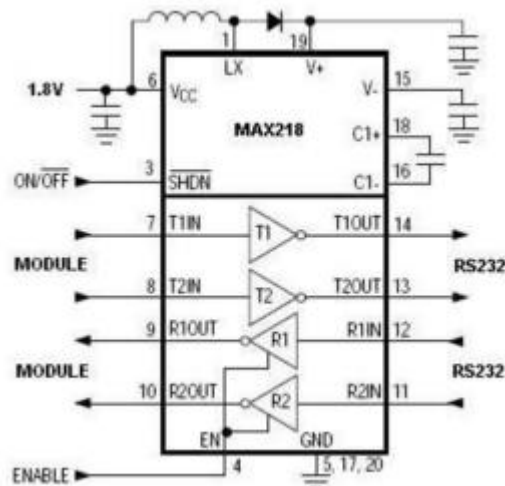


Figure 17: RS232 Level Adaption Circuitry Example

Note: In this case, the length of the lines on the application must be taken into account to avoid problems in the case of high-speed rates on RS232.

The RS232 serial port lines are usually connected to a DB9 connector as shown in the below figure. Signal names and directions are named and defined from the DTE point of view.

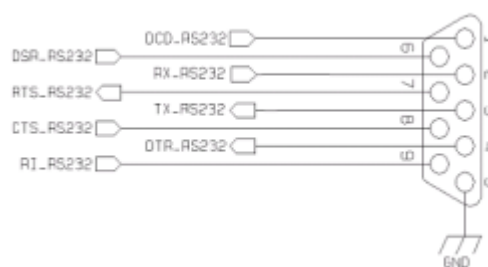


Figure 18: RS232 Serial Port Lines Connection Layout

6.8.3 I2C

The FE910C04 supports an I2C interface; the table below lists the I2C signals.

The I2C can also be used externally by the end customer application. FE910C04 supports I2C Master Mode only.

Table 21: I2C

Pin	Signal	I/O	Function	Type	Comment
I2C Interface					
B11	I2C_SCL	I/O	I2C clock	1.8V	Internal PU (2.2 KΩ)
B10	I2C_SDA	I/O	I2C Data	1.8V	Internal PU (2.2 KΩ)

6.8.4 I2S

The FE910C04 module supports a I2S(Bluetooth) interface.

Table 22: I2S

Pin	Signal	I/O	Function	Type	Comment
Bluetooth I2S					
B2	I2S_TX	O	Bluetooth I2S Data Output	1.8V	
B3	I2S_RX	I	Bluetooth I2S Data Input	1.8V	
B4	I2S_WS	I/O	Bluetooth I2S word select	1.8V	
B5	I2S_CLK	I/O	Bluetooth I2S clock	1.8V	

6.8.5 PCIe[TBD]

The FE910C04 module includes PCIe interface.

PCIe needs AC coupling series capacitors on the TX lines in both directions.

In order to interface PCIe with the application board that controls the modem, 220nF capacitors should be installed on PCIE_RX_P/M lines of the FE910C04. The series capacitors are already placed on PCIE_TX_P/M lines inside the FE910C04. Internally, 1.8V level 4.7k pull-up resistor is already mounted on PCIE_WAKE_N and PCIE_CLKREQ_N.

For the host PCIe three lines (WAKE, RESET, CLKREQ) pull-up resistance value, refer to the PCIe documentation and apply. (PCI Express Card Electromechanical Specification)

The suggested PCIe interface connection is shown in the diagram below:

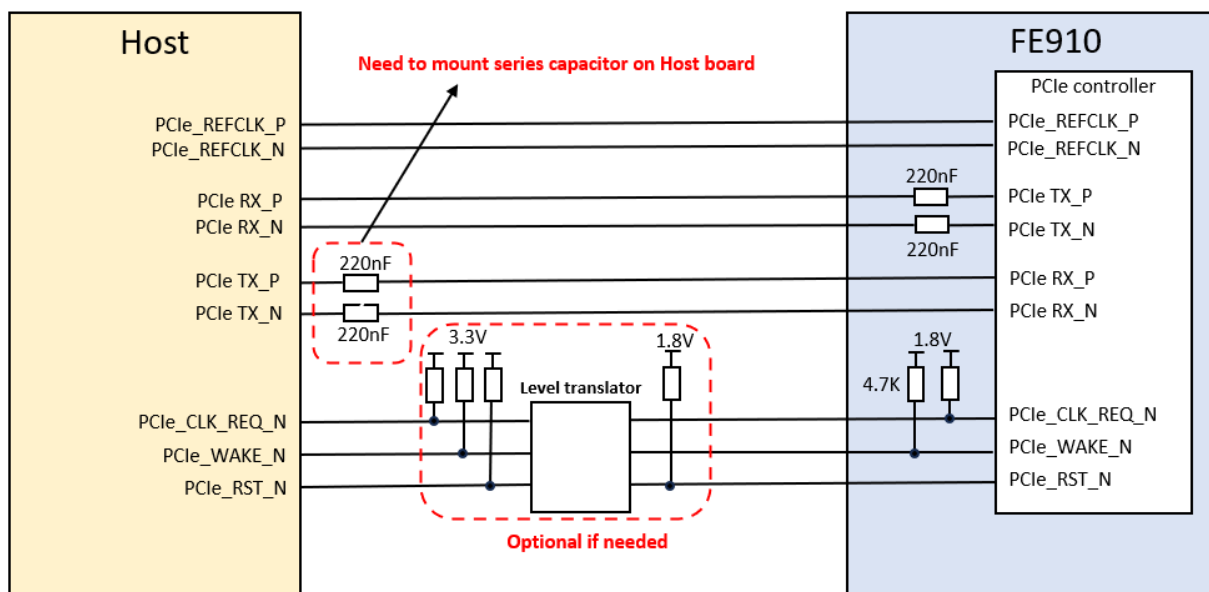


Figure 19: Connection for PCIe Interface

Note: The PCIe signal traces must be carefully routed: minimize trace lengths, number of vias, and capacitive loading. The impedance value should be as close as possible to 85 Ohm differential.

Table 23: PCIe Communication Port

Pin	Signal	I/O	Function	Type	Comment
PCIe Interface					
H15	PCIe_TX_P	O	PCIe receive - plus	Analog	
J15	PCIe_TX_N	O	PCIe receive - minus	Analog	
J14	PCIe_RX_P	I	PCIe receive - plus	Analog	
K14	PCIe_RX_N	I	PCIe receive - minus	Analog	
D10	PCIe_REFCLK_P	I/O	PCIe differential reference clock - plus	Analog	
D11	PCIe_REFCLK_N	I/O	PCIe differential reference clock - Minus	Analog	
D13	PCIe_CLK_REQ_N	I/O	PCIe reference clock request signal	1.8V	Internal PU (4.7 KΩ)
D14	PCIe_WAKE_N	I/O	PCIe wake up	1.8V	Internal PU (4.7 KΩ)
C14	PCIe_RST_N	I/O	PCIe reset	1.8V	

6.8.5.1 PCIe Layout Guidelines

The below guidelines will provide general guidelines for the PCIe interface to improve signal integrity.

- All other sensitive/high-speed signals and circuits must be protected from PCIe corruption.
- PCIe signals must be protected from noisy signals (clocks, SMPS, and so forth)
- Pay extra attention to crosstalk, ISI, and intraplane skew and impedance discontinuities.
- PCIe Tx AC coupling capacitors are better placed close to the source or receiver side to keep good SI of route on PCB.
- Each trace needs to be adjacent to a ground plane.
- To maintain impedance balance, maintain positive and negative traces as balanced as possible in terms of the signal and its return path.
- Avoid broadside coupling and routing a signal trace directly over another signal trace.
- External capacitors also should keep differential traces. Ensure not to stagger the capacitors. This can affect the differential integrity of the design and can create EMI.

Table 24: PCIe requirement

Type of guidance	Guideline	Requirement
General	Data rate	5 Gbps
	Impedance	85 ohms differential
	Bus length	Max 200 mm
Length matching	Intra-pair length match	0.7 mm
Spacing	Lane to other signals	4 x line width

Type of guidance	Guideline	Requirement
	Rx to Tx	3 x line width
Component	AC capacitance	220 nF

6.8.6 SGMII

The FE910C04 includes an integrated Ethernet MAC with an SGMII interface, with the following key features:

- This interface can be directly connected to external Ethernet devices which use SGMII interface. The Ethernet PHY chipset supports Qualcomm QEP8111 chipset(or other Ethernet PHY solutions).
- When enabled, an additional network interface will be available to the Linux kernel.
- When using an external PHY for Ethernet connectivity, the FE910C04 also includes the control interface for managing the external PHY.

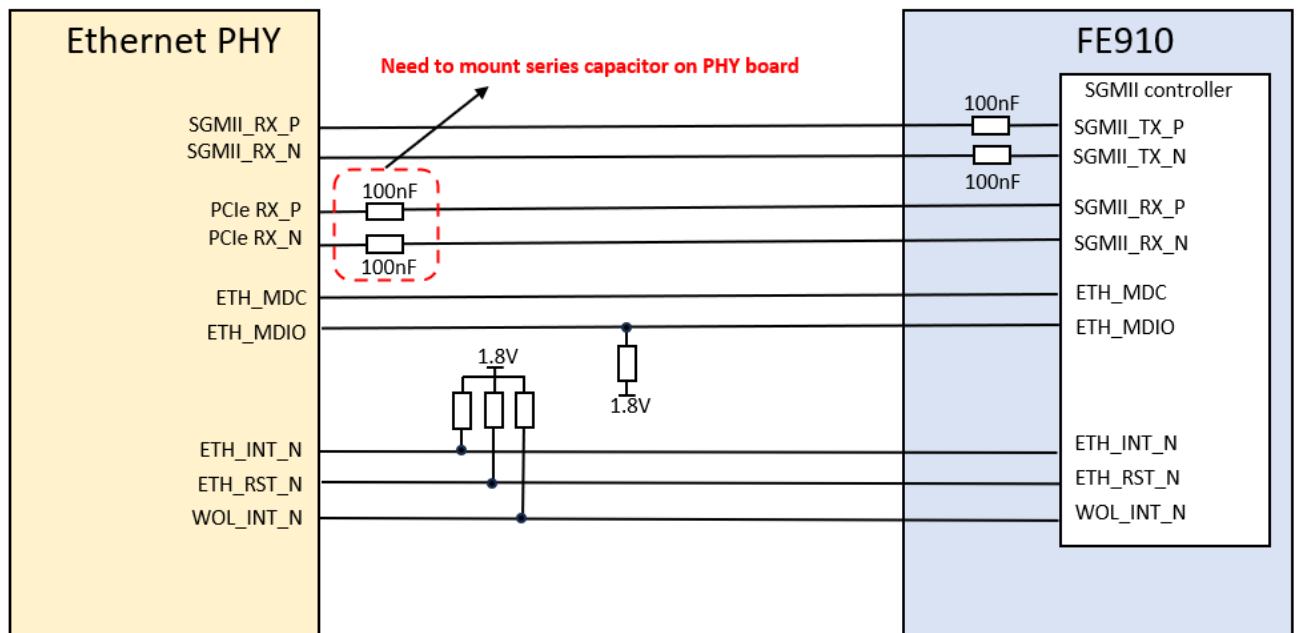


Figure 20: Connection for SGMII Interface

Table 25: SGMII

Pin	Signal	I/O	Function	Type	Comment
SGMII Interface					
D5	SGMII_TX_P	AO	SGMII transmit – plus	PHY	
D6	SGMII_TX_N	AO	SGMII transmit – minus	PHY	
E4	SGMII_RX_P	AI	SGMII receive – plus	PHY	
F4	SGMII_RX_N	AI	SGMII receive – minus	PHY	
C7	ETH_INT_N	I	Interrupt from Ethernet PHY	1.8V	Active low. Connect an external pull-up resistor.
D9	ETH_MDC	O	MAC to PHY Clock	1.8V	
A8	ETH_MDIO	I/O	MAC to PHY Data	1.8V	
A9	ETH_RST_N	O	Reset to Ethernet PHY	1.8V	Active low

Pin	Signal	I/O	Function	Type	Comment
					Connect an external pull-up resistor.
A10	ETH_PWR_EN	O	External power IC enable control pin for Ethernet PHY	1.8V	
D8	WOL_INT_N	I	Wake on LAN Interrupt	1.8V	Active low Connect an external pull-up resistor.

6.8.6.1 SGMII Layout Guidelines

The below guidelines will provide general guidelines for the SGMII interface to improve signal integrity.

- All other sensitive/high-speed signals and circuits must be protected from SGMII corruption.
- SGMII signals must be protected from noisy signals (clocks, SMPS, and so forth)
- Pay extra attention to crosstalk, ISI, and intraplane skew and impedance discontinuities.
- SGMII Tx AC coupling capacitors are better placed close to the source or receiver side to keep good SI of route on PCB.
- To maintain impedance balance, maintain positive and negative traces as balanced as possible in terms of the signal and its return path.
- Trace length matching between the reference clock, Tx, and Rx pairs are not required.
- External capacitors also should keep differential traces. Ensure not to stagger the capacitors. This can affect the differential integrity of the design and can create EMI.

Table 26: SGMII requirement

Type of guidance	Guideline	Requirement
General	Data rate	1.25 Gbps
	Impedance	90 ohms differential
	Bus length	Max 90 mm
Length matching	Intra-pair length match	0.7 mm
Spacing	Lane to other signals	3 x line width
	Rx to Tx	2 x line width
Component	AC capacitance	100 nF

6.8.7 SDIO[TBD]

The FE910C04 provides an SDIO port supporting the SDIO3.0 specification, which can be used to interface with a Wi-Fi chipset (Qualcomm QCA6174 chipset or other Wi-Fi solutions). The FE910C04 module includes an integrated SW driver to support the Qualcomm QCA6174 chipset. The FE910C04 module supports an Wi-Fi coexistence mechanism via the WCI (Wireless Coexistence Interface) port, which connects between the module and the external Wi-Fi IC.

Table 27: SDIO

Pin	Signal	I/O	Function	Type	Comment
SDIO(WiFi) Interface					
N13	WiFi_SD_CMD	O	Wi-Fi SD Command	1.8V	
L13	WiFi_SD_CLK	O	Wi-Fi SD Clock	1.8V	
J13	WiFi_SD_DATA0	I/O	Wi-Fi SD Serial Data 0	1.8V	
M13	WiFi_SD_DATA1	I/O	Wi-Fi SD Serial Data 1	1.8V	
K13	WiFi_SD_DATA2	I/O	Wi-Fi SD Serial Data 2	1.8V	
H13	WiFi_SD_DATA3	I/O	Wi-Fi SD Serial Data 3	1.8V	
L12	WiFi_SDRST	O	Wi-Fi Reset / Power enable control	1.8V	
M11	WiFi_SLEEP_CLK	O	Wi-Fi Sleep clock output(32.768KHz)	1.8V	
M10	RFCLK2	O	Wi-Fi clock output(38.4MHz)	1.8V	
L4	WOW	I	Wake On WLAN	1.8V	Active Low
M8	WCI_TX	O	Wireless coexistence interface TXD	1.8V	
M9	WCI_RX	I	Wireless coexistence interface RXD	1.8V	

6.8.7.1 Wi-Fi Coexistence[TBD]

The FE910C04 supports a Wi-Fi Coexistence interface; the table below lists the Wi-Fi Coexistence signals. Please note that some signals are alternate signals.

Table 28: Wi-Fi Coexistence

Pin	Signal	I/O	Function	Type	Comment
Wi-fi Coexistence					
M8	WCI_TX	O	Wireless coexistence interface TXD	1.8V	
M9	WCI_RX	I	Wireless coexistence interface RXD	1.8V	
J4	WLAN_TX_EN_TO_N79	I	Input to N79. N79 puts its LNA in isolation mode when this signal is high and frequency.	1.8V	
M5	N79_TX_EN_TO_WLAN	O	Output from N79. Wi-Fi puts its LNA in isolation mode when this signal is high and frequency.	1.8V	

6.8.8 DVI

The Hardware Design Guide module supports a digital audio interface.

The Hardware Design Guide module can be connected to an external codec through the digital interface. The product provides a single Digital Audio Interface (DVI) on the following pins:

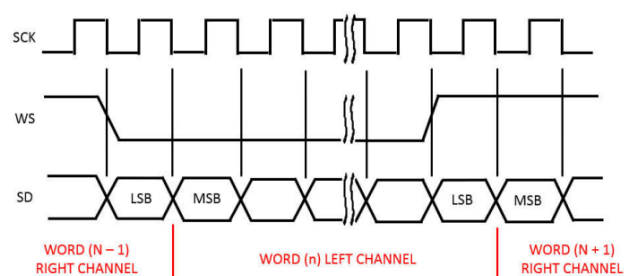
Table 29: DVI

Pin	Signal	I/O	Function	Type	Comment
Digital Voice Interface (DVI)					
B9	DVI_WAO	O	Digital Voice interface (WAO master output)	1.8V	
B6	DVI_RX	I	Digital Voice interface (Rx)	1.8V	
B7	DVI_TX	O	Digital Voice interface (Tx)	1.8V	

Pin	Signal	I/O	Function	Type	Comment
B8	DVI_CLK	O	Digital Voice interface (CLK master output)	1.8V	
B12	REF_CLK	O	Reference clock for external Codec (Audio Master clock)	1.8V	

6.8.8.1 DVI(I2S) Digital Audio Diagram

High-level I2S timing



I2S timing details – Tx & Rx

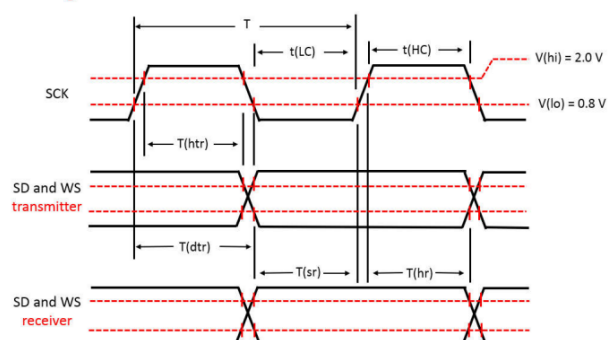


Figure 21: DVI(I2S) Timing Diagram

Table 30: I2S Interface Timing

Parameter	Description	Min	Typ	Max	Unit
Using internal SCK					
f	Frequency	-	-	12.288	MHz
T	Clock period	81.380	-	-	ns
t(HC)	Clock high	0.45*T	-	0.55*T	ns
t(LC)	Clock low	0.45*T	-	0.55*T	ns
t(sr)	SD and WS input setup time	16.276	-	-	ns
t(hr)	SD and WS input hold time	0	-	-	ns
t(dtr)	SD and WS output delay	-	-	65.100	ns
t(htr)	SD and WS output hold time	0	-	-	ns
Using external SCK					
f	Frequency	-	-	12.288	MHz
T	Clock period	81.380	-	-	ns
t(HC)	Clock high	0.45*T	-	0.55*T	ns
t(LC)	Clock low	0.45*T	-	0.55*T	ns
t(sr)	SD and WS input setup time	16.276	-	-	ns
t(hr)	SD and WS input hold time	0	-	-	ns

6.9 General Purpose I/O

The general-purpose I/O pads can be configured to act in three different ways:

- Input
- Output
- Alternative function (internally controlled)

Input pads can only be read, reporting digital values (high / low) present on the pad at the time of reading. Output pads can only be written or queried and set values on the pad output. Alternative function pads can be controlled internally by FE910C04 firmware and act according to the implementation.

The following GPIOs are always available as a primary function on the FE910C04.

Table 31: Primary GPIOs

Pin	Signal	I/O	Function	Type	Comment
General-Purpose I/O					
C8	GPIO_1	I/O	GPIO_1 / STAT_LED	1.8V	Default STAT_LED
C9	GPIO_2	I/O	GPIO_2	1.8V	
C10	GPIO_3	I/O	GPIO_3	1.8V	
C11	GPIO_4	I/O	GPIO_4	1.8V	
B14	GPIO_5	I/O	GPIO_5	1.8V	
C12	GPIO_6	I/O	GPIO_6	1.8V	
C13	GPIO_7	I/O	GPIO_7	1.8V	
K15	GPIO_8	I/O	GPIO_8 / SW_RDY	1.8V	Default SW_RDY
L15	GPIO_9	I/O	GPIO_9	1.8V	
G15	GPIO_10	I/O	GPIO_10	1.8V	

6.9.1 Using a GPIO as an INPUT

GPIO pads used as inputs can also be used as an interrupt source for software.

In general, all GPIO pads can also be used as an interrupt.

However, not all GPIO's can be used as a wakeup source of the module (wakeup from sleep). Only the following GPIO's can be used for waking up the system from sleep:

- GPIO_1
- GPIO_2
- GPIO_3
- GPIO_4
- GPIO_5
- GPIO_8

6.9.2 Using a GPIO as an OUTPUT

GPIO pads, when used as outputs, can drive 1.8V CMOS digital devices or compatible hardware. When set as outputs, the pads have a push-pull output, and therefore the pull-up resistor can be omitted.

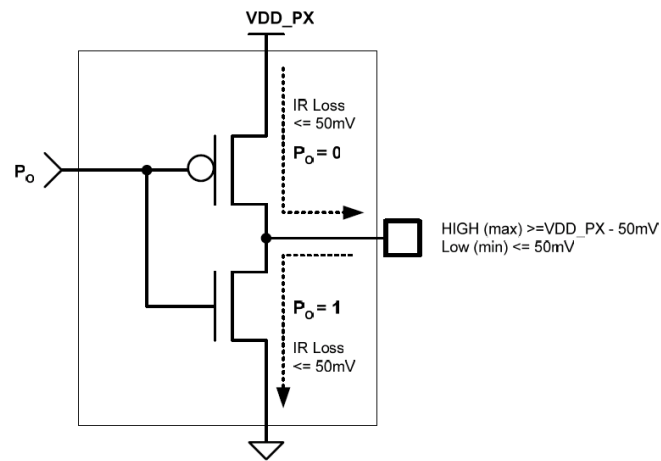


Figure 22: GPIO Output Pad Equivalent Circuit

6.10 External SIM Holder

The FE910C04 supports both Class B (2.95 V) and Class C (1.8 V), and a dual-SIM single-standby function is supported.

Table 32: USIM 1 and 2 Interfaces

PAD	Signal	I/O	Function	Type	Comment
SIM Card Interface 1					
A6	SIMCLK1	O	External SIM 1 signal – Clock	1.8/2.95V	
A7	SIMRST1	O	External SIM 1 signal – Reset	1.8/2.95V	
A5	SIMIO1	I/O	External SIM 1 signal - Data I/O	1.8/2.95V	Internal PU (20 KΩ)
A4	SIMIN1	I	External SIM 1 signal - Presence	1.8V	Internal PU (100 KΩ)
A3	SIMVCC1	-	External SIM 1 signal – Power supply for SIM 1	1.8/2.95V	
SIM Card Interface 2					
C1	SIMCLK2	O	External SIM 2 signal – Clock	1.8/2.95V	
D1	SIMRST2	O	External SIM 2 signal – Reset	1.8/2.95V	
C2	SIMIO2	I/O	External SIM 2 signal – Data I/O	1.8/2.95V	Internal PU (20 KΩ)
G4	SIMIN2	I	External SIM 2 signal – Presence	1.8V	Internal PU (100 KΩ)
D2	SIMVCC2	-	External SIM 2 signal – Power supply for SIM 2	1.8/2.95V	

Note: SIM2 can be assigned as an optional eSIM. In that case, UIM2 can't be used as an external SIM interface.

Note: FE910C04 module contains an internal pull-up resistor on SIMIOx, SIMINx. It is not necessary to install an external pull-up resistor.

Note: By default, the USIMx_DET pin is set to active low (inserted). As a result, when the USIMx_DET input is changed from logic 1 to logic 0, the FE910C04 will detect USIM card insertion. If it is required to change the USIM_DET pin to active high (inserted), please refer to AT#SIMINCFG of FE910C04 AT commands reference guide. To change the default value stored within the firmware without sending AT commands at each power-up, contact Telit Cinterion technical support.

6.10.1 SIM Schematic Example

Figure 23 shows how to design the application side and what values to assign to the components.

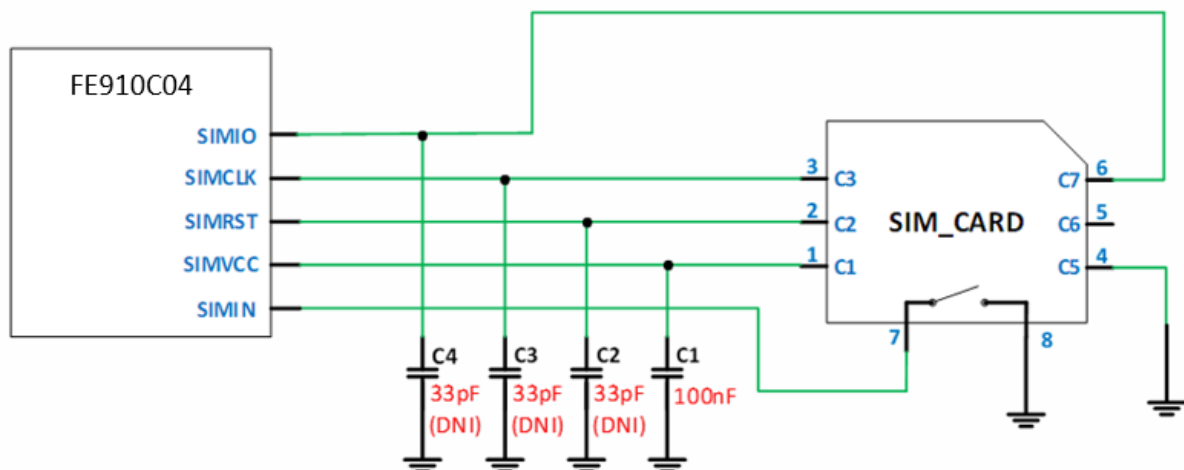


Figure 23: SIM Schematic example

6.10.2 eSIM[TBD]

FE910C04 module includes pad for an optional embedded SIM (DFN-8 package).

Customers interested in using an embedded SIM mounted on the FE910C04 can contact Telit Technical Support at:

- TS-EMEA@telit.com
- TS-AMERICAS@telit.com
- TS-APAC@telit.com
- TS-SRD@telit.com
- TS-ONEEDGE@telit.com

Alternatively, use: <https://www.telit.com/contact-us/>

6.11 Miscellaneous Functions

6.11.1 Indication of Network Service Availability

The STAT_LED(GPIO_1) pin status shows information on the network service availability and call status. In the FE910C04 module, the STAT_LED usually needs an external transistor to drive an external LED.

See the AT Command User Guide for details on the AT#SLED section.

Table 33: Network Service Availability Indication

LED Status		Device Status
Permanently off		Device off
Blinking	Blinking 1s on and 2s off	Registered in idle
	Blinking time depends on network condition in order to minimize power consumption	Registered in idle with power saving
Permanently on		Not registered

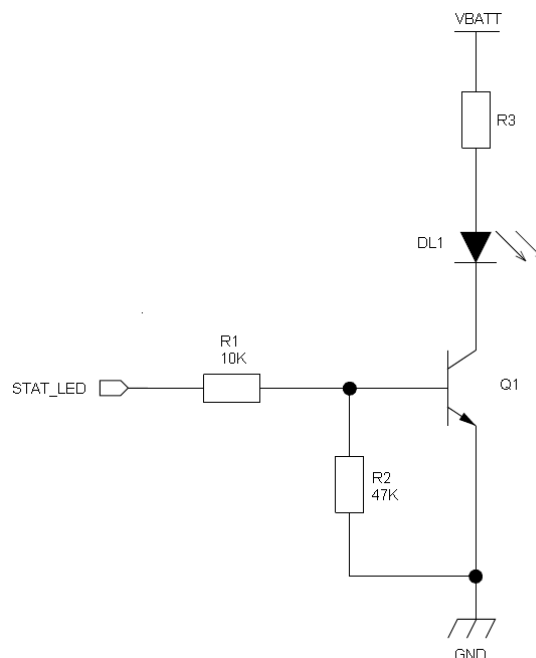


Figure 24: Status LED Circuit Example

6.11.2 Indication of Software Ready

The SW_RDY(GPIO_8) signal provides indication about the module's ability to receive commands. As long as the SW_RDY is asserted low, it indicates that the FE910C04 has not finished booting yet. Once the SW_RDY is asserted high, it indicates that the FE910C04 is ready to receive commands.

6.11.3 DPR

This signal is an input directly to the FE910C04 module from a suitable SAR sensor. Then FE910C04 module will reduce output TX power. DPR function is not available yet: specific implementation will be determined on customer request. For further information on the DPR function on FE910C04 module, please contact Telit Technical Support at:

- TS-EMEA@telit.com

- TS-AMERICAS@telit.com
- TS-APAC@telit.com
- TS-SRD@telit.com
- TS-ONEEDGE@telit.com

Alternatively, use: <https://www.telit.com/contact-us/>

6.11.4 ADC Converter

The FE910C04 module provides three on-board 16-bit Analog to Digital Converters. Each ADC reads the voltage level applied to the relevant pin, the accuracy is about 20mv@1.8v.

Table 34: ADC

Pin	Signal	I/O	Function	Type	Comment
ADC					
B1	ADC_IN1	AI	Analog/Digital Converter Input 1	Analog	
H4	ADC_IN2	AI	Analog/Digital Converter Input 2	Analog	
D7	ADC_IN3	AI	Analog/Digital Converter Input 3	Analog	

Table 35: ADC parameters

Item	Min	Max	Units
Input voltage range	0	1.875V	Volt

6.11.4.1 Using ADC Converter

AT command is available to use the ADC function.

The command is AT#ADC? The read value is expressed in mV.

Please refer to FE910C04 AT command user guide for the full description of this function.

6.12 USB PCIe boot Switch

This chapter describes the USB_PcIe boot mode switch functions.

Table 36: Miscellaneous Functions

Pin	Signal	I/O	Function	Type	Comment
Miscellaneous Functions					
P12	USB_PcIe_SW	I	PCle / USB interface boot switch OPEN(Internal Pull-Up) : USB LOW : PCle	1.8V	Internal PU (1 KΩ)

Note: USB mode : There is a internal pull-up 1.8V the module.
Do not use external pull-up 1.8V.

FE910C04 determines the host interface by checking the status of USB_PcIe_SW pin at the beginning of the power on sequences. A dual TR is designed inside the module, so boot is switched depending on the high/low status of USB_PcIe_SW (PAD P12).

- OPEN(Internal Pull-Up): USB boot mode
- LOW: PCle boot mode

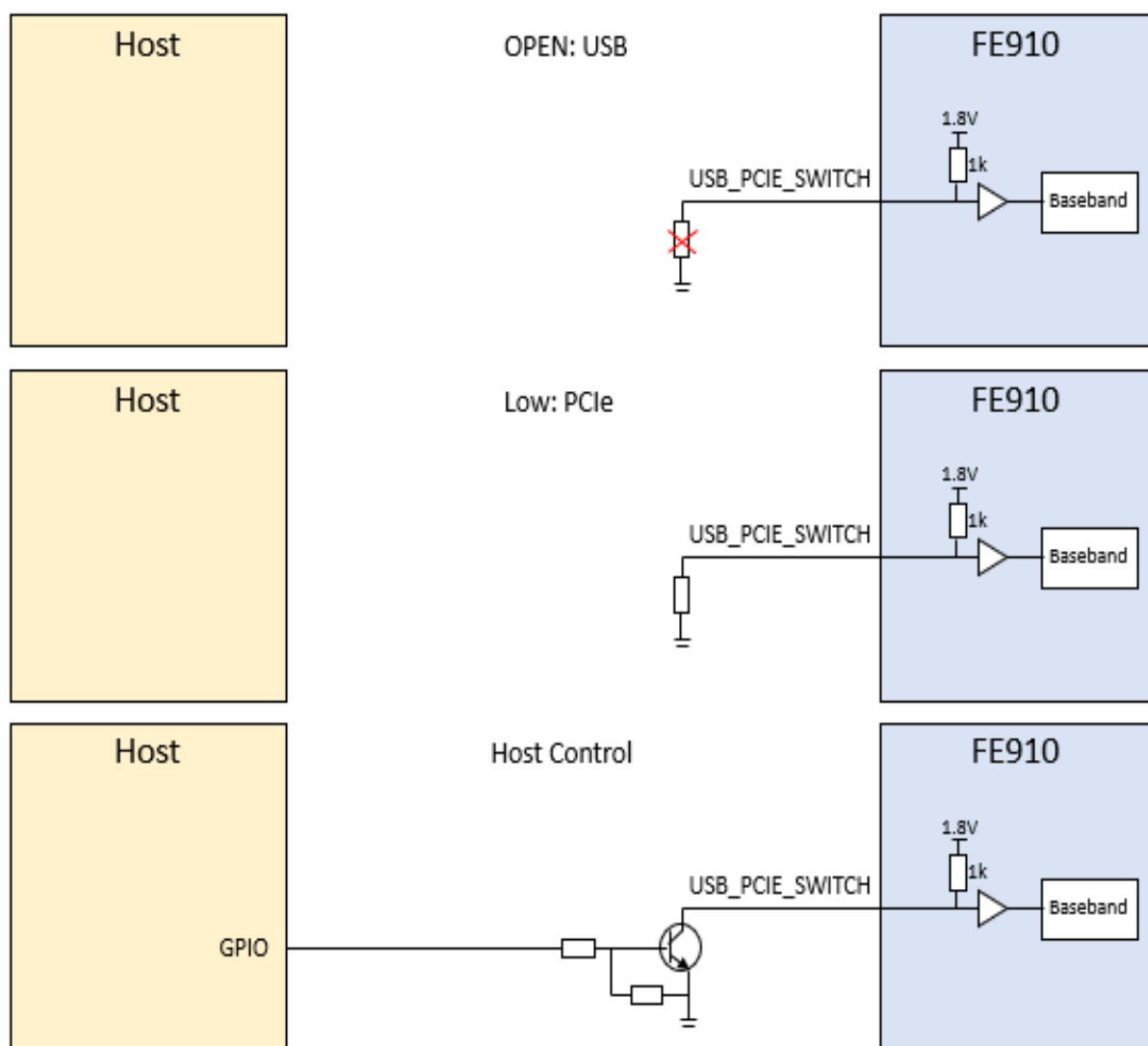


Figure 25: Example Schematic for USB PCIe Switch function

6.13 USB Boot

Emergency boot download mode is case of corrupted boot image has been flashed into the device or in case all other recovery modes failed to work.

The emergency download mode is triggered by FORCED_USB_BOOT signal (Pad F14). Asserting this signal high (1.8 V) during boot will force the system into emergency download.

In some cases of firmware upgrade FORCED_USB_BOOT pin must be set to 1.8V during power-on of FE910C04.

Table 37: Miscellaneous Functions

Pin	Signal	I/O	Function	Type	Comment
Miscellaneous Functions					
F14	USB_BOOT	I	Forced USB BOOT – emergency download	1.8V	

6.14 VAUX PWRMON

A regulated power supply output is provided to supply small devices from the module.

This output is active when the module is ON and turns OFF when the module is shut down. The operating range characteristics of the supply are as follows:

Table 38: Operating Range – VAUX Power Supply

Parameter	Min	Typical	Max	Units
Output voltage	1.75	1.80	1.85	Volts
Output current			100	mA
Output bypass capacitor (within the module)			1	uF

7 RF Section

7.1 Bands Variants

Table below summarizes all region variants within the FE910C04 family, showing the band sets supported in each variant.

Table 39: Bands Variant

Region Variant	LTE FDD	LTE TDD	NR FDD	NR TDD	GNSS
FE910C04-WW FE910C04-WWD	B1, B2, B3, B4, B5, B7, B8, B12, B13, B14, B17, B18, B19, B20, B25, B26, B28, B30, B66, B70, B71, B106	B34, B38, B39, B40, B41, B42, B43, B48	n1, n2, n3, n5, n7, n8, n12, n13, n14, n18, n20, n25, n26, n28, n30, n66, n70, n71	n38, n40, n41, n48, n77, n78, n79	GNSS L1/L5

7.2 Conducted Transmit Output Power

TX power follows the measurement conditions and specifications defined in 3GPP.

Table 40: Conducted Transmit Output Power

Band	Power class	RF Power (dBm) Nominal ¹⁾
5G NR Sub-6 n1, n2, n3, n5, n7, n8, n12, n13, n14, n18, n20, n25, n26, n28, n30 ³⁾ , n38, n40, n41, n48 ²⁾ , n66, n70, n71, n77, n78, n79	3 (0.2W)	23
LTE All Bands B1, B2, B3, B4, B5, B7, B8, B12, B13, B14, B17, B18, B19, B20, B25, B26, B28, B30 ³⁾ , B34, B38, B39, B40, B41, B42 ²⁾ , B43 ²⁾ , B48 ²⁾ , B66, B70, B71, B106	3 (0.2W)	23
LTE B41, B42 Supports Power Class 2	2 (0.4W)	26

Note: ¹⁾ RF Power Nominal : Max output power tolerance according to 3GPP TS 38.521-1, 3GPP TS 36.521-1 and 3GPP TS 34.121-1 or better

Note: ²⁾ LTE B42, B43, B48 / NR n48 : PC 3 Nominal RF Power 22dBm
These bands may show lower power due to Country-type approvals constraints

Note: ³⁾ LTE B30 / NR n30 : PC 3 Nominal RF Power 22dBm
These bands may show lower power due to Country-type approvals constraints

7.3 Conducted Receiver Sensitivity

The Sensitivity of the receiver follows the measurement conditions and specifications defined by 3GPP.

Table 41: 3GPP Compliance for Conducted Receiver Sensitivity

Technology	3GPP Compliance
4G LTE	Throughput >95%, According to 3GPP 36.521-1
5G NR Sub-6	Throughput >95%, According to 3GPP 38.521-1

FE910C04-WW/FE910C04-WWD

Table 42: LTE Typical RX sensitivity levels

E-UTRA Band	Typical Conducted Rx Sensitivity (dBm) *				
	BW(MHz)	PRx	DRx	Combined	3GPP
LTE FDD B1	10	-99	-100	-102.5	-97
LTE FDD B2	10	-99.5	-100	-103	-95
LTE FDD B3	10	-99	-100.5	-103	-94
LTE FDD B4	10	-99	-100	-102.5	-97
LTE FDD B5	10	-99.5	-100.5	-103	-95
LTE FDD B7	10	-99	-100	-102.5	-95
LTE FDD B8	10	-99	-100	-102.5	-94
LTE FDD B12	10	-99	-100	-103	-94
LTE FDD B13	10	-99.5	-101	-103.5	-94
LTE FDD B14	10	-99.5	-101	-103.5	-94
LTE FDD B17	10	-99	-100	-103	-94
LTE FDD B18	10	-99	-100.5	-103	-97
LTE FDD B19	10	-99	-100.5	-102.5	-97
LTE FDD B20	10	-99	-100.5	-103	-94
LTE FDD B25	10	-99.5	-100.5	-103	-93.5
LTE FDD B26	10	-99.5	-100.5	-103	-94.5
LTE FDD B28	10	-98.5	-100.5	-102.5	-95.5
LTE FDD B30	10	-97.5	-100	-102	-96
LTE TDD B34	10	-99	-99.5	-102	-97
LTE TDD B38	10	-97.5	-99.5	-101.5	-97
LTE TDD B39	10	-98.5	-100	-102	-97
LTE TDD B40	10	-97	-99.5	-101.5	-97
LTE TDD B41	10	-97	-99	-101	-95
LTE TDD B42	10	-98.5	-97	-100.5	-96
LTE TDD B43	10	-98.5	-97	-100.5	-96
LTE TDD B48	10	-98.5	-97	-100.5	-96
LTE FDD B66	10	-99	-100	-102.5	-96.5
LTE FDD B70	10	-97	-100	-102	-97
LTE FDD B71	10	-99.5	-100	-103	-94.2
LTE TDD B106	3	-105.5	-106.5	-109	-99.2

***3.8 Voltage / Room temperature**

Table 43: NR Typical sensitivity levels

NR Band	Typical Conducted Rx Sensitivity (dBm) *					
	BW(MHz)	SCS(kHz)	PRx	DRx	Combined	3GPP

NR FDD n1	20	15	-97	-98	-100	-93.8
NR FDD n2	20	15	-96.5	-98	-100	-91.8
NR FDD n3	20	15	-96.5	-98	-100	-90.8
NR FDD n5	20	15	-97	-98.5	-100.5	-86.8
NR FDD n7	20	15	-96.5	-98	-100	-91.8
NR FDD n8	20	15	-97	-98	-100	-85.8
NR FDD n12	15	15	-98	-99.5	-101.5	-84
NR FDD n13	10	15	-100	-101.5	-103.5	-93.8
NR FDD n14	10	15	-100	-101.5	-103.5	-93.8
NR FDD n18	15	15	-98	-99.5	-101.5	Not defined
NR FDD n20	20	15	-97	-98.5	-100.5	-89.8
NR FDD n25	20	15	-96.5	-98	-100	-90.3
NR FDD n26	20	15	-97	-98.5	-100.5	-87.6
NR FDD n28	20	15	-96.5	-98.5	-100.5	-90.8
NR FDD n30	10	15	-97	-100	-101	-95.8
NR TDD n38	20	30	-95.5	-98	-99.5	-94
NR TDD n40	20	30	-95.5	-97.5	-99.5	-94
NR TDD n41	20	30	-95.5	-98	-99.5	-92
NR TDD n48	20	30	-97	-96	-99	-92.9
NR FDD n66	20	15	-97	-97.5	-100	-93.3
NR FDD n70	15	15	-96	-99.5	-100.5	-95
NR FDD n71	20	15	-97	-98.5	-100.5	-86
NR TDD n77	20	30	-96.5	-95	-98.5	-92.2
NR TDD n78	20	30	-96.5	-95.5	-98.5	-92.7
NR TDD n79	20	30	-96	-95	-98	-92.7

*3.8 Voltage / Room temperature

Note: The sensitivity level may present a deviation of approximately +/- 2dB depending on model, device and channel; the level shown is the typical value.

7.4 LTE/5G Sub-6 Antenna Requirements

The antenna connection and board layout design are the most important aspect of the full product design as they strongly affect the general performance of the product, so read carefully and follow the requirements and the guidelines for a proper design.

The antenna and antenna transmission line on PCB for a Telit FE910C04 device shall fulfil the following requirements:

Table 44: LTE/ 5G Sub-6 Antenna Requirements

Item	Value
Frequency range	Depending on the frequency band(s) provided by the network operator, the customer shall use the most suitable antenna for that/those band(s)
Bandwidth	See Section 13 Reference Table of RF Bands Characteristics.
Impedance	50 ohm
Input power	Power Class 3: > 23dBm Average power Power Class 2: > 26dBm Average power
VSWR absolute max	≤ 10:1 (limit to avoid permanent damage)
VSWR recommended	≤ 2:1 (limit to fulfil all regulatory requirements)

7.4.1 LTE/5G Sub-6 Antenna PCB Line Guidelines

When using the FE910C04, since there's no antenna connector on the module, the antenna must be connected to the FE910C04 antenna pad (K1, F1, R9) by means of a transmission line implemented on the PCB.

This transmission line shall fulfil the following requirements:

Table 45: Antenna Line on PCB Requirements

Item	Value
Characteristic Impedance	50 ohm (+-10%)
Max Attenuation	0.3 dB
Coupling	Coupling with other signals shall be avoided
Ground Plane	The cold End (Ground Plane) of the antenna shall be equipotential to the FE910C04 ground pins

The transmission line should be designed according to the following guidelines:

- Make sure that the transmission line's characteristic impedance is 50 ohm.
- Keep the line on the PCB as short as possible, since the antenna line loss shall be less than about 0.3 dB.
- The geometry of the line must have uniform characteristics, constant cross-section, and avoid meanders and abrupt curves.
- Any kind of suitable geometry/structure (Microstrip, Stripline, Coplanar, Grounded Coplanar Waveguide...) can be used to implement the printed transmission line relating to the antenna.
- If a Ground plane is required in the geometry of the line, this plane must be continuous and sufficiently extended, so that the geometry can be as similar as possible to the related canonical model.
- Keep, if possible, at least one layer of the PCB used only for the Ground plane; If possible, use this layer as a reference Ground plane for the transmission line;
- It is advisable to surround (on both sides) the PCB transmission line with Ground, avoiding that other signal tracks face directly the antenna line track.
- Avoid crossing any un-shielded transmission line footprint with other signal tracks on different layers.
- The ground surrounding the antenna line on the PCB must be tightly connected to the main Ground Plane through holes (at least once every 2mm), placed near the edges of the ground facing the line track.
- Place EM noisy devices as far as possible from the FE910C04 antenna line.
- Keep the antenna line far away from the FE910C04 power supply lines.
- If EM noisy devices (such as fast switching ICs, LCD and so on) are present on the PCB hosting the FE910C04, take care of the shielding of the antenna line by burying it in an inner layer of PCB and surrounding it with the Ground planes, or shield it with a metal frame cover.
- If EM noisy devices are not present around the line, the use of geometries such as Microstrip or Grounded Coplanar Waveguide is preferable, since they typically ensure less attenuation if compared to a Stripline of the same length.

The following image shows the suggested layout for the Antenna pad connection:

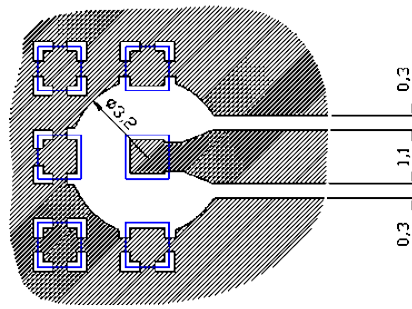


Figure 26: Layout for the Antenna Pad Connection

7.4.2 PCB Guidelines in Case of FCC Certification

If FCC certification is required for an application using FE910C04, according to FCC KDB 996369 for modular approval requirements, the transmission line must be similar to the one implemented on the FE910C04 interface board and described in the following chapter.

7.4.2.1 Transmission Line Design

When designing the FE910C04 interface board, the placement of components was chosen properly, to keep the length of the line as short as possible, thus leading to the lowest possible power losses. A Grounded Coplanar Waveguide (G-CPW) line has been chosen since this kind of transmission line ensures good impedance control and can be implemented in an outer PCB layer as needed in this case. An SMA female connector has been used to feed the line.

The interface board is made on an FR4, 4-layer PCB. The substrate material is characterized by relative permittivity $\epsilon_r = 4.6 \pm 0.4$ @ 1 GHz, $\tan \delta = 0.019$ to 0.026 @ 1 GHz.

A characteristic impedance of nearly 50 ohm is achieved using a track width = 1.1 mm, and clearance from a coplanar ground plane = 0.3 mm on each side. The line uses the reference ground plane on layer 3, while copper is removed from layer 2 below the line. The height of the trace above the ground plane is 1.335 mm. The calculated characteristic impedance is 51.6 ohm, and the estimated line loss is less than 0.1 dB.

The line geometry is shown below:

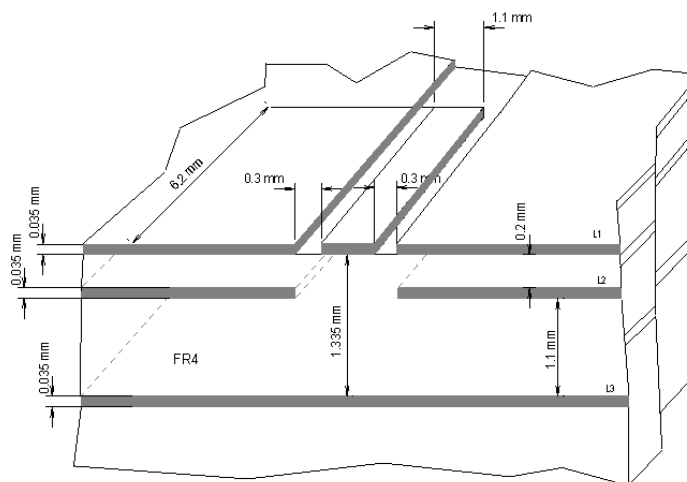


Figure 27: Line Geometry

7.4.2.2 Transmission Line Measurements

An E5071C Keysight (Full-2-port calibration) was used in this measurement session.

A calibrated coaxial cable was soldered to the pad corresponding to the RF output; an SMA connector was soldered to the board to characterize the losses of the transmission line including the connector itself. During Return Loss/impedance measurements, the transmission line has been terminated to a 50-ohm load.

The return Loss plot of the line under test is shown below:

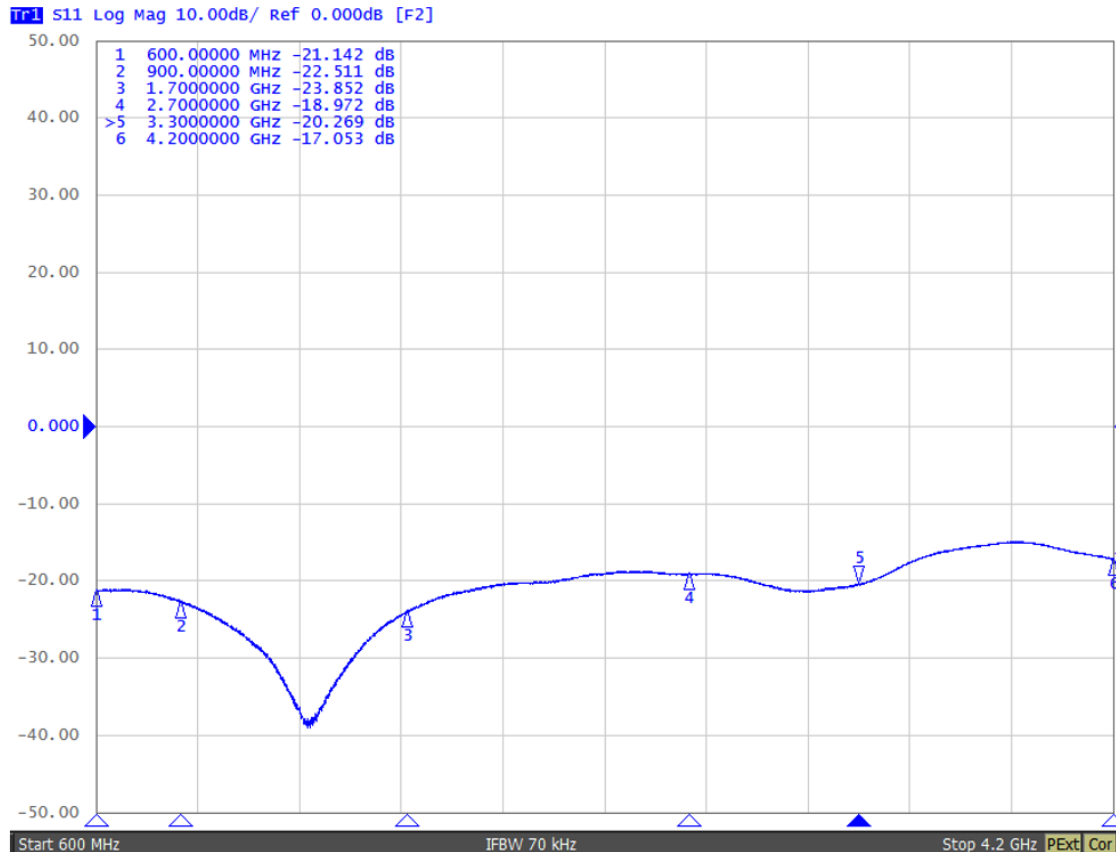


Figure 28: Return Loss plot of the line under test

The input impedance of the line (in Smith Chart format, once the line has been terminated to a 50-ohm load) is shown in the following figure:

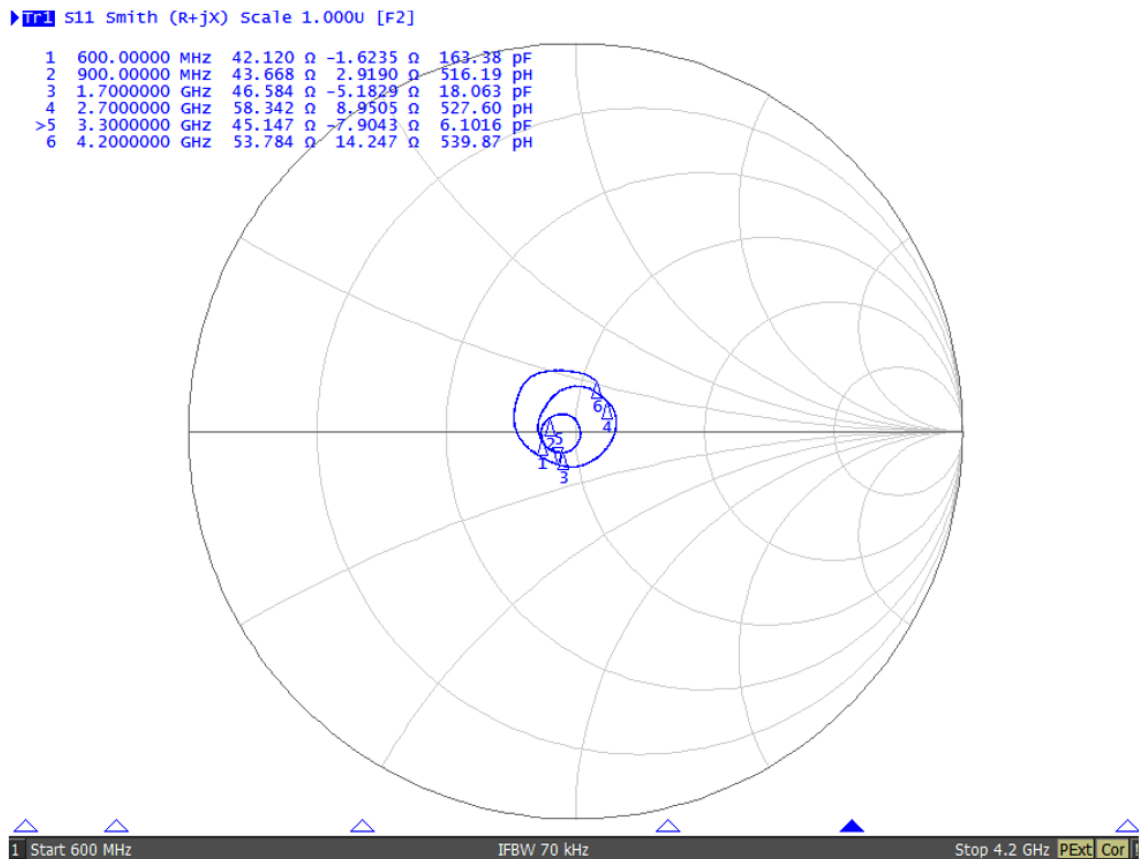


Figure 29: Line input impedance

Insertion Loss of G-CPW line plus SMA connector is shown below:

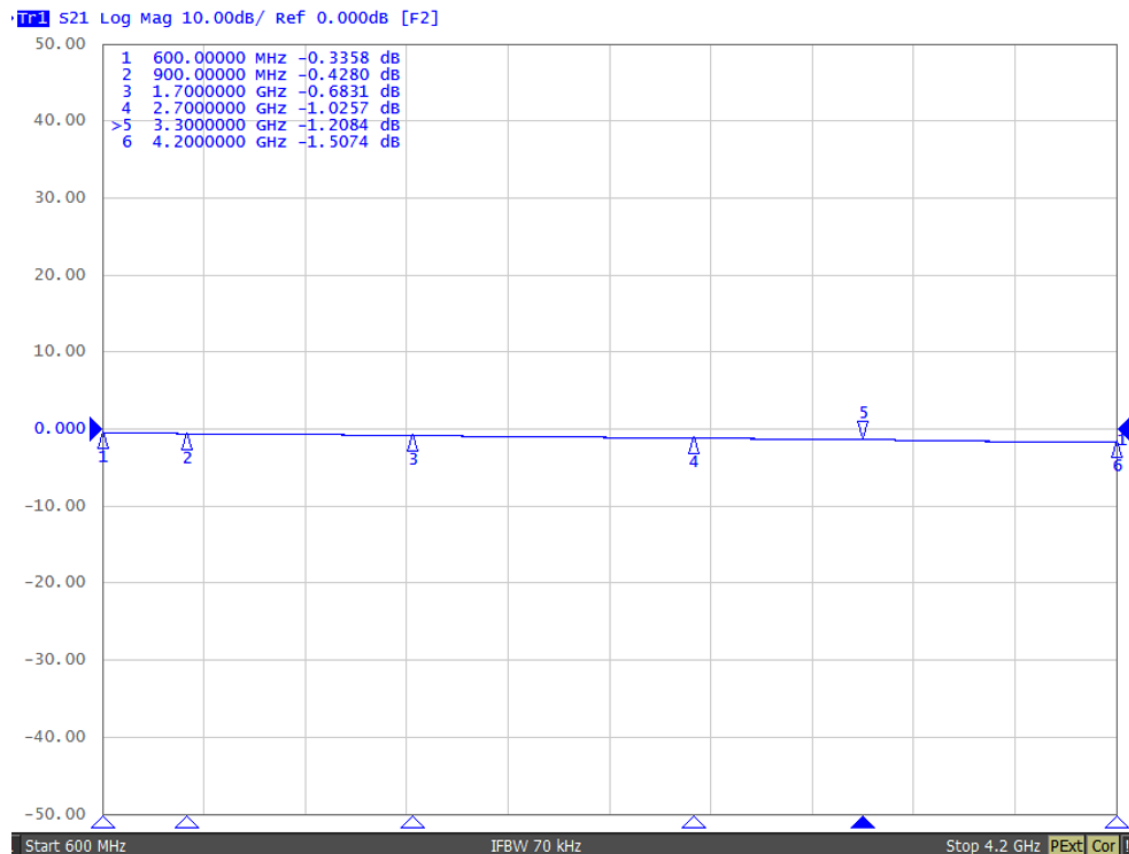


Figure 30: Insertion Loss of G-CPW line plus SMA connector

7.4.2.3 Antenna Installation Guidelines

- Install the antenna in a place covered by the LTE signal with 5G FR1 Sub-6 support.
- The Antenna must not be installed inside metal cases.
- The Antenna must be installed according to the Antenna manufacturer's instructions.
- The Antenna integration should optimize the Radiation Efficiency. Efficiency values > 50% are recommended on all frequency bands.
- The Antenna integration should not perturb the radiation pattern described in the documentation of the Antenna manufacturer.
- It is preferable to get an omnidirectional radiation pattern.
- The Antenna Gain must not exceed the values indicated in regulatory requirements, where applicable, to meet the related EIRP limitations. The Typical antenna Gain in most M2M applications does not exceed 2dBi.
- If the device antenna is located farther than 20cm from the human body and there are no co-located transmitters, then the Telit FCC/IC approvals can be re-used by the end product.
- If the device antenna is located closer than 20cm from the human body or there are co-located transmitters, then additional FCC/IC testing may be required for the end product (Telit FCC/IC approvals cannot be reused).

8 GNSS Section

The FE910C04 module includes a state-of-art receiver that can simultaneously search and track satellite signals from multiple satellite constellations. This multi-GNSS receiver uses the entire spectrum of GNSS systems available: GPS, GLONASS, BeiDou, Galileo, and QZSS.

8.1 GNSS Signals Pin-out

Table 46: GNSS Signals Pin-out

Pin	Signal	I/O	Function	Type
R9	ANT_GNSS	I	GNSS Antenna (50 ohm)	
R7	GNSS_LNA_EN	O	GNSS External LNA Enable	CMOS 1.8V

8.2 RF Front-End Design

The FE910C04 Module contains a pre-select SAW filter but does not contain the LNA necessary to achieve the maximum sensitivity. The active antenna (antenna with a built-in low noise amplifier) must be used and must be supplied with a proper bias-tee circuit.

8.2.1 Guidelines of PCB Line for GNSS Antenna

- Make sure that the antenna line impedance is 50 ohm.
- Keep the antenna line on the PCB as short as possible to reduce the loss.
- The Antenna line must have uniform characteristics, constant cross-section, and avoid meanders and abrupt curves.
- If possible, keep one layer of the PCB used only for the Ground plane.
- Surround (on both sides, above and below) the antenna line on PCB with Ground, avoid having other signal tracks facing directly the antenna line of track.
- The ground around the antenna line on PCB must be strictly connected to the Ground Plane by placing away once per 2mm at least.
- Place EM noisy devices as far as possible from the antenna line.
- Keep the antenna line far away from the power supply lines.
- Keep the antenna line far away from high-speed digital and LTE/5G RF lines.
- If there are noisy EM devices around the PCB hosting the module, such as fast switching ICs, take care of the shielding of the antenna line by burying it inside the layers of PCB and surrounding it with Ground planes, or shielding it with a metal frame cover.
- If there are no noisy EM devices around the PCB hosting the module, use a strip line on the superficial copper layer for the antenna line. The line attenuation will be lower than a buried one.

8.3 GNSS Antenna Requirements

GNSS active antenna must be used or integrated into the application.

8.3.1 GNSS Antenna Specification

Table 47: GNSS Antenna specification

Item	Value
Frequency range	• GPS L1: 1574.4 ~ 1576.4 MHz (centered on 1575.42 MHz) • GLONASS (GLO): 1597.5 ~ 1605.9 MHz (centered on 1601.7 MHz) • BeiDou (BDS): 1559.1 ~ 1563.1 MHz (centered on 1561 MHz) • Galileo (GAL): 1573.4 ~ 1577.5 MHz (centered on 1575.42 MHz) • GPS L5: 1166.22 ~ 1186.68 MHz (centered on 1176.45 MHz) • BDS B2a: 1166.22 ~ 1186.68 MHz (centered on 1176.45 MHz) • Galileo E5a: 1166.22 ~ 1186.68 MHz (centered on 1176.45 MHz)
Gain	15 ~ 30dB
Impedance	50 hm
Noise Figure of LNA	< 1.5 (recommended)
DC supply voltage	DC 1.8 ~ 3.3V
VSWR	≤ 3:1 (recommended)

Note:

- In the case of the GNSS antenna placed close to the module, a 15dB gain is sufficient, in the case of a long cable the gain must be increased up to 30 dB.
- It is recommended to add a DC block to the customer's GNSS application to prevent damage to the FE910C04 module due to unwanted DC voltage.
- It is recommended to add PI matching network near the GNSS connector on the application board in case that RF matching is needed.

8.3.2 GNSS Antenna – Installation Guidelines

- The antenna must be installed according to the antenna manufacturer's instructions to obtain maximum performance from the GNSS receiver.
- The position of the antenna must be carefully evaluated if operating in conjunction with any other antenna or transmitter.
- The antenna must not be installed inside metal cases or near any obstacle that may degrade features such as antenna lobes and gain.

8.3.3 Powering the External LNA (Active Antenna)

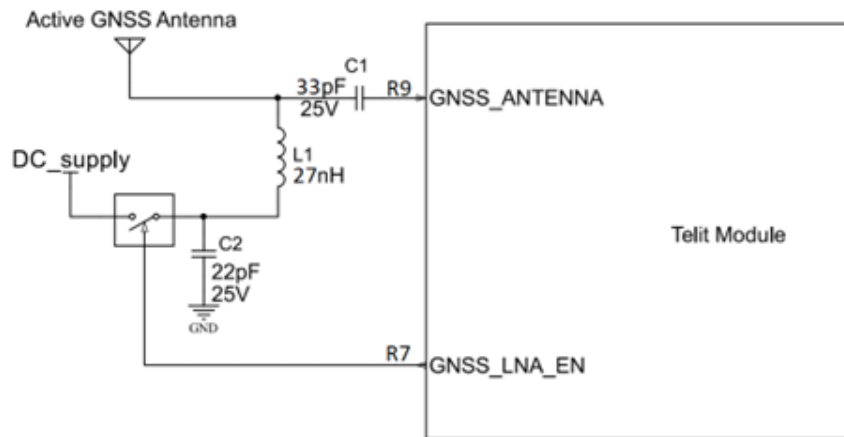
The LNA of the active antenna needs a power source because the 1.8V or 3V DC voltage required by the active antenna is not supplied by the FE910C04 module, but can be easily included by the host design.

The electrical characteristics of the GPS_LNA_EN signal are:

Table 48: GPS_LNA_EN Signal Characteristics

Level	Min	Max
Output High Level	1.6V	1.9V
Output Low Level	0V	0.3V

Example of external antenna bias circuitry:


Figure 31: Antenna Bias Circuitry Example

Be aware of the max bias current in case of unwanted short circuits on the antenna cable, since the decoupling inductor may be damaged.

In the case of LNA with a 1.8V supply, VAUX/POWERMON pin can be used to supply an active GNSS antenna

Warning: In case of using the module in standalone mode, the GNSS_LNA_EN signal is not available and must be provided by the external host.

8.4 GNSS Characteristics

The table below specifies the GNSS characteristics and expected performance without GNSS active Antenna. The values are related to typical environments and conditions.

Table 49: GNSS Characteristics

Parameters		Typical Measurement	Notes
Sensitivity	Tracking Sensitivity	-158dBm	Standalone or MS Based
	Acquisition	-154dBm	
	Cold Start	-146dBm	
TTFF	Hot	1 sec	Open Sky, mean TTFF
	Warm	21 sec	Open Sky, mean TTFF
	Cold	26 sec	Open Sky, mean TTFF
Supported update rate		10 Hz	
CEP-50		<2m	Open Sky conditions Standalone

9 Mechanical Design

9.1 Drawing

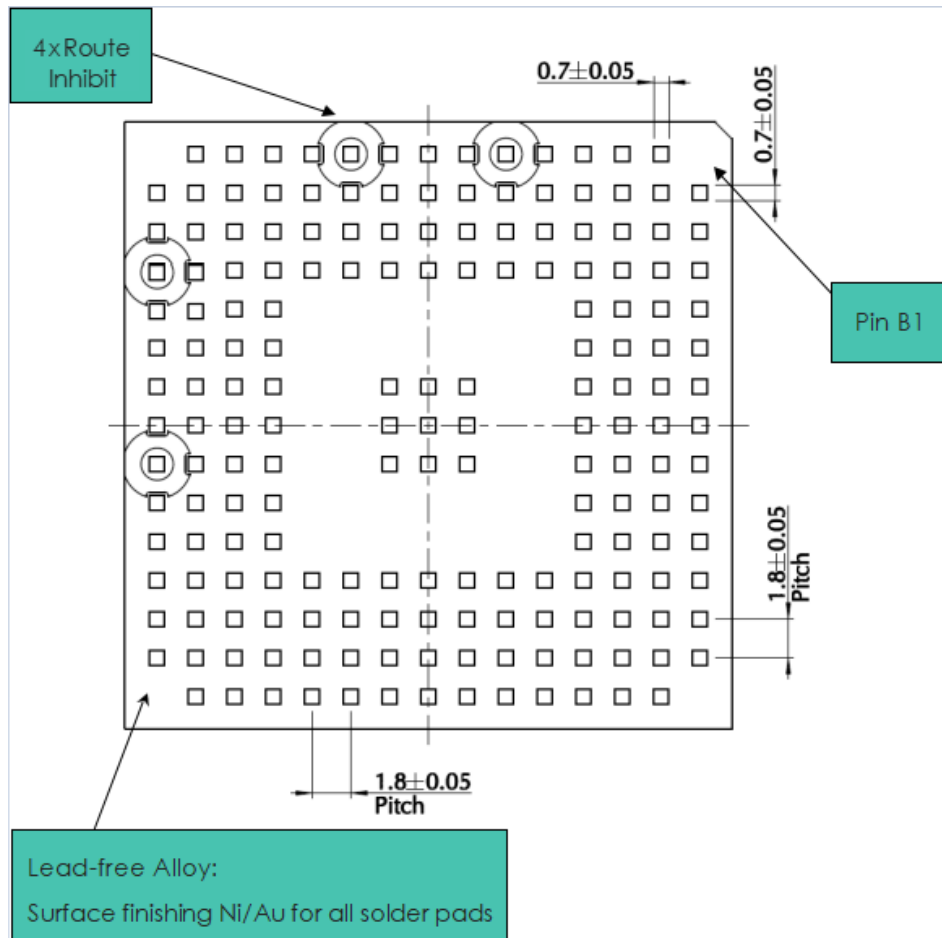


Figure 32: Mechanical Design Drawing - Bottom View

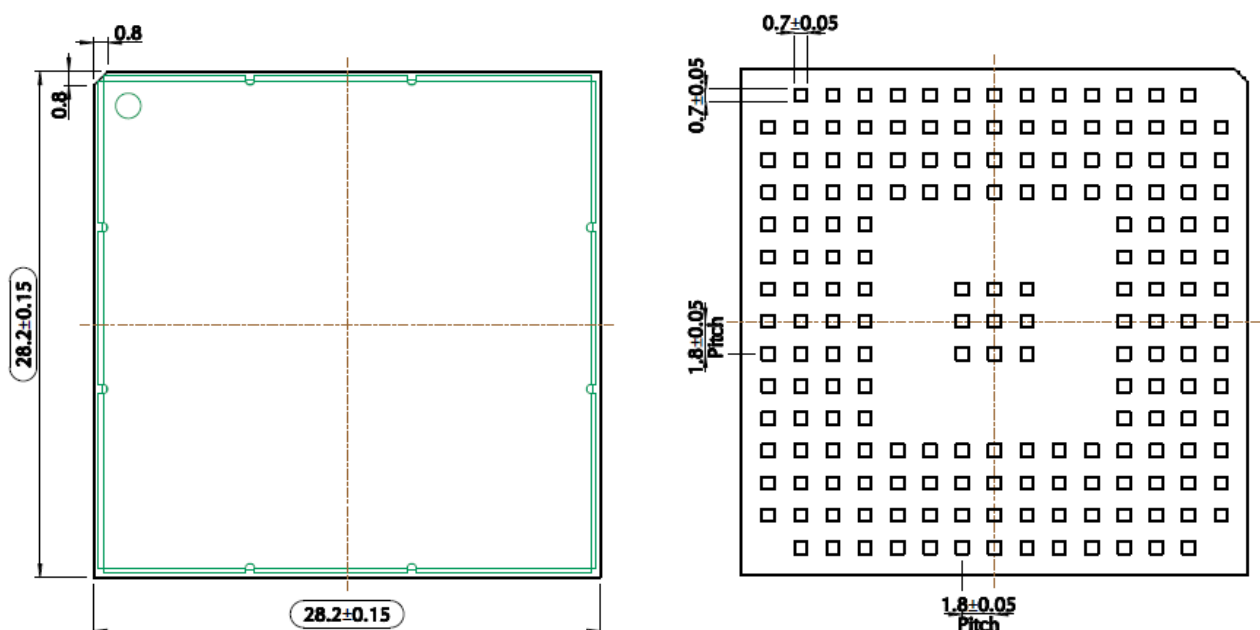


Figure 33: FE910C04 Mechanical Dimensions

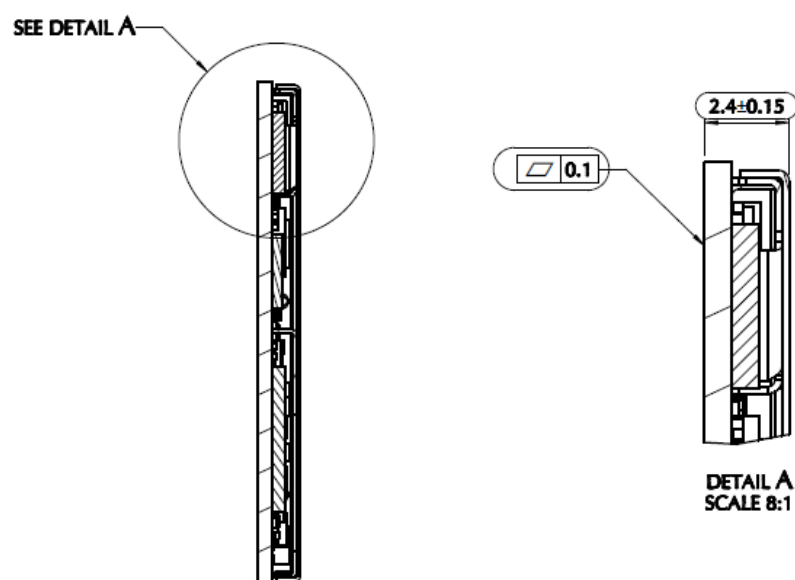


Figure 34: FE910C04 Mechanical Dimensions - Side view

10 Application PCB Design

The FE910C04 modules have been designed to be compliant with a standard lead-free SMT process.

10.1 CAD symbols, PCB footprints and 3D models

CAD symbols, PCB footprints and 3D models of Telit Cinterion modules are available on request.

For any further information, contact Telit Cinterion technical support.

10.2 Recommended Footprint for the Application

Top View

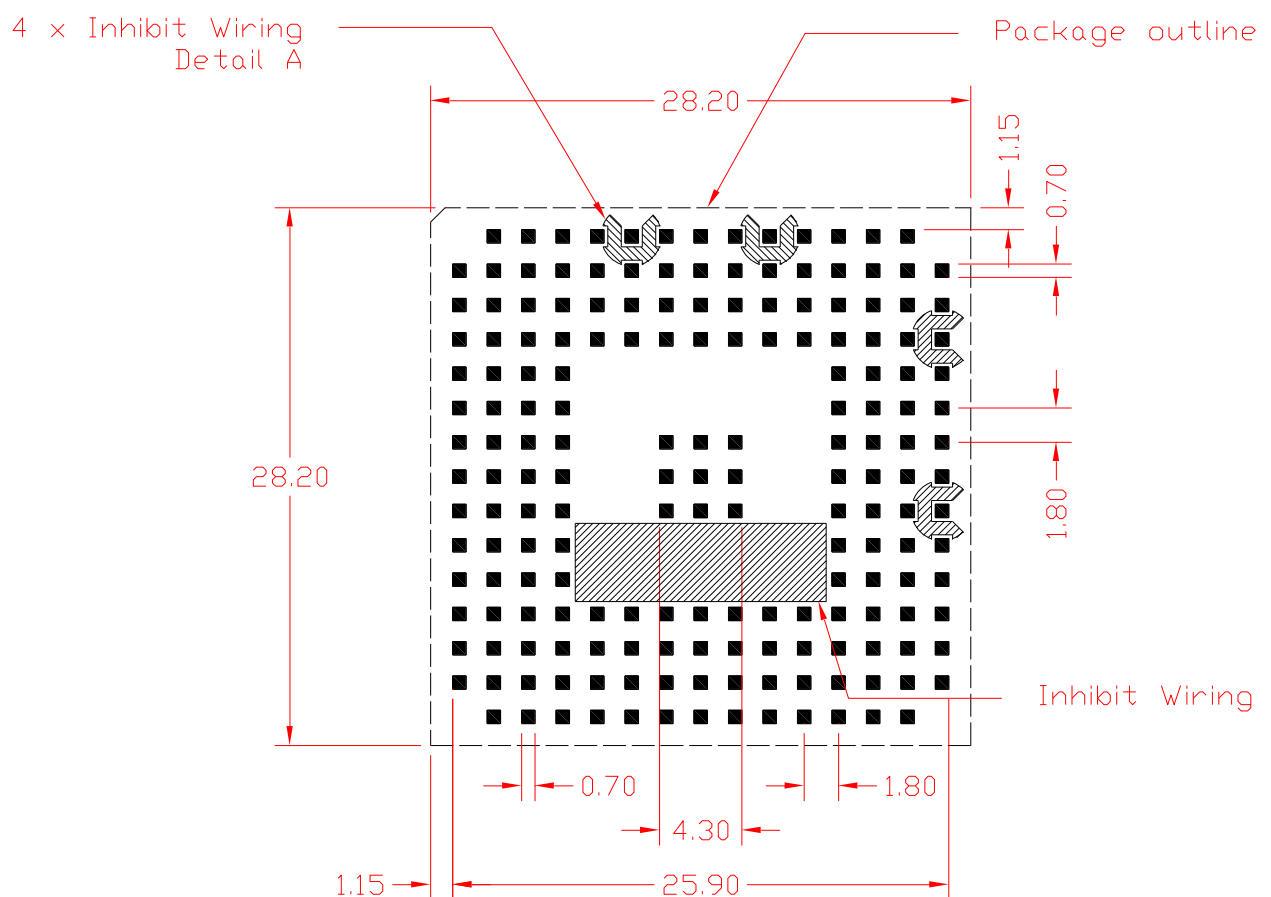


Figure 35: Footprint (dimensions in mm)

10.2.1 Solder Resist pattern

A solder resist pattern (dimensions in mm)

Top Transparent View

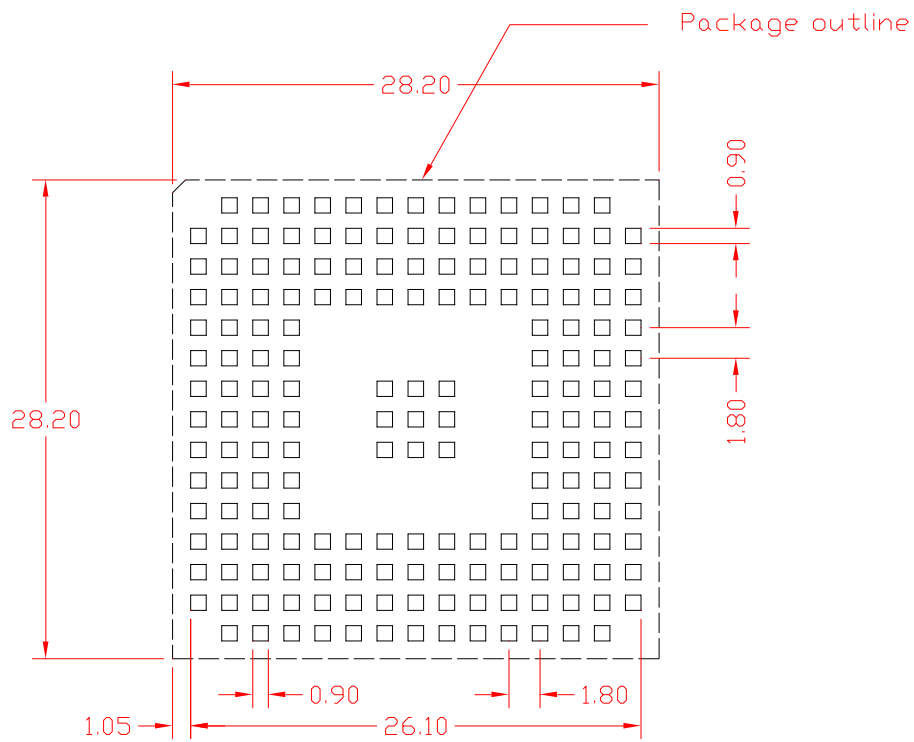


Figure 36: Top Transparent View

10.2.2 Inhibit Wiring Areas

Top Transparent View (dimensions in mm)

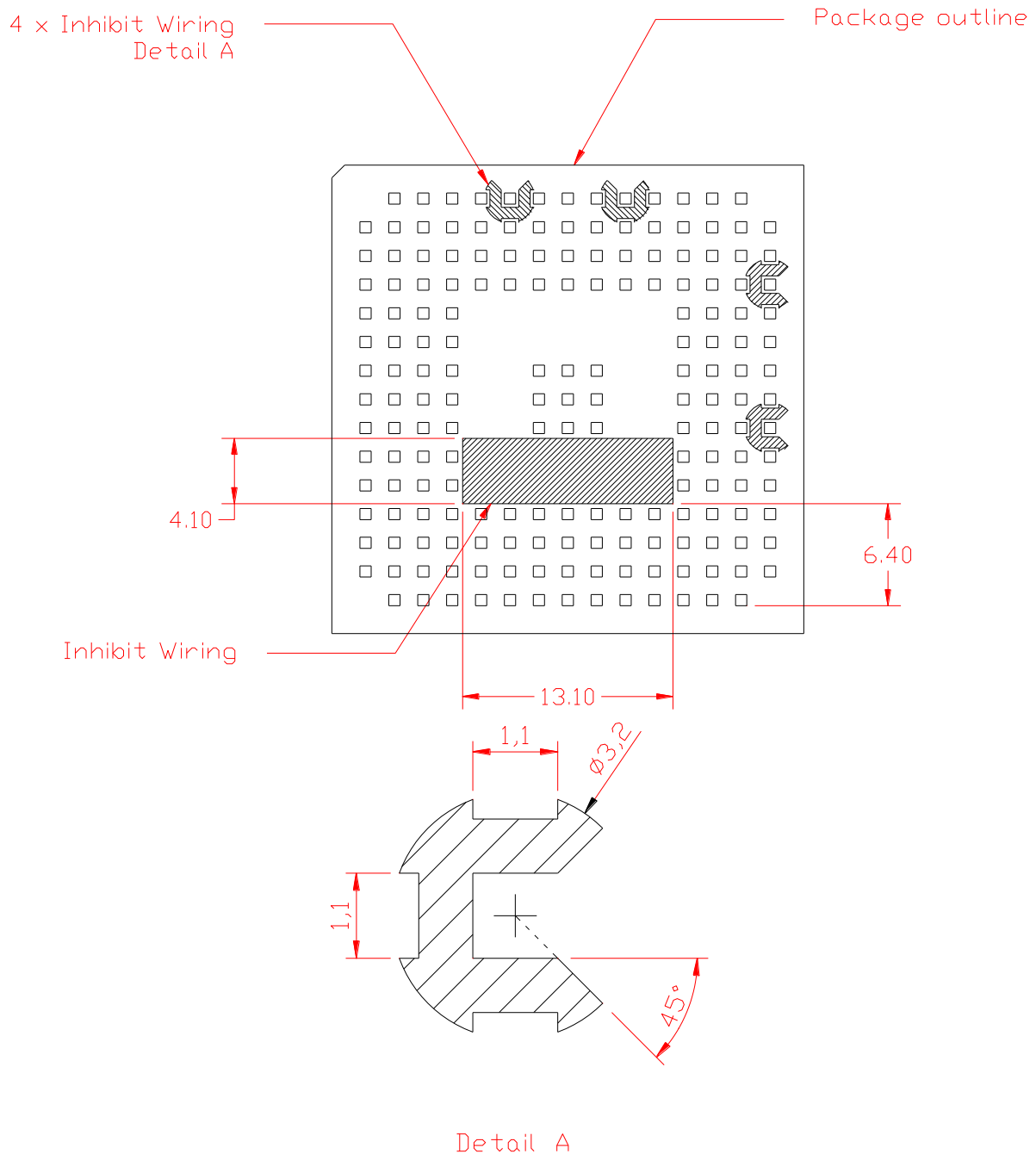


Figure 37: Inhibit Wiring Area

To easily rework the FE910C04 it is recommended to consider on the application a 1.5 mm placement inhibit area around the module.

It is also suggested, as a common rule for an SMT component, to avoid a mechanical part of the application being in direct contact with the module.

Note: In the customer application, the region under WIRING INHIBIT (see figure above) must be clear from signal or ground paths.

10.3 PCB Pad Design

In PCB design, the solder pads can be defined either as Solder Mask Defined (SMD) or Non-Solder Mask Defined (NSMD). The difference between these two solder mask pad definitions is in the proximity of the solder mask to the metal pad. In SMD pads, the solder mask opening is smaller than the metal pad and overlaps the metal on all sides. The solder mask opening defines the solderable area of the pad. In NSMD pads, the solder mask opening is larger than the metal pad and does not overlap the metal. The metal edge defines the solderable area of the pad (see Figure below).

Since the metal etching process in PCB manufacturing has significantly tighter alignment and etching tolerances than the alignment registration of the solder masking process, with NSMD pads, it is possible to obtain a more accurate solder pad land pattern. Also, with SMD pads, the solder mask overlapping the metal pad introduces additional height above the metal surface which may affect solder joint adhesion and reliability. Non-solder mask defined (NSMD) type is recommended for the solder pads on the PCB.

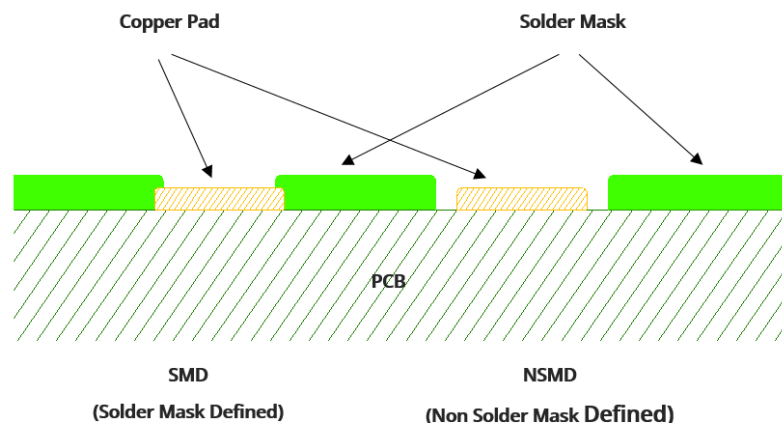


Figure 38: PCB Solder Pad Recommendations

10.4 Recommendations for PCB Pad Dimensions

It is not recommended to place via or micro-via not covered by the solder resist in an area of 0,3 mm around the pads unless it carries the same signal as the pad itself

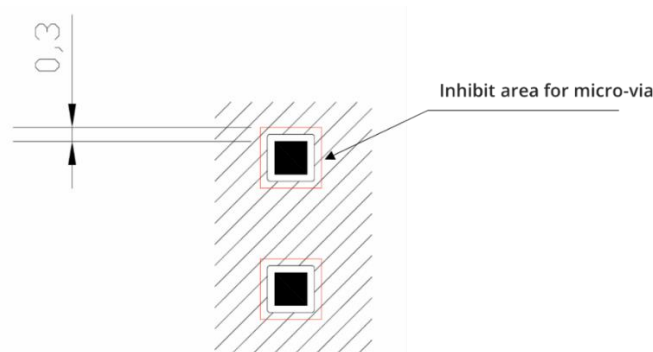


Figure 39: Pad Dimensions Recommendations

Holes in the pad are allowed only for blind holes and not for through holes.

Recommendations for PCB pad surfaces:

Table 50: Recommendations for PCB Pad Surfaces

Finish	Layer Thickness (um)	Properties
Electroless Ni / Immersion Au	3 – 7 / 0.05 – 0.15	good solder ability protection, high shear force values

The PCB must be able to resist the higher temperatures which are occurring during the lead-free process. This issue should be discussed with the PCB supplier. Generally, the wettability of tin-lead solder paste on the described surface plating is better than compared to the lead-free solder paste.

It is not necessary to panel the application's PCB, however, in that case, it is recommended to use milled contours and predrilled board breakouts; scoring or v-cut solutions are not recommended.

10.5 Thermal Performance

FR4 is one of the most commonly used PCB materials, it is a flame-retardant composite material, composed of fibreglass-reinforced and epoxy laminate. One of the features of the FR4 is to have a very low thermal conductivity. An inexpensive way to improve thermal transfer for FR-4 PCBs is to add thermal vias-plated through-holes (PTH) between the conductive layers. Vias are created by drilling holes and copper plating them, in the same way, a PTH or via is used for electrical interconnections between layers. A series of plated through-hole thermal vias should be located in the GND area underneath the Telit module of the PCB, to provide a thermal connection from the PCB GND to additional metal layers of the PCB.

The application PCB layout should include plated through-hole thermal vias for efficient heat dissipation from the Telit module into the PCB. One of the following thermal via types should be used:

- Open-plated through-hole vias that will provide lower PCB fabrication costs but may fill with solder.
- Plugged and capped plated through-hole vias will provide higher PCB fabrication costs but will not fill with solder.

Telit recommends creating areas of 10 mils (0.254-mm) vias arranged on a 25 mil (0.635-mm) rectilinear matrix. The reason for this choice is the combination of cost, performance and manufacturability. According to several PCB manufacturers, 10-mil holes and 25-mil spacing are reasonable and repeatable production choices.

A uniform metal plating thickness on the PCB will ensure reliable, high Telit module solder assembly yield.

10.6 Stencil

A silk-screen process will be required for the deposition of solder paste on the PCB, for the reflow of the Telit module on the PCB. The silk-screen process requires the use of a metal stencil based on an opening where the solder paste is transferred through the openings on the solder pads of the application PCB. To minimize solder voids and ensure maximum electrical and thermal connectivity of the module to the PCB, large pads, solder volume, and solder strain must be considered in the stencil design. The design and

fabrication of the stencil determine the quality of the solder paste deposition onto the PCB and the resulting solder joint after reflow. The primary stencil parameters are aperture size, thickness, and fabrication method. The stencil should be made from stainless steel and the apertures layout can be the same as the recommended footprint (1:1). The recommended thickness shall be 127 μm (5 mil). A stencil thickness of 152 μm (6 mil) can be used as well.

10.7 Solder Paste

Various types and grades of solder paste can be used for surface mounting Telit modules. For lead-free applications, an Sn-Ag (SA) or Sn-Ag-Cu (SAC) solder paste can be used. Any Type 3 solder paste that is either water-soluble or not clean is acceptable.

We recommend using only “no clean” solder paste to avoid the cleaning of the modules after assembly.

10.8 Solder Reflow

Recommended solder reflow profile:

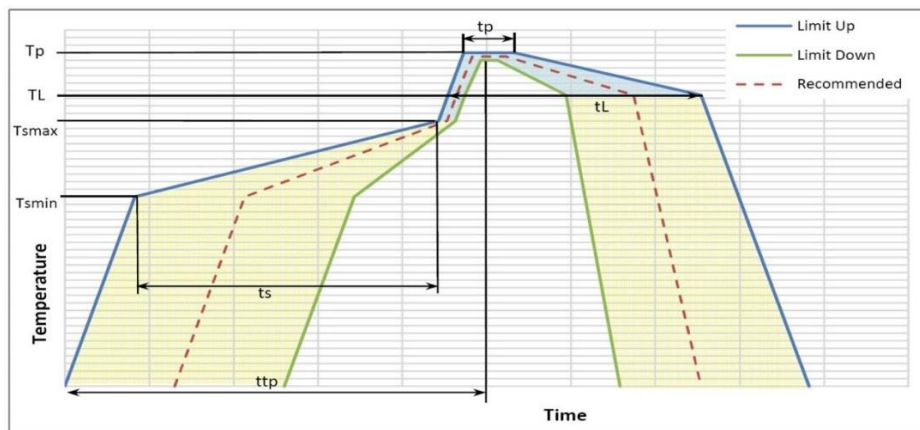


Figure 40: Recommended Solder Reflow Profile

Table 51: Profile Feature Recommendations

Profile Feature	Pb-Free Assembly Free
Average ramp-up rate (T_L to T_P)	3°C/second max
Preheat - Temperature Min (T_{smin}) - Temperature Max (T_{smax}) - Time (min to max) (t_s)	150°C 200°C 60-180 seconds
T_{smax} to T_L Ramp-up Rate	3°C/second max
Time maintained above: - Temperature (T_L) - Time (t_L)	217°C 60-150 seconds
Peak Temperature (T_p)	245 +0/-5°C
Time within 5°C of actual Peak Temperature (t_p)	10-30 seconds
Ramp-down Rate	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

Note: All temperatures refer to the topside of the package, measured on the package body surface.

Warning: THE FE910C04 MODULE WITHSTANDS ONE REFLOW PROCESS ONLY.

Warning: The above solder reflow profile represents the typical SAC reflow limits and does not guarantee adequate adherence of the module to the customer application throughout the temperature range. Customers must optimize the reflow profile depending on the overall system taking into account such factors as thermal mass and warpage.

10.9 Inspection

An inspection of the solder joint between the solder pads of the Telit module and the application PCB should be performed. The best visual inspection tool for inspection of the Telit module solder joints on the PCB is a transmission X-ray, which can identify defects such as solder bridging, shorts, opens, and large voids (Note: small voids in large solder joints are not detrimental to the reliability of the solder joint).

11 Packaging

11.1 Tray

The FE910C04 modules are packaged on trays that can be used in SMT processes for pick & place handling. The first Marketing and Engineering samples of the FE910C04 series will be shipped with the current packaging of the FE910C04 modules (on trays of 36 pieces each). The mass production units of FE910C04 will be shipped according to the following drawings:

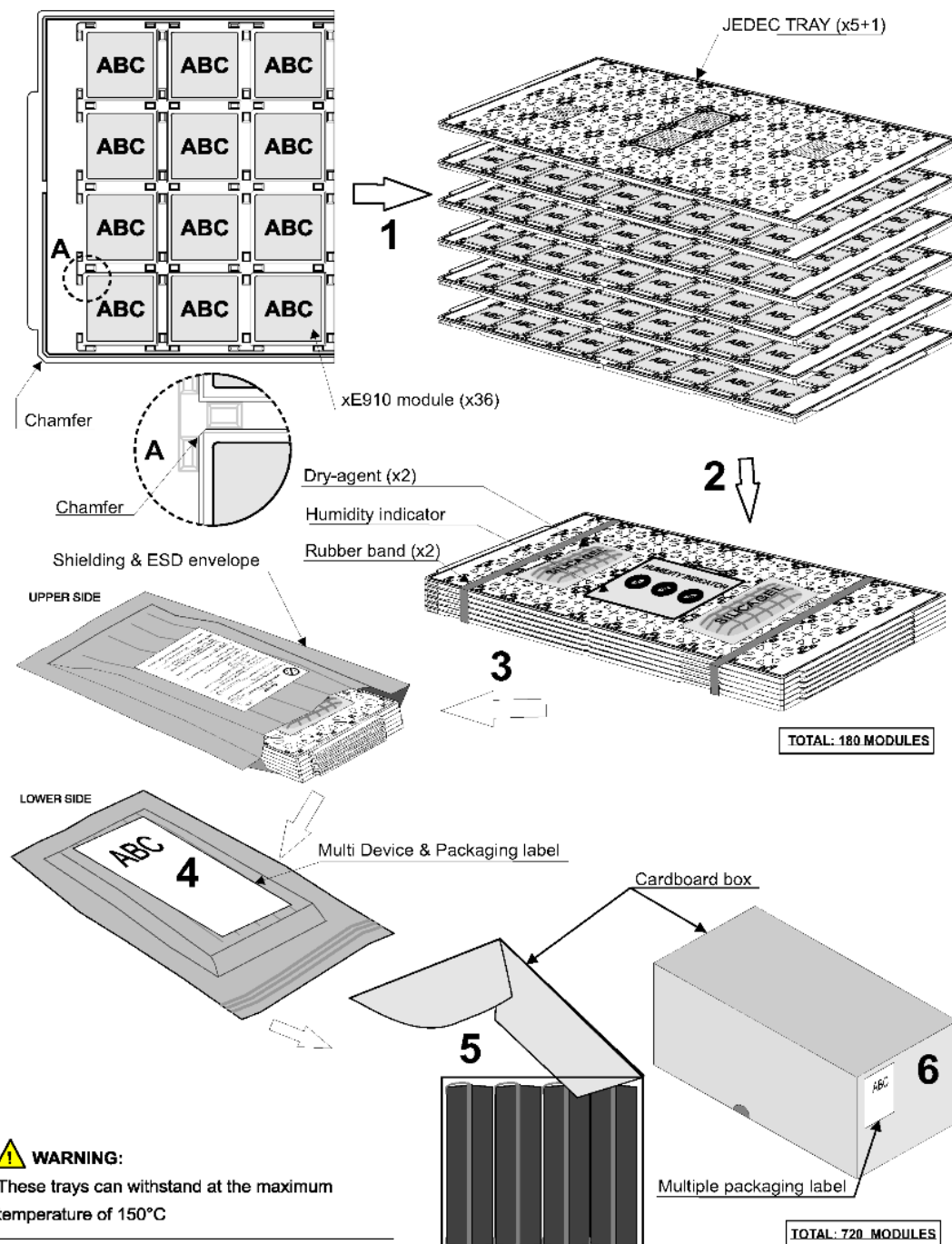


Figure 41: Tray Packaging

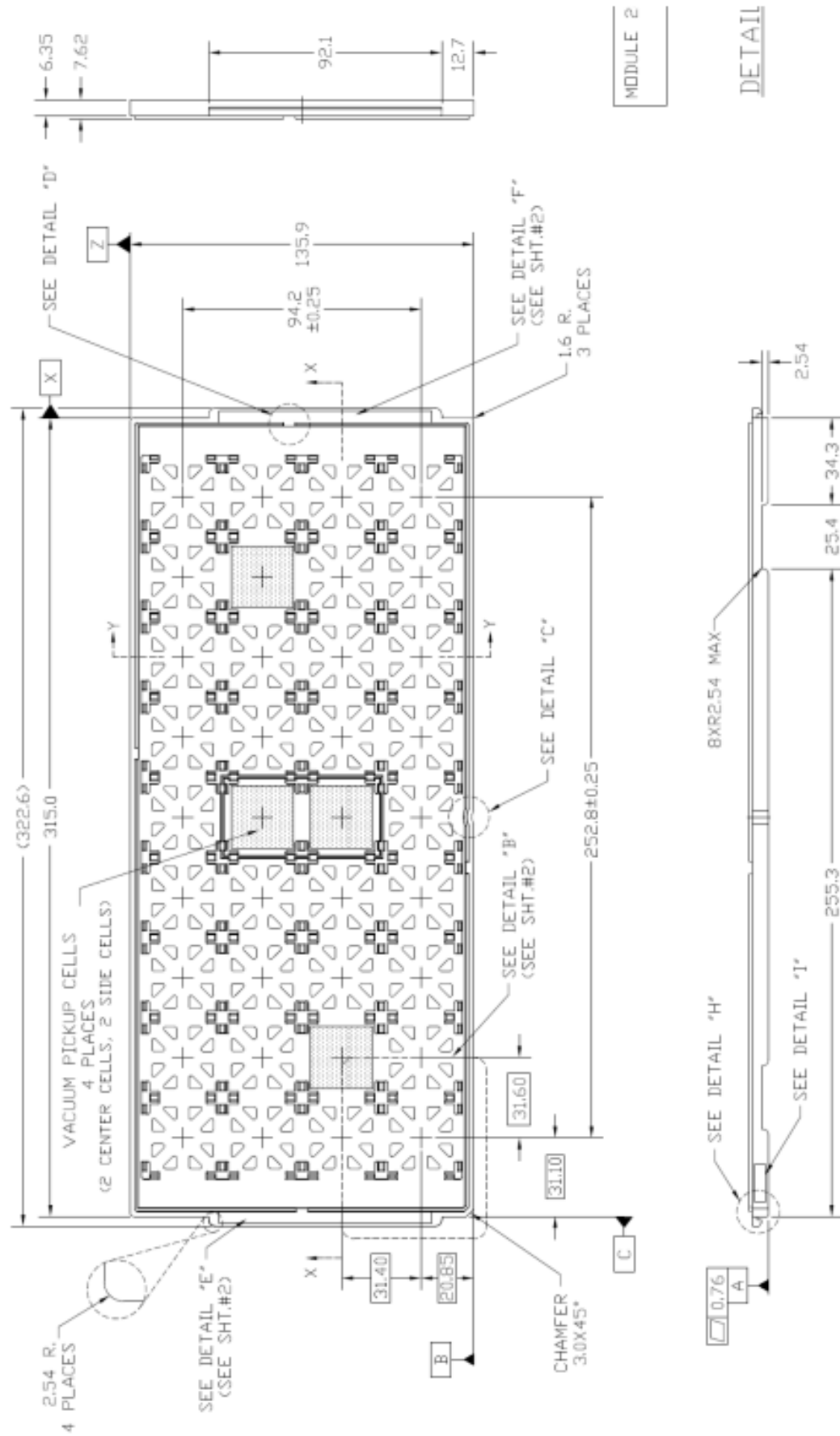


Figure 42: Tray Dimensions

11.2 Reel

The FE910C04 can be packaged on reels of 200 pieces each. See the figure for module positioning into the carrier.

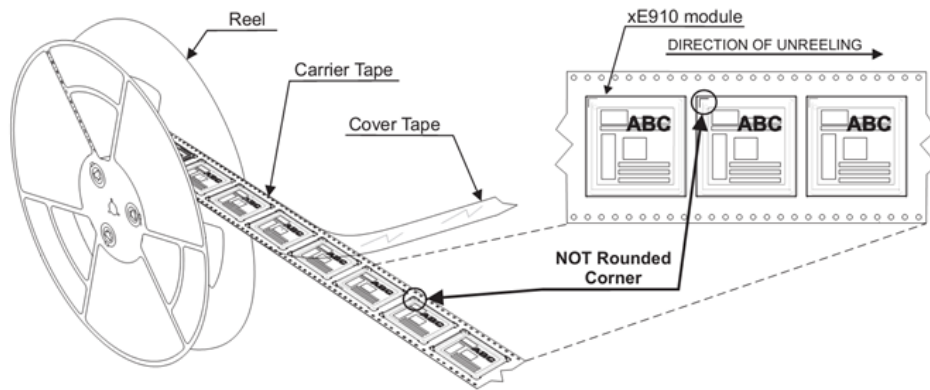


Figure 43: Module Positioning into the Carrier

11.3 Carrier Tape Detail

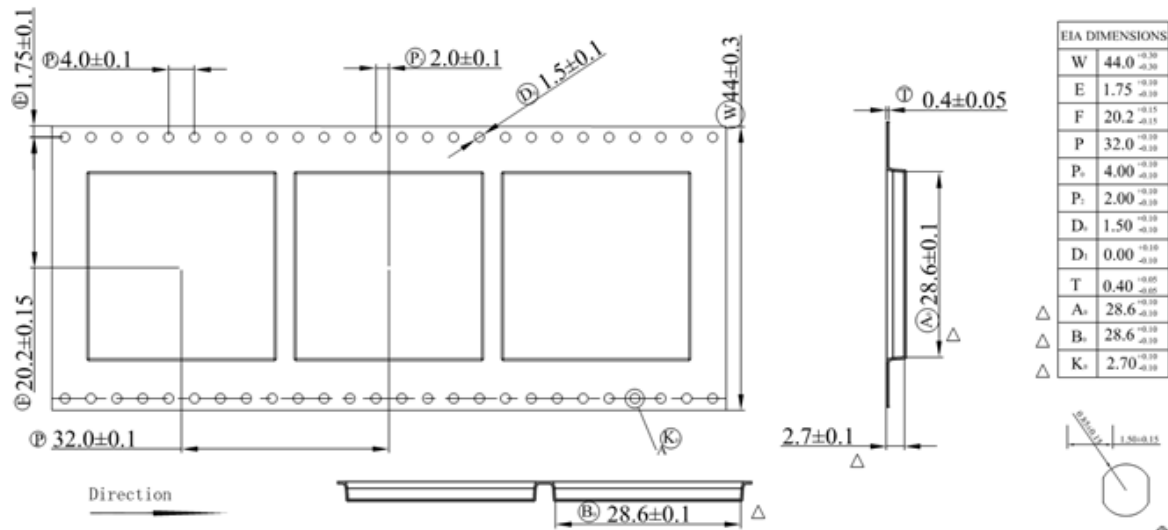


Figure 44: Carrier Tape Detail

11.4 Reel Detail

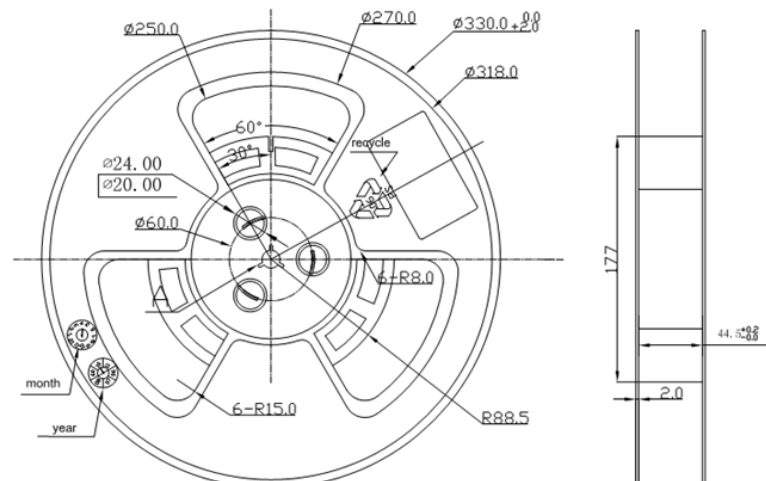


Figure 45: Reel Detail

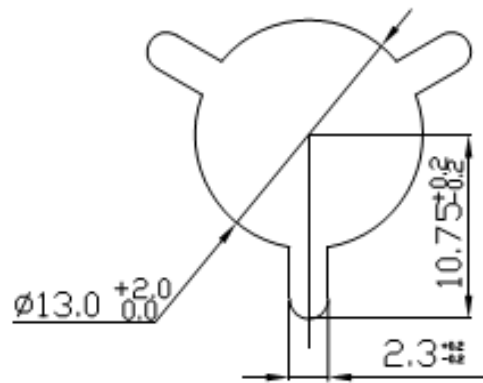


Figure 46: Detail

11.5 Packaging Detail

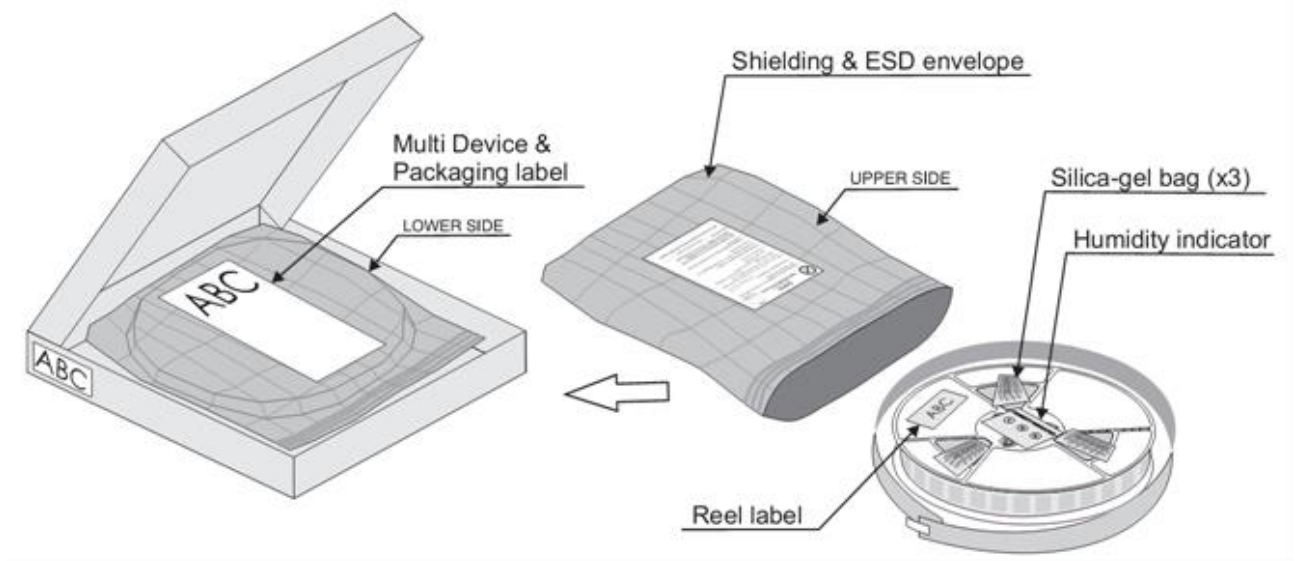


Figure 47: Packaging Detail

11.6 Moisture Sensitivity

The FE910C04 is a Moisture Sensitive Device level 3, according to standard IPC/JEDEC J-STD-020, and takes care of all the relative requirements for using this kind of component. Moreover, the customer has to take care of the following conditions:

- a Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH).
- b An environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5.
- c The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition b) "IPC/JEDEC J-STD-033D paragraph 5.2" is respected
- d Baking is required if conditions b) or c) are not respected
- e Baking is required if the humidity indicator inside the bag indicates 10% RH or more.

12 Conformity Assessment Issues [TBD]

12.1 Approvals Compliance Summary [TBD]

Table 52: Legend Description

Legend	Description
	The equipment is compliant
	Type approval is in progress
	The equipment is not compliant

Table 53: Americas Approvals Compliance Summary

Region	Americas									
Country & Type Approval	AR ENACOM	BR ANATEL	CA ISED	CO CRC	MX IFETEL	PE MTC	US FCC	BOL ATT	ECU ARCOTEL	PY CONATEL
FE910C04-WW										
FE910C04-WWD										

Table 54: APAC Approvals Compliance Summary

Region	APAC					
Country & Type Approval	AU RCM	CH CCC	JP JRL / JTBL	KR KCC	SG IMDA	TW NCC
FE910C04-WW						
FE910C04-WWD						

Table 55: EMEA Approvals Compliance Summary

Region	EMEA	
Country & Type Approval	EU RED	UK UKCA
FE910C04-WW		
FE910C04-WWD		

Note: For approvals not included in the above, contact Telit support.

12.2 Americas Approvals [TBD]

USA FCC

FCC Certificates

The FCC Grants can be found here: <https://www.fcc.gov/oet/ea/fccid>

Applicable FCC Rules

Table 56: Applicable FCC Rules

Model	Applicable FCC rules
FE910C04-WW	Title 47 CFR Part 2, Part 22, Part 24, Part 27, Part 90, Part 96
FE910C04-WWD	

FCC Regulatory Notices

Modification Statement

Telit has not approved any changes or modifications to this device by the user. Any changes or modifications could void the user's authority to operate the equipment.

Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Wireless Notice

This device complies with FCC radiation exposure limits set forth for an uncontrolled environment and meets the FCC radio frequency (RF) Exposure Guidelines. This transmitter must not be co-located or operate in conjunction with any other antenna or transmitter. The antenna should be installed and operated with a minimum distance of 20 cm between the radiator and your body

FCC Class B digital device notice

This equipment has been tested and found to comply with the limits for a Class B digital device, according to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used per the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by taking one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment to an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Information for the OEMs and Integrators

The following statement must be included with all versions of this document supplied to an OEM or integrator but should not be distributed to the end user.

1. This device is intended for OEM integrators only.
2. See the full Grant of Equipment document for other restrictions

Manual Information to the End User

The OEM integrator should be aware not to provide information to the end-user on how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as shown in this manual

Information on test modes and additional testing requirements

The module has been evaluated in mobile stand-alone conditions. For operational conditions other than a stand-alone modular transmitter in a host (multiple, simultaneously transmitting modules or other transmitters in a host), additional testing may be required (collocation, retesting...). If this module is intended for use in a portable device, you are responsible for separate approval to satisfy the SAR requirements of FCC Part 2.1093.

Additional testing, Part 15 Subpart B disclaimer

The modular transmitter is only authorized by the FCC for the specific rule parts (for example, FCC transmitter rules) listed on the grant, and the host product manufacturer is responsible for compliance with any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuitry), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed. The end product with an embedded module may also need to pass the FCC Part 15 unintentional emission testing requirements and be properly authorized per FCC Part 15.

FCC Antenna Info

This radio transmitter has been approved by FCC to operate with the antenna types listed below with the maximum allowable gain indicated. Antenna types not included in this list, with a gain greater than the maximum gain indicated for that type, are strictly prohibited from use with this device.

Table 57: FCC Antenna Type

Model	Antenna Type
FE910C04-WW	Omnidirectional Monopole Antenna
FE910C04-WWD	

Table 58: Max Antenna gain for FCC in dBi

Max gain for FCC (dBi)		
Operation Mode	Freq. (MHz)	Max Allowable Antenna Gain (dBi)
LTE B2	1850.7	9.00
LTE B4	1710.7	6.00
LTE B5	824.7	10.41
LTE B7	2502.5	9.00
LTE B12	699.7	9.70
LTE B13	799.5	10.17
LTE B14	788.0	10.21

Max gain for FCC (dBi)		
LTE B17	704.0	9.73
LTE B25	1850.7	9.00
LTE B26 Part 90	814.7	10.36
LTE B26	824.7	10.41
LTE B30	2307.5	1.00
LTE B38	2572.5	9.00
LTE B41	2498.5	9.00
LTE B41 (HPUE)	2498.5	6.00
LTE B42	3550.0	10.50
LTE B42	3600.0	0.50
LTE B43	3700.0	0.50
LTE B43	3800.0	10.50
LTE B48	3552.5	0.50
LTE B66	1710.7	6.00
LTE B70	1710.0	6.00
LTE B71	665.50	9.48
LTE B106	901.0	9.92
5G NR n2	1850.7	9.00
5G NR n5	824.7	10.41
5G NR n7	2502.5	9.00
5G NR n12	699.7	9.70
5G NR n13	779.5	10.17
5G NR n14	788.0	10.21
5G NR n25	1850.7	9.00
5G NR n26 Part90	814.7	10.36
5G NR n26	824.7	10.41
5G NR n30	2307.5	1.00
5G NR n38	2572.5	9.00
5G NR n41_PC3	2498.5	9.00
5G NR n48	3552.5	0.50
5G NR n66	1710.7	6.00
5G NR n70	1710.0	6.00
5G NR n71	665.50	9.48
5G NR n77_PC3	4200.00	5.99
5G NR n78_PC3	3800.00	5.99

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.



Labelling requirements for the host device

The host device shall be properly labelled to identify the modules within the host device. The certification label of the module shall be visible at all times when installed in the host device, otherwise, the host device must be labelled to display the FCC ID of the module, preceded by the words "Contains transmitter module", or the word "Contains", or similar wording expressing the same meaning, as in the below table.

Table 59: Host device FCC label

Model / HVIN	Host device FCC label
FE910C04-WW	Contains FCC ID: RI7FE910C04WW
FE910C04-WWD*	

* Data-only variants share the same HW as related voice variants and the voice features are disabled by SW.

Canada ISED

ISED Database

The products ISED certified can be found here:

Les produits certifiés ISED peuvent être trouvés ici:

<https://sms-sgs.ic.gc.ca/equipmentSearch/searchRadioEquipments?execution=e1s1&lang=en>

Applicable ISED Rules

Table 60: Applicable ISED rules / Règles ISDE applicables

Model	Applicable ISED rules /Règles ISDE applicables 2
FE910C04-WW	RSS-Gen Issue 5, RSS-102 Issue 6, RSS-130 Issue 2, RSS-132 Issue 4, RSS-133 Issue 7, RSS-139 Issue 4, RSS-140 Issue 1, RSS-192 Issue 5, RSS-195 Issue 2, RSS-199 Issue 4, RSS-198 Issue 1
FE910C04-WWD	

ISED Regulatory Notices

Modification Statement / Déclaration de modification

Telit has not approved any changes or modifications to this device by the user. Any changes or modifications could void the user's authority to operate the equipment.

Telit n'approuve aucune modification apportée à l'appareil par l'utilisateur, quelle qu'en soit la nature. Tout changement ou modification peuvent annuler le droit d'utilisation de l'appareil par l'utilisateur.

Interference Statement / Déclaration d'interférence

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux applicables RSS standards d'Industrie Canada. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire

de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Radio Exposure Notice / Avis d'exposition radio

This device complies with ISED radiation exposure limits set forth for an uncontrolled environment and meets the RSS-102 of the ISED radio frequency (RF) Exposure rules. Antenna gain must be less than the values reported in the table below:

Le présent appareil est conforme à l'exposition aux radiations FCC / ISED définies pour un environnement non contrôlé et répond aux directives d'exposition de la fréquence de la FCC radiofréquence (RF) et RSS-102 de la fréquence radio (RF) ISED règles d'exposition. Gain de l'antenne doit être ci-dessous:

Table 61: ISED Antenna Type

Model	Antenna Type / Type d'Antenne
FE910C04-WW	Antenne monopôle omnidirectionnelle
FE910C04-WWD	

Table 62: Max Antenna gain for ISED in dBi / Gain d'antenne max pour ISED en dBi

Max gain for ISED/ Gain max pour ISED (dBi)		
Operation Mode	Freq. (MHz)	Max Allowable Antenna Gain (dBi)
LTE B2	1850.7	9.00
LTE B4	1710.7	6.00
LTE B5	824.7	7.10
LTE B7	2502.5	9.00
LTE B12	699.7	6.61
LTE B13	799.5	6.93
LTE B14	788.0	6.97
LTE B17	704.0	6.63
LTE B25	1850.7	9.00
LTE B26	824.7	7.10
LTE B30	2307.5	1.00
LTE B38	2572.5	9.00
LTE B41	2498.5	9.00
LTE B41 (HPUE)	2498.5	6.00
LTE B42	3600.0	7.50
LTE B42 (HPUE)	3600.0	3.00
LTE B43	3800.0	7.50
LTE B48	3552.5	0.50
LTE B66	1710.7	6.00
LTE B71	665.5	6.46
5G NR n2	1850.7	9.00
5G NR n5	824.7	7.10
5G NR n7	2502.5	9.00
5G NR n12	699.7	6.61

Max gain for ISED/ Gain max pour ISED (dBi)		
5G NR n13	779.5	6.93
5G NR n14	788.0	6.97
5G NR n25	1850.7	9.00
5G NR n26	824.7	7.10
5G NR n30	2307.5	1.00
5G NR n38	2572.5	9.00
5G NR n41_PC3	2498.5	9.00
5G NR n48	3552.5	0.50
5G NR n66	1710.7	6.00
5G NR n71	665.5	6.46
5G NR n77_PC3	4200.0	5.99
5G NR n78_PC3	3800.0	5.99

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

L'émetteur ne doit pas être colocalisé ni fonctionner conjointement avec à autre antenne ou autre émetteur.

This equipment must be installed and operated following provided instructions and the antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter. End-users and installers must be provided with antenna installation instructions and consider removing the no-collocation statement.

Cet équipement doit être installé et utilisé conformément aux instructions fournies et la ou les antennes utilisées pour cet émetteur doivent être installées pour fournir une distance de séparation d'au moins 20 cm de toutes les personnes et ne doivent pas être co-localisées ou fonctionner en conjonction avec toute autre antenne ou émetteur. Les utilisateurs finaux et les installateurs doivent recevoir les instructions d'installation de l'antenne et envisager de supprimer la déclaration de non-collocation.

Information on test modes and additional testing requirement / Informations sur les modes de test et exigences de test supplémentaires

The module has been evaluated in mobile stand-alone conditions. For operational conditions other than a stand-alone modular transmitter in a host (multiple, simultaneously transmitting modules or other transmitters in a host), additional testing may be required (collocation, retesting...) If this module is intended for use in a portable device, you are responsible for separate approval to satisfy the SAR requirements IC RSS-102.

Le module a été évalué dans des conditions mobiles autonomes. Pour des conditions de fonctionnement autres qu'un émetteur modulaire autonome dans un hôte (plusieurs modules transmettant simultanément ou d'autres émetteurs dans un hôte), des tests supplémentaires peuvent être nécessaires (colocalisation, retest...) Si ce module est destiné à être utilisé dans un appareil portable, vous êtes responsable de l'approbation séparée pour satisfaire aux exigences SAR IC RSS-102.

Labelling requirements for the host device /

Exigences d'étiquetage pour le périphérique hôte

The host device shall be properly labelled to identify the modules within the host device. The certification label of the module shall be visible at all times when installed in the host device, otherwise, the host device must be labelled to display the IC of the module, preceded by the words "Contains transmitter module", or the word "Contains", or similar wording expressing the same meaning, as in the following table.

L'appareil hôte doit être étiqueté comme il faut pour permettre l'identification des modules qui s'y trouvent. L'étiquette de certification du module donné doit être posée sur l'appareil hôte à un endroit bien en vue en tout temps. En l'absence d'étiquette, l'appareil hôte doit porter une étiquette donnant le IC du module, précédé des mots « Contient un module d'émission », du mot « Contient » ou d'une formulation similaire exprimant le même sens, comme en tableau suivant.

Table 63: Host device IC label / Étiquette IC du dispositif hôte

Model / HVIN	Host device IC label / Étiquette IC du dispositif hôte
FE910C04-WW	Contains IC: 5131A-FE910C04WW
FE910C04-WWD*	

* Data-only variants share the same hardware as related voice variants and the voice features are disabled by SW.

Les variantes avec seulement data fonctionnalité partagent le même hardware que les variantes avec les fonctionnalités vocales qui sont désactivées par le SW.

CAN ICES-3 (B) / NMB-3 (B)

This Class B digital apparatus complies with Canadian ICES-003.

Cet appareil numérique de classe B est conforme à la norme canadienne ICES-003.

Brazil ANATEL

ANATEL Regulatory Notices

Agência Nacional de Telecomunicações (ANATEL) of Brazil



"Este equipamento não tem direito à proteção contra interferência prejudicial e não pode causar interferência em sistemas devidamente autorizados".

"This equipment is not entitled to protection against harmful interference and must not cause interference in duly authorized systems"

FE910C04-WW / FE910C04-WWD Homologation # **TBD**

12.3 APAC Approvals **[TBD]**

Australia RCM

Following the above Approval Compliance Summary table, where applicable (green dot), hereby, Telit Communications S.p.A declares that the equipment complies with the Regulatory Compliance Mark (RCM) of Australia.

Note: The equipment listed may not work when the main power fails.

Japan JRL/JTBL

JRL/JTBL Regulatory Notices

Antenna info

According to Japanese regulatory rules, module certification is valid only with the specific antennas registered to and approved by Japan Radio Law (JRL) certified body to module certification. Customers who are going to use modules under JRL are responsible to contact Telit technical support or sales to get the list of these antennas.

Dial Function

The Japan Telecommunication Business Law (JTBL) Module Certification for “FE910C04” is for a “non-Auto Redial Function” device.

In case the customer implements the “Auto Redial” function into the Application Device by controlling FE910C04, the customer cannot utilize FE910C04 JTBL certification, and they must apply JTBL as an “Application Device” System.

Taiwan NCC

NCC Regulatory Notices

According to National Communication Commission (NCC) Taiwan requirements, the module and the packaging shall be identified as described in the following lines. Shall be added also the specified safety warning statement.

Brand name: Telit Cinterion or 

Model name: FE910C04-WW / FE910C04-WWD

Product name: 5G Radio module

NCC logo: 

NCC ID: TBD

NCC safety warning statement: “減少電磁波影響，請妥適使用”

12.4 EMEA Approvals [TBD]

EU RED

EU Declaration of Conformity

Following the above Approval Compliance Summary table, where applicable (green dot), hereby, Telit Communications S.p.A declares that the equipment complies with Directive 2014/53/EU.

The full text of the EU Declaration of Conformity is available at the following internet address: <https://www.telit.com/red>



Text of 2014/53/EU Directive (RED) requirements can be found here:

<https://eur-lex.europa.eu/legal-content/EN/TXT/?uri=CELEX:32014L0053>

RED Antennas

This radio transmitter has been approved under RED to operate with the antenna types listed below with the maximum permissible gain indicated. The usage of a different antenna in the final hosting device may need a new assessment of host conformity to RED.

Table 64: RED Antenna Type

Model	Antenna Type
FE910C04-WW	Omnidirectional Monopole Antenna
FE910C04-WWD	

Table 65: Max Antenna gain for RED in dBi

Max gain for RED (dBi)		
Operation Mode	Freq. (MHz)	Max Allowable Antenna Gain (dBi)
LTE B1	1920.00	12.85
LTE B3	1710.00	12.35
LTE B5	824.00	9.17
LTE B7	2500.00	12.96
LTE B8	880.00	9.46
LTE B28	703.00	9.22
LTE B20	832.00	8.48
LTE B34	2010.00	12.96
LTE B38	2570.00	12.96
LTE B40	2302.50	12.96
LTE B41(HPUE)	2496.00	9.96
LTE B41_PC3	2496.00	9.96
LTE B42_PC3	3400.00	14.46
LTE B43_PC3	3600.00	14.46
5G NR n1	1920.00	12.85
5G NR n3	1710.00	12.35
5G NR n5	824.00	9.17
5G NR n7	2500.00	12.96
5G NR n8	880.00	9.46
5G NR n20	832.00	9.22
5G NR n28	703.00	8.48
5G NR n38	2570.00	12.96
5G NR n40	2302.50	12.96
5G NR n41_PC3	2496.00	12.96
5G NR n77_PC3	3300.00	12.96
5G NR n78_PC3	3300.00	12.96

UK UKCA

UKCA Declaration of Conformity

Following the above Approval Compliance Summary table, where applicable (green dot), hereby, Telit Communications S.p.A declares that the equipment complies with the Radio Equipment Regulations 2017 for UKCA.

The full text of the UKCA declaration of conformity is available at the following internet address: <https://www.telit.com/ukca>

The UKCA requirements can be found here:

<https://www.gov.uk/guidance/using-the-ukca-marking>

12.5 RoHS, REACH, and WEEE Info

RoHS Info

Any requests on information related to RoHS certifications can be addressed to Chemical.Certifications@telit.com.

REACH Info

Any requests on information related to REACH certifications can be addressed to Chemical.Certifications@telit.com.

WEEE Info



This symbol means that according to local laws and regulations your product and/or its battery shall be disposed of separately from household waste. When this product reaches its end of life, take it to a collection point designated by local authorities. Proper recycling of your product will protect human health and the environment.

13 Reference Table of RF Bands Characteristics

Table 66: LTE RF Bands Characteristics

E-UTRA BAND	Freq. Tx (MHz)	Freq. Rx (MHz)	Channels	Tx-Rx Offset
B1 - 2100	1920 ~ 1980	2110 ~ 2170	Tx: 18000 ~ 18599 Rx: 0 ~ 599	190 MHz
B2 - 1900 PCS	1850 ~ 1910	1930 ~ 1990	Tx: 18600 ~ 19199 Rx: 600 ~ 1199	80 MHz
B3 - 1800+	1710 ~ 1785	1805 ~ 1880	Tx: 19200 ~ 19949 Rx: 1200 ~ 1949	95 MHz
B4 - AWS-1	1710 ~ 1755	2110 ~ 2155	Tx: 19950 ~ 20399 Rx: 1950 ~ 2399	400 MHz
B5 - 850	824 ~ 849	869 ~ 894	Tx: 20400 ~ 20649 Rx: 2400 ~ 2649	45 MHz
B7 - 2600	2500 ~ 2570	2620 ~ 2690	Tx: 20750 ~ 21449 Rx: 2750 ~ 3449	120 MHz
B8 - 900 GSM	880 ~ 915	925 ~ 960	Tx: 21450 ~ 21799 Rx: 3450 ~ 3799	45 MHz
B12 - 700 a	699 ~ 716	729 ~ 746	Tx: 23010 ~ 23179 Rx: 5010 ~ 5179	30 MHz
B13 - 700 c	777 ~ 787	746 ~ 756	Tx: 23180 ~ 23279 Rx: 5180 ~ 5279	-31 MHz
B14 - 700 PS	788 ~ 798	758 ~ 768	Tx: 23280 ~ 23379 Rx: 5280 ~ 5379	-30 MHz
B17 - 700 b	704 ~ 716	734 ~ 746	Tx: 23730 ~ 23849 Rx: 5730 ~ 5849	30 MHz
B18 - 800 Lower	815 ~ 830	860 ~ 875	Tx: 23850 ~ 23999 Rx: 5850 ~ 5999	45 MHz
B19 - 800 Upper	830 ~ 845	875 ~ 890	Tx: 24000 ~ 24149 Rx: 6000 ~ 6149	45 MHz
B20 - 800 DD	832 ~ 862	791 ~ 821	Tx: 24150 ~ 24449 Rx: 6150 ~ 6449	-41 MHz
B25 - 1900+	1850 ~ 1915	1930 ~ 1995	Tx: 26040 ~ 26689 Rx: 8040 ~ 8689	80 MHz
B26 - 850+	814 ~ 849	859 ~ 894	Tx: 26690 ~ 27039 Rx: 8690 ~ 9039	45 MHz
B28 - 700 APT	703 ~ 748	758 ~ 803	Tx : 27210 ~ 27659 Rx : 9210 ~ 9659	55 MHz
B30 - 2300 WCS	2305 ~ 2315	2350 ~ 2360	Tx: 27660 ~ 27759 Rx: 9770 ~ 9869	45 MHz
B34 - 2000	2010 ~ 2025	2010 ~ 2025	Tx: 36200 ~ 36349 Rx: 36200 ~ 36349	0 MHz
B38 - 2600	2570 ~ 2620	2570 ~ 2620	Tx: 37750 ~ 38249	0 MHz

E-UTRA BAND	Freq. Tx (MHz)	Freq. Rx (MHz)	Channels	Tx-Rx Offset
			Rx: 37750 ~ 38249	
B39 - 1900+	1880 ~ 1920	1880 ~ 1920	Tx: 38250 ~ 38649 Rx: 38250 ~ 38649	0 MHz
B40 - 2300	2300 ~ 2400	2300 ~ 2400	Tx: 38650 ~ 39649 Rx: 38650 ~ 39649	0 MHz
B41 - 2600+	2496 ~ 2690	2496 ~ 2690	Tx: 39650 ~ 41589 Rx: 39650 ~ 41589	0 MHz
B42 - 3500	3400 ~ 3600	3400 ~ 3600	Tx: 41590 ~ 43589 Rx: 41590 ~ 43589	0 MHz
B43 - 3700	3600 ~ 3800	3600 ~ 3800	Tx: 43590 ~ 45589 Rx: 43590 ~ 45589	0 MHz
B48 - 3600	3550 ~ 3700	3550 ~ 3700	Tx: 55240 ~ 56739 Rx: 55240 ~ 56739	0 MHz
B66 - AWS	1710 ~ 1780	2110 ~ 2200	Tx: 131972 ~ 132671 Rx: 66436 ~ 67335	400 MHz
B70 - AWS-4	1695 - 1710	1995 - 2020	Tx: 132972 ~ 133121 Rx: 68336 ~ 68585	300 MHz
B71 - 600	663 ~ 698	617 ~ 652	Tx: 133122 ~ 133471 Rx: 68586 ~ 68935	-46 MHz
B106 - 900	896 ~ 901	935 ~ 940	TX: 134292 ~ 134341 RX: 70656 ~ 70705	39 MHz

Table 67: 5G NR RF Bands Characteristics

NR BAND	SCS (kHz)	Freq. Tx (MHz)	Freq. Rx (MHz)	Channels	Tx-Rx Offset
n1 - 2100	15	1920 ~ 1980	2110 ~ 2170	Tx: 384000 ~ 396000 Rx: 422000 ~ 434000	190 MHz
n2 - 1900 PCS	15	1850 ~ 1910	1930 ~ 1990	Tx: 370000 ~ 382000 Rx: 386000 ~ 398000	80 MHz
n3 - 1800	15	1710 ~ 1785	1805 ~ 1880	Tx: 342000 ~ 357000 Rx: 361000 ~ 376000	95 MHz
n5 - 850	15	824 ~ 849	869 ~ 894	Tx: 164800 ~ 169800 Rx: 173800 ~ 178800	45 MHz
n7 - 2600	15	2500 ~ 2570	2620 ~ 2690	Tx: 500000 ~ 514000 Rx: 524000 ~ 538000	120 MHz
n8 - 900	15	880 ~ 915	925 ~ 960	Tx: 176000 ~ 183000 Rx: 185000 ~ 192000	45 MHz
n12 - 700 a	15	699 ~ 716	729 ~ 746	Tx: 139800 ~ 143200 Rx: 145800 ~ 149200	30 MHz
n13 - 700 c	15	777 ~ 787	746 ~ 756	Tx: 155400 ~ 157400 Rx: 149200 ~ 151200	-31 MHz
n14 - 700 PS	15	788 ~ 798	758 ~ 768	Tx: 157600 ~ 159600 Rx: 151600 ~ 153600	-30 MHz

NR BAND	SCS (kHz)	Freq. Tx (MHz)	Freq. Rx (MHz)	Channels	Tx-Rx Offset
n18 - 800 Lower	15	815 ~ 830	860 ~ 875	Tx: 163000 ~ 166000 Rx: 172000 ~ 175000	45 MHz
n20 - 800	15	832 ~ 862	791 ~ 821	Tx: 166400 ~ 172400 Rx: 158200 ~ 164200	-41 MHz
n25 - 1900+	15	1850 ~ 1915	1930 ~ 1995	Tx: 370000 ~ 383000 Rx: 386000 ~ 399000	80 MHz
n26 - 850+	15	814 ~ 849	859 ~ 894	Tx: 162800 ~ 169800 Rx: 171800 ~ 178800	45 MHz
n28 - 700 APT	15	703 ~ 748	758 ~ 803	Tx: 140600 ~ 149600 Rx: 151600 ~ 160600	55 MHz
n30 - WCS	15	2305 ~ 2315	2350 ~ 2360	Tx: 461000 ~ 463000 Rx: 470000 ~ 472000	45 MHz
n38 - 2600	30	2570 ~ 2620	2570 ~ 2620	Tx: 514000 ~ 524000 Rx: 514000 ~ 524000	0 MHz
n40 - 2300	30	2300 ~ 2400	2570 ~ 2620	Tx: 460000 ~ 480000 Rx: 460000 ~ 480000	0 MHz
n41 - 2600+	30	2496 ~ 2690	2570 ~ 2620	Tx: 460000 ~ 480000 Rx: 460000 ~ 480000	0 MHz
n48 - 3600	30	3550 ~ 3700	2570 ~ 2620	Tx: 636668 ~ 646666 Rx: 636668 ~ 646666	0 MHz
n66 - AWS-3	15	1710 ~ 1780	2110 ~ 2200	Tx: 342000 ~ 356000 Rx: 422000 ~ 440000	400 MHz
n70 - AWS-4	15	1695 ~ 1710	1995 ~ 2020	Tx: 339000 ~ 342000 Rx: 399000 ~ 404000	300 MHz
n71 - 600	15	663 ~ 698	617 ~ 652	Tx: 132600 ~ 139600 Rx: 123400 ~ 130400	-46 MHz
n77 - 3700	30	3300 ~ 4200	3300 ~ 4200	Tx: 620000 ~ 680000 Rx: 620000 ~ 680000	0 MHz
n78 - 3500	30	3300 ~ 3800	3300 ~ 4200	Tx: 620000 ~ 653332 Rx: 620000 ~ 653332	0 MHz
n79 - 4700	30	4400 ~ 5000	3300 ~ 4200	Tx: 693334 ~ 733332 Rx: 693334 ~ 733332	0 MHz

14 Acronyms and Abbreviations

Table 68: Acronyms and Abbreviations

Acronym	Definition
ADC	Analog – Digital Converter
CLK	Clock
CMOS	Complementary Metal – Oxide Semiconductor
CS	Chip Select
DAC	Digital – Analog Converter
DTE	Data Terminal Equipment
ESR	Equivalent Series Resistance
GPIO	General Purpose Input Output
HS	High Speed
HSDPA	High-Speed Downlink Packet Access
HSIC	High-Speed Inter Chip
HSUPA	High-Speed Uplink Packet Access
I2C	Inter-integrated circuit
I2S	Inter-IC sound
I/O	Input Output
MISO	Master Input – Slave Output
MOSI	Master Output – Slave Input
MRDY	Master Ready
PCB	Printed Circuit Board
PCIe	Peripheral component interconnect express
RTC	Real-Time Clock
SGMII	Serial Gigabit media-independent interface
SIM	Subscriber Identification Module
SPI	Serial Peripheral Interface
SRDY	Slave Ready
TTSC	Telit Technical Support Centre
UART	Universal Asynchronous Receiver Transmitter
UMTS	Universal Mobile Telecommunication System
USB	Universal Serial Bus
VNA	Vector Network Analyzer
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access

15 Related Documents

For current documentation and downloads, refer to <https://dz.telit.com/>.

Table 69: Related Documents

S.no	Doc Code	Document Title
1	80791ST11208A	FE910C04 Family AT Commands Reference Guide
2	1VV0301984	FE910C04 Family Software User guide
3		

16 Document History

Table 70: Document History

Revision	Date	Changes
4	2025-07-03	Added LTE Band 70 and LTE Band 106 support Updated 4.1 – Pin-out Updated 4.2 – Signals That Must Be Connected Updated 4.3 – LGA Pads Layout Updated 6.7 – Fast Power Down Updated 6.8.6 – SGMII Updated 6.11.4 – ADC Converter Updated Table 3: Main features (NR/LTE Peak data rates) Updated Table 58, 62, 65 Max Antenna Gain Updated Table 9 Connected mode - LTE/NR Max power consumption Updated Table 42: LTE Typical Rx sensitivity levels Updated Table 43: NR Typical Rx sensitivity levels Updated 12 Conformity Assessment Issues - Add “FE910C04-WWD” to table 57/59/60/61/63 - Update the regulatory version
3	2025-03-25	Update new variant FE910C04-WWD Updated Figure 1 Block Diagram Updated 4.1 – Pin-out Updated 4.2 – Signals that Must Be Connected Updated 4.3 – LGA Pads Layout Updated 6.2 – Power On Updated 6.2 – Power Off Updated 6.5 – Hardware Shutdown Updated 6.8.2 – UART Updated 8.4 – GNSS Characteristic Updated Table 2: Product Variants and their Frequency Bands Updated Table 4: Temperature Range Updated Table 7: Power supply requirements Updated Table 8: Idle mode Updated Table 9: Connected Mode. Updated Table 30: Power Supply Requirements Updated Table 39: Bands Variant Updated Table 40: Conducted Transmit Output Power Updated Table 42: LTE Typical RX sensitivity levels Updated Table 47: GNSS Antenna specification – Frequency range Updated Table 49: GNSS Characteristics Updated Table 66: LTE RF Bands Characteristics Updated 12 Conformity Assessment Issues
2	2025-02-18	Updated 4.2 – Signals that Must Be Connected Updated 6.2 – Power On Updated 6.3 – Power Off

Revision	Date	Changes
		Updated 6.4 – Shutdown by Software Command Updated 6.5 – Hardware Shutdown Updated 6.6 – Unconditional Shutdown Updated 6.7 – Fast Power Down
1	2024-12-18	Updated 3.4 – Main features Updated 3.5 – Block Diagram Updated 4.1 – Pin-out Updated 4.2 – Signals that Must Be Connected Updated 4.3 – LGA Pads Layout Updated 5.2 – Power Consumption Updated 6.12 – USB PCIe boot Switch Updated 6.8.1.1 – USB Layout Guidelines Updated 6.8.5 – PCIe Updated 6.8.6 – SGMII Updated 6.8.6.1 – SGMII Layout Guidelines Updated 6.8.7.1 – Wi-Fi Coexistence Updated 6.9 – General purpose I/O Updated 7.2 – Conducted Transmit Output Power Updated 7.3 – Conducted Receiver Sensitivity Updated 7.4.2.2 – Transmission Line Measurement Updated 8.4 – GNSS Characteristics
0	2024-07-23	Initial release

From Mod.0818 Rev.13

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