



FE912C04

Hardware Design Guide

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1 Applicability Table

Table 1: Applicability Table

Products
FE912C04-NA
FE912C04-RW

2 Introduction

2.1 Scope

This document introduces the Telit FE912C04 module and presents possible and recommended hardware solutions for the development of a product based on the FE912C04 module. All the features and solutions described in this document are applicable to all FE912C04 variants, where “FE912C04” refers to the variants listed in the applicability table.

Note: FE912C04 refers to all modules listed in the Applicability Table. This document covers all the basic functions of a wireless module; it cannot include every hardware solution or every product that can be designed. Where the suggested hardware configurations are not to be considered mandatory, the information provided should be used as a guide and starting point to successfully develop the product with the Telit FE912C04 module.

Note: The integration of the LTE/5G FE912C04 cellular module within a user application must be done according to the design rules described in this manual.

2.2 Audience

This document is intended for system integrators that are using the Telit FE912C04 module in their products.

2.3 Contact Information, Support

For technical support and general questions, e-mail:

- TS-EMEA@telit.com
- TS-AMERICAS@telit.com
- TS-APAC@telit.com
- TS-SRD@telit.com
- TS-ONEEDGE@telit.com

Alternatively, use: <https://www.telit.com/contact-us/>

For Product information and technical documents, visit: <https://www.telit.com>

2.4 Conventions

Note: Provide advice and suggestions that may be useful when integrating the module.

Danger: This information MUST be followed, or catastrophic equipment failure or personal injury may occur.

Warning: Alerts the user on important steps about the module integration.

All dates are in ISO 8601 format, that is YYYY-MM-DD.

2.5 Terms and Conditions

Refer to <https://www.telit.com/hardware-terms-conditions/>.

2.6 Disclaimer

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3 General Product Description

3.1 Overview

The FE912C04 is an industrial-grade, LTE Cat4 / 5G RedCap module series ideal for IoT applications that need 5G mid-speed data communication. The optional embedded GNSS receiver makes the FE912C04 ideal for all-in-one tracking use cases in which more precise, faster-refreshing, satellite-based positioning and navigation must complement cellular-based positioning.

FE912C04 is available in hardware variants as listed in Applicability Table. For differences in the designated RF band sets – refer to Section 3.2.Bands Variants.

Note:

(EN) The integration of the FE912C04 cellular module within user application shall be done according to the design rules described in this manual.

(IT) L'integrazione del modulo cellulare FE912C04 all'interno dell'applicazione dell'utente dovrà rispettare le indicazioni progettuali descritte in questo manuale.

(DE) Die Integration des FE912C04 Mobilfunk-Moduls in ein Gerät muß gemäß der in diesem Dokument beschriebenen Konstruktionsregeln erfolgen.

(SL) Integracija FE912C04 modula v uporabniški aplikaciji bo morala upoštevati projektna navodila, opisana v tem priročniku.

(SP) La utilización del modulo FE912C04 debe ser conforme a los usos para los cuales ha sido diseñado descritos en este manual del usuario.

(FR) L'intégration du module cellulaire FE912C04 dans l'application de l'utilisateur sera faite selon les règles de conception décrites dans ce manuel.

(HE) ייעשה המשתמש יישום בתוך FE912C04 הסלולרי המודול של השילוב זה במדריך המתוארים התכנון לכללי בהתאם.

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3.2 Product Variants and Frequency Bands

Table 2 summarizes all region variants within the FE912C04 family, showing the band sets supported in each variant.

Different bands combinations are available:

Table 2: Product Variants and their Frequency Bands

Region Variant	LTE Cat4	5G FR1 RedCap	GNSS
FE912C04-NA	B2, B4, B5, B7, B12, B13, B14, B17, B25, B26, B30, B41, B48, B66, B71	n2, n5, n7, n12, n13, n14, n25, n26, n41, n48, n66, n71, n77, n78	GNSS L1/L5
FE912C04-RW	B1, B2, B3, B4, B5, B7, B8, B20, B28, B40, B41	n1, n3, n5, n7, n8, n20, n28, n40, n41, n77, n78	GNSS L1/L5

For details information about frequencies and bands, refer to the [RF Section](#).

Note: Cellular technologies and frequency bands that are enabled may vary based on the firmware version and firmware configuration used.

3.3 Target Market

FE912C04 can be used for rugged industrial applications where tamper-resistance, confidentiality, integrity, and authenticity of end-user information are essential. Target applications may include:

- Body Cameras
- Surveillance camera applications

3.4 Main Features

The FE912C04 series of cellular modules features an LTE CAT4, 5G modem baseband and RF transceiver to cover 600MHz~5GHz bands for worldwide roaming.

Table 3: Functional Features

Function	Features
Modem	5G NR RedCap, 3GPP Release 17 • DL 200Mbps / UL 100Mbps FDD, TDD LTE CAT4 • DL 150Mbps/ UL 50Mbps Support for SIM profile switching. Regional variants with optimal choice of RF bands for worldwide coverage of countries and MNOs
Two USIM ports – dual voltage	• Class B and Class C support • Hot swap support • Clock rates up to 5 MHz
Application processor	Application processor to run customer application code • ARM Cortex-A7 up to 1.7 GHz 2Gbit NAND Flash + 2Gbit LPDDR2 533 MHz MCP
Interfaces	Rich set of interfaces, including: • USB2.0 • UART • USIM x2 • GPIOs • Antenna ports
Form factor	Form factor (28x31mm)

Function	Features
Environment and quality requirements	The entire module is designed and qualified by Telit for satisfying the environment and quality requirements.
Single supply module	The module generates all its internal supply voltages.
Operating temperature	Range -40 °C to +85 °C (conditions as defined in Section 3.7 Temperature Range)

3.5 Block Diagram

Figure1 below shows an overview of the internal architecture of the FE912C04 module. It includes the following sub-functions:

- Application processor and Modem subsystem with their external interfaces. These two functions are contained in a single SOC.
- RF front end and antenna ports.
- Rich IO interfaces. Depending on which FE912C04 software features are enabled, some of its exported interfaces due to multiplexing may be used internally and therefore may not be usable by the application.

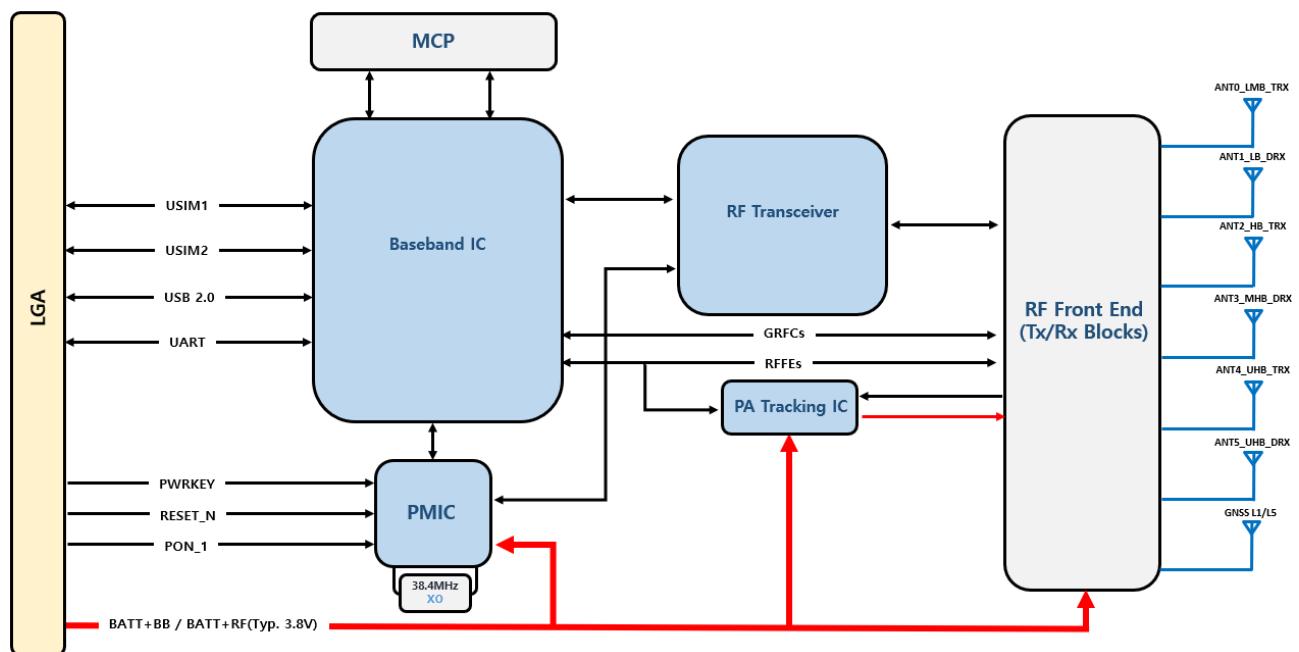


Figure 1: Block Diagram

3.6 Mechanical Specifications

3.6.1 Dimensions

The overall dimensions of FE912C04 are:

Table 4: Dimensions

Mechanical dimensions	mm
Length	28.0 mm, +/- 0.15 mm tolerance
Width	31.0 mm, +/- 0.15 mm tolerance
Thickness	2.4 mm, +/- 0.2 mm tolerance

3.6.2 Weight

The nominal weight of the FE912C04 is 5 grams.

3.7 Temperature Range

Table 5: Temperature Range

Mode	Temperature	Note
Operating Temperature Range	-20°C ~ +55°C	The module is fully functional(*) in all the temperature range and it fully meets the 3GPP specifications.
	-40°C ~ +85°C	The module is fully functional (*) in all the temperature range, might slightly deviate from the 3GPP specifications.
Storage and non-operating Temperature Range	-40°C ~ +90°C	The module is not powered and not connected to power supply

Note: (*) Functional: if applicable, the module is able to make and receive voice calls, data calls, send and receive SMS and data traffic.

4 Pins Allocation

4.1 Pin-out

Table 6: Pin-out Information

Pin	Signal	I/O	Function	Type	Comment
USB HS 2.0 Communication Port					
183	USB_D+	I/O	USB differential Data (+)		
184	USB_D-	I/O	USB differential Data (-)		
182	USB_VBUS	I	USB connection detect		
179	USB_ID	I	USB ID detect		
30	USB_BOOT	I	Force the module into emergency download mode	1.8V	Active high
Debug UART					
89	DBG_UART_TX	O	Debug UART transmit	1.8V	
88	DBG_UART_RX	I	Debug UART receive	1.8V	
COEX UART					
29	COEX_UART_TX	O	COEX UART transmit	1.8V	
32	COEX_UART_RX	I	COEX UART receive	1.8V	
SIM Card Interface 1					
141	USIM1_CLK	O	External SIM 1 signal – Clock	1.8 / 2.95 V	
142	USIM1_RST	O	External SIM 1 signal – Reset	1.8 / 2.95 V	
138	USIM1_DATA	I/O	External SIM 1 signal - Data I/O	1.8 / 2.95 V	
143	USIM1_DET	I	External SIM 1 signal - Presence	1.8V	
139	USIM1_VDD	-	External SIM 1 signal – Power supply for SIM 1	1.8 / 2.95 V	
SIM Card Interface 2					
147	USIM2_CLK	O	External SIM 2 signal – Clock	1.8 / 2.95 V	
145	USIM2_RST	O	External SIM 2 signal – Reset	1.8 / 2.95 V	
144	USIM2_DATA	I/O	External SIM 2 signal – Data I/O	1.8 / 2.95 V	
146	USIM2_DET	I	External SIM 2 signal – Presence	1.8V	
148	USIM2_VDD	-	External SIM 2 signal – Power supply for SIM 2	1.8 / 2.95 V	
Antenna Tuner General Purpose Digital I/O					
103	GRFC0	O	GPIO Antenna switch control	1.8V	
106	GRFC1	O	GPIO Antenna switch control	1.8V	
118	GRFC2	O	GPIO Antenna switch control	1.8V	
121	GRFC3	O	GPIO Antenna switch control	1.8V	
RF Section					
98	PRx_LBMB	I/O	Primary antenna for Low/Mid band	RF	50 Ohm impedance
133	DRx_LB	I/O	Secondary antenna for Low band	RF	50 Ohm impedance

Pin	Signal	I/O	Function	Type	Comment
107	PRx_HB	I/O	Primary antenna for High band	RF	50 Ohm impedance
125	DRx_MBHB	I/O	Secondary antenna for Mid/High band	RF	50 Ohm impedance
113	PRx_UHB	I/O	Primary antenna for Ultra High band	RF	50 Ohm impedance
119	DRx_UHB	I/O	Secondary antenna for Ultra High band	RF	50 Ohm impedance
GNSS Section					
66	GNSS	I	GNSS antenna	RF	50 Ohm impedance
41	GNSS_1PPS	O	GNSS 1PPS signal	1.8V	
36	GNSS_UART_TXD	O	UART transmit	1.8V	UART for GNSS
39	GNSS_UART_RXD	I	UART receive	1.8V	UART for GNSS
37	GNSS_UART_RTS	I	UART Request to Send	1.8V	UART for GNSS
34	GNSS_UART_CTS	O	UART Clear to Send	1.8V	UART for GNSS
Module Turn ON/OFF					
171	PWRKEY	I	Power ON / OFF		Active low. Internally pulled up to 1.5V
173	PON_1	I	Turn on the module automatically		Active high. If unused, pull it down to GND. Internally pulled up to 1.8V
172	RESET_N	I	Reset the module		Active low. Internally pulled up to 1.5V
ADC					
18	ADC0	I	Analog Digital Converter	0 ~ 1.875 V	
Miscellaneous Functions					
15	DPR	I	Dynamic power reduction	1.8 V	Active low
90	W_DISABLE#	I	Airplane mode control	1.8 V	Active low Pulled up by default. Internal 4.7 K PU.
Indication Functions					

Pin	Signal	I/O	Function	Type	Comment
23	SLEEP_IND	O	Indicate module sleep mode	1.8 V	If unused, keep these pins open.
24	STATUS	O	indicate module operaton status	1.8 V	
25	NET_MODE	O	Indicate network registration	1.8 V	
27	NET_STATUS	O	Indicate network activity	1.8 V	
Power Supply					
162	VBATT	-	Main Power Supply (Digital Section)	Power	
163	VBATT	-	Main Power Supply (Digital Section)	Power	
165	VBATT	-	Main Power Supply (Digital Section)	Power	
156	VBATT_RF		Main Power Supply (RF Section)	Power	
157	VBATT_RF	-	Main Power Supply (RF Section)	Power	
159	VBATT_RF	-	Main Power Supply (RF Section)	Power	
160	VBATT_RF	-	Main Power Supply (RF Section)	Power	
43	VDD_EXT	O	Power for external circuitry	1.8V	
Ground					
5	GND	-	Ground		
6	GND	-	Ground		
13	GND	-	Ground		
14	GND	-	Ground		
19	GND	-	Ground		
28	GND	-	Ground		
33	GND	-	Ground		
35	GND	-	Ground		
40	GND	-	Ground		
48	GND	-	Ground		
53	GND	-	Ground		
57	GND	-	Ground		
60	GND	-	Ground		
63	GND	-	Ground		
65	GND	-	Ground		
67	GND	-	Ground		
68	GND	-	Ground		
69	GND	-	Ground		
72	GND	-	Ground		
87	GND	-	Ground		
91	GND	-	Ground		
92	GND	-	Ground		
93	GND	-	Ground		
94	GND	-	Ground		
95	GND	-	Ground		
96	GND	-	Ground		

Pin	Signal	I/O	Function	Type	Comment
97	GND	-	Ground		
99	GND	-	Ground		
100	GND	-	Ground		
101	GND	-	Ground		
102	GND	-	Ground		
104	GND	-	Ground		
105	GND	-	Ground		
108	GND	-	Ground		
109	GND	-	Ground		
110	GND	-	Ground		
111	GND	-	Ground		
112	GND	-	Ground		
114	GND	-	Ground		
115	GND	-	Ground		
116	GND	-	Ground		
117	GND	-	Ground		
120	GND	-	Ground		
122	GND	-	Ground		
123	GND	-	Ground		
124	GND	-	Ground		
126	GND	-	Ground		
127	GND	-	Ground		
128	GND	-	Ground		
129	GND	-	Ground		
130	GND	-	Ground		
131	GND	-	Ground		
132	GND	-	Ground		
134	GND	-	Ground		
135	GND	-	Ground		
136	GND	-	Ground		
137	GND	-	Ground		
140	GND	-	Ground		
150	GND	-	Ground		
151	GND	-	Ground		
153	GND	-	Ground		
154	GND	-	Ground		
155	GND	-	Ground		
158	GND	-	Ground		
166	GND	-	Ground		
168	GND	-	Ground		

Pin	Signal	I/O	Function	Type	Comment
169	GND	-	Ground		
174	GND	-	Ground		
176	GND	-	Ground		
181	GND	-	Ground		
185	GND	-	Ground		
186	GND	-	Ground		
187	GND	-	Ground		
188	GND	-	Ground		
189	GND	-	Ground		
190	GND	-	Ground		
191	GND	-	Ground		
192	GND	-	Ground		
193	GND	-	Ground		
194	GND	-	Ground		
195	GND	-	Ground		
196	GND	-	Ground		
197	GND	-	Ground		
198	GND	-	Ground		
199	GND	-	Ground		
200	GND	-	Ground		
201	GND	-	Ground		
202	GND	-	Ground		
203	GND	-	Ground		
204	GND	-	Ground		
205	GND	-	Ground		
206	GND	-	Ground		
207	GND	-	Ground		
208	GND	-	Ground		
209	GND	-	Ground		
210	GND	-	Ground		
211	GND	-	Ground		
212	GND	-	Ground		
213	GND	-	Ground		
214	GND	-	Ground		
215	GND	-	Ground		
216	GND	-	Ground		
217	GND	-	Ground		
218	GND	-	Ground		
219	GND	-	Ground		
220	GND	-	Ground		

Pin	Signal	I/O	Function	Type	Comment
221	GND	-	Ground		
222	GND	-	Ground		
223	GND	-	Ground		
224	GND	-	Ground		
225	GND	-	Ground		
226	GND	-	Ground		
227	GND	-	Ground		
228	GND	-	Ground		
229	GND	-	Ground		
230	GND	-	Ground		
Reserved for Internal Use					
1	TC_1	-	Reserved		HWKEY
2	TC_2	-	Reserved		JTAG_TRST_N
3	TC_3	-	Reserved		JTAG_TCK
4	TC_4	-	Reserved		JTAG_SRST_N
7	TC_5	-	Reserved		JTAG_TMS
9	TC_6	-	Reserved		JTAG_TDI
10	TC_7	-	Reserved		SDX_RESOUT_N
12	TC_8	-	Reserved		JTAG_TDO
Reserved					
8	Reserved	-	Reserved		
11	Reserved	-	Reserved		
16	Reserved	-	Reserved		
17	Reserved	-	Reserved		
20	Reserved	-	Reserved		
21	Reserved	-	Reserved		
22	Reserved	-	Reserved		
26	Reserved	-	Reserved		
31	Reserved	-	Reserved		
38	Reserved	-	Reserved		
42	Reserved	-	Reserved		
44	Reserved	-	Reserved		
45	Reserved	-	Reserved		
46	Reserved	-	Reserved		
47	Reserved	-	Reserved		
49	Reserved	-	Reserved		
50	Reserved	-	Reserved		
51	Reserved	-	Reserved		
52	Reserved	-	Reserved		

Pin	Signal	I/O	Function	Type	Comment
54	Reserved	-	Reserved		
55	Reserved	-	Reserved		
56	Reserved	-	Reserved		
58	Reserved	-	Reserved		
59	Reserved	-	Reserved		
61	Reserved	-	Reserved		
62	Reserved	-	Reserved		
64	Reserved	-	Reserved		
70	Reserved	-	Reserved		
71	Reserved	-	Reserved		
73	Reserved	-	Reserved		
74	Reserved	-	Reserved		
75	Reserved	-	Reserved		
76	Reserved	-	Reserved		
77	Reserved	-	Reserved		
78	Reserved	-	Reserved		
79	Reserved	-	Reserved		
80	Reserved	-	Reserved		
81	Reserved	-	Reserved		
82	Reserved	-	Reserved		
83	Reserved	-	Reserved		
84	Reserved	-	Reserved		
85	Reserved	-	Reserved		
86	Reserved	-	Reserved		
149	Reserved	-	Reserved		
152	Reserved	-	Reserved		
161	Reserved	-	Reserved		
164	Reserved	-	Reserved		
167	Reserved	-	Reserved		
170	Reserved	-	Reserved		
175	Reserved	-	Reserved		
177	Reserved	-	Reserved		
178	Reserved	-	Reserved		
180	Reserved	-	Reserved		

Note: When the UART signals are used as the communication port between the host and the modem, the RTS must be connected to GND (on the module side) if flow control is not used. If the UART port is not used, all UART signals can be left disconnected.

Warning: Reserved pins must not be connected.

4.2 Signals that Must Be Connected

The below table lists the FE912C04 signals that must be connected even if not used by the end application.

Table 7: FE912C04 signals that must be connected.

PAD	Signal	Notes
162, 163, 165, 156, 157, 159, 160	VBATT & VBATT_RF	Main Power Supply(Digital / RF Section)
5, 6, 13, 14, 19, 28, 33, 35, 40, 48, 53, 57, 60, 63, 65, 67, 68, 69, 72, 87, 91, 92, 93, 94, 95, 96, 97, 99, 100, 101, 102, 104, 105, 108, 109, 110, 111, 112, 114, 115, 116, 117, 120, 122, 123, 124, 126, 127, 128, 129, 130, 131, 132, 134, 135, 136, 137, 140, 150, 151, 153, 154, 155, 158, 166, 168, 169, 174, 176, 181, 185, 186, 187, 188, 189, 190, 191, 192, 193, 194, 195, 196, 197, 198, 199, 200, 201, 202, 203, 204, 205, 206, 207, 208, 209, 210, 211, 212, 213, 214, 215, 216, 217, 218, 219, 220, 221, 222, 223, 224, 225, 226, 227, 228, 229, 230	GND	
171	PWRKEY	Main power ON/OFF signal
173	PON_1	If not used, float
172	RESET_N	Reset the module
183	USB_D+	If not used, float
184	USB_D-	If not used, float
182	USB_VBUS	USB connection detect
30	USB_BOOT	Force the module into emergency download mode
36	GNSS_UART_TX	If not used, float
39	GNSS_UART_RX	If not used, float
37	GNSS_UART_RTS	If not used, float
34	GNSS_UART_CTS	If not used, float
89	DEBUG_UART_TXD	If not used, float
88	DEBUG_UART_RXD	If not used, float
98	PRx_LBMB	If not used, connect to 50 Ohm termination
133	DRx_LB	If not used, connect to 50 Ohm termination
107	PRx_HB	If not used, connect to 50 Ohm termination

PAD	Signal	Notes
125	DRx_MBHB	If not used, connect to 50 Ohm termination
113	PRx_UHB	If not used, connect to 50 Ohm termination
119	DRx_UHB	If not used, connect to 50 Ohm termination
66	GNSS	If not used, connect to 50 Ohm termination
29	COEX_UART_TX	If not used, float
32	COEX_UART_RX	If not used, float

4.3 LGA Pads Layout

Top View

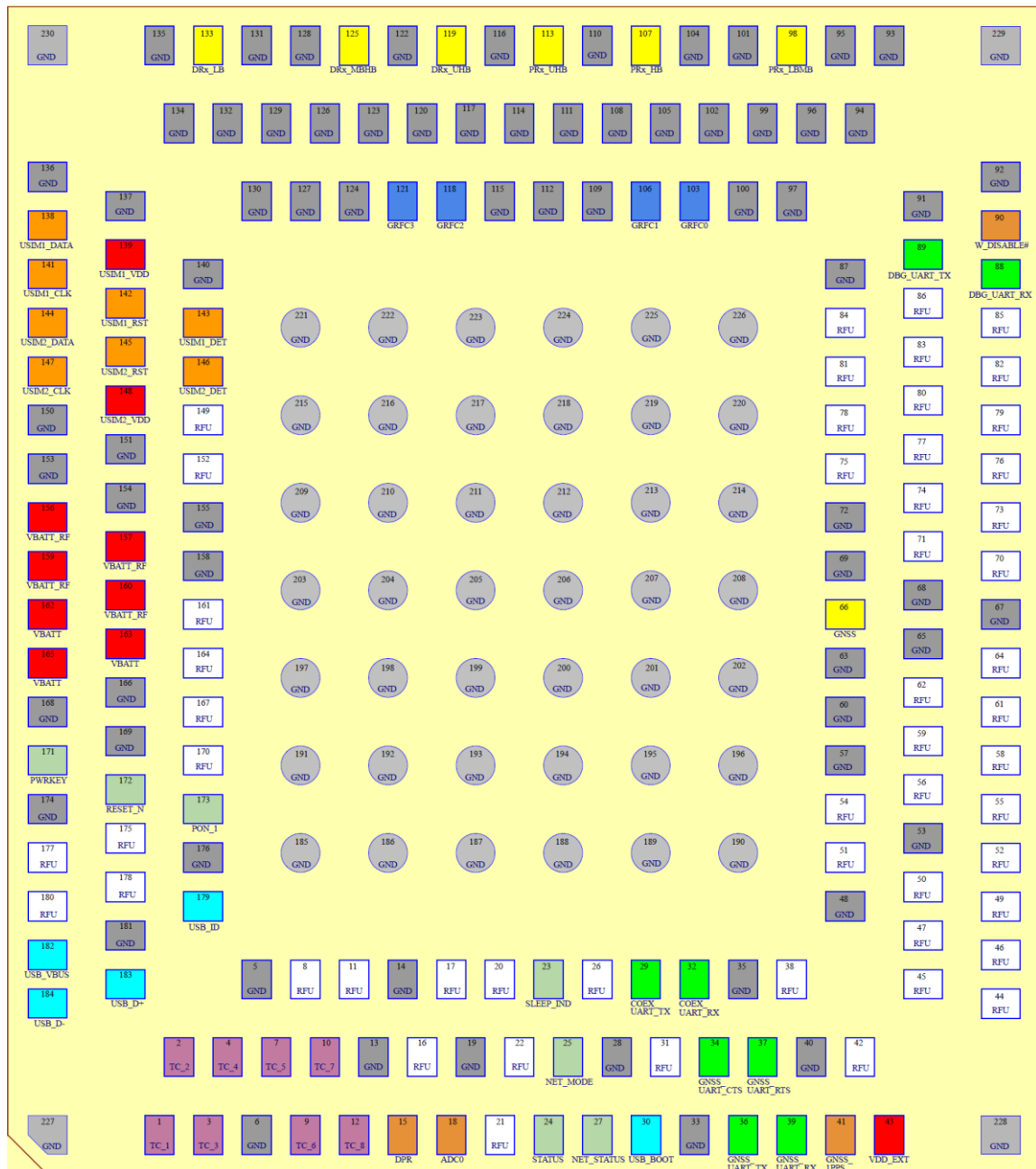
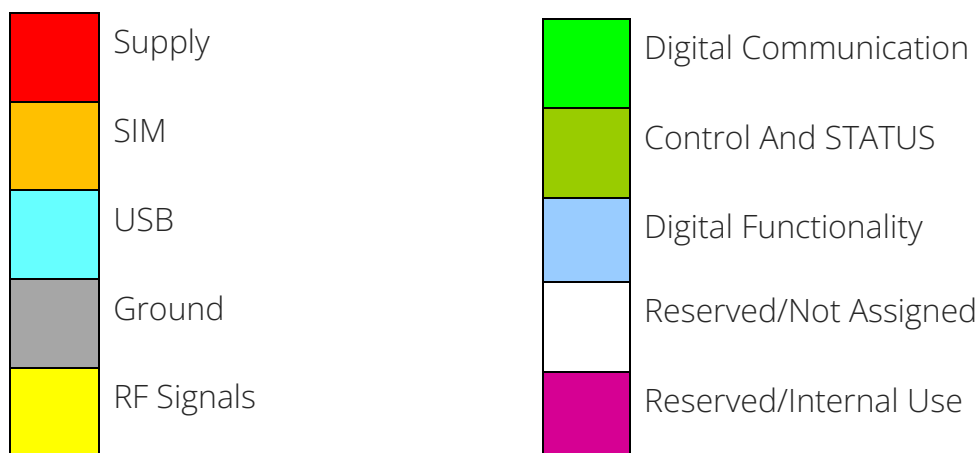


Figure 2: LGA Pads Layout



5 Power Supply

The power supply circuitry and the board layout are a very important part of the full product design and they strongly reflect on the product's overall performance, so the requirements and the guidelines that will follow should be read carefully for a proper design.

5.1 Power Supply Requirements

The external power supply must be connected to VBATT and VBATT_PA pads and must fulfil the following requirements:

Table 8: Power Supply Requirements

Power Supply	Value
Nominal Supply Voltage	3.8 V
Operating Voltage Range	3.4 V - 4.2 V
Max ripple on module input supply	30 mV

Note:

- The Operating Voltage Range MUST never be exceeded; the application's power supply section must be designed with care to avoid an excessive voltage drop
- If the voltage drop exceeds the limits, it may cause an unintentional module power off.
- The voltage must be at least VBATTmin to power the module.
- The exceeding voltage and drop in MUST never be exceeded.
- For PTCRB approval on the final products the power supply is required to be within the "Normal Operating Voltage Range".

5.2 Power Consumption

5.2.1 Idle Mode

Table 9: Idle Mode

Mode	Band	Measure (Typ)	Condition
Turn off	-	37 uA	Power off
RF Disabled	-	1.51 mA	AT+CFUN=0 (USB disconnect)
	-	1.73 mA	AT+CFUN=4 (USB disconnect), Flight mode.
Idle Mode	B5	3.26 mA	LTE DRX@0.32s (USB selective suspend)
		2.82 mA	LTE DRX@0.64s (USB selective suspend)
		2.69 mA	LTE DRX@1.28s (USB selective suspend)
		2.62 mA	LTE DRX@2.56s (USB selective suspend)
	n66	3.88 mA	5G NR DRX@0.32s (USB selective suspend)
		3.4 mA	5G NR DRX@0.64s (USB selective suspend)
		2.95 mA	5G NR DRX@1.28s (USB selective suspend)
		2.92 mA	5G NR DRX@2.56s (USB selective suspend)

Table 10: GNSS Mode

Mode		Measure (Typ)	Condition
Active State (LTE Idel mode)	Acquisition	67 mA	L1+L5 All Constellations (USB Active)
	Tracking	66 mA	L1+L5 All Constellations (USB Active)

5.2.2 FE912C04 Connected Mode

Table 11: FE912C04 Connected Mode

Mode	Band	Measure (Typ)	Condition
LTE Cat4 (USB Active, GNSS OFF)	B5	435 mA	LTE FDD LB @ 23.5dBm
	B5	115 mA	LTE FDD LB @ 0 dBm
	B1	535 mA	LTE FDD MB @ 23.5dBm
	B1	150 mA	LTE FDD MB @ 0 dBm
	B7	575 mA	LTE FDD HB @ 23.5dBm
	B7	145 mA	LTE FDD HB @ 0 dBm
	B41 (HPUE)	480 mA	LTE TDD HB @ 26dBm
	B41 (HPUE)	90 mA	LTE TDD HB @ 0dBm
	B48	225 mA	LTE TDD UHB @ 23.5dBm
	B48	100 mA	LTE TDD UHB @ 0 dBm
5G SA (USB Active, GNSS OFF)	n5	355 mA	5G NR FDD LB @ 23.5 dBm
	n5	90 mA	5G NR FDD LB @ 0 dBm
	n1	450 mA	5G NR FDD MB @ 23.5 dBm
	n1	105 mA	5G NR FDD MB @ 0 dBm
	n7	475 mA	5G NR FDD HB @ 23.5 dBm
	n7	115 mA	5G NR FDD HB @ 0 dBm
	n77	195 mA	5G NR TDD UHB @ 23.5 dBm
	n77	100 mA	5G NR TDD UHB @ 0 dBm

Note:

- Worst/best case current values depend on network configuration, not under module control.
- The electrical design for the power supply must ensure a peak current output of at least 2.0A.
- The support of specific network wireless technology depends on the product variant configuration.
- The power supply must be designed to withstand current peaks without large voltage drops. This means that both the electrical design and the board layout must be designed for this current flow.
- If the voltage drops during the peaks, the current absorption is too high. The device may even shut down due to a drop in the supply voltage.

5.3 General Design Rule

The main guidelines for the Power Supply Design include three different design steps:

- The electrical design of the power supply
- The thermal design
- The PCB layout

5.3.1 Electrical Design Guidelines

The electrical design of the power supply strongly depends on the power source where this power is drained. We will distinguish them into three categories:

- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)
- Battery

5.3.1.1 +5V Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, so there's not a big difference between the input source and the desired output and a linear regulator can be used. A switching power supply will not be suitable due to the low drop out requirements.
- When using a linear regulator, a proper heat sink shall be provided to dissipate the power generated.
- A Bypass low ESR capacitor of adequate capacity must be provided to cut the current absorption peaks close to the Module, a 100 μ F capacitor is usually suitable.
- Make sure the low ESR capacitor on the power supply output is rated at least 10V.
- A protection diode must be placed near the power input to protect the FE912C04 module from power polarity inversion.

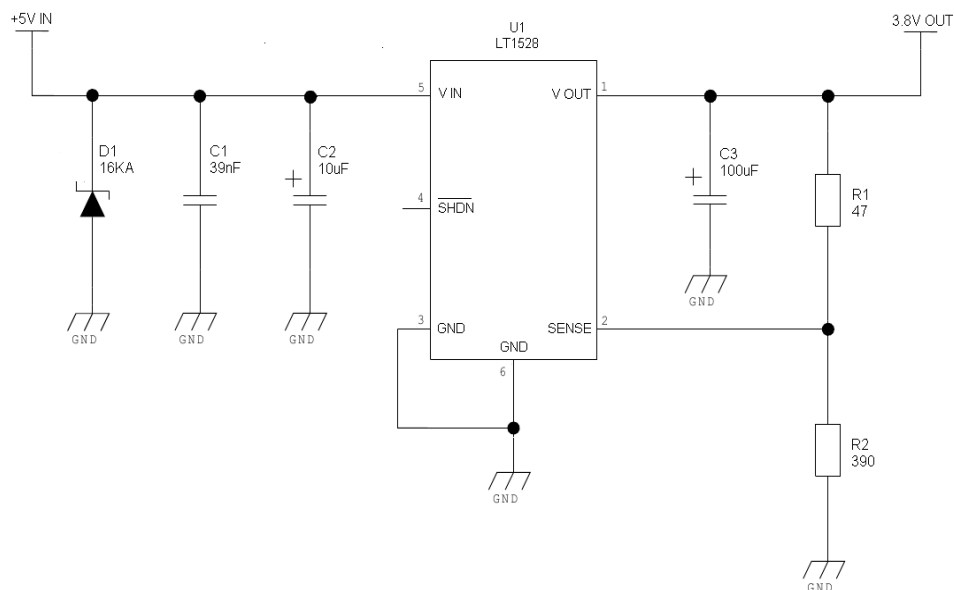


Figure 3: An Example of Linear Regulator with 5V Input

5.3.1.2 +12V Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, so due to the big difference between the input source and the desired output, a linear regulator is not suitable and shall not be used. A switching power supply will be preferable because of its better efficiency.
- When using a switching regulator, a 500kHz or more, switching frequency regulator is preferable because of its smaller inductor size and its faster transient response. This allows the regulator to respond quickly to the current peak absorption.
- In any case, the frequency and Switching design selection are related to the application to be developed since the switching frequency could also generate EMC interferences.
- For the car PB battery, the input voltage can rise to 15.8V and this should be kept in mind when choosing components: all components in the power supply must withstand this voltage.
- A Bypass low ESR capacitor of adequate capacity must be provided to cut the current absorption peaks, a 100μF capacitor is usually suitable.
- Make sure the low ESR capacitor on the power supply output is rated at least 10V.
- For Car applications, a spike protection diode should be inserted close to the power input, to clean the supply from the spikes.

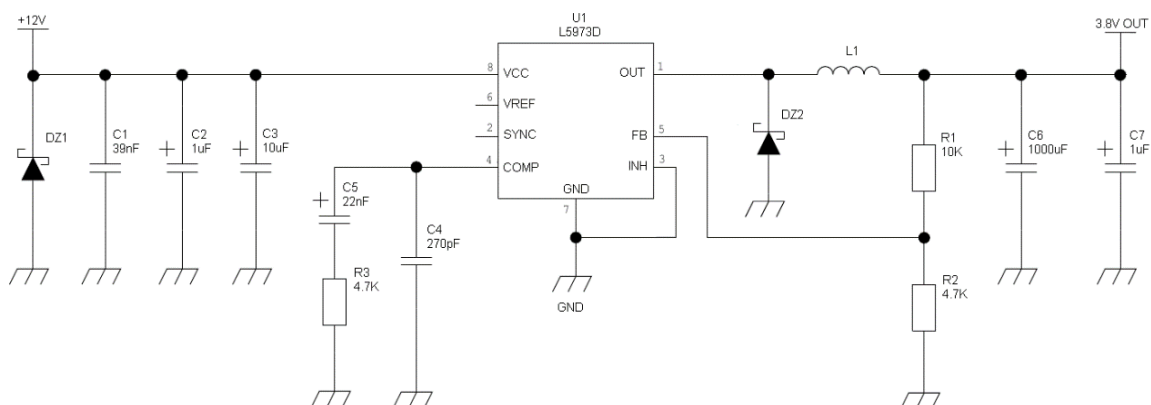


Figure 4: An Example of Switching Regulator with 12V Input

5.3.1.3 Battery Source Power Supply Design Guidelines

The desired nominal output for the power supply is 3.8V and the maximum voltage allowed is 4.2V, so a single 3.7V Li-Ion cell battery type is suitable to supply power to the Telit FE912C04 module.

- A Bypass low ESR capacitor of adequate capacity must be provided to cut the current absorption peaks, a 100μF tantalum capacitor is usually suitable.
- Make sure the low ESR capacitor (usually a tantalum one) is rated at least 10V.
- A protection diode must be placed near the power input to protect the FE912C04 module from power polarity inversion. Otherwise, the battery connector must be done in such a way to avoid polarity inversions when connecting the battery.
- The battery capacity must be at least 500 mAh to withstand the current peaks of 2A.

Note: DON'T USE any Ni-Cd, Ni-MH, and Pb battery types directly connected with FE912C04. Their use can lead to overvoltage on the FE912C04 and damage it. USE ONLY Li-Ion battery types.

5.3.2 Thermal Design Guidelines

The thermal design for the power supply heat sink should be done with the following specifications:

- Considering the very low current during Idle, especially if the Power Saving function is enabled, it is possible to consider from the thermal point of view that the device absorbs significant current only during an Active Call or Data session.
- For the heat generated by the FE912C04 module, consider it to be 2W.
- The FE912C04 supports different RATs: 4G, and 5G Sub-6.
- Based on the Radio Access Technology, the FE912C04 modem might exhibit high current consumption, thus proper thermal designs are essential to dissipate heat well.
- The FE912C04 is designed to conduct the heat flow from the module IC's towards the bottom of the PCB across GND metal layers.
- The generated heat is mostly conducted to the grounding plane under the FE912C04 module. The application board should be properly designed to dissipate this heat.
- The design of the application board must ensure that the area under the FE912C04 module is as large as possible. Make sure the FE912C04 is mounted on the large ground area of application board and provides plenty of ground vias to dissipate heat.

Note:

- Make PCB design to have the best connection of GND pads to large surfaces of copper.
- The average consumption during transmission depends on the power level at which the device is requested to transmit over the network. Therefore, the average current consumption varies significantly.
- The thermal design for the power supply should be made keeping an average consumption at maximum transmission level during calls of LTE/5G plus average consumption in GNSS Tracking mode.

5.3.3 Power Supply PCB Layout Guidelines

As seen in the guidelines for electrical design, the power supply shall have a low ESR capacitor on the output to cut the current peaks on the input, to protect the supply from spikes. The placement of this component is crucial for the correct working of the circuitry. A misplaced component can be useless or can even decrease the power supply performance.

- The Bypass low ESR capacitor must be placed close to the Telit FE912C04 power input pads or, in the case the power supply is a switching type it can be placed close to the inductor to cut the ripple, provided the PCB trace from the capacitor to the FE912C04 is wide enough to ensure a voltage drop less connection even during 2A current peak.
- The protection diode must be placed close to the input connector where the power source is drained.
- The PCB's traces from the input connector to the power regulator IC must be wide enough to ensure no voltage drops occurs when a 2 A current peak is absorbed.
- The PCB traces to the FE912C04 and the Bypass capacitor must be wide enough to ensure no significant voltage drops occurs. This is for the same reason as the previous point. Try to keep this trace as short as possible.
- To reduce the EMI due to switching, it is important to keep the mesh involved very small; therefore the input capacitor, the output diode (if not embodied in the IC) and the regulator, shall form a very small loop. This is done to reduce the radiated field (noise) at the switching frequency (100-500 kHz usually).
- A dedicated ground for the Switching regulator separated by the common ground plane is suggested.
- The placement of the power supply on the board should be done in such a way as to guarantee that the high current return paths in the ground plane are not overlapped with any noise-sensitive circuitry, such as the microphone amplifier/buffer or earphone amplifier.
- The power supply input cables should be kept separate from noise-sensitive lines such as microphone/earphone cables.
- The insertion of an EMI filter on VBATT pins is suggested in those designs where the antenna is placed close to the battery or supply lines. A ferrite bead-like Murata BLM18EG101TN1 or Taiyo Yuden P/N FBMH1608HM101 can be used for this purpose.

The below figure shows the recommended circuit:

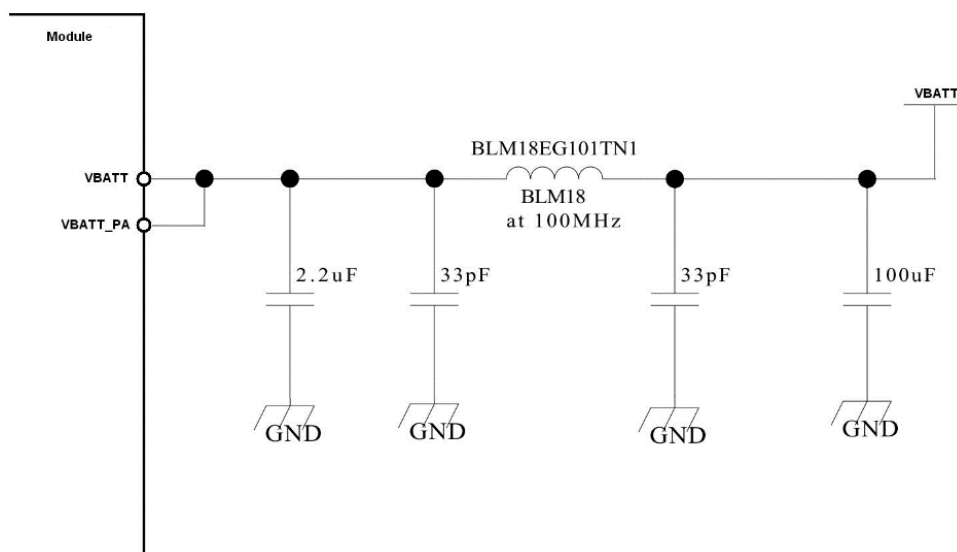


Figure 5: Recommended Circuit

5.3.4 Bypass Capacitor on Power Supplies

When a sudden voltage step to or cut from the power supplies is asserted, the steep transition causes some reactions such as overshoot and undershoot. This abrupt voltage transition can affect the device causing it to fail or to malfunction.

Bypass capacitors are needed to alleviate this behaviour. The behaviour may appear for different applications. Customers must pay special attention to this issue when they design their application board.

The length and width of the power lines must be considered carefully, and the capacitance of the capacitors must be selected accordingly.

The capacitor will also avoid power supplies ripple and the switching noise caused.

In particular, a suitable bypass capacitor must be mounted on the following lines on the application board:

- VBATT & VBATT_PA (Pad 162, 163, 165, 156, 157, 159, 160)
- USB_VBUS (Pad 182)

Recommended values are:

- 100uF for both VBATT and VBATT_RF together
- 4.7uF for USB_VBUS

However, customers should consider that the capacitance mainly depends on the conditions of their application board.

Generally, more capacitance is required when the power line is longer.

6 Digital Section

6.1 Logic Levels

Unless otherwise specified, all the interface circuits of the FE912C04 are 1.8V CMOS logic. Only few specific interfaces (such as USIM) are capable of dual voltage I/O.

The following tables show the logic level specifications used in the FE912C04 interface circuits.

6.1.1 1.8V Standard GPIOs

Table 12: Operating Range – Interface Levels (1.8V CMOS)

Pad	Parameter	Min	TYP	Max	Unit	Comment
V _{IH}	Input high level	VCC * 0.7	1.8	VCC + 0.3	[V]	
V _{IL}	Input low level	-0.3	-	0.3 * VCC	[V]	
V _{OH}	Output high level	VCC - 0.45	-	VCC	[V]	
V _{OL}	Output low level	0	-	0.45	[V]	
I _{IL}	Low-level input leakage current	-1	-	-	[uA]	No pull-up
I _{IH}	High-level input leakage current	-	-	10	[uA]	No pull-down
R _{PU}	Pull-up resistance	20	-	60	[kΩ]	
R _{PD}	Pull-down resistance	20	-	60	[kΩ]	

6.1.2 1.8V SIM Card Pads

Table 13: Operating Range – SIM Pads Working at 1.8V

Pad	Parameter	Min	TYP	Max	Unit	Comment
VCC	Supply Voltage	1.65	1.8	1.95	[V]	
V _{IH}	Input high level	VCC * 0.7	-	VCC + 0.3	[V]	
V _{IL}	Input low level	-0.3	-	VCC * 0.2	[V]	
V _{OH}	Output high level	0.8 * VCC	-	VCC	[V]	
V _{OL}	Output low level	0	-	0.4	[V]	
I _{IL}	Low-level input leakage current		-	1000	[uA]	No pull-up
I _{IH}	High-level input leakage current	-20	-	20	[uA]	No pull-down
R _{PU}	Pull-up resistance	10	-	100	[kΩ]	
R _{PD}	Pull-down resistance	10	-	100	[kΩ]	

6.1.3 2.95V SIM Card Pads

Table 14: Operating Range – For SIM Pads Operating at 2.95 V

Pad	Parameter	Min	TYP	Max	Unit	Comment
Vcc	Supply voltage	2.7	2.95	3.05	[V]	
V _{IH}	Input high level	0.7 * VCC	-	VCC + 0.3	[V]	
V _{IL}	Input low level	-0.3	-	0.2 * VCC	[V]	

Pad	Parameter	Min	TYP	Max	Unit	Comment
V _{OH}	Output high level	0.8 * VCC	-	VCC	[V]	
V _{OL}	Output low level	0		0.4	[V]	
I _{IL}	Low-level input leakage current		-	1000	[uA]	No pull-up
I _{IH}	High-level input leakage current	-20	-	20	[uA]	No pull-down
R _{PU}	Pull-up resistance	10	-	100	[kΩ]	
R _{PD}	Pull-down resistance	10	-	100	[kΩ]	

6.2 Power On

To turn on the FE912C04 module, the PWRKEY pad must be asserted low for more than 680ms and then released.

The maximum current that can be drained from the PWRKEY pad is 0.12 mA. This pin is pulled up internally; customers should expect to see VBATT at the output.

Figure 6 illustrates a simple circuit to power on the module using an inverted buffer output.

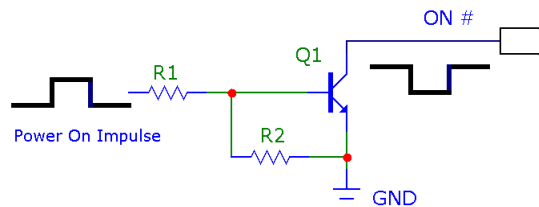


Figure 6: Power-on Circuit; illustrates a simple circuit to power on the module using an inverted buffer output.

Note:

- Do not use any pull up resistor on the PWRKEY line, it is internally pulled up. Using pull up resistor may bring to latch up problems on the FE912C04 power regulator and improper power on/off of the module. The line PWRKEY must be connected only in open collector or open drain configuration.
- To avoid back powering it is recommended to prevent any HIGH logic level signal from being applied to the digital pins of FE912C04 when the module is powered off or during an ON-OFF transition.

After turning on the FE912C04 module, a predefined internal boot sequence performs the HW and SW initialization of the module, which takes some time to complete. During this process, the FE912C04 is not accessible.

As shown in Figure 7, the FE912C04 becomes operational at least 50 seconds after PWRKEY is asserted.

Note:

During the Initialization state, AT commands are not available. The DTE host must wait for the Activation state prior to communicating with the FE912C04.

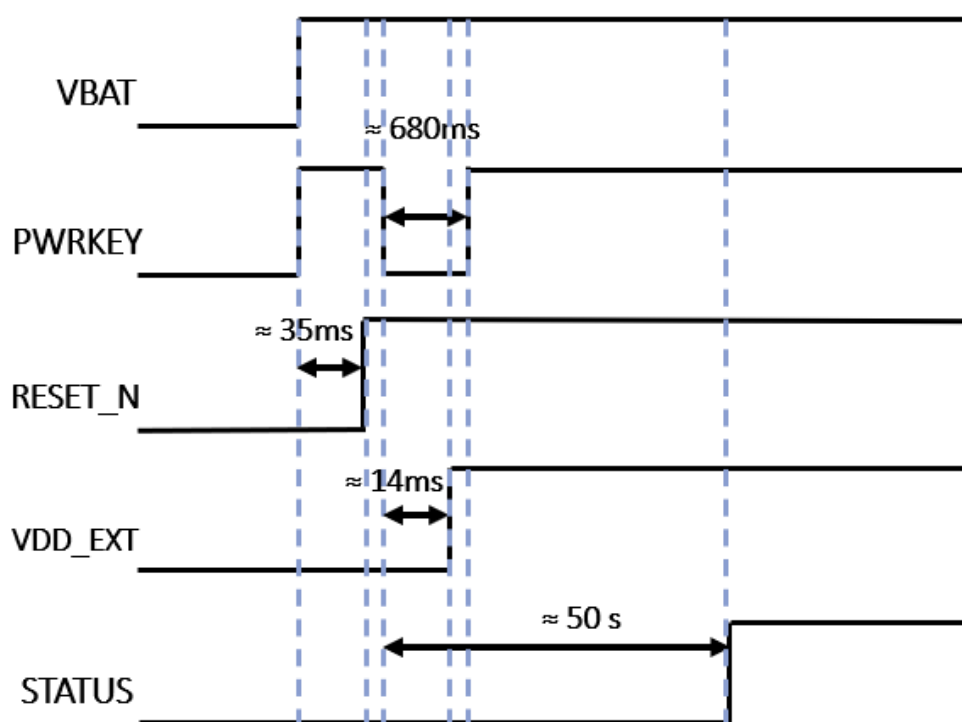


Figure 7: Power Up Timing

Note:

- To check whether the FE912C04 is fully operational, monitor the STATUS hardware line. When STATUS goes high, the module is fully operational and is ready to accept AT commands.
- During the SW initialization of the FE912C04, the SW configures all pads and interfaces in the desired status. When VDD_EXT goes high, this indicates that the initialization of all I/O pads is completed.
- Do not use any pull-up resistor on the PWRKEY line as it is pulled up internally. Using a pull-up resistor may cause latch-up problems on the FE912C04 power regulator and improper power on/off of the module. The PWRKEY line must be connected only in an open-collector configuration
- Active low signals are labeled with a name that ends with "#" or with "_N"
- To avoid back powering it is recommended to prevent any HIGH logic level signal from being applied to the digital pins of FE912C04 when the module is powered off or during an ON-OFF transition.

Table 15: Pin Description of PON_1

Pin	Signal	I/O	Function	Type	Comment
Indication Functions					
173	PON_1	I	Turn on the module automatically		Active high. If unused, pull it down to GND. Internally pulled up to 1.8V

6.3 Power Off

Turning off the device can be done in the following different ways:

- Shutdown by software using AT#SHDN software command.
- Hardware shutdown using PWRKEY pad.

When the device is shutdown by a software command or a hardware shutdown, it sends a detach disconnection request to the network, informing the network that the device will no longer be reachable.

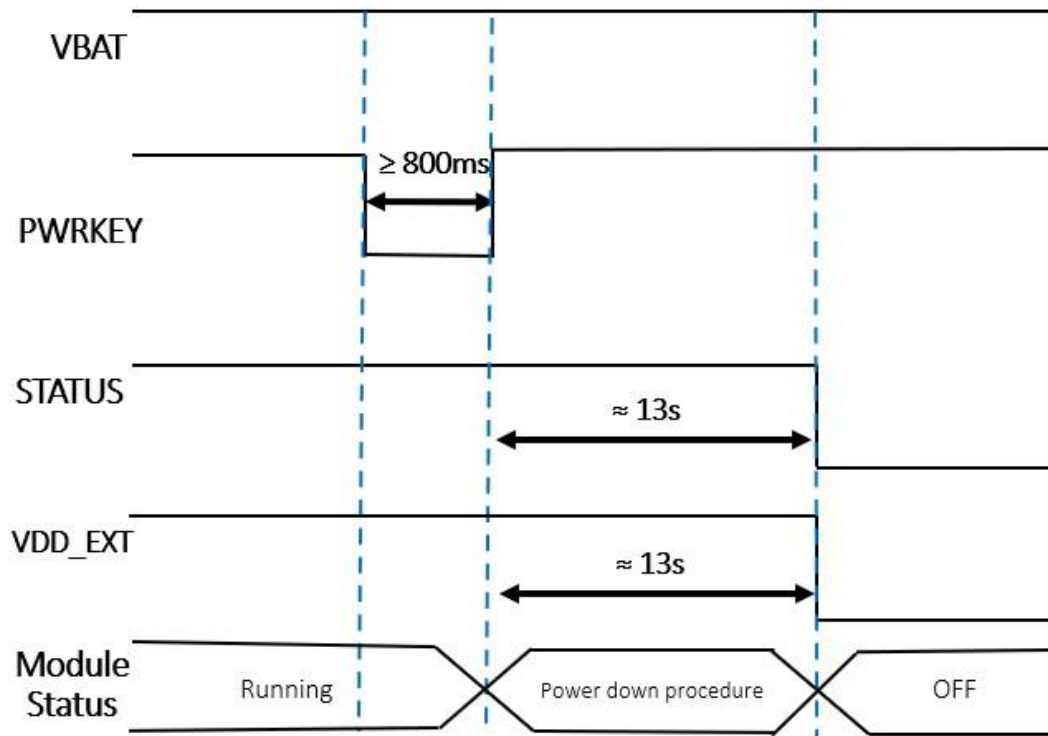


Figure 8: Power Down Timing

Note:

- To check if the device has turned off, monitor the VDD_EXT hardware line. When PWRMON goes low, this indicates that the device is turned off.
- To avoid a back-powering effect it is recommended to prevent any HIGH logic level signal from being applied to the digital pins of the FE912C04 when the module is powered off or during an ON-OFF transition.

Warning:

Not following the recommended shut-down procedures might damage the device and consequently void the warranty.

6.4 Shutdown by Software Command

The FE912C04 module can be shutdown via a software command.

When a shutdown command is sent, the FE912C04 enters the Finalization state and at the end of the finalization process shuts down PWRMON.

The duration of the Finalization state may vary depending on the current situation of the module, so it is not possible to define a value.

Usually, it will take more than 13 seconds from sending a shutdown command until a complete shutdown is achieved. The DTE host should monitor the PWRMON status to observe the actual power-off.

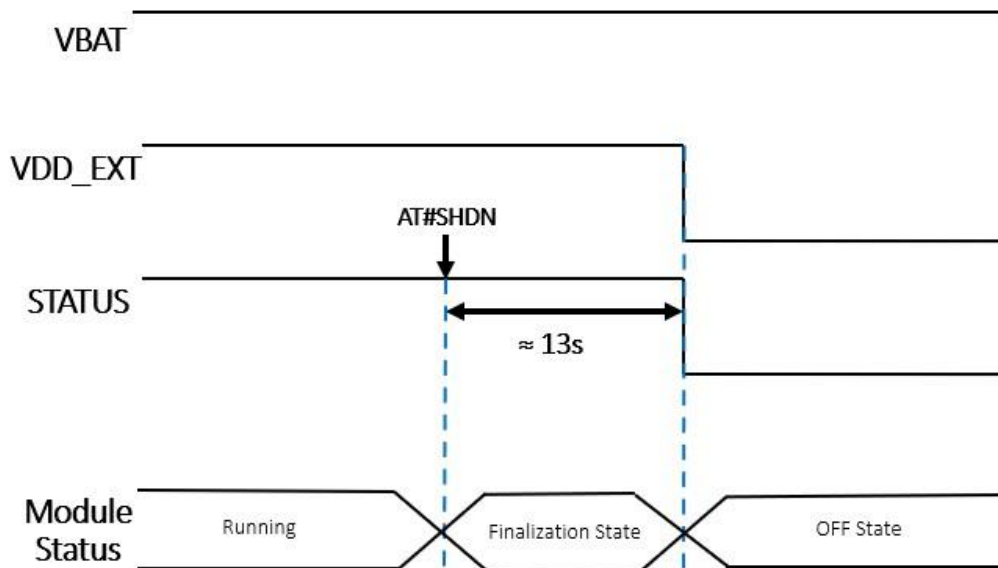


Figure 9: Shutdown by Software Command

6.5 RESET_N

The module can be reset by driving RESET_N low for at 800ms~ 1s and then releasing it. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

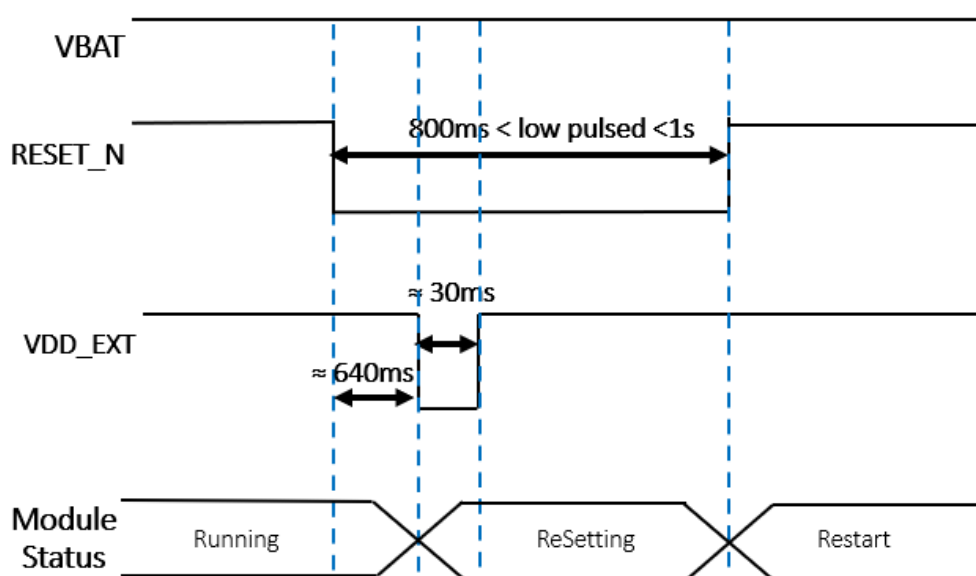


Figure 10: Reset Timing

6.6 Communication Ports

6.6.1 USB

The FE912C04 module includes a Universal Serial Bus (USB) transceiver, which operates at USB high-speed (480Mbps/sec). It can also operate with USB full-speed hosts (12Mbps/sec).

It is compliant with the USB 2.0 specification and can be used for control and data transfers, as well as for diagnostic monitoring and firmware update.

The USB port is typically the main interface between the FE912C04 module and OEM hardware.

Note: The USB_D+ and USB_D- signals have a clock rate of 480 MHz. The signal traces must be routed carefully. Minimize trace lengths, number of vias, and capacitive loading. The impedance value should be as close as possible to 90 Ohms differential.

Table 16: USB Interface Signals

Signal	Pad No.	Usage
USB_VBUS	182	Power and cable detection for the internal USB transceiver. Acceptable input voltage range 1.3 ~ 5.5 V
USB_D-	184	Minus (-) line of the differential, bi-directional USB signal to/from the peripheral device
USB_D+	183	Plus (+) line of the differential, bi-directional USB signal to/from the peripheral device
USB_ID	179	USB ID detect
USB_BOOT	30	Force the module into emergency download mode

Note: USB_VBUS input power is used internally to detect the USB port and start the enumeration process. It is a power supply pin with a maximum consumption of 5 mA. Do not use pull up or a voltage divider for sourcing this supply.

Note: Even if USB communication is not used, it is still highly recommended to place an optional USB connector on the application board. At least USB signal test points are required as USB physical communication is needed in the case of SW update.

6.6.1.1 USB Layout Guidelines

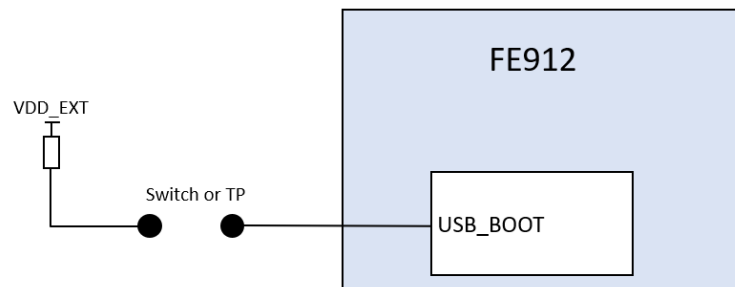
- If third-party components are required for signal improvement, place them closer to the USB connector.
- There are relatively fast edge rate, so must be routed away from sensitive circuits and signals (RF, audio, and XO).
- Route the RF signals at a 2.4 GHz frequency with the highest isolation possible from USB traces.

- Keep isolation between the D+ and D- to avoid crosstalk.
- USB 2.0 signal, maximum trace length should be less than 200 mm.
- Route the USB signal traces in inner layer of the PCB and surround the traces with ground on the same layer and with ground planes on adjacent layers above and below.

Table 17: USB requirement

Type of guidance	Guideline	Requirement
General	Data rate	480 Mbps
	Impedance	90 ohms differential
	Bus length	Max 200 mm
Length matching	Intra-pair length match	2 mm
Spacing	Lane to other signals	3 x line width

6.6.1.2 USB_BOOT


Figure 11: USB_BOOT Reference Circuit

Note: If the USB_BOOT pin goes high before turning on the module, FE912C04 will be entering emergency download mode when powered on. In this mode, FE912C04 supports firmware upgrades over the USB 2.0 interface.

6.6.2 UART

The serial port is typically a secondary interface between the FE912C04 module and OEM hardware. The following serial ports are available on the module:

- UART for GNSS supports 115200 bps baud rate. It supports RTS and CTS hardware flow control.
- COEX UART supports 115200 bps baud rate. This interface is used for WWAN/WLAN coexistence.
- Debug UART supports 115200 bps baud rate. (Linux console and log output).

Table 18: UART Interface

Pin	Signal	I/O	Function	Type	Comment
Debug UART					
89	DBG_UART_TX	O	Debug UART transmit	1.8V	
88	DBG_UART_RX	I	Debug UART receive	1.8V	

Pin	Signal	I/O	Function	Type	Comment
COEX UART					
29	COEX_UART_TX	O	COEX UART transmit	1.8V	
32	COEX_UART_RX	I	COEX UART receive	1.8V	
GNSS Section					
36	GNSS_UART_TXD	O	UART transmit	1.8V	UART for GNSS
39	GNSS_UART_RXD	I	UART receive	1.8V	UART for GNSS
37	GNSS_UART_RTS	I	UART Request to Send	1.8V	UART for GNSS
34	GNSS_UART_CTS	O	UART Clear to Send	1.8V	UART for GNSS

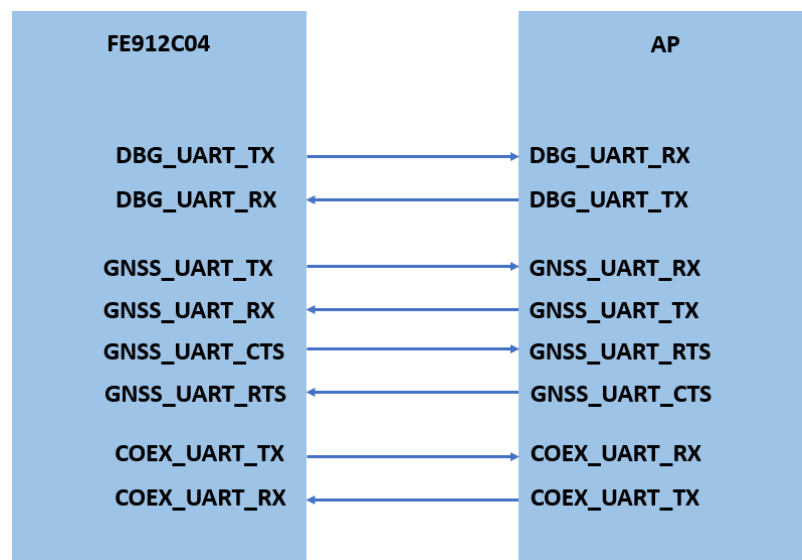


Figure 12: UART Interface Connection

Note: The Debug UART is used as the SW main debug console. It is required to place test points on this interface even if not used.

Note: For minimum implementations, only the TXD and RXD lines need be connected. The other lines can be left open provided a software flow control is implemented.

FE912C04 provides 1.8 V UART interfaces. Use a level shifter if the application is equipped with a 3.3 V UART interface.

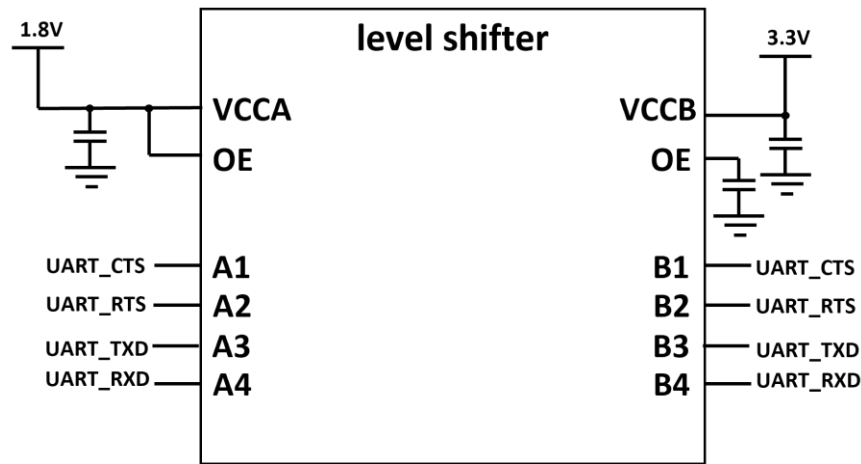


Figure 13: Level Shifter Schematic Example for UART

6.6.2.1 RS232 Level Translation

To interface the FE912C04 with a PC COM port or an RS232 (EIA/TIA-232) application, a level translator is required. This level translator must perform the following actions:

- Invert the electrical signal in both directions.
- Change the level from 0/1.8 V to ± 15 V

The RS232 UART 16450, 16550, 16650 and 16750 chipsets accept signals with lower levels on the RS232 side (EIA/TIA-562), allowing a lower voltage-multiplying ratio on the level translator. Note that the negative signal voltage must be less than 0 V and hence some sort of level translation is always required.

The easiest way to translate the levels and invert the signal is by using a single chip-level translator. There are a multitude of them, differing in the number of drivers and receivers and in the levels (make sure to get a true RS232 level translator, not a RS485 or other standards).

By convention, the driver is the level translator from the 0 – 1.8 V UART to the RS232 level. The receiver is the translator from the RS232 level to 0 – 1.8 V UART. To translate the whole set of control lines of the UART, the following is required:

- 2 drivers
- 2 receivers

Warning: The digital input lines, operating at 1.8 V CMOS levels, have an absolute maximum input voltage of 2.0 V. The level translator IC outputs on the module side (i.e. FE912 inputs) will cause damage to the module inputs if the level translator is powered with +3.8 V power. So, the level translator IC must be powered by a dedicated +1.8 V power supply.

As an example, RS232 level adaption circuitry could use a MAXIM transceiver (MAX218). In this case, the chipset is capable of translating directly from 1.8 V to the RS232 levels (example on 4 signals only).

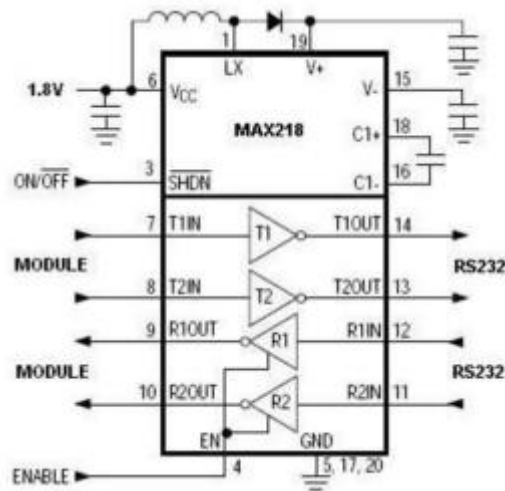


Figure 14: RS232 Level Adaption Circuitry Example

Note: In this case, the length of the lines on the application must be taken into account to avoid problems in the case of high-speed rates on RS232.

The RS232 serial port lines are usually connected to a DB9 connector as shown in the below. Signal names and directions are named and defined from the DTE point of view.

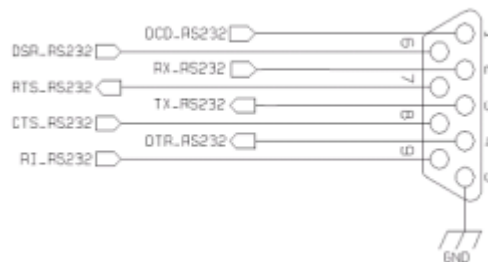


Figure 15: RS232 Serial Port Lines Connection Layout

6.7 Indication Interfaces

Table 19: Indication Signals

Pin	Signal	I/O	Function	Type	Comment
Indication Functions					
23	SLEEP_IND	O	Indicate module sleep mode	1.8 V	
24	STATUS	O	indicate module operaton status	1.8 V	
25	NET_MODE	O	Indicate network registration	1.8 V	
27	NET_STATUS	O	Indicate network activity	1.8 V	

6.7.1 STATUS

The STATUS pin is an output pin, indicating the FE912C04's operation status. It will output a high level when the module is powered on successfully.

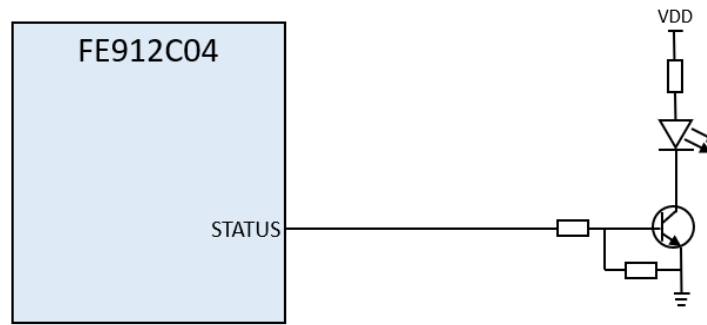


Figure 16: STATUS Circuit Example

6.7.2 SLEEP_IND

The SLEEP_IND pin is an output pin, indicating the FE912C04's sleep mode. It will output a high level when the module enters sleep mode.

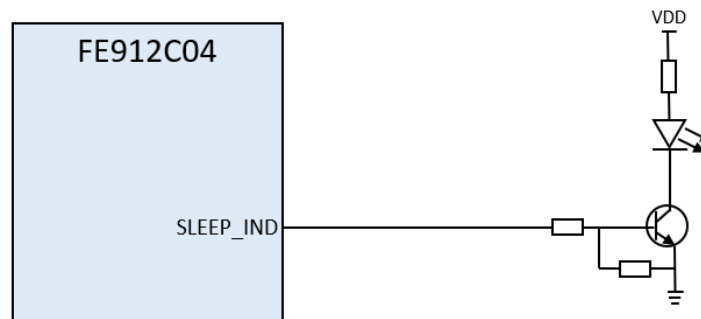


Figure 17: SLEEP_IND Circuit Example

6.7.3 Network Status Indication

The FE910C04 provides two network indication pins: NET_MODE and NET_STATUS which can drive network status indication LEDs. The following tables logic level changes of NET_MODE and NET_STATUS in different network status.

Table 20: Working State of the Network Status Indication

Pin Name	STATUS	Description
NET_MODE	Always High	Registered on LTE network
	Always Low	Others
NET_STATUS	Flicker slowly (200 ms High / 1800 ms Low)	Network searching
	Flicker slowly (1800 ms High / 200 ms Low)	Idle
	Flicker quickly (125 ms High / 125 ms Low)	Data transfer is on-going

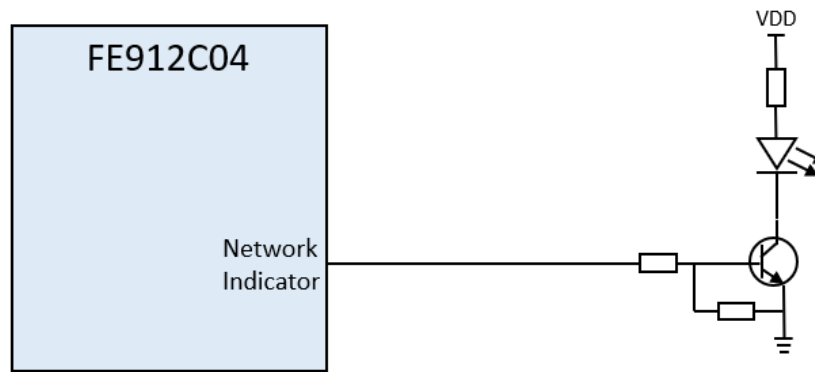


Figure 18: Network Status Indication Circuit Example

6.8 W_DISABLE#

The FE912C04 provides W_DISABLE# to enable or disable airplane mode through hardware operation. W_DISABLE# is pulled up by default and driving it low will set the module to airplane mode.

Table 21: W_DISABLE# Pad

PAD	Signal	I/O	Function	Type	Comment
90	W_DISABLE#	I	Airplane mode	1.8 V	Active Low (internal 4.7 K PU)

The RF function can also be enabled or disabled through software AT commands.

Table 22: RF Function Status

W_DISABLE#	AT Commands	RF Function Status
High	AT+CFUN=1	Enabled
High	AT+CFUN=0	Disabled
	AT+CFUN=4	
Low	AT+CFUN=0	Disabled
	AT+CFUN=1	
	AT+CFUN=4	

6.9 DPR

The FE912C04 provides a DPR (Dynamic Power Reduction) pin for SAR (Specific Absorption Rate) detection. The signal is sent by a host system proximity sensor to the module to provide an input trigger, which will reduce the output power in radio transmission.

Table 23: DPR Pad

PAD	Signal	I/O	Function	Type	Comment
15	DPR	I	Dynamic Power Reduction	1.8 V	Active Low

Table 24: DPR Function

DPR	Description
High / Floating	Max transmitting power will NOT be backed off
Low	Max transmitting power will be backed off

6.10 External SIM Holder

The FE912C04 supports both Class B (2.95 V) and Class C (1.8 V), and a dual-SIM single-standby function is supported.

Table 25: USIM 1 and 2 Interfaces

PAD	Signal	I/O	Function	Type	Comment
SIM Card Interface 1					
141	USIM1_CLK	O	SIM 1 Clock	1.8 / 2.95V	
142	USIM1_RST	O	SIM 1 Reset	1.8 / 2.95V	
138	USIM1_DATA	I/O	SIM 1 Data	1.8 / 2.95V	
143	USIM1_DET	I	SIM 1 Detect	1.8V	
139	USIM1_VDD	-	SIM 1 Power supply	1.8 / 2.95V	
SIM Card Interface 2					
147	USIM2_CLK	O	SIM 2 Clock	1.8 / 2.95V	
145	USIM2_RST	O	SIM 2 Reset	1.8 / 2.95V	
144	USIM2_DATA	I/O	SIM 2 Data	1.8 / 2.95V	
146	USIM2_DET	I	SIM 2 Detect	1.8V	
148	USIM2_VDD	-	SIM 2 Power supply	1.8 / 2.95V	

Note: By default, the USIMx_DET pin is set to active low (inserted). As a result, when the USIMx_DET input is changed from logic 1 to logic 0, the FE912C04 will detect USIM card insertion. If it is required to change the USIM_DET pin to active high (inserted), please refer to AT#SIMINCFG of FE912C04 AT commands reference guide.

To change the default value stored within the firmware without sending AT commands at each power-up, contact Telit Cinterion technical support.

6.10.1 SIM Schematic Example

This section presents the recommended schematics for the design of SIM interfaces on the application boards. The FE912C04 supports two external SIM interfaces.

The below figure illustrates how to design the application side and what values to assign to the components.

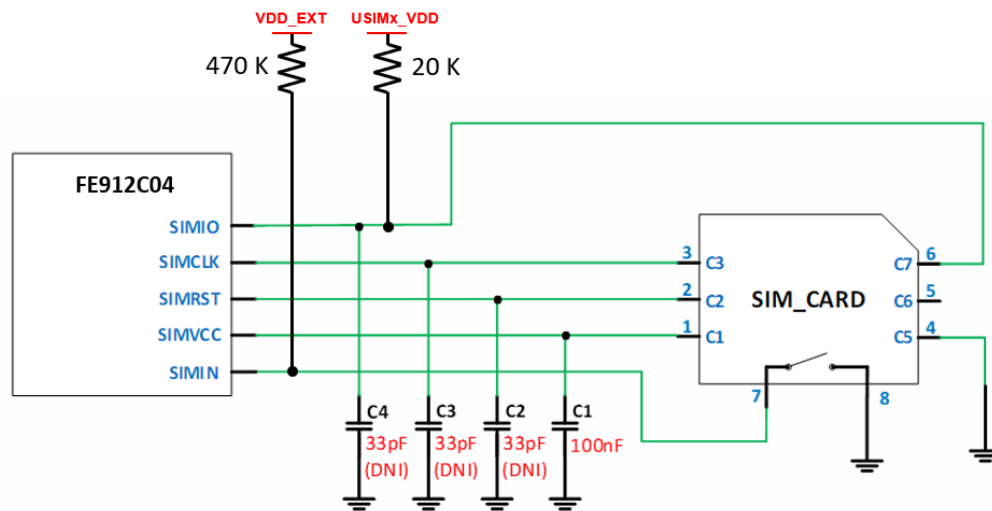


Figure 19: SIM Schematic

To enhance the reliability and availability of the USIM card in applications, please follow the criteria below in USIM circuit design.

- Keep the USIM card connector as close as possible to the module. Keep the trace length as short as possible, 200 mm at most.
- Keep USIM card signal traces away from RF and VPH_PWR traces.
- To avoid crosstalk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with ground surrounded.
- For better ESD protection, it is recommended to add a TVS array with a parasitic capacitance not exceeding 50 pF. The 22-ohm resistors should be added in series between the module and the USIM card connector to suppress EMI spurious transmission and enhance ESD protection. The 33 pF capacitors are used to filter out RF interference.
- The pull-up resistor on the USIM_DATA trace improves anti-jamming capability and should be placed close to the USIM card connector.
- The USIM card hot-plug function is supported by default.

6.10.2 ADC Converter

The FE912C04 module provides one on-board Analog to Digital converters. Each ADC reads the voltage level applied to the relevant pin, the accuracy is about 20mv@1.8v.

Table 26: ADC

Pin	Signal	I/O	Function	Type	Comment
ADC					
18	ADC0	I	Analog Digital Converter Input	Analog Input	

Table 27: ADC parameters

Item	Min	Type	Max	Units
Input voltage range	1.828	1.875	1.922	Volt
Accuracy	-20	+/-10	20	mV
Input Resistance	10	-	-	Mohm
Sample Clock	-	4.8	-	MHz

6.10.2.1 Using ADC Converter

AT command is available to use the ADC function.

The command is AT#ADC? The read value is expressed in mV.

Please refer to FE912C04 AT command user guide for the full description of this function.



7 RF Section

7.1 Bands Variants

Table below summarizes all region variants within the FE912C04 family, showing the band sets supported in each variant.

Different bands combinations are available:

Table 28: Bands Variant

Region Variant	LTE FDD	LTE TDD	NR FDD	NR TDD	GNSS
FE912C04-NA	B2, B4, B5, B7, B12, B13, B14, B17, B25, B26, B30, B66, B71	B41, B48	n2, n5, n7, n12, n13, n14, n25, n26, n66, n71	n41, n48, n77, n78	GNSS L1/L5
FE912C04-RW	B1, B2, B3, B4, B5, B7, B8, B20, B28	B40, B41	n1, n3, n5, n7, n8, n20, n28	n40, n41, n77, n78	GNSS L1/L5

7.2 Conducted Transmit Output Power

TX power follows the measurement conditions and specifications defined in 3GPP.

Table 29: TX Output Power

Band	Power class	RF Power (dBm) Nominal ¹⁾
5G NR Sub-6 n1, n2, n3, n5, n7, n8, n12, n13, n14, n20, n25, n26, n28, n40, n41, n48 ²⁾ , n66, n71, n77, n78	3 (0.2W)	23.5
LTE All Bands B1, B2, B3, B4, B5, B7, B8, B12, B13, B14, B17, B20, B25, B26, B28, B30 ³⁾ , B40, B41, B48 ²⁾ , B66, B71	3 (0.2W)	23.5
LTE B41 Supports Power Class 2	2 (0.4W)	26

Note: ¹⁾ RF Power Nominal : Max output power tolerance according to 3GPP TS 38.521-1, 3GPP TS 36.521-1 and 3GPP TS 34.121-1 or better

Note: ²⁾ LTE B48 / NR n48 : PC 3 Nominal RF Power 22dBm
These bands may show lower power due to Country-type approvals constraints

Note: ³⁾ LTE B30 : PC 3 Nominal RF Power 22dBm
These bands may show lower power due to Country-type approvals constraints

7.3 Conducted Receiver Sensitivity

Below the 3GPP measurement conditions used to define the RX sensitivity:

Table 30: RX Sensitivity Measurement Setup

Mode	Value
4G LTE	Throughput >95% 10MHz, According to 3GPP 36.521-1
5G NR Sub-6	Throughput >95% 10MHz/20MHz, According to 3GPP 38.521-1

Table 31: LTE Typical sensitivity levels of FE912C04-NA

E-UTRA Band	Typical Conducted Rx Sensitivity (dBm) *				
	BW(MHz)	PRx	DRx	Combined	3GPP(2RX)
LTE FDD B2	10	-100	-99.5	-103	-95
LTE FDD B4	10	-100.5	-99.5	-103.5	-97
LTE FDD B5	10	-99.5	-101	-103.5	-95
LTE FDD B7	10	-97.5	-99.5	-102	-95
LTE FDD B12	10	-99.5	-101	-103.5	-94
LTE FDD B13	10	-100.5	-101.5	-104	-94
LTE FDD B14	10	-101	-101	-104	-94
LTE FDD B17	10	-99.5	-101	-103.5	-94
LTE FDD B25	10	-100	-99.5	-103.5	-93.5
LTE FDD B26	10	-99.5	-101	-103.5	-94.5
LTE FDD B30	10	-98.5	-99	-102	-96
LTE TDD B41	10	-97	-97.5	-100	-95
LTE FDD B48	10	-97.5	-98.5	-101	-96
LTE TDD B66	10	-100.5	-99.5	-103	-96.5
LTE FDD B71	10	-99	-100.5	-103	-94.2

Table 32: NR Typical sensitivity levels of FE912C04-NA

NR Band	Typical Conducted Rx Sensitivity (dBm) *					
	BW(MHz)	SCS(kHz)	PRx	DRx	Combined	3GPP(2RX)
NR FDD n2	10	15	-100	-100	-103	-94.8
NR FDD n5	10	15	-99.5	-101	-103.5	-94.8
NR FDD n7	10	15	-99	-100	-102.5	-94.8
NR FDD n12	10	15	-100	-100.5	-103.5	-93.8
NR FDD n13	10	15	-101	-101.5	-104	-93.8
NR FDD n14	10	15	-101	-101	-104	-93.8
NR FDD n25	10	15	-100	-100	-103	-93.3
NR FDD n26	10	15	-100	-101	-103	-94.5
NR TDD n41	20	30	-94.5	-95	-97.5	-91.9
NR TDD n48	20	30	-96	-98.5	-100	-92.9
NR FDD n66	10	15	-100.5	-100	-103	-96.3
NR FDD n71	10	15	-99.5	-101	-103	-94.0
NR TDD n77	20	30	-96.5	-98	-100	-92.4
NR TDD n78	20	30	-96.5	-98.5	-100.5	-92.9

Table 33: LTE Typical sensitivity levels of FE912C04-RW

Mode	Typical Conducted Rx Sensitivity (dBm) *				
	BW(MHz)	PRx	DRx	Combined	3GPP(2RX)

Mode	Typical Conducted Rx Sensitivity (dBm) *				
LTE FDD B1	10	-98.5	-100	-102.5	-97
LTE FDD B2	10	-99	-100.5	-103	-95
LTE FDD B3	10	-98	-100	-102.5	-94
LTE FDD B4	10	-99.5	-100	-103	-97
LTE FDD B5	10	-99.5	-101	-103.5	-95
LTE FDD B7	10	-97	-99.5	-101.5	-95
LTE FDD B8	10	-99.5	-101.5	-103.5	-94
LTE FDD B20	10	-100	-101.5	-104	-94
LTE FDD B28	10	-100	-102	-104.5	-95.5
LTE TDD B40	10	-98.5	-98.5	-102	-97
LTE TDD B41	10	-97	-97.5	-100.5	-95

Table 34: NR Typical sensitivity levels of FE912C04-RW

NR Band	Typical Conducted Rx Sensitivity (dBm) *					
	BW(MHz)	SCS(kHz)	PRx	DRx	Combined	3GPP(2RX)
NR FDD n1	10	15	-98.5	-100	-102.5	-96.8
NR FDD n3	10	15	-98.5	-100	-102	-93.8
NR FDD n5	10	15	-100	-101.5	-104	-94.8
NR FDD n7	10	15	-98.5	-99.5	-102	-94.8
NR FDD n8	10	15	-100	-101.5	-103.5	-93.8
NR FDD n20	10	15	-100	-102	-104	-93.8
NR FDD n28	10	15	-101	-102	-104	-95.5
NR TDD n40	20	30	-96	-96	-99	-93.9
NR TDD n41	20	30	-94.5	-95	-97.5	-91.9
NR TDD n77	20	30	-97	-97.5	-100	-92.4
NR TDD n78	20	30	-96.5	-98	-100	-92.9

Note: The sensitivity level may present a deviation of approximately +/- 2dB depending on model, device and channel; the level shown is the typical value.

7.4 Antenna Requirements

The antenna connection and board layout design are the most important aspect of the full product design as they strongly affect the general performance of the product, so read carefully and follow the requirements and the guidelines for a proper design.

The antenna and antenna transmission line on PCB for a Telit FE912C04 device shall fulfil the following requirements:

Table 35: Antenna and Antenna Transmission Line on PCB

Item	Value
Frequency range	Depending on the frequency band(s) provided by the network operator, the customer shall use the most suitable antenna for that/those band(s)
Bandwidth	See Section 13 Reference Table of RF Bands Characteristics
Impedance	50 ohm
Input power	Power Class 3: > 23dBm Average power Power Class 2: > 26dBm Average power
VSWR absolute max	≤ 10:1 (limit to avoid permanent damage)
VSWR recommended	≤ 2:1 (limit to fulfil all regulatory requirements)

7.4.1 PCB Design Guidelines

When using the FE912C04, since there's no antenna connector on the module, the antenna must be connected to the FE912C04 antenna pad (98, 107, 113, 119, 125, 133, 66) by means of a transmission line implemented on the PCB.

This transmission line shall fulfil the following requirements:

Table 36: FE912C04 Antenna Pad Requirements

Item	Value
Characteristic Impedance	50 ohm (+-10%)
Max cable insertion loss	2 dB
Coupling	Coupling with other signals shall be avoided
Ground Plane	The cold End (Ground Plane) of the antenna shall be equipotential to the FE912C04 ground pins

The transmission line should be designed according to the following guidelines:

- Make sure that the transmission line's characteristic impedance is 50 ohm.
- Keep the line on the PCB as short as possible, since the antenna line loss shall be less than about 2 dB.
- The geometry of the line must have uniform characteristics, constant cross-section, and avoid meanders and abrupt curves.
- Any kind of suitable geometry/structure (Microstrip, Stripline, Coplanar, Grounded Coplanar Waveguide) can be used to implement the printed transmission line relating to the antenna.
- If a Ground plane is required in the geometry of the line, this plane must be continuous and sufficiently extended, so that the geometry can be as similar as possible to the related canonical model.
- Keep, if possible, at least one layer of the PCB used only for the Ground plane; If possible, use this layer as a reference Ground plane for the transmission line;
- It is advisable to surround (on both sides) the PCB transmission line with Ground, avoiding that other signal tracks face directly the antenna line track.
- Avoid crossing any un-shielded transmission line footprint with other signal tracks on different layers.
- The ground surrounding the antenna line on the PCB must be tightly connected to the main Ground Plane through holes (at least once every 2mm), placed near the edges of the ground facing the line track.
- Place EM noisy devices as far as possible from the FE912C04 antenna line.
- Keep the antenna line far away from the FE912C04 power supply lines.
- If EM noisy devices (such as fast switching ICs, LCD and so on) are present on the PCB hosting the FE912C04, take care of the shielding of the antenna line by burying it in an inner layer of PCB and surrounding it with the Ground planes, or shield it with a metal frame cover.
- If EM noisy devices are not present around the line, the use of geometries such as Microstrip or Grounded Coplanar Waveguide is preferable, since they typically ensure less attenuation if compared to a Stripline of the same length.

The following image shows the suggested layout for the Antenna pad connection:

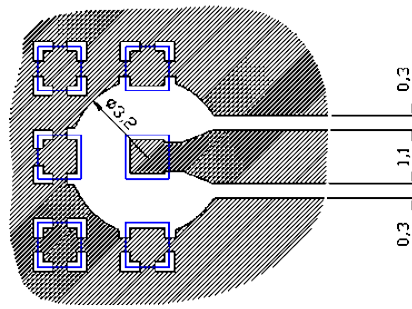


Figure 20: Layout for the Antenna Pad Connection

7.4.2 PCB Guidelines in Case of FCC Certification

If FCC certification is required for an application using FE912C04, according to FCC KDB 996369 for modular approval requirements, the transmission line must be similar to the one implemented on the FE912C04 interface board and described in the following chapter.

7.4.2.1 Transmission Line Design

When designing the FE912C04 interface board, the placement of components was chosen properly, to keep the length of the line as short as possible, thus leading to the lowest possible power losses. A Grounded Coplanar Waveguide (G-CPW) line has been chosen since this kind of transmission line ensures good impedance control and can be implemented in an outer PCB layer as needed in this case. An SMA female connector has been used to feed the line.

The interface board is made on an FR4, 4-layer PCB. The substrate material is characterized by relative permittivity $\epsilon_r = 4.6 \pm 0.4$ @ 1 GHz, $\tan \delta = 0.019$ to 0.026 @ 1 GHz.

A characteristic impedance of nearly 50 ohm is achieved using a track width = 1.1 mm, and clearance from a coplanar ground plane = 0.3 mm on each side. The line uses the reference ground plane on layer 3, while copper is removed from layer 2 below the line. The height of the trace above the ground plane is 1.335 mm. The calculated characteristic impedance is 51.6 ohm, and the estimated line loss is less than 0.1 dB.

The line geometry is shown below:

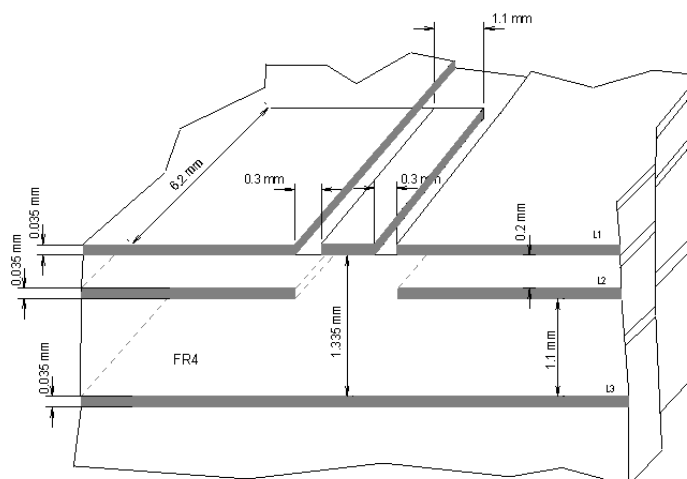


Figure 21: Line Geometry

7.4.2.2 Transmission Line Measurements

An E5071C Keysight (Full-2-port calibration) was used in this measurement session. A calibrated coaxial cable was soldered to the pad corresponding to the RF output; an SMA connector was soldered to the board to characterize the losses of the transmission line including the connector itself. During Return Loss/impedance measurements, the transmission line has been terminated to a 50-ohm load.

The return Loss plot of the line under test is shown below:

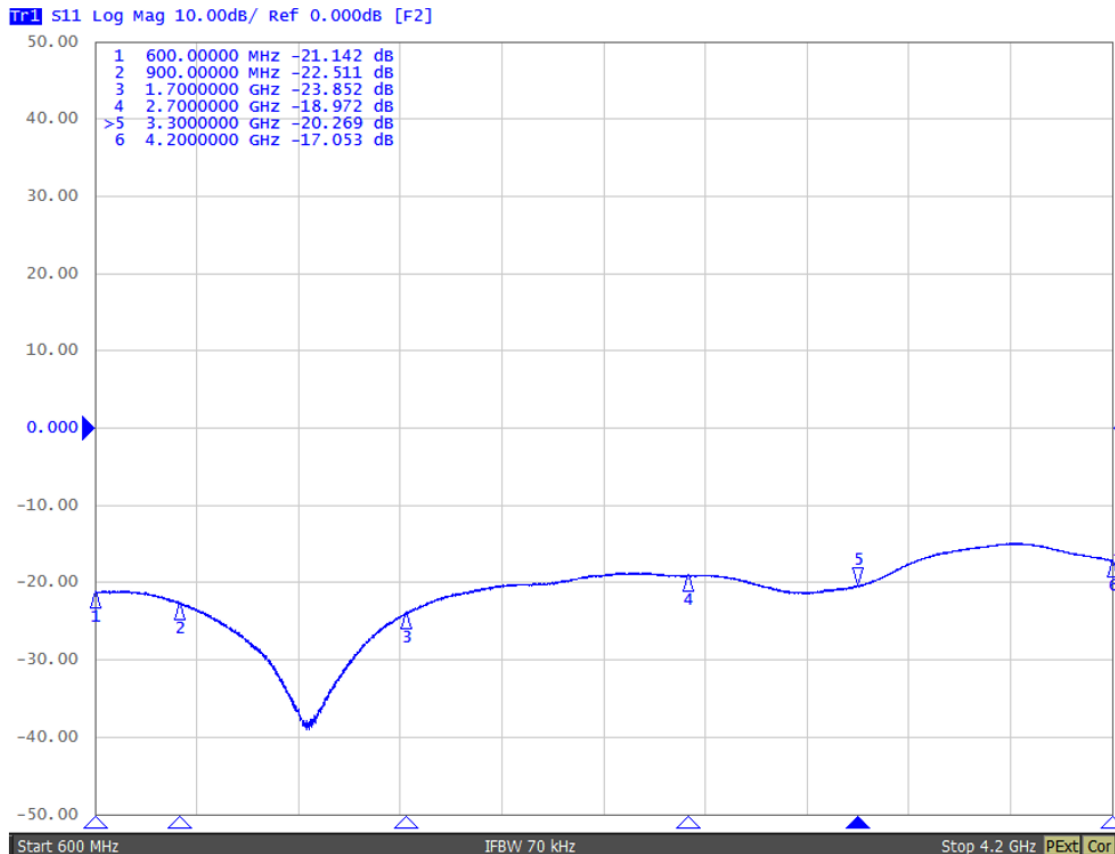


Figure 22: Return Loss plot of the line under test

The input impedance of the line (in Smith Chart format, once the line has been terminated to a 50-ohm load) is shown in the following figure:

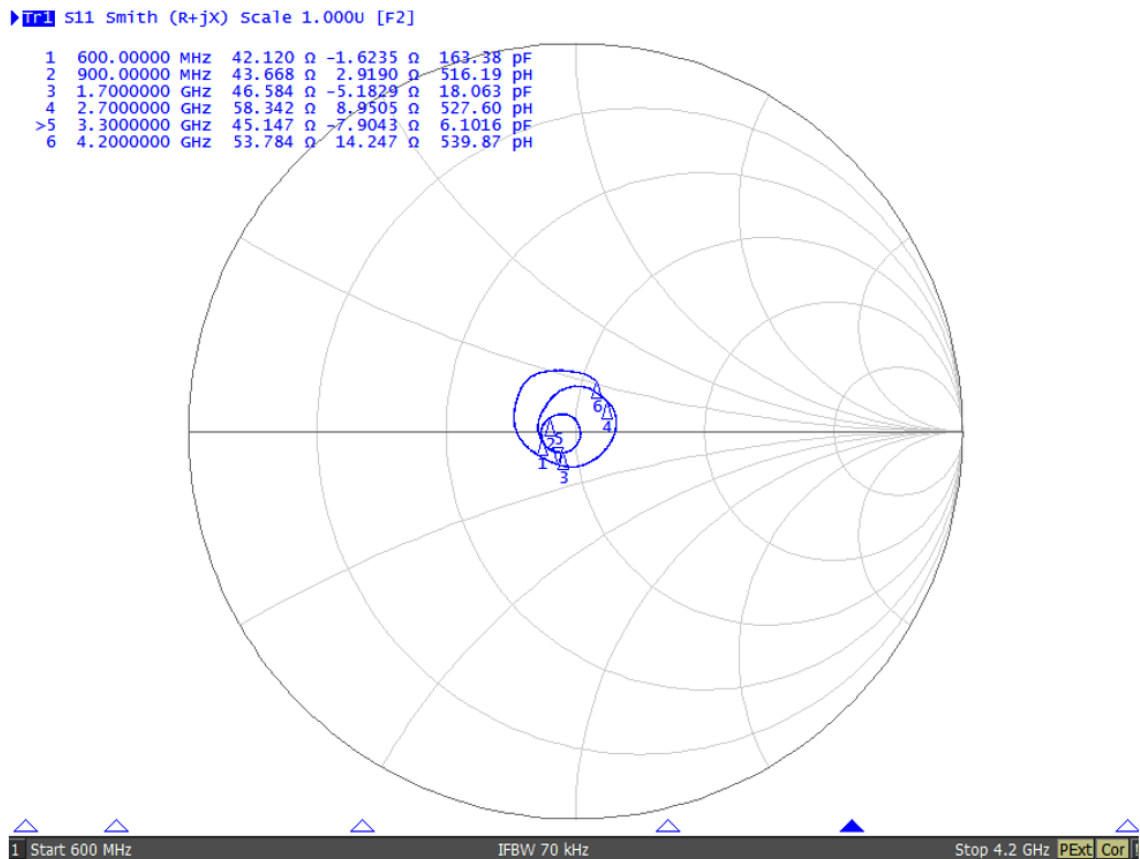


Figure 23: Line input impedance

Insertion Loss of G-CPW line plus SMA connector is shown below:

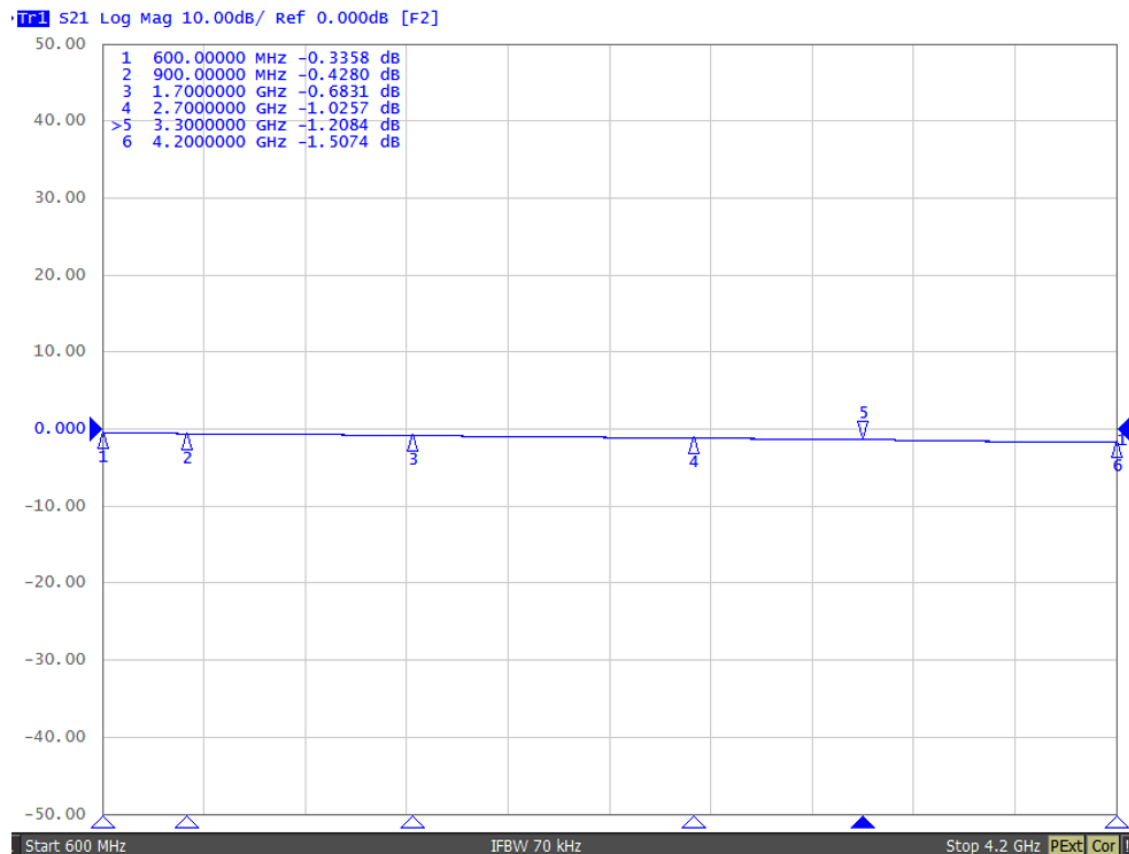


Figure 24: Insertion Loss of G-CPW line plus SMA connector

7.4.2.3 Antenna Installation Guidelines

- Install the antenna in a place covered by the LTE signal with 5G FR1 RedCap support.
- The Antenna must not be installed inside metal cases.
- The Antenna must be installed according to the Antenna manufacturer's instructions.
- The Antenna integration should optimize the Radiation Efficiency. Efficiency values > 50% are recommended on all frequency bands.
- The Antenna integration should not perturb the radiation pattern described in the documentation of the Antenna manufacturer.
- It is preferable to get an omnidirectional radiation pattern.
- The Antenna Gain must not exceed the values indicated in regulatory requirements, where applicable, to meet the related EIRP limitations. The Typical antenna Gain in most M2M applications does not exceed 2dBi.
- If the device antenna is located farther than 20cm from the human body and there are no co-located transmitters, then the Telit FCC/IC approvals can be re-used by the end product.
- If the device antenna is located closer than 20cm from the human body or there are co-located transmitters, then additional FCC/IC testing may be required for the end product (Telit FCC/IC approvals cannot be reused).

8 GNSS Section

The FE912C04 module includes a state-of-art receiver that can simultaneously search and track satellite signals from multiple satellite constellations. This multi-GNSS receiver uses GPS, GLONASS, BeiDou, and Galileo.

Table 37: GNSS supported bands

Product	Constellations
FE912C04-NA FE912C04-RW	L1/L5

8.1 GNSS Characteristics

The table below specifies the GNSS characteristics and expected performance. The values are related to typical environments and conditions.

Table 38: GNSS Characteristics

Parameters		Typical Measurement	Notes
Sensitivity	Tracking Sensitivity	-162 dBm	Standalone or MS Based
	Acquisition	-158 dBm	
	Cold Start	-147 dBm	
TTFF	Hot	1 sec	Open Sky, mean TTFF
	Warm	21 sec	Open Sky, mean TTFF
	Cold	26 sec	Open Sky, mean TTFF
Supported update rate		10Hz	
CEP-50		<2m	Open Sky conditions. Standalone

8.1.1 GNSS Signals PIN-OUT

Following is the list of involved Pins:

Table 39: GNSS Signals PIN-OUT

PAD	Signal	I/O	Function	Type	Comment
GNSS Section					
66	ANT_GNSS	I	GNSS antenna (50 Ohm)	RF	Reserved on variant without GNSS
41	GNSS_1PPS	O	GNSS 1PPS signal	1.8V	Reserved on variant without GNSS
36	GNSS_UART_TXD	O	UART transmit	1.8V	UART for GNSS
39	GNSS_UART_RXD	I	UART receive	1.8V	UART for GNSS
37	GNSS_UART_RTS	I	UART Request to Send	1.8V	UART for GNSS
34	GNSS_UART_CTS	O	UART Clear to Send	1.8V	UART for GNSS

8.1.2 Digital signals

8.1.2.1 GNSS_PPS

The GNSS receiver generates a one-pulse-per-second signal for synchronization. It is mapped on Pad 41.

8.1.3 GNSS Module Controlled Mode

In Controlled Mode, the GNSS receiver can be controlled by the Cellular part through specific AT commands (refer to the Telit AT Commands Reference Guide).

The NMEA stream can be retrieved through the AT interface or USB physical port of the Module.

8.2 RF Front End Design

The FE912C04 Module contains a SAW filter and LNA necessary to achieve maximum sensitivity.

8.2.1 Guidelines of PCB Line for GNSS Antenna

- Make sure that the antenna line impedance is 50ohm.
- Keep the antenna line on the PCB as short as possible to reduce the loss.
- The Antenna line must have uniform characteristics, constant cross-section, and avoid meanders, and abrupt curves.
- If possible, keep one layer of the PCB used only for the Ground plane.
- Surround (on both sides, above and below) the antenna line on PCB with Ground, avoid having other signal tracks directly facing the antenna line of the track.
- The ground around the antenna line on PCB must be strictly connected to the Ground Plane by placing away once per 2 mm at least.
- Place EM noisy devices as far as possible from the antenna line.
- Keep the antenna line far away from power supply lines.
- Keep the antenna line far away from GSM RF lines.
- If there are noisy EM devices around the PCB hosting the module, such as fast switching ICs, take care of the shielding of the antenna line by burying it inside the layers of PCB and surrounding it with Ground planes, or shielding it with a metal frame cover.
- If there are no noisy EM devices around the PCB hosting the module, use a strip line on the superficial copper layer for the antenna line. The line attenuation will be lower than a buried one.

8.2.2 Hardware-based Solution for GNSS and LTE Coexistence

When the GNSS receiver is operative, the LTE transmission may desensitize the GNSS receiver in particular if the decoupling between the LTE and GNSS antennas is low.

8.3 GNSS Antenna Requirements

Table 40: GNSS Antenna specification

Item	Value
Frequency range	• GPS L1: 1574.4 ~ 1576.4 MHz (centered on 1575.42 MHz) • GLONASS (GLO): 1597.5 ~ 1605.9 MHz (centered on 1601.7 MHz) • BeiDou (BDS): 1559.1 ~ 1563.1 MHz (centered on 1561 MHz) • Galileo (GAL): 1573.4 ~ 1577.5 MHz (centered on 1575.42 MHz) • GPS L5: 1166.22 ~ 1186.68 MHz (centered on 1176.45 MHz) • BDS B2a: 1166.22 ~ 1186.68 MHz (centered on 1176.45 MHz) • Galileo E5a: 1166.22 ~ 1186.68 MHz (centered on 1176.45 MHz)
Passive Antenna Gain	1.5 dBi < Gain < 3dBi
Impedance	50 ohm
VSWR	≤ 2:1 (recommended)

8.3.1 GNSS Standalone Mode

The FE912C04 module can be also used in Standalone mode.

8.3.2 GNSS Antenna – Installation Guidelines

- To obtain the best performance from the GNSS receiver, the antenna must be installed according to the manufacturer's instructions.
- The antenna location must be carefully evaluated if operating in conjunction with any other antenna or transmitter.
- The antenna must not be installed inside metal cases or near any obstacle that may degrade features such as antenna lobes and gain.

9 Mechanical Design

9.1 General

The FE912C04 module is designed comply with a standard lead-free soldering process.

9.2 Finishing & Dimensions

The below figure shows the mechanical dimensions of the FE912C04 module.

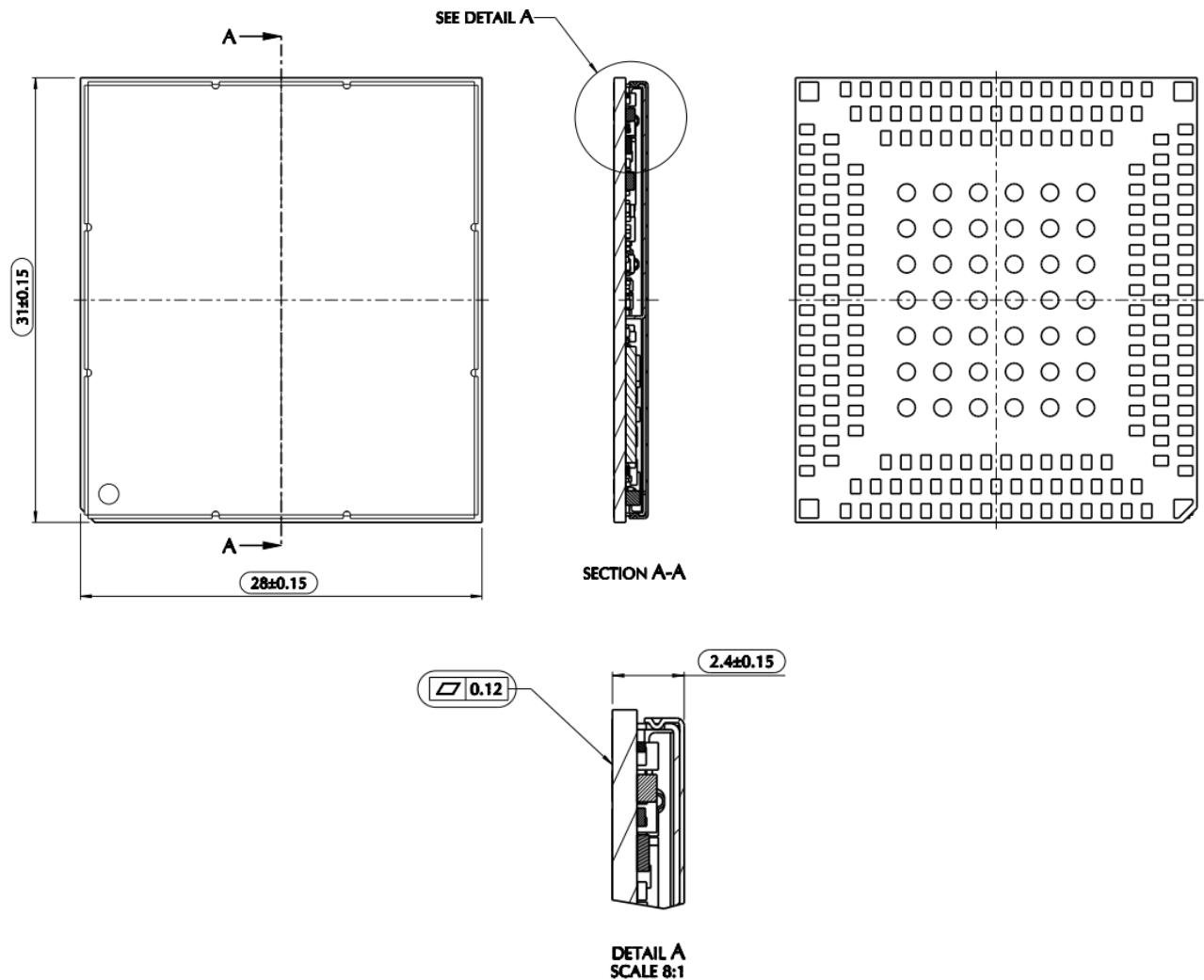


Figure 25: FE912C04 Mechanical Dimensions

10 Application PCB Design

The FE912C04 modules have been designed to be compliant with a standard lead-free SMT process.

10.1 Recommended Footprint for the Application

Top View

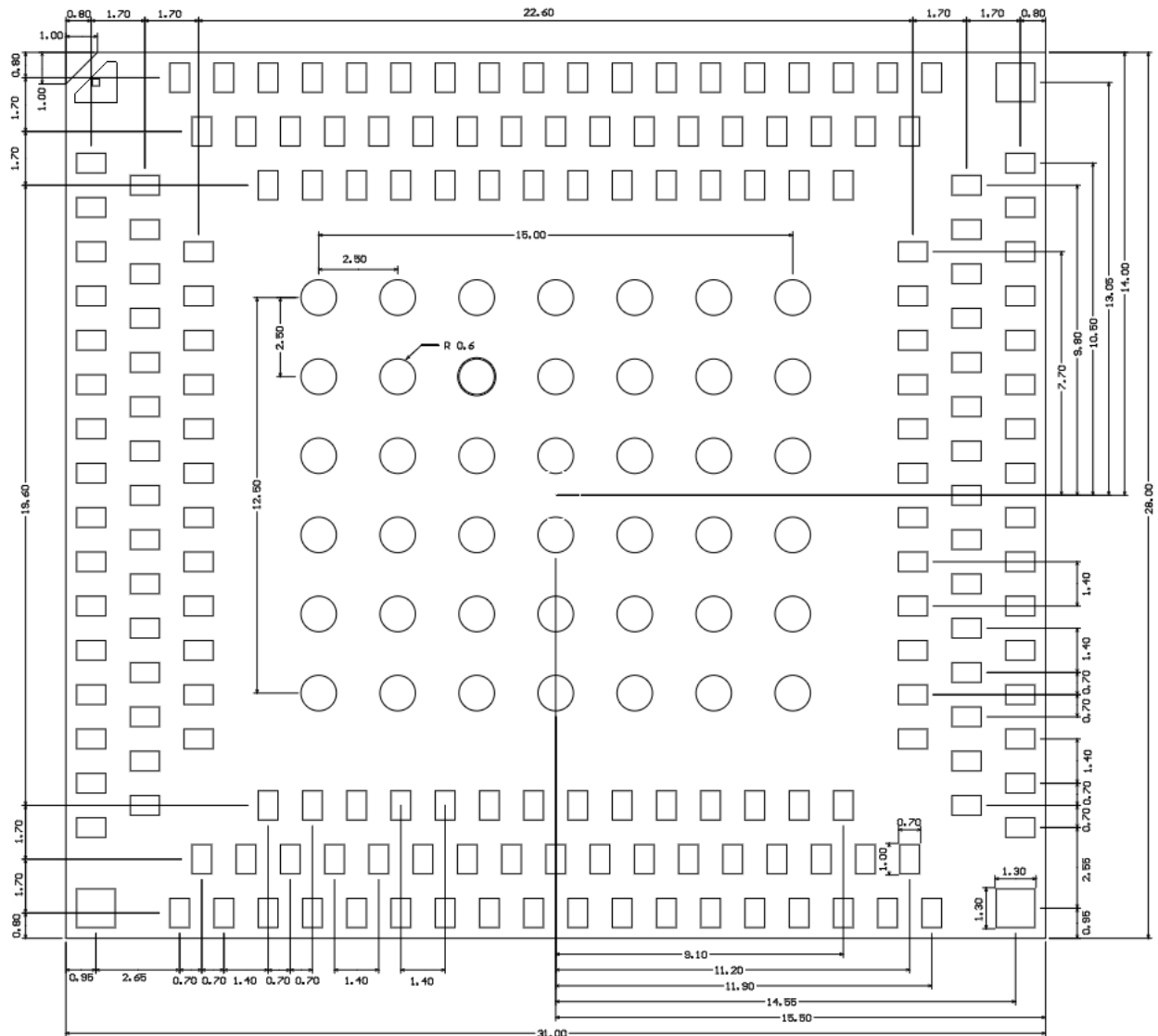


Figure 26: Footprint

To easily rework the FE912C04 it is recommended to consider on the application a 1.5 mm placement inhibit area around the module.

It is also suggested, as common rule for an SMT component, to avoid having a mechanical part of the application in direct contact with the module.

10.2 PCB Pad Design

In PCB design, the solder pads can be defined either as Solder Mask Defined (SMD) or Non-Solder Mask Defined (NSMD). The difference between these two solder mask pad definitions is in the proximity of the solder mask to the metal pad. In SMD pads, the solder mask opening is smaller than the metal pad and overlaps the metal on all sides.

The solder mask opening defines the solderable area of the pad. In NSMD pads, the solder mask opening is larger than the metal pad and does not overlap the metal. The metal edge defines the solderable area of the pad (see Figure below).

Since the metal etching process in PCB manufacturing has significantly tighter alignment and etching tolerances than the alignment registration of the solder masking process, with NSMD pads, it is possible to obtain a more accurate solder pad land pattern. Also, with SMD pads, the solder mask overlapping the metal pad introduces additional height above the metal surface which may affect solder joint adhesion and reliability. Non-solder mask defined (NSMD) type is recommended for the solder pads on the PCB.

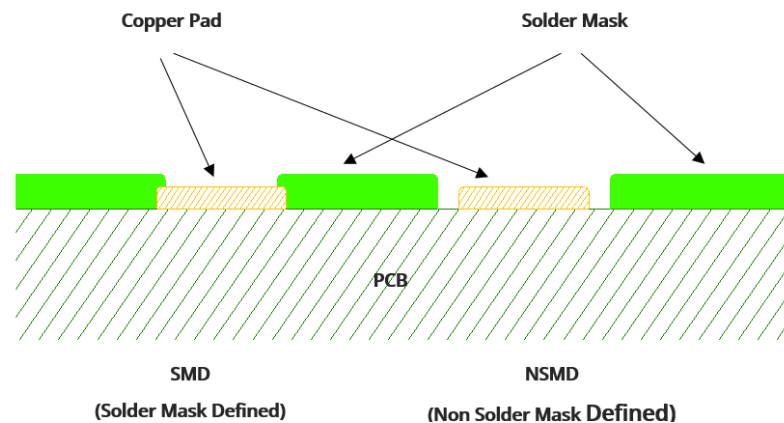


Figure 27: PCB Solder Pad Recommendations

10.3 Recommendations for PCB Pad Dimensions

It is not recommended to place via or micro-via not covered by the solder resist in an area of 0,3 mm around the pads unless it carries the same signal as the pad itself

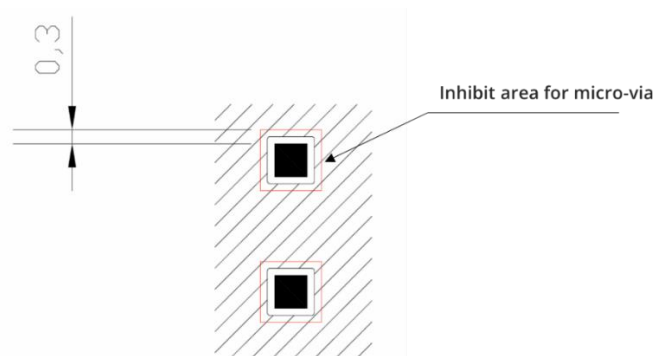


Figure 28: Pad Dimensions Recommendations

Holes in the pad are allowed only for blind holes and not for through holes.

Recommendations for PCB pad surfaces:

Table 41: Recommendations for PCB Pad Surfaces

Finish	Layer Thickness (um)	Properties
Electroless Ni / Immersion Au	3 - 7 / 0.05 - 0.15	good solder ability protection, high shear force values

The PCB must be able to resist the higher temperatures which are occurring during the lead-free process. This issue should be discussed with the PCB supplier. Generally, the wettability of tin-lead solder paste on the described surface plating is better than compared to the lead-free solder paste.

It is not necessary to panel the application's PCB, however, in that case, it is recommended to use milled contours and predrilled board breakouts; scoring or v-cut solutions are not recommended.

10.4 Thermal Performance

FR4 is one of the most commonly used PCB materials, it is a flame-retardant composite material, composed of fibreglass-reinforced and epoxy laminate. One of the features of the FR4 is to have a very low thermal conductivity. An inexpensive way to improve thermal transfer for FR-4 PCBs is to add thermal vias-plated through-holes (PTH) between the conductive layers. Vias are created by drilling holes and copper plating them, in the same way, a PTH or via is used for electrical interconnections between layers. A series of plated through-hole thermal vias should be located in the GND area underneath the Telit module of the PCB, to provide a thermal connection from the PCB GND to additional metal layers of the PCB.

The application PCB layout should include plated through-hole thermal vias for efficient heat dissipation from the Telit module into the PCB. One of the following thermal via types should be used:

- Open-plated through-hole vias that will provide lower PCB fabrication costs but may fill with solder.
- Plugged and capped plated through-hole vias will provide higher PCB fabrication costs but will not fill with solder.

Telit recommends creating areas of 10 mils (0.254-mm) vias arranged on a 25 mil (0.635-mm) rectilinear matrix. The reason for this choice is the combination of cost, performance and manufacturability. According to several PCB manufacturers, 10-mil holes and 25-mil spacing are reasonable and repeatable production choices.

A uniform metal plating thickness on the PCB will ensure reliable, high Telit module solder assembly yield.

10.5 Stencil

A silk-screen process will be required for the deposition of solder paste on the PCB, for the reflow of the Telit module on the PCB. The silk-screen process requires the use of a metal stencil based on an opening where the solder paste is transferred through the openings on the solder pads of the application PCB. To minimize solder voids and ensure maximum electrical and thermal connectivity of the module to the PCB, large pads, solder volume, and solder strain must be considered in the stencil design. The design and fabrication of the stencil determine the quality of the solder paste deposition onto the PCB and the resulting solder joint after reflow. The primary stencil parameters are aperture size, thickness, and fabrication method. The stencil should be made from stainless steel and the apertures layout can be the same as the recommended footprint (1:1). The recommended thickness shall be 127 μm (5 mil). A stencil thickness of 152 μm (6 mil) can be used as well.

10.6 Solder Paste

Various types and grades of solder paste can be used for surface mounting Telit modules. For lead-free applications, an Sn-Ag (SA) or Sn-Ag-Cu (SAC) solder paste can be used. Any Type 3 solder paste that is either water-soluble or not clean is acceptable.

We recommend using only “no clean” solder paste to avoid the cleaning of the modules after assembly.

10.7 Solder Reflow

Recommended solder reflow profile:

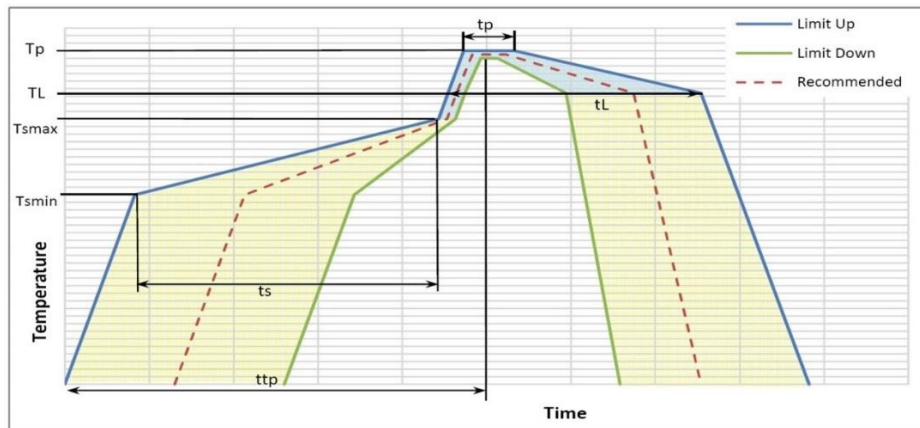


Figure 29: Recommended Solder Reflow Profile

Table 42: Profile Feature Recommendations

Profile Feature	Pb-Free Assembly Free
Average ramp-up rate (T_L to T_P)	3°C/second max
Preheat - Temperature Min (T_{smmin}) - Temperature Max (T_{smmax}) - Time (min to max) (t_s)	150°C 200°C 60-180 seconds
T_{smmax} to T_L Ramp-up Rate	3°C/second max
Time maintained above: - Temperature (T_L) - Time (t_L)	217°C 60-150 seconds
Peak Temperature (T_P)	245 +0/-5°C
Time within 5°C of actual Peak Temperature (t_p)	10-30 seconds
Ramp-down Rate	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

Note: All temperatures refer to the topside of the package, measured on the package body surface.

Warning: THE FE912C04 MODULE WITHSTANDS ONE REFLOW PROCESS ONLY.

Warning: The above solder reflow profile represents the typical SAC reflow limits and does not guarantee adequate adherence of the module to the customer application throughout the temperature range. Customers must optimize the reflow profile depending on the overall system taking into account such factors as thermal mass and warpage.

10.8 Inspection

An inspection of the solder joint between the solder pads of the Telit module and the application PCB should be performed. The best visual inspection tool for inspection of the Telit module solder joints on the PCB is a transmission X-ray, which can identify defects such as solder bridging, shorts, opens, and large voids (Note: small voids in large solder joints are not detrimental to the reliability of the solder joint).

11 Packaging

11.1 Tray

The FE912C04 modules are packaged on trays that can be used in SMT processes for pick & place handling. The first Marketing and Engineering samples of the FE912C04 series will be shipped with the current packaging of the FE912C04 modules (on trays of 27 pieces each). The mass production units of FE912C04 will be shipped according to the following drawings:

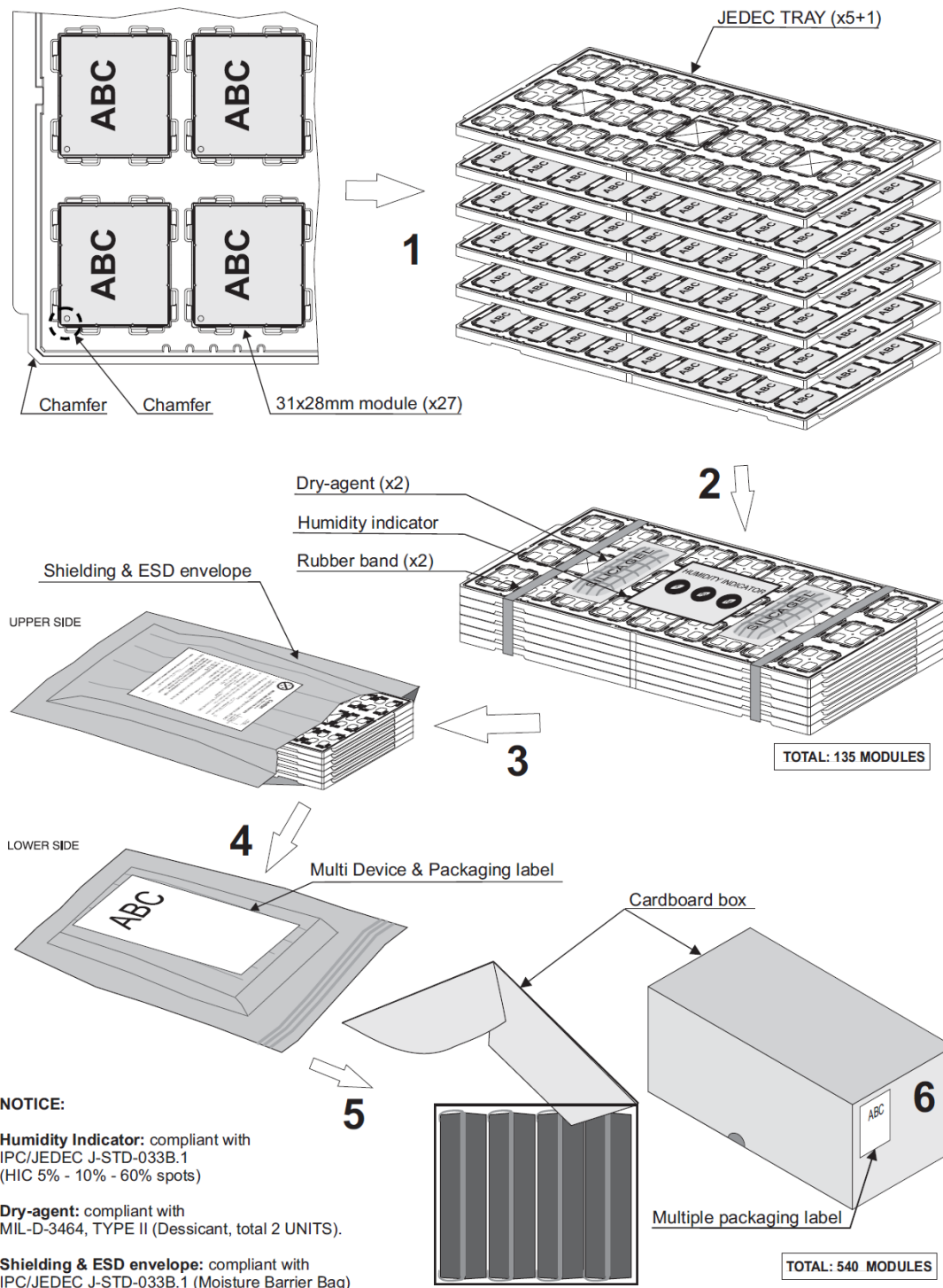


Figure 30: Tray Packaging

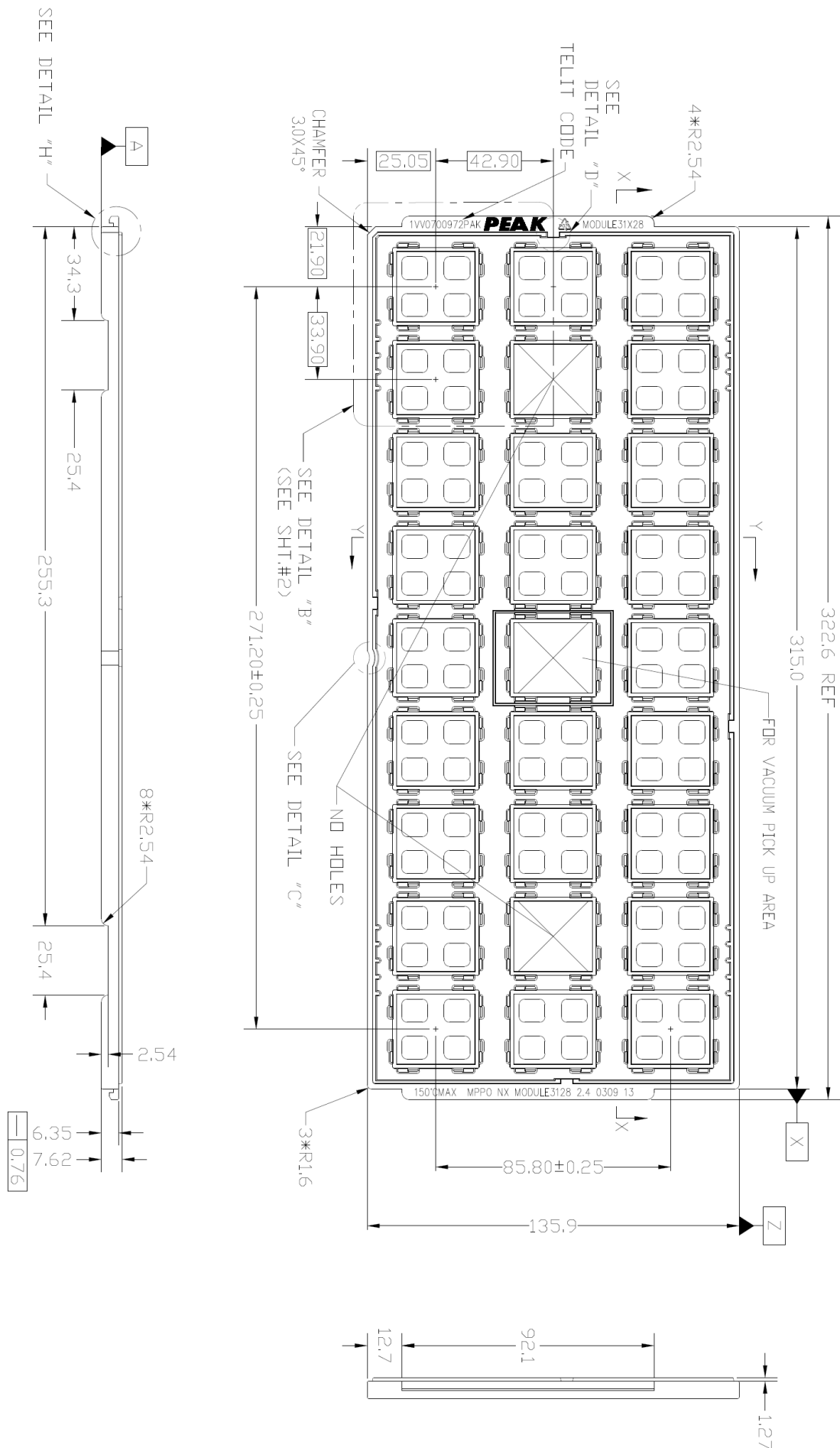


Figure 31: Tray Dimensions

11.2 Reel

The FE912C04 can be packaged on reels of 400 pieces each. See the figure for module positioning into the carrier.

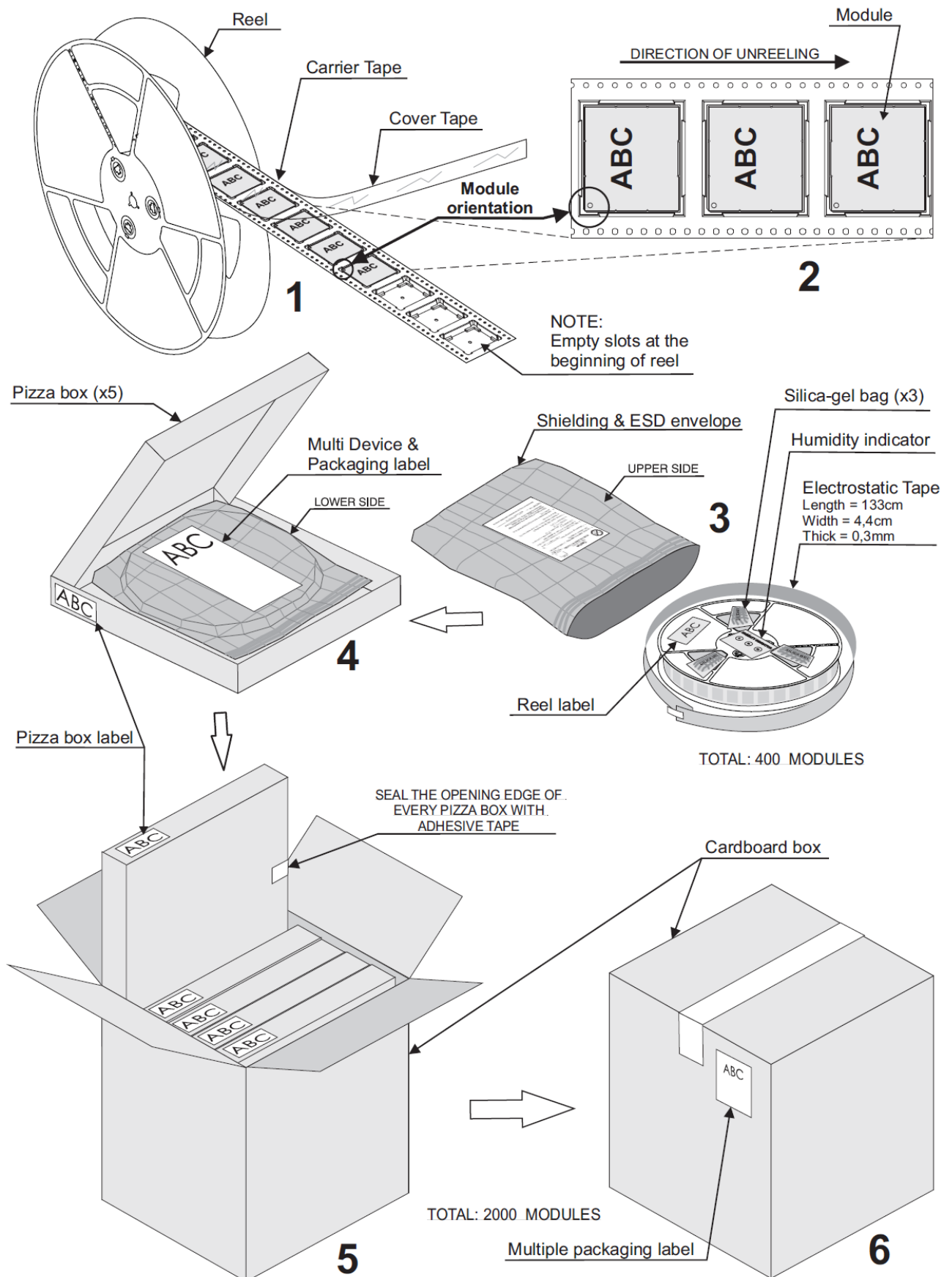


Figure 32: Module Positioning into the Carrier

11.3 Carrier Tape Detail

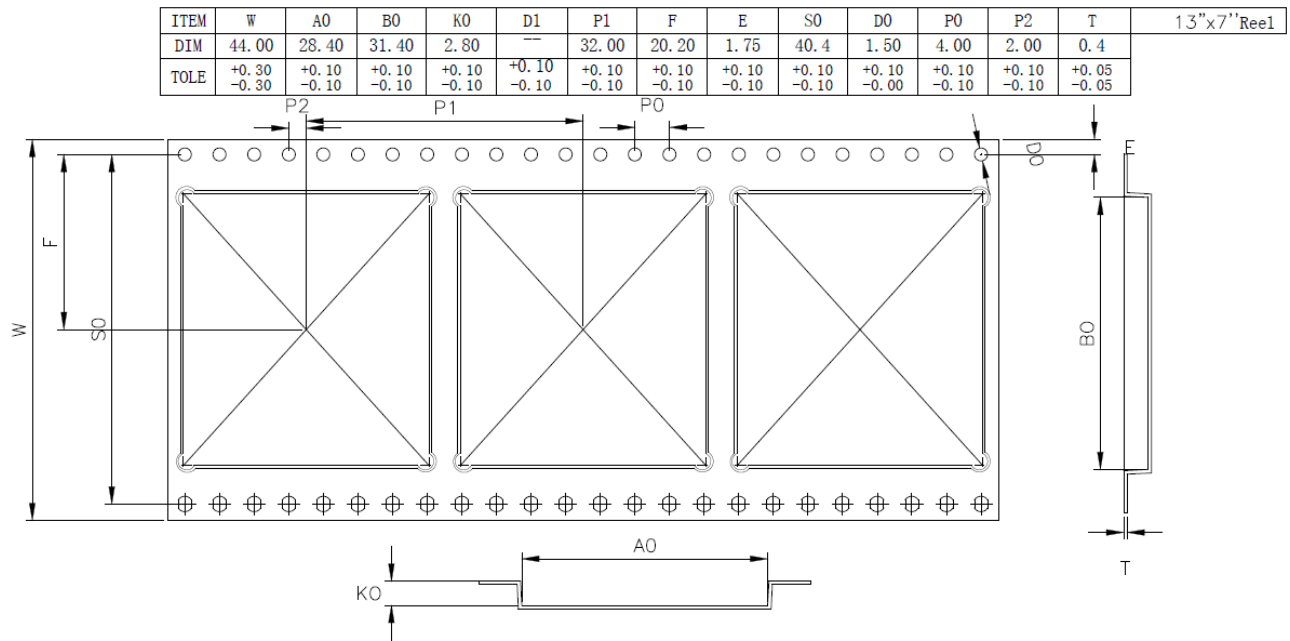


Figure 33: Carrier Tape Detail

11.4 Reel Detail

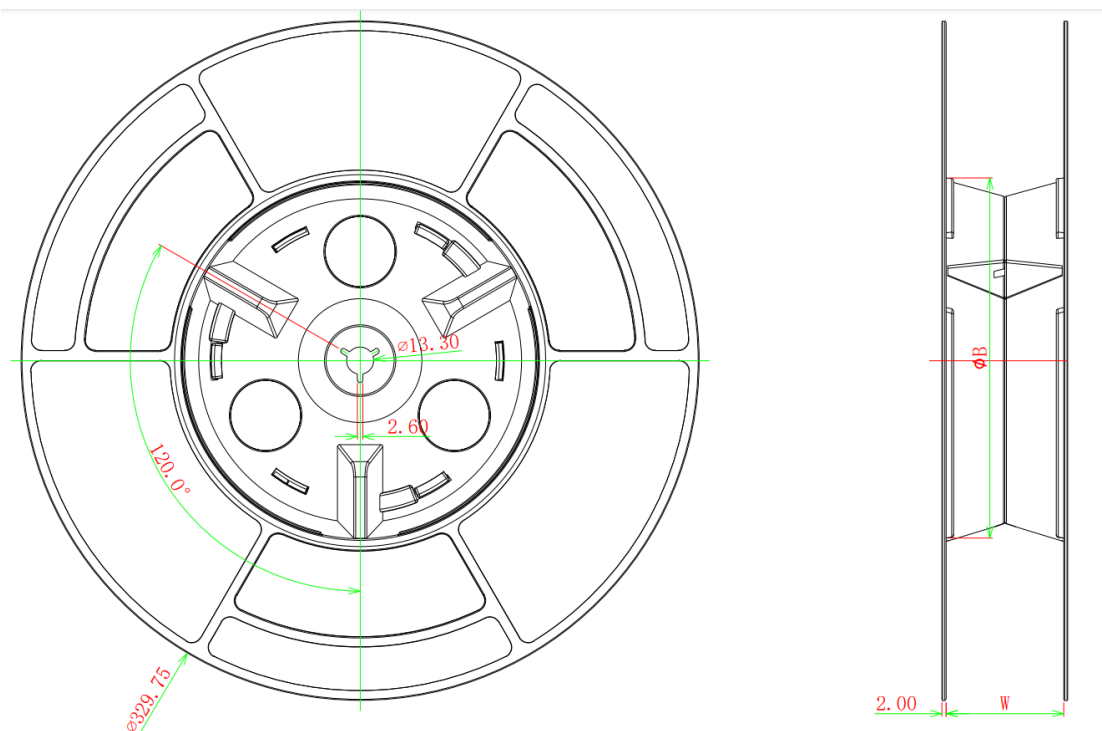


Figure 34: Reel Detail

11.5 Moisture Sensitivity

The FE912C04 is a Moisture Sensitive Device level 3, according to standard IPC/JEDEC J-STD-020, and takes care of all the relative requirements for using this kind of component. Moreover, the customer has to take care of the following conditions:

- a** Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH).

- b** An environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J STD-033A paragraph 5.
- c** The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition b) "IPC/JEDEC J-STD-033D paragraph 5.2" is respected
- d** Baking is required if conditions b) or c) are not respected
- e** Baking is required if the humidity indicator inside the bag indicates 10% RH or more.

12 Conformity Assessment Issues [TBD]

12.1 Approvals Compliance Summary [TBD]

Table 43: Legend Description

Legend	Description
	The equipment is compliant
	Type approval is in progress
	The equipment is not compliant

Table 44: Americas Approvals Compliance Summary

Region	Americas									
Country & Type Approval	AR ENACOM	BR ANATEL	CA ISED	CO CRC	MX IFETEL	PE MTC	US FCC	BOL ATT	ECU ARCOTEL	PY CONATEL
FE912C04-NA										
FE912C04-RW										

Table 45: APAC Approvals Compliance Summary

Region	APAC				
Country & Type Approval	AU RCM	CH CCC	JP JRL / JTBL	SG IMDA	TW NCC
FE912C04-NA					
FE912C04-RW					

Table 46: EMEA Approvals Compliance Summary

Region	EMEA	
Country & Type Approval	EU RED	UK UKCA
FE912C04-NA		
FE912C04-RW		

Note: For approvals not included in the above, contact Telit support.

12.2 Americas Approvals

12.2.1 USA FCC

12.2.1.1 FCC Certificates

The FCC Grants can be found here: <https://www.fcc.gov/oet/ea/fccid>

Applicable FCC Rules

Table 47: Applicable FCC Rules

Model	Applicable FCC rules
FE912C04-NA	Title 47 CFR Part 2, Part 22, Part 24, Part 27, Part 90, Part 96

12.2.1.2 FCC Regulatory Notices

Modification Statement

Telit has not approved any changes or modifications to this device by the user. Any changes or modifications could void the user's authority to operate the equipment.

Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Wireless Notice

This device complies with FCC radiation exposure limits set forth for an uncontrolled environment and meets the FCC radio frequency (RF) Exposure Guidelines. This transmitter must not be co-located or operate in conjunction with any other antenna or transmitter. The antenna should be installed and operated with a minimum distance of 20 cm between the radiator and your body

FCC Class B digital device notice

This equipment has been tested and found to comply with the limits for a Class B digital device, according to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used per the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by taking one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment to an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Information for the OEMs and Integrators

The following statement must be included with all versions of this document supplied to an OEM or integrator but should not be distributed to the end user.

- 1 This device is intended for OEM integrators only.
- 2 See the full Grant of Equipment document for other restrictions

Manual Information to the End User

The OEM integrator should be aware not to provide information to the end-user on how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as shown in this manual

Information on test modes and additional testing requirements

The module has been evaluated in mobile stand-alone conditions. For operational conditions other than a stand-alone modular transmitter in a host (multiple, simultaneously transmitting modules or other transmitters in a host), additional testing may be required (collocation, retesting...). If this module is intended for use in a portable device, you are responsible for separate approval to satisfy the SAR requirements of FCC Part 2.1093.

Additional testing, Part 15 Subpart B disclaimer

The modular transmitter is only authorized by the FCC for the specific rule parts (for example, FCC transmitter rules) listed on the grant, and the host product manufacturer is responsible for compliance with any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuitry), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed. The end product with an embedded module may also need to pass the FCC Part 15 unintentional emission testing requirements and be properly authorized per FCC Part 15.

12.2.1.3 FCC Antenna Info

This radio transmitter has been approved by FCC to operate with the antenna types listed below with the maximum allowable gain indicated. Antenna types not included in this list, with a gain greater than the maximum gain indicated for that type, are strictly prohibited from use with this device.

Table 48: FCC Antenna Type

Model	Antenna Type
FE912C04-NA	Omnidirectional Monopole Antenna

Table 49: Max Antenna gain for FCC in dBi

Max gain for FCC (dBi)		
Operation Mode	Freq. (MHz)	Max Allowable Antenna Gain (dBi)
LTE B2	1850.7	8.50
LTE B4	1710.7	5.50
LTE B5	824.7	9.91
LTE B7	2502.5	8.50
LTE B12	699.7	9.19
LTE B13	799.5	9.67
LTE B14	788.0	9.71
LTE B17	704.0	9.22
LTE B25	1850.7	8.50
LTE B26	824.7	9.91
LTE B26 Part 90	814.7	9.86
LTE B30	2307.5	1.00
LTE B41	2498.5	8.50

Max gain for FCC (dBi)		
LTE B41 (HPUE)	2498.5	6.00
LTE B48	3552.50	0.50
LTE B66	1710.70	5.50
LTE B71	665.50	8.98
5G NR n2	1850.7	8.50
5G NR n5	824.7	9.91
5G NR n7	2502.5	8.50
5G NR n12	699.7	9.19
5G NR n13	779.5	9.67
5G NR n14	788.0	9.71
5G NR n25	1850.7	8.50
5G NR n26	824.7	9.91
5G NR n26 Part90	814.7	9.86
5G NR n41_PC3	2498.5	8.50
5G NR n48	3552.50	0.40
5G NR n66	1710.70	5.50
5G NR n71	665.50	8.98
5G NR n77_PC3	4200.00	5.49
5G NR n78_PC3	3800.00	5.49

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Labelling requirements for the host device

The host device shall be properly labelled to identify the modules within the host device. The certification label of the module shall be visible at all times when installed in the host device, otherwise, the host device must be labelled to display the FCC ID of the module, preceded by the words "Contains transmitter module", or the word "Contains", or similar wording expressing the same meaning, as in the below table.

Table 50: Host device FCC label

Model / HVIN	Host device FCC label
FE912C04-NA	Contains FCC ID: RI7FE912C04NA

* Data-only variants share the same HW as related voice variants and the voice features are disabled by SW. The new FVIN has the same stack as the originally approved voice variant but w/o voice support and this is to satisfy mainly the need of MNOs in the USA.

12.2.2 Canada ISED

12.2.2.1 ISED Database

The products ISED certified can be found here:

Les produits certifiés ISED peuvent être trouvés ici:

<https://sms-sgs.ic.gc.ca/equipmentSearch/searchRadioEquipments?execution=e1s1&lang=en>

12.2.2.2 Applicable ISED Rules

Table 51: Applicable ISED rules / Règles ISDE applicables

Model	Applicable ISED rules /Règles ISDE applicables 2
FE912C04-NA	RSS-Gen Issue 5, RSS-102 Issue 6, RSS-130 Issue 2, RSS-132 Issue 4, RSS-133 Issue 7, RSS-139 Issue 4, RSS-140 Issue 1, RSS-192 Issue 5, RSS-195 Issue 2, RSS-199 Issue 4, RSS-198 Issue 1

12.2.2.3 ISED Regulatory Notices

Modification Statement / Déclaration de modification

Telit has not approved any changes or modifications to this device by the user. Any changes or modifications could void the user's authority to operate the equipment.

Telit n'approuve aucune modification apportée à l'appareil par l'utilisateur, quelle qu'en soit la nature. Tout changement ou modification peuvent annuler le droit d'utilisation de l'appareil par l'utilisateur.

Interference Statement / Déclaration d'interférence

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux applicables RSS standards d'Industrie Canada. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Radio Exposure Notice / Avis d'exposition radio

This device complies with ISED radiation exposure limits set forth for an uncontrolled environment and meets the RSS-102 of the ISED radio frequency (RF) Exposure rules. Antenna gain must be less than the values reported in the table below:

Le présent appareil est conforme à l'exposition aux radiations FCC / ISED définies pour un environnement non contrôlé et répond aux directives d'exposition de la fréquence de la FCC radiofréquence (RF) et RSS-102 de la fréquence radio (RF) ISED règles d'exposition. Gain de l'antenne doit être ci-dessous:

Table 52: ISED Antenna Type

Model	Antenna Type / Type d'Antenne
FE912C04-NA	Antenne monopôle omnidirectionnelle

Table 53: Max Antenna gain for ISED in dBi / Gain d'antenne max pour ISED en dBi

Max gain for ISED/ Gain max pour ISED (dBi)		
Operation Mode	Freq. (MHz)	Max Allowable Antenna Gain (dBi)
LTE B2	1850.7	8.50
LTE B4	1710.7	5.50
LTE B5	824.7	6.60
LTE B7	2502.5	8.50

Max gain for ISED/ Gain max pour ISED (dBi)		
LTE B12	699.7	6.11
LTE B13	799.5	6.43
LTE B14	788.0	6.47
LTE B17	704.0	6.13
LTE B25	1850.7	8.50
LTE B26	824.7	6.60
LTE B30	2307.5	1.00
LTE B41	2498.5	8.50
LTE B41 (HPUE)	2498.5	6.00
LTE B48	3552.50	0.50
LTE B66	1710.70	5.50
LTE B71	665.50	5.96
5G NR n2	1850.7	8.50
5G NR n5	824.7	6.60
5G NR n7	2502.5	8.50
5G NR n12	699.7	6.11
5G NR n13	779.5	6.43
5G NR n14	788.0	6.47
5G NR n25	1850.7	8.50
5G NR n26	824.7	6.60
5G NR n41_PC3	2498.5	8.50
5G NR n48	3552.50	0.40
5G NR n66	1710.70	5.50
5G NR n71	665.50	5.96
5G NR n77_PC3	4200.00	5.49
5G NR n78_PC3	3800.00	5.49

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

L'émetteur ne doit pas être colocalisé ni fonctionner conjointement avec à autre antenne ou autre émetteur.

This equipment must be installed and operated following provided instructions and the antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter. End-users and installers must be provided with antenna installation instructions and consider removing the no-collocation statement.

Cet équipement doit être installé et utilisé conformément aux instructions fournies et la ou les antennes utilisées pour cet émetteur doivent être installées pour fournir une distance de séparation d'au moins 20 cm de toutes les personnes et ne doivent pas être co-localisées ou fonctionner en conjonction avec toute autre antenne ou émetteur. Les utilisateurs finaux et les

installateurs doivent recevoir les instructions d'installation de l'antenne et envisager de supprimer la déclaration de non-collocation.

Information on test modes and additional testing requirement / Informations sur les modes de test et exigences de test supplémentaires

The module has been evaluated in mobile stand-alone conditions. For operational conditions other than a stand-alone modular transmitter in a host (multiple, simultaneously transmitting modules or other transmitters in a host), additional testing may be required (collocation, retesting...) If this module is intended for use in a portable device, you are responsible for separate approval to satisfy the SAR requirements IC RSS-102.

Le module a été évalué dans des conditions mobiles autonomes. Pour des conditions de fonctionnement autres qu'un émetteur modulaire autonome dans un hôte (plusieurs modules transmettant simultanément ou d'autres émetteurs dans un hôte), des tests supplémentaires peuvent être nécessaires (colocalisation, retest...) Si ce module est destiné à être utilisé dans un appareil portable, vous êtes responsable de l'approbation séparée pour satisfaire aux exigences SAR IC RSS-102.

Labelling requirements for the host device / Exigences d'étiquetage pour le périphérique hôte

The host device shall be properly labelled to identify the modules within the host device. The certification label of the module shall be visible at all times when installed in the host device, otherwise, the host device must be labelled to display the IC of the module, preceded by the words "Contains transmitter module", or the word "Contains", or similar wording expressing the same meaning, as in the following table.

L'appareil hôte doit être étiqueté comme il faut pour permettre l'identification des modules qui s'y trouvent. L'étiquette de certification du module donné doit être posée sur l'appareil hôte à un endroit bien en vue en tout temps. En l'absence d'étiquette, l'appareil hôte doit porter une étiquette donnant le IC du module, précédé des mots « Contient un module d'émission », du mot « Contient » ou d'une formulation similaire exprimant le même sens, comme en tableau suivant.

Table 54: Host device IC label / Étiquette IC du dispositif hôte

Model / HVIN	Host device IC label / Étiquette IC du dispositif hôte
FE912C04-NA	Contains IC: 5131A-FE912C04NA

* Data-only variants share the same hardware as related voice variants and the voice features are disabled by SW. The new FVIN has the same stack as the originally approved voice variant but w/o voice support and this is to satisfy mainly the need of MNOs in the USA.

Les variantes avec seulement data fonctionnalité partagent le même hardware que les variantes avec les fonctionnalités vocales qui sont désactivées par le SW. Le nouveau FVIN a le même stack que la variante avec fonctionnalités vocales approuvée d'origine, mais sans la prise en charge vocale et cela pour satisfaire principalement le besoin des MNO aux États-Unis.

CAN ICES-3 (B) / NMB-3 (B)

This Class B digital apparatus complies with Canadian ICES-003.

Cet appareil numérique de classe B est conforme à la norme canadienne ICES-003.

12.2.3 Brazil ANATEL [TBD]

12.2.3.1 ANATEL Regulatory Notices

Agência Nacional de Telecomunicações (ANATEL) of Brazil

Note: For Wi-Fi or BT modules, insert following lines:

"Este equipamento não tem direito à proteção contra interferência prejudicial e não pode causar interferência em sistemas devidamente autorizados".

"This equipment is not entitled to protection against harmful interference and must not cause interference in duly authorized systems"



FE912C04-RW Homologation # TBD

12.3 APAC Approvals [TBD]

12.3.1 Australia RCM

Following the above Approval Compliance Summary table, where applicable (green dot), hereby, Telit Communications S.p.A declares that the equipment complies with the Regulatory Compliance Mark (RCM) of Australia.

Note: The equipment listed may not work when the main power fails.

12.3.2 Japan JRL/JTBL [TBD]

12.3.2.1 JRL/JTBL Regulatory Notices

Antenna info

According to Japanese regulatory rules, module certification is valid only with the specific antennas registered to and approved by Japan Radio Law (JRL) certified body to module certification. Customers who are going to use modules under JRL are responsible to contact Telit technical support or sales to get the list of these antennas.

Dial Function

The Japan Telecommunication Business Law (JTBL) Module Certification for "FE912C04-RW" is for a "non-Auto Redial Function" device.

In case the customer implements the "Auto Redial" function into the Application Device by controlling FE912C04-RW, the customer cannot utilize FE912C04-RW JTBL certification, and they must apply JTBL as an "Application Device" System.

12.3.3 Taiwan NCC [TBD]

12.3.3.1 NCC Regulatory Notices

According to National Communication Commission (NCC) Taiwan requirements, the module and the packaging shall be identified as described in the following lines. Shall be added also the specified safety warning statement.

Brand name: Telit Cinterion or 

Model name: FE912C04-RW

Product name: 5G Radio module

NCC logo: 

NCC ID: TBD

NCC safety warning statement : “減少電磁波影響，請妥適使用”

12.4 EMEA Approvals

12.4.1 EU RED

12.4.1.1 EU Declaration of Conformity

Following the above Approval Compliance Summary table, where applicable (green dot), hereby, Telit Communications S.p.A declares that the equipment complies with Directive 2014/53/EU.

The full text of the EU Declaration of Conformity is available at the following internet address: <https://www.telit.com/red>

Text of 2014/53/EU Directive (RED) requirements can be found here:

<https://eur-lex.europa.eu/legal-content/EN/TXT/?uri=CELEX:32014L0053>

12.4.1.2 RED Antennas

This radio transmitter has been approved under RED to operate with the antenna types listed below with the maximum permissible gain indicated. The usage of a different antenna in the final hosting device may need a new assessment of host conformity to RED.

Table 55: RED Antenna Type

Model	Antenna Type
FE912C04-RW	Omnidirectional Monopole Antenna

Table 56: Max Antenna gain for RED in dBi

Max gain for RED (dBi)		
Operation Mode	Freq. (MHz)	Max Allowable Antenna Gain (dBi)
LTE B1	1920.00	12.35
LTE B3	1710.00	11.85
LTE B5	824.00	8.67
LTE B7	2500.00	12.46
LTE B8	880.00	8.96
LTE B20	832.00	8.72
LTE B40	2302.50	12.46
LTE B41(HPUE)	2496.00	9.96
LTE B28	703.00	7.98
5G NR n1	1920.00	12.35

Max gain for RED (dBi)		
5G NR n3	1710.00	11.85
5G NR n5	824.00	8.67
5G NR n7	2500.00	12.46
5G NR n8	880.00	8.96
5G NR n20	832.00	8.72
5G NR n40	2302.50	12.46
5G NR n41_PC3	2496.00	12.46
5G NR n28	703.00	7.98
5G NR n77_PC3	3300.00	12.46
5G NR n78_PC3	3300.00	12.46

12.4.2 UK UKCA

12.4.2.1 UKCA Declaration of Conformity

Following the above Approval Compliance Summary table, where applicable (green dot), hereby, Telit Communications S.p.A declares that the equipment complies with the Radio Equipment Regulations 2017 for UKCA.

The full text of the UKCA declaration of conformity is available at the following internet address: <https://www.telit.com/ukca>

The UKCA requirements can be found here:

<https://www.gov.uk/guidance/using-the-ukca-marking>

12.5 RoHS, REACH, and WEEE Info

12.5.1 RoHS Info

Any requests on information related to RoHS certifications can be addressed to Chemical.Certifications@telit.com.

12.5.2 REACH Info

Any requests on information related to REACH certifications can be addressed to Chemical.Certifications@telit.com.

12.5.3 WEEE Info



This symbol means that according to local laws and regulations your product and/or its battery shall be disposed of separately from household waste. When this product reaches its end of life, take it to a collection point designated by local authorities. Proper recycling of your product will protect human health and the environment.

13 Reference Table of RF Bands Characteristics

Table 57: LTE RF Bands Characteristics

E-UTRA BAND	Freq. Tx (MHz)	Freq. Rx (MHz)	Channels	Tx-Rx Offset
B1 - 2100	1920 ~ 1980	2110 ~ 2170	Tx: 18000 ~ 18599 Rx: 0 ~ 599	190 MHz
B2 - 1900 PCS	1850 ~ 1910	1930 ~ 1990	Tx: 18600 ~ 19199 Rx: 600 ~ 1199	80 MHz
B3 - 1800+	1710 ~ 1785	1805 ~ 1880	Tx: 19200 ~ 19949 Rx: 1200 ~ 1949	95 MHz
B4 - AWS-1	1710 ~ 1755	2110 ~ 2155	Tx: 19950 ~ 20399 Rx: 1950 ~ 2399	400 MHz
B5 - 850	824 ~ 849	869 ~ 894	Tx: 20400 ~ 20649 Rx: 2400 ~ 2649	45 MHz
B7 - 2600	2500 ~ 2570	2620 ~ 2690	Tx: 20750 ~ 21449 Rx: 2750 ~ 3449	120 MHz
B8 - 900 GSM	880 ~ 915	925 ~ 960	Tx: 21450 ~ 21799 Rx: 3450 ~ 3799	45 MHz
B12 - 700 a	699 ~ 716	729 ~ 746	Tx: 23010 ~ 23179 Rx: 5010 ~ 5179	30 MHz
B13 - 700 c	777 ~ 787	746 ~ 756	Tx: 23180 ~ 23279 Rx: 5180 ~ 5279	-31 MHz
B14 - 700 PS	788 ~ 798	758 ~ 768	Tx: 23280 ~ 23379 Rx: 5280 ~ 5379	-30 MHz
B17 - 700 b	704 ~ 716	734 ~ 746	Tx: 23730 ~ 23849 Rx: 5730 ~ 5849	30 MHz
B20 - 800 DD	832 ~ 862	791 ~ 821	Tx: 24150 ~ 24449 Rx: 6150 ~ 6449	-41 MHz
B25 - 1900+	1850 ~ 1915	1930 ~ 1995	Tx: 26040 ~ 26689 Rx: 8040 ~ 8689	80 MHz
B26 - 850+	814 ~ 849	859 ~ 894	Tx: 26690 ~ 27039 Rx: 8690 ~ 9039	45 MHz
B28 - 700 APT	703 ~ 748	758 ~ 803	Tx : 27210 ~ 27659 Rx : 9210 ~ 9659	55 MHz
B30 - 2300 WCS	2305 ~ 2315	2350 ~ 2360	Tx: 27660 ~ 27759 Rx: 9770 ~ 9869	45 MHz
B40 - 2300	2300 ~ 2400	2300 ~ 2400	Tx: 38650 ~ 39649 Rx: 38650 ~ 39649	0 MHz
B41 - 2600+	2496 ~ 2690	2496 ~ 2690	Tx: 39650 ~ 41589 Rx: 39650 ~ 41589	0 MHz
B48 - 3600	3550 ~ 3700	3550 ~ 3700	Tx: 55240 ~ 56739 Rx: 55240 ~ 56739	0 MHz
B66 - AWS	1710 ~ 1780	2110 ~ 2200	Tx: 131972 ~ 132671 Rx: 66436 ~ 67335	400 MHz

E-UTRA BAND	Freq. Tx (MHz)	Freq. Rx (MHz)	Channels	Tx-Rx Offset
B71 - 600	663 ~ 698	617 ~ 652	Tx: 133122 ~ 133471 Rx: 68586 ~ 68935	-46 MHz

Table 58: 5G NR RF Bands Characteristics

NR BAND	SCS (kHz)	Freq. Tx (MHz)	Freq. Rx (MHz)	Channels	Tx-Rx Offset
n1 - 2100	15	1920 ~ 1980	2110 ~ 2170	Tx: 384000 ~ 396000 Rx: 422000 ~ 434000	190 MHz
n2 - 1900 PCS	15	1850 ~ 1910	1930 ~ 1990	Tx: 370000 ~ 382000 Rx: 386000 ~ 398000	80 MHz
n3 - 1800	15	1710 ~ 1785	1805 ~ 1880	Tx: 342000 ~ 357000 Rx: 361000 ~ 376000	95 MHz
n5 - 850	15	824 ~ 849	869 ~ 894	Tx: 164800 ~ 169800 Rx: 173800 ~ 178800	45 MHz
n7 - 2600	15	2500 ~ 2570	2620 ~ 2690	Tx: 500000 ~ 514000 Rx: 524000 ~ 538000	120 MHz
n8 - 900	15	880 ~ 915	925 ~ 960	Tx: 176000 ~ 183000 Rx: 185000 ~ 192000	45 MHz
n12 - 700 a	15	699 ~ 716	729 ~ 746	Tx: 139800 ~ 143200 Rx: 145800 ~ 149200	30 MHz
n13 - 700 c	15	777 ~ 787	746 ~ 756	Tx: 155400 ~ 157400 Rx: 149200 ~ 151200	-31 MHz
n14 - 700 PS	15	788 ~ 798	758 ~ 768	Tx: 157600 ~ 159600 Rx: 151600 ~ 153600	-30 MHz
n20 - 800	15	832 ~ 862	791 ~ 821	Tx: 166400 ~ 172400 Rx: 158200 ~ 164200	-41 MHz
n25 - 1900+	15	1850 ~ 1915	1930 ~ 1995	Tx: 370000 ~ 383000 Rx: 386000 ~ 399000	80 MHz
n26 - 850+	15	814 ~ 849	859 ~ 894	Tx: 162800 ~ 169800 Rx: 171800 ~ 178800	45 MHz
n28 - 700 APT	15	703 ~ 748	758 ~ 803	Tx: 140600 ~ 149600 Rx: 151600 ~ 160600	55 MHz
n40 - 2300	30	2300 ~ 2400	2570 ~ 2620	Tx: 460000 ~ 480000 Rx: 460000 ~ 480000	0 MHz
n41 - 2600+	30	2496 ~ 2690	2570 ~ 2620	Tx: 460000 ~ 480000 Rx: 460000 ~ 480000	0 MHz
n48 - 3600	30	3550 ~ 3700	2570 ~ 2620	Tx: 636668 ~ 646666 Rx: 636668 ~ 646666	0 MHz
n66 - AWS-3	15	1710 ~ 1780	2110 ~ 2200	Tx: 342000 ~ 356000 Rx: 422000 ~ 440000	400 MHz
n71 - 600	15	663 ~ 698	617 ~ 652	Tx: 132600 ~ 139600 Rx: 123400 ~ 130400	-46 MHz
n77 - 3700	30	3300 ~ 4200	3300 ~ 4200	Tx: 620000 ~ 680000 Rx: 620000 ~ 680000	0 MHz

NR BAND	SCS (kHz)	Freq. Tx (MHz)	Freq. Rx (MHz)	Channels	Tx-Rx Offset
n78 - 3500	30	3300 ~ 3800	3300 ~ 4200	Tx: 620000 ~ 653332 Rx: 620000 ~ 653332	0 MHz

14 Acronyms and Abbreviations

Table 59: Acronyms and Abbreviations

Acronym	Definition
ADC	Analog – Digital Converter
CLK	Clock
CMOS	Complementary Metal – Oxide Semiconductor
CS	Chip Select
DAC	Digital – Analog Converter
DTE	Data Terminal Equipment
ESR	Equivalent Series Resistance
GPIO	General Purpose Input Output
HS	High Speed
HSDPA	High-Speed Downlink Packet Access
HSIC	High-Speed Inter Chip
HSUPA	High-Speed Uplink Packet Access
I/O	Input Output
MISO	Master Input – Slave Output
MOSI	Master Output – Slave Input
MRDY	Master Ready
PCB	Printed Circuit Board
RTC	Real-Time Clock
SIM	Subscriber Identification Module
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access

15 Related Documents

For current documentation and downloads, refer to <https://dz.telit.com/>.

Table 60: Related Documents

S.no	Doc Code	Document Title
1	80815ST11205A	FE912C04 Family AT Commands Reference Guide
2	1VV0301972	FE912C04 Family Software User guide

16 Document History

Table 61: Document History

Revision	Date	Changes
4	2025-03-25	Updated Figure 1 Block Diagram Updated Table 49,53,56 Max Antenna gain
3	2025-03-14	Updated 5.2 Power Consumption Updated 6.3 Power On Updated 6.4 Shutdown by Software Command Updated 6.5 RESET_N Updated 7.3 Conducted Receiver Sensitivity Updated Table 38: GNSS Characteristics Updated Table 40: GNSS antenna specification – Frequency range Updated 12. Conformity Assessment issues
2	2024-12-19	Updated 4.2 Signals that Must Be Connected Updated 5.2 Power Consumption Updated 5.3.4 Bypass Capacitor on Power Supplies Updated 6.1.1 1.8V Standard GPIOs Updated 6.2 Power On Updated 6.3 Power Off Updated 6.5 RESET_N Updated 6.6.1 USB Updated 6.10 External SIM Holder Updated 7.2 Conducted Transmit Output Power Updated 7.3 Conducted Receiver Sensitivity
1	2024-08-12	Restructured the document and updated content. Updated 5.2 Power Consumption Updated 7.3 RX sensitivity
0	2024-07-23	Initial release

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