



FE990B Family

Hardware Design Guide

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Contents

1	Applicability Table.....	6
2	Introduction.....	7
2.1	Scope	7
2.2	Audience	7
2.3	Contact Information, Support	7
2.4	Conventions	7
2.5	Terms and Conditions	8
2.6	Disclaimer	8
3	General Product Description.....	9
3.1	Overview	9
3.2	Product Variants and Frequency Bands	9
3.3	Main Features	9
3.4	Mechanical Specifications	11
3.4.1	Dimensions	11
3.4.2	Weight	11
3.4.3	Coplanarity	11
3.5	Temperature Range	11
4	Pins Allocation.....	12
4.1	Pin-out	12
4.2	LGA Pads Layout	27
5	Power Supply	28
5.1	Power Supply Requirements	28
5.2	Power Consumption	28
5.2.1	Idle/Operation Mode	28
5.3	General Design Rule	29
5.3.1	Electrical Design Guidelines	30
5.3.2	+5V Source Power Supply Design Guidelines	30
5.3.3	+12V Source Power Supply Design Guidelines	30
5.3.4	Thermal Design Guidelines	31
5.3.5	Power Supply PCB Layout Guidelines	31
5.4	VAUX Power Output	32
5.5	RTC – Real Time Clock	32
6	Digital Section	33
6.1	Logic Levels	33
6.2	Power On	34
6.2.1	Initialization and Activation State	34
6.2.2	AUTO_ON_N	37
6.3	Power Off	37
6.3.1	Shutdown via Software Command	37
6.3.2	Hardware Shutdown	38
6.3.3	Unconditional Hardware Shutdown	39
6.3.4	RESET_N Function	40
6.4	Powering OFF the Module	40
6.5	Fast Power Down	40
6.5.1	Fast Shut Down by Hardware	41
6.5.2	Fast Shutdown by Software	41

6.6	Communication Ports	42
6.6.1	USB	42
6.6.1.1	USB Layout Guidelines	43
6.6.2	PCIe	44
6.6.2.1	PCIe Layout Guidelines	49
6.6.2.2	Host Interface Switch Function	51
6.6.3	SIM	52
6.6.3.1	SIM Schematic Example	53
6.6.3.2	eSIM	53
6.6.4	UART	53
6.6.4.1	RS232 Level Translation	55
6.6.5	USXGMII	57
6.6.5.1	Ethernet Layout Guidelines	59
6.7	Peripheral Ports	61
6.7.1	SPI	61
6.7.2	I2C	62
6.7.3	SDC/eMMC 5.1	62
6.7.3.1	SDC/eMMC 5.1 Layout Guidelines	65
6.7.4	I2S/PCM	66
6.7.4.1	I2S Digital Audio Diagram	68
6.7.4.2	PCM Digital Audio Diagram	68
6.8	General Purpose I/O	69
6.8.1	Using a GPIO pad as Input	70
6.8.2	Using a GPIO as Output	70
6.9	Miscellaneous Functions	70
6.9.1	DPR	70
6.9.2	LED	70
6.9.3	ADC Converter	71
6.9.3.1	Using the ADC	71
6.9.4	DAC Converter (TBD)	71
6.9.4.1	Enabling DAC	72
6.9.4.2	Low Pass Filter Example	72
6.10	Forced USB Boot	72
6.11	VAUX Power Output	73
6.12	Temperature Monitor Function	73
7	RF Section.....	74
7.1	Frequency Bands	74
7.2	CA/MIMO/EN-DC (TBD)	76
7.3	RF Performance	77
7.3.1	Conducted Transmit Output Power	77
7.3.2	Conducted Receiver Sensitivity	77
7.4	Antenna Interface	80
7.4.1	Antenna Configuration	80
7.5	Antenna Requirements	83
7.5.1	Antenna Connection	84
7.5.2	PCB Guidelines in Case of FCC Certification	84
7.5.2.1	Transmission Line Design	84
7.5.3	Antenna Installation Guidelines	85
7.6	GNSS Receiver	85

7.6.1	GNSS RF Front End Design	86
7.7	GNSS Characteristics	86
8	Mechanical Design.....	88
8.1	General	88
8.2	Drawing	88
9	Application PCB Design.....	89
9.1	Recommended Footprint for the Application	89
9.2	PCB Pad Design	90
9.3	Recommendations for PCB Pad Dimensions	90
9.4	Cleaning	91
9.5	Stencil	91
9.6	Solder Paste	91
9.7	Solder Reflow	91
10	Application Guide.....	93
10.1	Debug of the FE990B Module in Production	93
10.2	Bypass Capacitor on Power Supplies	93
10.3	EMC Recommendations	93
11	Packaging.....	95
11.1	Tray	95
11.2	Moisture Sensitivity	96
12	Conformity Assessment Issues.....	97
12.1	Approvals Compliance Summary	97
12.2	Americas Approvals	97
12.2.1	USA FCC	97
12.2.1.1	FCC Certificates	97
12.2.1.2	Applicable FCC Rules	97
12.2.1.3	FCC Regulatory Notices	98
12.2.1.4	FCC Antenna Info	99
12.2.2	Canada ISED	101
12.2.2.1	ISED Database	101
12.2.2.2	Applicable ISED Rules	102
12.2.2.3	ISED Regulatory Notices	102
12.2.3	Brazil ANATEL	105
12.2.3.1	ANATEL Regulatory Notices	105
12.3	APAC Approvals	105
12.3.1	Japan Approvals	105
12.3.2	JRL/JTBL Regulatory Notices	106
12.3.3	Taiwan NCC	106
12.3.3.1	NCC Regulatory Notices	106
12.4	EMEA Approvals	106
12.4.1	EU RED	106
12.4.1.1	EU Declaration of Conformity	106
12.4.1.2	RED Antennas	106
12.4.2	UK UKCA	108
12.4.2.1	UKCA Declaration of Conformity	108
12.5	RoHS and REACH Info	108
12.5.1	RoHS Info	108
12.5.2	REACH Info	108

13	Acronyms and Abbreviations.....	109
14	Related Documents	110
15	Document History	111



1 Applicability Table

Table 1: Applicability Table

Products
FE990B40-RW(D)
FE990B40-NA(D)
FE990B34-RW(D)
FE990B34-NA(D)

- Note:** The applied MCP varies depending on the Hardware version.
- HW1.00: 8G+8G MCP Memory
 - HW1.10: 16G+16G MCP Memory



2 Introduction

2.1 Scope

This document introduces the Telit FE990B Family module and presents possible and recommended hardware solutions for the development of a product based on this module. All the features and solutions described in this document applies to all FE990B Family variants listed in the applicability table.

This document cannot include every hardware solution or every product that can be designed. Where the suggested hardware configurations are not to be considered mandatory, the information provided should be used as a guide and starting point for the proper development of the product with the Telit FE990B Family module.

2.2 Audience

This document is intended for system integrators using the Telit FE99B module in their products.

2.3 Contact Information, Support

For technical support and general questions, e-mail:

- TS-EMEA@telit.com
- TS-AMERICAS@telit.com
- TS-APAC@telit.com
- TS-SRD@telit.com
- TS-ONEEDGE@telit.com

Alternatively, use: <https://www.telit.com/contact-us/>

For product information and technical documents, visit: <https://www.telit.com>

2.4 Conventions

Note: Provide advice and suggestions that may be useful when integrating the module.

Danger: This information MUST be followed, or catastrophic equipment failure or personal injury may occur.

Warning: Alerts the user on important steps about the module integration.

All dates are in ISO 8601 format, that is YYYY-MM-DD.

2.5 Terms and Conditions

Refer to <https://www.telit.com/terms-conditions/>.

2.6 Disclaimer

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3 General Product Description

3.1 Overview

This document presents the possible and recommended hardware solutions useful for developing a product with the Telit FE990B Family module.

The FE990B Family is an LGA module designed for applications such as M2M and industrial IoT device platforms, supporting the following technologies:

- 5G sub-6/4G/3G networks for data communication
- Industrial-grade quality design

The module functions as a front-end for mobile products, providing mobile communication capabilities to an external host CPU through its extensive interfaces. Additionally, its robust CPU and interfaces enable the implementation of customer applications without needing an external CPU, thereby optimizing both cost and power consumption.

3.2 Product Variants and Frequency Bands

Operating frequencies in 5G, LTE, and WCDMA modes conform to 3GPP specifications. The table below lists the FE990B operating frequencies on 5G, LTE, and WCDMA modes.

Table 2: Product Variants and their Frequency Bands

Product	WCDMA	LTE	5G	VoLTE	Region
FE990B40-RW(D) FE990B34-RW(D)	B1, B5, B6, B8, B19	B1, B3, B5, B7, B8, B18, B19, B20, B28, B32, B38, B40, B41, B42, B43, B68	n1, n3, n5, n7, n8, n20, n28, n38, n40, n41, n75, n76(TBD), n77, n78, n79	Y	East Asia
FE990B40-NA(D) FE990B34-NA(D)	-	B2, B4, B5, B7, B12, B13, B14, B17, B25, B26, B29, B30, B38, B41, B42, B43, B48, B66, B71	n2, n5, n7, n12, n13, n14, n25, n26, n29, n30, n38, n41, n48, n66, n70, n71, n77, n78	Y	North America

For more details information about frequencies and bands, refer to the RF Section.

Note: Cellular technologies and enabled frequency bands may vary based on the firmware version and configuration used.
FE990B40/B34-NAD product is Data only product without a Voice feature.

3.3 Main Features

Table 3: Functional Features

Function	Features
Modem	• Multi-RAT cellular modem for data communication • 5G: FR1 (Sub-6), Rel 17 - FE990B40 NSA up to 4.9 Gbps on DL, 0.55 Gbps on UL SA up to 4.1 Gbps on DL, 0.90 Gbps on UL - FE990B34 NSA up to 3.6 Gbps on DL, 0.55 Gbps on UL

Function	Features
	SA up to 2.8 Gbps on DL, 0.90 Gbps on UL 4G: CAT 20 (2.0 Gbps) on DL, CAT 18 (210 Mbps) on UL, Rel 17 3G: HSPA+ Rel 8 up to 42/11 Mbps in DL/UL
Support Bands	5G: n1/n2/n3/n5/n7/n8/n12/n13/n14/n20/n25/n26/n28/n29(SDL)/n30/n38/n40/n41/n48/n66/n70/n71/n75/n77/n78/n79 4G: B1/B2/B3/B4/B5/B7/B8/B12/B13/B14/B17/B18/B19/B20/B25/B26/B28/B29(SDL)/B30/B32(SDL)/B38/B40/B41/B42/B43/B48/B66/B68/B71 3G: B1/B5/B6/B19/B8
1Tx/4Rx(4x4 DL MIMO)	5G: Operating bands 4G: Operating bands
2Tx(2x2 UL MIMO)/4Rx (4x4 DL MIMO)	5G - NA: n2/n5/n7/n25/n30/n38/n41/n48/n66/n70/n71/n77/n78 - RW: n1/n3/n5/n7/n8/n28/n38/n40/n41/n77/n78/n79
1Tx/1Rx (2nd Rx Diversity)	4G: Operating bands 3G: Operating bands
GNSS	- Dual frequency GNSS - Upper L-band: GPS/Glonass/Beidou/Galileo/SBAS - Lower L-band: GPS/Galileo
USIM – Dual Voltage	- Two SIM supports - UIM1 – Class B and Class C support - UIM2 – Class C (UIM2 also can be assigned as optional eSIM)
Application processor	Application processor to run customer application code - Quad-core Arm Cortex A55 processor at up to 2.2 GHz running the Linux operating system. 8Gbit NAND Flash + 8Gbit LPDDR4x 2133 MHz MCP is supported, 16Gbit + 16 Gbit LPDDR4x 2133 MHz MCP is also supported
Interfaces	- PCIe x 3; PCIe0 (Gen 4, 1L or Gen 3, 2L), PCIe1 (Gen 3, 2L), PCIe2 (Gen3, 1L) - USB 3.1 Gen 2 2x USXGMII for Ethernet MAC - USIM x 2 (only USIM1 is supported dual voltage) - UART - SPI - I2C x 2 - I2S - SDC, SDIO 6 GPIOs
Antenna Connection	4 Cellular/GNSS antenna ports 1 Dedicated GNSS antenna port
Operating Temperature	- Operating temperature range: - 40 deg C ~ + 85 deg C - Storage Temperature range: - 40 ~ +85 deg C
Operating Humidity	≤95%, non-condensing

3.4 Mechanical Specifications

3.4.1 Dimensions

The overall dimensions of the FE990B family are:

- Length: 41 mm
- Width: 41 mm
- Thickness: 2.9 mm

3.4.2 Weight

The nominal weight of the FE990B40-RW is 12.5 grams.

3.4.3 Coplanarity

The coplanarity is 0.12 mm.

3.5 Temperature Range

Table 4: Temperature Range

Mode	Temperature	Note
Operating Temperature Range	-20°C ~ +55°C	The module is fully functional(*) in all temperature ranges and it fully meets the 3GPP specifications.
	-40°C ~ +85°C	The module is fully functional (*) in all temperature ranges, but might slightly deviate from the 3GPP specifications.
Storage and Non-Operating Temperature Range	-40°C ~ +85°C	The module is not powered and not connected to the power supply

Note: (*) Functional: if applicable, the module can make and receive voice calls, and data calls, send and receive SMS, and handle data traffic.

Note: EU RED compliance from -30°C to +75°C



4 Pins Allocation

4.1 Pin-out

Table 5: USB Communication Port (Firmware upgrade and Data)

Pin	Signal	I/O	Function	Type	Comment
USB Communication Port (Firmware upgrade and Data)					
AC47	USB_DP	I/O	USB differential Data (+)	Analog	Float if USB 2.0 is unused.
AD45	USB_DM	I/O	USB differential Data (-)	Analog	
V45	USB_ID	I	USB ID	1.2 V	Used for USB OTG to determine host or client mode.
AE47	USB_VBUS	I	Enable the pin for the internal USB transceiver. (not for power supply) USB connection detect	Vmax: 5.5 V Vnom: 5.0 V VIH: Min. 1.3 V VIL: Max. 0.85 V	Detection threshold (USB presence is detected) VIH: Min.1.3 V. Detection threshold (USB presence is not detected) VIL: Max. 0.85 V
AF45	USB_VBUS				
Y47	USB_SS_TX_P	O	USB 3.1 super-speed transmit - Plus	Analog Output	Float if USB 3.1 is unused.
Z45	USB_SS_TX_M	O	USB 3.1 super-speed transmit - Minus	Analog Output	
W47	USB_SS_RX_P	I	USB 3.1 super-speed receive - Plus	Analog Input	
X45	USB_SS_RX_M	I	USB 3.1 super-speed receive - Minus	Analog Input	

Table 6: PCIe Communication Port

Pin	Signal	I/O	Function	Type	Comment
PCIe Communication Port					
X49	PCIE0_CLKREQ_N	OD	PCIe0 reference clock request signal	OD	Internal PU (4.7 K) Input: Master Output: Slave
Z49	PCIE0_RST_N	I/O	PCIe0 reset	I/O	Input: Slave Output: Master
T49	PCIE0_WAKE_N	OD	PCIe0 wake up	OD	Internal PU (4.7 K) Input: Master Output: Slave
V51	PCIE0_REFCLK_P	I/O	PCIe0 differential reference clock - Plus	Analog Input/Output	Float if PCIe0 is unused.

Pin	Signal	I/O	Function	Type	Comment
W50	PCIE0_REFCLK_M	I/O	PCIE0 differential reference clock - Minus	Analog Input/Output	Connected during one lane operation.
R51	PCIE0_TX0_P	O	PCIE0 transmit 0 - Plus	Analog Output	Float all signals if PCIE0 is unused. If using only one lane, connect PCIE0_TX0_M/P and float PCIE0_TX1_M/P.
S50	PCIE0_TX0_M	O	PCIE0 transmit 0 - Minus	Analog Output	
T51	PCIE0_TX1_P	O	PCIE0 transmit 1 - Plus	Analog Output	
U50	PCIE0_TX1_M	O	PCIE0 transmit 1 - Minus	Analog Output	
X51	PCIE0_RX0_P	I	PCIE0 receive 0 - Plus	Analog Input	Float all signals if PCIE 0 is unused. If using only one lane, connect PCIE0_RX0_M/P and float PCIE0_RX1_M/P.
Y50	PCIE0_RX0_M	I	PCIE0 receive 0 - Minus	Analog Input	
Z51	PCIE0_RX1_P	I	PCIE0 receive 1 - Plus	Analog Input	
AA50	PCIE0_RX1_M	I	PCIE0 receive 1 - Minus	Analog Input	
AH49	PCIE1_CLKREQ_N	I	PCIE1 reference clock request signal	DI	Internal PU (4.7 K) RC only
AK49	PCIE1_RST_N	O	PCIE1 reset	DO	RC only
AD49	PCIE1_WAKE_N	I	PCIE1 wake up	DI	Internal PU (4.7 K) RC only
AH51	PCIE1_REFCLK_P	I/O	PCIE1 differential reference clock - Plus	Analog Input/Output	Float if PCIE1 is unused. Connected during one lane operation.
AJ50	PCIE1_REFCLK_M	I/O	PCIE1 differential reference clock - Minus	Analog Input/Output	
AD51	PCIE1_TX0_P	O	PCIE1 transmit 0 - Plus	Analog Output	Float all signals if PCIE1 is unused. If using only one lane, connect PCIE1_TX0_M/P and float PCIE1_TX1_M/P.
AE50	PCIE1_TX0_M	O	PCIE1 transmit 0 - Minus	Analog Output	
AF51	PCIE1_TX1_P	O	PCIE1 transmit 1 - Plus	Analog Output	
AG50	PCIE1_TX1_M	O	PCIE1 transmit 1 - Minus	Analog Output	
AK51	PCIE1_RX0_P	I	PCIE1 receive 0 - Plus	Analog Input	Float all signals if PCIE1 is unused. If using only one lane, connect PCIE1_RX0_M/P and float PCIE1_RX1_M/P.
AL50	PCIE1_RX0_M	I	PCIE1 receive 0 - Minus	Analog Input	
AM51	PCIE1_RX1_P	I	PCIE1 receive 1 - Plus	Analog Input	
AN50	PCIE1_RX1_M	I	PCIE1 receive 1 - Minus	Analog Input	
AU49	PCIE2_CLKREQ_N	I	PCIE2 reference clock request signal	DI	Internal PU (4.7 K) RC only
AW49	PCIE2_RST_N	O	PCIE2 reset	DO	RC only
AP49	PCIE2_WAKE_N	I	PCIE2 wake up	DI	Internal PU (4.7 K) RC only
AU51	PCIE2_REFCLK_P	I/O	PCIE2 reference clock request signal - Plus	Analog Input/Output	Float all signals if PCIE2 is unused.

Pin	Signal	I/O	Function	Type	Comment
AV50	PCIE2_REFCLK_M	I/O	PCIe2 differential reference clock - Minus	Analog Input/Output	
AX50	PCIE2_RX0_M	I	PCIe2 receive 0 - Minus	Analog Input	
AW51	PCIE2_RX0_P	I	PCIe2 receive 0 - Plus	Analog Input	
AT50	PCIE2_TX0_M	O	PCIe2 transmit 0 - Minus	Analog Output	
AS51	PCIE2_TX0_P	O	PCIe2 transmit 0 - Plus	Analog Output	

Table 7: SIM Card 1 Interface

Pin	Signal	I/O	Function	Type	Comment
SIM Card 1 Interface					
BE17	UIM1_VCC	-	Power supply for the SIM 1	1.8/2.95 V	
BD18	UIM1_IO	O	SIM 1 Data I/O	1.8/2.95 V	
BC19	UIM1_DET	I	SIM 1 presence detection	1.8V	
BD20	UIM1_RST	O	SIM 1 reset	1.8/2.95 V	
BE19	UIM1_CLK	O	SIM 1 clock	1.8/2.95 V	

Table 8: SIM Card 2 Interface

Pin	Signal	I/O	Function	Type	Comment
SIM Card 2 Interface					
BE13	UIM2_VCC	-	Power supply for the SIM 2	1.8 V	
BD14	UIM2_IO	O	SIM 2 Data I/O	1.8 V	
BC17	UIM2_DET	I	SIM 2 presence detection	1.8 V	
BD16	UIM2_RST	O	SIM 2 reset	1.8 V	
BE15	UIM2_CLK	O	SIM 2 clock	1.8 V	
BC15	RFU	-	-	-	

Table 9: SPI

Pin	Signal	I/O	Function	Type	Comment
SPI					
M5	SPI_CLK	O	SPI Clock output	1.8V	
K5	SPI_CS_N	O	SPI Chip select output	1.8V	
N7	SPI_MISO	I	SPI data Master Input Slave Output	1.8V	
L7	SPI_MOSI	O	SPI data Master Output Slave Input	1.8V	

Table 10: GPIO

Pin	Signal	I/O	Function	Type	Comment
General Purpose Input Output					
X3	TGPIO1	I/O	General Purpose I/O	1.8V	
Y5	TGPIO2	I/O	General Purpose I/O	1.8V	
X7	TGPIO3	I/O	General Purpose I/O	1.8V	
BD12	TGPIO4	I/O	General Purpose I/O	1.8V	
BC13	TGPIO5	I/O	General Purpose I/O	1.8V	
BA16	TGPIO6	I/O	General Purpose I/O	1.8V	

Table 11: ADC

Pin	Signal	I/O	Function	Type	Comment
ADC					
E34	ADC1	A/I	Analog Digital Converter 1 Input	Analog Input	
E36	ADC2	A/I	Analog Digital Converter 2 Input	Analog Input	

Table 12: DAC

Pin	Signal	I/O	Function	Type	Comment
DAC					
C39	DAC_OUT	DO	Digital to analog converter	Output	TBD

Table 13: RF Section

Pin	Signal	I/O	Function	Type	Comment
RF Section					
AU1	ANT0	AIO	Antenna interface: 5G NR LTE	RF	Impedance: 50 ohm
AK1	ANT1	AIO	Antenna interface: 5G NR GNSS	RF	Impedance: 50 ohm
AB1	ANT2	AI	Antenna interface: 5G NR LTE	RF	Impedance: 50 ohm
T1	ANT3	AIO	Antenna interface: 5G NR LTE	RF	Impedance: 50 ohm

Table 14: GNSS Section

Pin	Signal	I/O	Function	Type	Comment
GNSS Section					
J1	ANT4	AI	GNSS	RF	Impedance: 50 ohm

Table 15: Ant control

Pin	Signal	I/O	Function	Type	Comment
Tuner					
G35	RFFE0_DATA	I/O	External antenna tuner control 0 – Data	1.2 V	
G37	RFFE0_CLK	O	External antenna tuner control 0 – Clock	1.2 V	
G39	RFFE1_DATA	I/O	External antenna tuner control 1 – Data	1.2 V	
G41	RFFE1_CLK	O	External antenna tuner control 1 – Clock	1.2 V	

Table 16: Miscellaneous Functions

Pin	Signal	I/O	Function	Type	Comment
Miscellaneous Functions					
A41	ON_OFF_N	I	Power On/Off	0.7 V	Active low
B42	RESET_N	I	Reset	1.2 V	Active low
B44	SHDN_N	I	Shutdown	1.2 V	Active low
AA47	USB_BOOT	I	Forced USB BOOT – emergency download	1.8 V	
C43	SW_RDY	O	Indicates that the boot sequence was completed successfully	1.8 V	
C41	AUTO_ON_N	I	Power On automatically	1.8 V	Active low
A45	LED_N	O	Network status LED	1.8 V	Active low/Open drain
A43	USB_PCIE_SWITCH	I	PCIe/USB interface switch	1.8 V	Default: Low Low: PCIe High: USB
E40	PWM	O	Pulse Width Modulation	1.8 V	TBD
E38	DPR	I	Dynamic Power Reduction	1.8 V	
BA12	VAUX/PWRMON	O	Supply output for external accessories/Power ON monitor	1.8 V	
AY13	VDD_IO	O	IO voltage for internal ICs This power rail is always on while FE990Bxx is working.	1.8 V	
C37	5G_GNSS_SYNC_PULSE	O	GNSS synchronization pulse signal	1.8 V	

Table 17: Debug UART

Pin	Signal	I/O	Function	Type	Comment
DBG UART					
BA10	DEBUG_UART_TX	O	Debug UART transmit	1.8 V	
AY11	DEBUG_UART_RX	I	Debug UART receive	1.8 V	

Table 18: Main UART

Pin	Signal	I/O	Function	Type	Comment
Main UART					
G13	UART1_TX	I	UART1 transmit	1.8 V	
E12	UART1_RX	O	UART1 receive	1.8 V	
C13	UART1_CTS	O	UART1 Clear to Send (CTS)	1.8 V	
E14	UART1_RTS	I	UART1 Request to Send (RTS)	1.8 V	
C9	UART1_DTR	I	UART Input for Data terminal ready (DTR)	1.8 V	
C11	UART1_DCD	O	UART Output for Data Carrier Detect (DCD)	1.8 V	
E10	UART1_DSR	O	UART Output for Data Set Ready (DSR)	1.8 V	

Pin	Signal	I/O	Function	Type	Comment
G11	UART1_RI	O	UART Output for Ring Indication (RI)	1.8 V	

Table 19: Coexistence UART

Pin	Signal	I/O	Function	Type	Comment
COEX UART					
G25	COEX_UART_RX	I	Coexistence UART receive	1.8 V	
E26	COEX_UART_TX	O	Coexistence UART transmit	1.8 V	

Table 20: I2S

Pin	Signal	I/O	Function	Type	Comment
I2S					
AF7	I2S_D0	O	I2S Data Input	1.8 V	
AE5	I2S_D1	I	I2S Data Output	1.8 V	
AD7	I2S_SCK	I/O	I2S clock	1.8 V	
AC5	I2S_WS	I/O	I2S word select	1.8 V	

Table 21: I2C

Pin	Signal	I/O	Function	Type	Comment
I2C					
T7	I2C1_SCL	OD	I2C1 serial clock	1.8V	Internal PU (2.2 K)
S5	I2C1_SDA	OD	I2C1 serial data	1.8V	Internal PU (2.2 K)
R7	I2C2_SCL	OD	I2C2 serial clock	1.8V	Internal PU (2.2 K)
P5	I2C2_SDA	OD	I2C2 serial data	1.8V	Internal PU (2.2 K)

Table 22: Bluetooth UART (TBD)

Pin	Signal	I/O	Function	Type	Comment
BT UART					
G17	BT_UART_TXD	I	Bluetooth UART Output for Transmit	1.8 V	
E16	BT_UART_RXD	O	Bluetooth UART Input for Receive	1.8 V	
G19	BT_UART_CTS_N	O	Bluetooth UART Output for Clear to Send	1.8 V	
E18	BT_UART_RTS_N	I	Bluetooth UART Input for Request to Send	1.8 V	

Table 23: Bluetooth I2S (TBD)

Pin	Signal	I/O	Function	Type	Comment
BT I2S					
AH3	BT_EN	O	Bluetooth enable	1.8 V	
C23	BT_I2S_WS	I/O	Bluetooth I2S word select	1.8	
E22	BT_I2S_D0	O	Bluetooth I2S DATA Input	1.8	
C21	BT_I2S_D1	I	Bluetooth I2S DATA Output	1.8	
E24	BT_I2S_SCK	I/O	Bluetooth I2S continuous serial clock	1.8	

Table 24: SD Card/eMMC

Pin	Signal	I/O	Function	Type	Comment
SDC/eMMC					
N49	SDC_CLK	O	Secure digital controller clock	1.8 V	If unused, keep it open.
M50	SDC_CMD	I/O	Secure digital controller command	1.8 V	If unused, keep it open.
G51	SDC_DATA_0	I/O	Secure digital controller data bit 0	1.8 V	If unused, keep it open.
H50	SDC_DATA_1	I/O	Secure digital controller data bit 1	1.8 V	If unused, keep it open.
J51	SDC_DATA_2	I/O	Secure digital controller data bit 2	1.8 V	If unused, keep it open.
K50	SDC_DATA_3	I/O	Secure digital controller data bit 3	1.8 V	If unused, keep it open.
N45	SDC_DET	I	SD card detect	1.8 V	Internal PU (470 K)
P47	SDC_VSEL	O	Selects the voltage of the LDO that powers the VCCB pin of the SD card level shifter	1.8 V	If unused, keep it open.
R45	SDC_VDD	I	Power supply for SD/MMC card	1.8 V	2.95 V needs an external Level shifter. If unused, connect to VDD_IO
L51	SDC_RCLK	I	SDC return clock	1.8 V	If unused, keep it open.
L45	SDC_PWR_EN	O	SDC power enable	1.8 V	
J49	SDC_DATA4	I/O	Secure digital controller data bit 4	1.8 V	If unused, keep it open.
K47	SDC_DATA5	I/O	Secure digital controller data bit 5	1.8 V	If unused, keep it open.
L49	SDC_DATA6	I/O	Secure digital controller data bit 6	1.8 V	If unused, keep it open.
M47	SDC_DATA7	I/O	Secure digital controller data bit 7	1.8 V	If unused, keep it open.
BD10	RESOUT_N	O	Reset out for eMMC	1.8 V	Do not install pull-up/down resistor

Table 25: WLAN

Pin	Signal	I/O	Function	Type	Comment
WLAN					
AS45	WLAN_CLK	AO	76.8 MHz WLAN clock output		
AM45	WLAN_SLEEP_CLK	AO	32.768 kHz sleep clock output	1.8 V	
AR5	2G_WLAN_DIS/WLAN_EN	O	WLAN 2 GHz disable (QFW)/WLAN enable (WCN)	1.8 V	
AP7	2G_PWR_EN/WCN_SW_CTRL_WLAN	O	WLAN 2 GHz power enable (QFW)/Input from WCN785x to switch between active and sleep mode for WLAN	1.8 V	
AT5	5G_WLAN_DIS	O	WLAN 5 GHz disable (QFW)	1.8 V	
AS7	5G_PWR_EN	O	WLAN 5 GHz power enable (QFW)	1.8 V	
AV5	6G_WLAN_DIS/WCN_SW_CTRL	O	WLAN 6 GHz disable (QFW)/Input from WCN785x to switch between active and sleep modes for Bluetooth.	1.8 V	
AU7	6G_PWR_EN	O	WLAN 6 GHz power enable	1.8 V	
AN5	LAA_AS_EN	O	GPIO allows SDR to power on the WCN785x AON domain. Control logic in the WCN785x AON domain allows SDX to control 5/6 GHz xLNA (LNA in FEMs).	1.2 V	When WCN785x is sleeping or disabled
AY3	WCN_DEV_SOL	I	Sign of life (SOL) signal coming from WCN to SDX	1.2 V	TBD
AW3	WCN_HOST_SOL	O	Sign of life (SOL) signal sent from SDX to WCN	1.2 V	TBD
AJ5	LAA_RX	O	Toggle xFEMs to high gain (logic high) or high isolation (logic low)	1.2 V	When WCN785x is sleeping or disabled
AL5	PA_MUTING	O	GPIO that informs WCN785x if SPDT has been toggled to LTE; if high, WCN785x will not enable 2.4 GHz chain1 Tx	1.2 V	
AS3	SDX_TO_HST_CTL	O	Indicate FE990Bxx SSR (Subsystem Reset) to host	1.8 V	Enable/Disable by AT#PCIEGPIOSSR command
AU3	HST_TO_SDH_CTL	I	Indicate host SSR (Subsystem Reset) to FE990Bxx	1.8 V	
AP3	E911	O	Indicate FE990Bxx-RW state to host	1.8 V	
AK7	HST_WL_TX_EN_TON79	O	Output to N79.		FE990Bxx-RW only

Pin	Signal	I/O	Function	Type	Comment
			When this signal goes high, SDR disables N79 and puts N79 LNA in isolation mode.		
AM7	N79_TX_EN_TO_WLAN	I	Input from N79. Wi-Fi puts its LNA in isolation mode when this signal is high and frequency.		FE990Bxx-RW only
BA18	SP2T_XOR	-	N46/B46 SP2T Switch GRFC	1.2 V	TBD

Table 26: Ethernet MAC

Pin	Signal	I/O	Function	Type	Comment
USXGMII					
BA30	USXGMII_0_CLK	O	MDIO Interface Clock for ETH0 PHY		
AY33	USXGMII_0_INT_N	I	Interrupts input from Ethernet PHY 0		
BE33	USXGMII_0_RX_P	I	USXGMII 0 receive – plus	AI	Float all signals if USXGMII is unused.
BD34	USXGMII_0_RX_M	I	USXGMII 0 receive – minus	AI	
BE31	USXGMII_0_TX_P	O	USXGMII 0 transmit – plus	AO	
BD32	USXGMII_0_TX_M	O	USXGMII 0 transmit – plus	AO	
AY31	USXGMII_0_RST_N	O	Reset for ETH0 PHY		
BA32	USXGMII_0_DATA	I/O	MDIO data for ETH0 PHY		
BA34	USXGMII_1_CLK	O	MDIO Interface Clock for ETH1 PHY		
AY37	USXGMII_1_INT_N	I	Interrupts input from Ethernet PHY 1		
BE37	USXGMII_1_RX_P	I	USXGMII 1 receive – plus	AI	Float all signals if USXGMII is unused.
BD38	USXGMII_1_RX_M	I	USXGMII 1 receive – minus	AI	
BE35	USXGMII_1_TX_P	O	USXGMII 1 transmit – plus	AO	
BD36	USXGMII_1_TX_M	O	USXGMII 1 transmit – plus	AO	
AY35	USXGMII_1_RST_N	O	Reset for ETH1 PHY		
BA36	USXGMII_1_DATA	I/O	MDIO data for ETH1 PHY		
BC31	ETH0_PWR_EN	O	Enables the power regulators for ethernet PHY 0	1.8 V	Ethernet PHY Control
BC35	ETH1_PWR_EN	O	Enables the power regulators for ethernet PHY 1	1.8 V	Ethernet PHY Control
BA38	PPS_ETH_PHY	O	Pulse per second (PPS) signal for Ethernet PHY	1.8 V	

Table 27: Power Supply

Pin	Signal	I/O	Function	Type	Comment
Power Supply					
BD42	VPH_PWR	I	Power supply	Power	
BE47	VPH_PWR	I	Power supply	Power	
BD46	VPH_PWR	I	Power supply	Power	

Pin	Signal	I/O	Function	Type	Comment
BD44	VPH_PWR	I	Power supply	Power	
BE45	VPH_PWR	I	Power supply	Power	
BE43	VPH_PWR	I	Power supply	Power	
BD28	VPH_PWR_PA	I	Power supply (RF Section)	Power	
BD26	VPH_PWR_PA	I	Power supply (RF Section)	Power	
BE27	VPH_PWR_PA	I	Power supply (RF Section)	Power	
BD24	VPH_PWR_PA	I	Power supply (RF Section)	Power	
BE25	VPH_PWR_PA	I	Power supply (RF Section)	Power	
BE23	VPH_PWR_PA	I	Power supply (RF Section)	Power	
BD22	VPH_PWR_PA	I	Power supply (RF Section)	Power	
BA42	AUX_PWR2	O	Auxiliary power supply 0.9V from PMIC This Power rail is always on while FE990B is working.	Power	Power supply for Wi-fi/BT
AY41	AUX_PWR1	O	Auxiliary power supply 1.2V from PMIC This Power rail is always on while FE990B is working.	Power	Power supply for Wi-fi/BT
BD40	AUX_PWR2	O	Auxiliary power supply 0.9V from PMIC This Power rail is always on while FE990B is working.	Power	Power supply for Wi-fi/BT
BA40	AUX_PWR3	O	Auxiliary power supply 1.9V from PMIC This Power rail is always on while FE990B is working.	Power	Power supply for Wi-fi/BT

Table 28: SFP+

Pin	Signal	I/O	Function	Type	Comment
SFP+					
AY19	SFP_PWR_EN	O	SFP module power enable	1.8 V	Not Supported
AY25	SFP_TX_FAULT	O	SFP TX FAULT	1.8 V	Not Supported
BA24	SFP_RS0	I	SFP Rate Select 0	1.8 V	Not Supported
BA22	SFP_RS1	I	SFP Rate Select 1	1.8 V	Not Supported
AY23	SFP_RX_LOS	O	SFP RX_Loss of Signal	1.8 V	Not Supported
AY21	SFP_TX_DIS	O	SFP module TX disable, turns off transmitter laser output	1.8 V	Not Supported
BA20	SFP_MOD_ABS	-	SFP module definition, Module Absent	1.8 V	Not Supported

Table 29: GND

Pin	Signal	I/O	Function	Type	Comment
GND					
AG47	GND	-	Ground		
AB45	GND	-	Ground		

Pin	Signal	I/O	Function	Type	Comment
AR50	GND	-	Ground		
AP51	GND	-	Ground		
BD30	GND	-	Ground		
E42	GND	-	Ground		
BC21	GND	-	Ground		
BC25	GND	-	Ground		
BE29	GND	-	Ground		
BC27	GND	-	Ground		
AE2	GND	-	Ground		
C19	GND	-	Ground		
P2	GND	-	Ground		
B30	GND	-	Ground		
M2	GND	-	Ground		
N3	GND	-	Ground		
AN2	GND	-	Ground		
AZ2	GND	-	Ground		
AX2	GND	-	Ground		
AR2	GND	-	Ground		
AY51	GND	-	Ground		
AZ50	GND	-	Ground		
BA51	GND	-	Ground		
BC39	GND	-	Ground		
AH7	GND	-	Ground		
G21	GND	-	Ground		
BE41	GND	-	Ground		
W2	GND	-	Ground		
Y2	GND	-	Ground		
AG2	GND	-	Ground		
E20	GND	-	Ground		
AB51	GND	-	Ground		
AC50	GND	-	Ground		
B18	GND	-	Ground		
B36	GND	-	Ground		
U5	GND	-	Ground		
V7	GND	-	Ground		
F2	GND	-	Ground		
B12	GND	-	Ground		
BC45	GND	-	Ground		
BE39	GND	-	Ground		
E1	GND	-	Ground		

Pin	Signal	I/O	Function	Type	Comment
G1	GND	-	Ground		
L1	GND	-	Ground		
N1	GND	-	Ground		
R1	GND	-	Ground		
V1	GND	-	Ground		
X1	GND	-	Ground		
Z1	GND	-	Ground		
AD1	GND	-	Ground		
AF1	GND	-	Ground		
AH1	GND	-	Ground		
AM1	GND	-	Ground		
AP1	GND	-	Ground		
AS1	GND	-	Ground		
AW1	GND	-	Ground		
AY1	GND	-	Ground		
W5	GND	-	Ground		
AB49	GND	-	Ground		
C33	GND	-	Ground		
BC41	GND	-	Ground		
E32	GND	-	Ground		
R49	GND	-	Ground		
H2	GND	-	Ground		
K2	GND	-	Ground		
S2	GND	-	Ground		
U2	GND	-	Ground		
AA2	GND	-	Ground		
AC2	GND	-	Ground		
AJ2	GND	-	Ground		
AL2	GND	-	Ground		
AT2	GND	-	Ground		
AV2	GND	-	Ground		
AF3	GND	-	Ground		
J3	GND	-	Ground		
T3	GND	-	Ground		
AB3	GND	-	Ground		
AK3	GND	-	Ground		
A5	GND	-	Ground		
A7	GND	-	Ground		
B8	GND	-	Ground		
B28	GND	-	Ground		

Pin	Signal	I/O	Function	Type	Comment
B10	GND	-	Ground		
A11	GND	-	Ground		
A13	GND	-	Ground		
A17	GND	-	Ground		
B16	GND	-	Ground		
B22	GND	-	Ground		
B14	GND	-	Ground		
A19	GND	-	Ground		
B20	GND	-	Ground		
A23	GND	-	Ground		
B24	GND	-	Ground		
E28	GND	-	Ground		
B26	GND	-	Ground		
A25	GND	-	Ground		
A29	GND	-	Ground		
N51	GND	-	Ground		
P50	GND	-	Ground		
E51	GND	-	Ground		
S47	GND	-	Ground		
T45	GND	-	Ground		
F50	GND	-	Ground		
V49	GND	-	Ground		
G49	GND	-	Ground		
AF49	GND	-	Ground		
AM49	GND	-	Ground		
BE11	GND	-	Ground		
BC29	GND	-	Ground		
AG5	GND	-	Ground		
A31	GND	-	Ground		
B32	GND	-	Ground		
B34	GND	-	Ground		
A35	GND	-	Ground		
BA1	GND	-	Ground		
A39	GND	-	Ground		
A37	GND	-	Ground		
BE21	GND	-	Ground		
AY39	GND	-	Ground		
BC23	GND	-	Ground		
C45	GND	-	Ground		
G31	GND	-	Ground		

Pin	Signal	I/O	Function	Type	Comment
AP45	GND	-	Ground		
AU45	GND	-	Ground		
AV47	GND	-	Ground		
AL47	GND	-	Ground		
AS49	GND	-	Ground		
AY15	GND	-	Ground		
BA14	GND	-	Ground		
BA26	GND	-	Ground		
AY27	GND	-	Ground		
1~60	GND	-	Center Ground		

Table 30: Reserved

Pin	Signal	I/O	Function	Type	Comment
Reserved					
A9	Reserved	-	Reserved		
A15	Reserved	-	Reserved		
A21	Reserved	-	Reserved		
A27	Reserved	-	Reserved		
A33	Reserved	-	Reserved		
AY49	Reserved	-	Reserved		
Z3	Reserved	-	Reserved		
AA5	Reserved	-	Reserved		
AB7	Reserved	-	Reserved		
Z7	Reserved	-	Reserved		
AD3	Reserved	-	Reserved		
B38	Reserved	-	Reserved		
B40	Reserved	-	Reserved		
C17	Reserved	-	Reserved		
G3	Reserved	-	Reserved		
B46	Reserved	-	Reserved		
L3	Reserved	-	Reserved		
V3	Reserved	-	Reserved		
A47	Reserved	-	Reserved		
BC43	Reserved	-	Reserved		
AN47	Reserved	-	Reserved		
AH45	Reserved	-	Reserved		
AJ47	Reserved	-	Reserved		
AK45	Reserved	-	Reserved		
AR47	Reserved	-	Reserved		
AT47	Reserved	-	Reserved		
G33	Reserved	-	Reserved		

Pin	Signal	I/O	Function	Type	Comment
G27	Reserved	-	Reserved		
BA28	Reserved	-	Reserved		
AY29	Reserved	-	Reserved		
AY17	Reserved	-	Reserved		
AM3	Reserved	-	Reserved		
C27	Reserved	-	Reserved		
C25	Reserved	-	Reserved		
R3	Reserved	-	Reserved		
BC33	Reserved	-	Reserved		
G23	Reserved	-	Reserved		
BC37	Reserved	-	Reserved		
G15	Reserved	-	Reserved		
C15	Reserved	-	Reserved		
C35	Reserved	-	Reserved		
U47	Reserved	-	Reserved		
C7	Reserved	-	Reserved		
B6	Reserved	-	Reserved		
A1	Reserved	-	Reserved		
C29	Reserved	-	Reserved		
C31	Reserved	-	Reserved		
G29	Reserved	-	Reserved		
E30	Reserved	-	Reserved		
BE5	Reserved	-	Reserved		
BC7	Reserved	-	Reserved		
BD6	Reserved	-	Reserved		
BD8	Reserved	-	Reserved		
BE7	Reserved	-	Reserved		
BE9	Reserved	-	Reserved		
BC9	Reserved	-	Reserved		
BC11	Reserved	-	Reserved		

Warning: Reserved pins must not be connected.

Top View

[illegible]

Figure 1: LGA Pads Layout

5 Power Supply

The power supply circuitry and the board layout are a very important part of the full product design and they strongly reflect on the product's overall performance, so the requirements and the guidelines that will follow should be read carefully for a proper design.

5.1 Power Supply Requirements

The external power supply must be connected to VBATT and VBATT_PA pads and must fulfill the following requirements:

Table 31: Power Supply Requirements

Power Supply	Value
Nominal Supply Voltage	3.8V
Operating Voltage Range	3.4 V - 4.2 V
Maximum ripple on the module input supply	30 mV
Peak current consumption*	3.8 V @ [3.5A]

*The peak current must be higher than the average current due to TDD bands and power class 3.

5.2 Power Consumption

5.2.1 Idle/Operation Mode

Table 32: Idle Mode

Mode	Measure (Typical)	Mode Description
IDLE mode		
AT+CFUN=1	30 mA	No call connection USB is connected to the host
Airplane mode		
AT+CFUN=4	14 mA	Disabled TX and RX; the module is not registered on the network USB is disconnected
Standby mode		
AT+CFUN=5	WCDMA	5.1 mA
	*RW variant	4.2 mA
	LTE	5.6 mA
		4.5 mA
	LTE CDRx	9.7 mA
		LTE FDD CDRx with 320 ms long CDRx cycle BW 20 MHz Standby with searched enabled Standby with idle DRx: 1.28 sec
NR Sub-6		6 mA
		5.1 mA

Mode		Measure (Typical)	Mode Description
		4.7 mA	NR Sub6 Idle 20 MHz Drx (2.56 sec)
	NR SA Sub-6	18 mA	NR SA Sub6 TDD 100 MHz CDRx: 160 ms

Table 33: Operating Mode

Mode	Measure* (Typical)	Mode Description
NR-NSA		
NSA mode 1CC+1FR1	1000mA	EN-DC_1A(1DL/UL SISO)-n78A(1DL/1UL SISO)
		LTE : BW 20MHz, 1 RB, QPSK DL/QPSK UL, 23dBm
		FR1 : BW 100MHz, Inner RB 137(Number)@64(Position), QPSK DL/QPSK UL, 23 dBm
NR-SA		
NSA mode 4CC+1FR1	2000mA	EN-DC_3C(DL4x4)_7C(DL4x4) -n78A(1DL 4x4MIMO/1UL SISO/100M)
		LTE : BW 20MHz, Full RB, 256QAM DL/QPSK UL(1.5Gbps DL/4Mbps UL)
		FR1 : BW100MHz, Full RB, 256QAM DL/QPSK UL(1.8Gbps DL/1.6Mbps)
SA mode 1FR1	350mA	FR1(n78A) : BW100MHz, Full RB, 256QAM DL/QPSK UL(1.8Gbps /1.6Mbps)
SA mode 2FR1	550mA	FR1(CA_n78A_n78A) : BW200MHz, Full RB, 256QAM DL/QPSK UL(3.6Gbps/1.6Mbps)
LTE		
Single-mode (1DL/1UL SISO)	750mA	Non-CA ,B3 BW 10MHz, 1 RB, 23dBm, QPSK DL/QPSK UL
4DLCA (4x4MIMO) with 1UL(SISO)	1650mA	CA_1A-7C-28A, Full RB, 256QAM DL/ QPSK UL(1.5Gbps DL/4Mbps UL)
WCDMA		
WCDMA Voice	750mA	WCDMA B1 voice call (Tx=23dBm)
WCDMA HSPA	750mA	WCDMA B1 data call (DC-HSDPA up to 42Mbps, Max through-put)

Note: The worst and best case current consumption values depend on the mobile network configuration, which is outside the module's control.

(*) Loop-back mode in call equipment.

(*) Operating at 3.8V under room temperature.

5.3 General Design Rule

The main guidelines for the Power Supply Design include three different design steps:

- The electrical design of the power supply
- The thermal design
- The PCB layout

5.3.1 Electrical Design Guidelines

The electrical design of the power supply strongly depends on the power source where this power is drained. These sources can be categorized as follows:

- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)

5.3.2 +5V Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, the small difference between the input source and the desired output voltage suggests using a linear regulator. A switching power supply is not suitable due to the low dropout requirements.
- When using a linear regulator, a proper heat sink must be provided.
- A low ESR bypass capacitor of adequate capacity must be provided to smoothen current absorption peaks close to the Module: a 100 μ F capacitor is usually suitable.
- Ensure the low ESR capacitor on the power supply output is rated at least 16V.
- A protection diode must be inserted close to the modem power input to protect the FE990B from power polarity inversion.

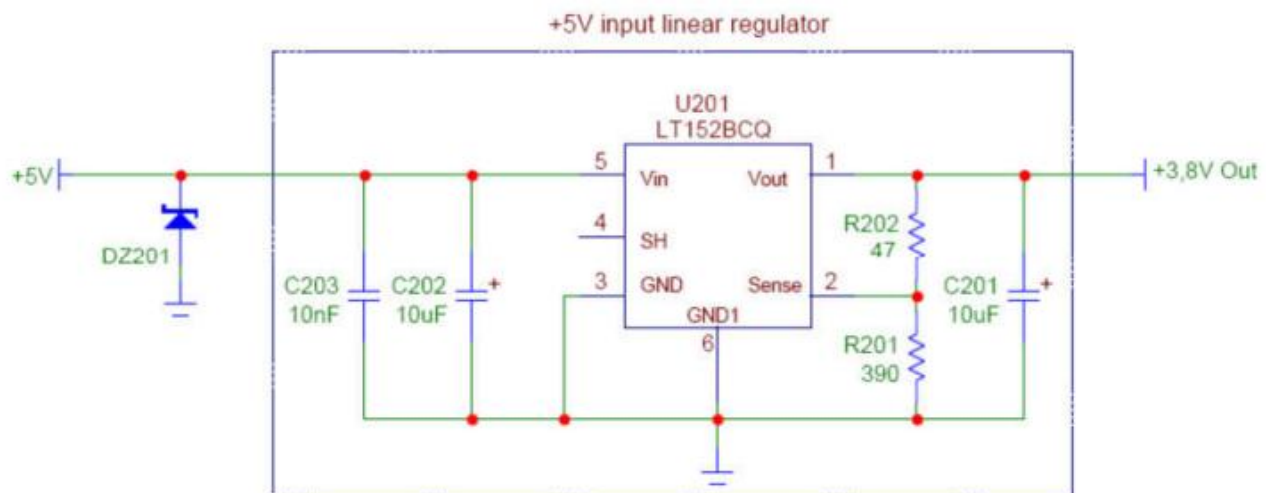


Figure 2: An Example of Linear Regulator with 5V Input

5.3.3 +12V Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V: due to the high difference between the input and the desired output voltage values, a linear regulator is not suitable and should not be used. A switching power supply is recommended because of its better efficiency.
- When using a switching regulator, a 500kHz or higher switching frequency regulator is preferable because of its smaller inductor size and faster transient response. This allows the regulator to respond quickly to the current peak absorption.
- In any case, frequency and Switching design selection are related to the application to be developed since the switching frequency could also generate EMC interferences.
- A Bypass low ESR capacitor of adequate capacity must be provided to cut the current absorption peaks, a 100 μ F capacitor is usually suitable.
- Make sure the low ESR capacitor on the power supply output is rated at least 16V.

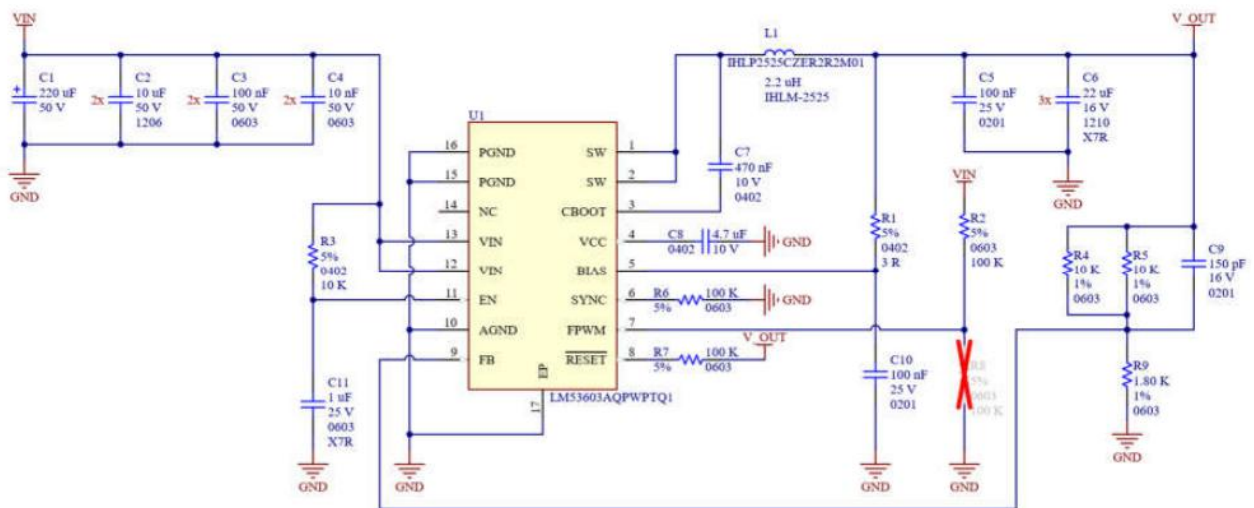


Figure 3: An Example of Switching Regulator with 12V Input

5.3.4 Thermal Design Guidelines

This section provides thermal design guidelines useful for developing a product with the FE990B module.

Proper thermal protection design protects against human or component damage under worst-case conditions.

Furthermore, it reduces the probability of failure and does not adversely affect the use of the module, and greatly extends the operation time with maximum performance.

For more details, please refer to the thermal design guidelines.

Note: The FE990B Family supports 3G, 4G, and 5G Sub-6 RATs. Based on the Radio Access Technology, the FE990B module may exhibit different current consumption levels, thus proper thermal designs are essential to properly dissipate heat.

5.3.5 Power Supply PCB Layout Guidelines

As mentioned in the electrical design guidelines, the power supply shall have a low ESR capacitor on the output to reduce current peaks on the input and protect the supply from spikes. The placement of this component is crucial for proper circuit performance. A misplaced component can be useless or even decrease the power supply performance.

- The Bypass low ESR capacitor must be placed close to the Telit FE990B power input pads or, in the case of switching power supply, it can be placed close to the inductor to reduce ripple, provided the PCB trace from the capacitor to the FE990B is wide enough to ensure minimal voltage drop even during 3.5 A current peak.
- The protection diode must be placed close to the input connector where the power source is drained.
- The PCB traces from the input connector to the power regulator IC must be wide enough to ensure no voltage drops occur when a 3.5 A current peak is absorbed.
- PCB traces FE990B and the Bypass capacitor must be wide enough to ensure no significant voltage drops occur. This is for the same reason as the previous point. These traces must be kept as short as possible.

- To reduce the EMI due to switching, it is important to keep the mesh as small as possible; therefore, the input capacitor, output diode (if not embedded in the IC), and the regulator, shall form a very small loop. This is to reduce the radiated field (noise) at the switching frequency (100-500 kHz usually).
- A dedicated ground for the Switching regulator separated by the common ground plane is suggested.
- Power supply placement on the board should guarantee that the high current return paths in the ground plane do not overlap with any noise-sensitive circuitry, such as audio amplifiers.
- Power supply input cables or traces should be kept separate from noise-sensitive lines such as microphone/earphone cables.

5.4 VAUX Power Output

A regulated power supply output is provided to supply accessories from the module, such as level translators, audio codecs, sensors, and so on.

This output is active when the module is ON and turns OFF when the module is shut down.

The operating range characteristics of the supply are:

Table 34: Operating Range Characteristics of the Supply

Item	Min	Typical	Max
Output voltage	1.75V	1.80V	1.85V
Output current	-	-	200mA
Output bypass capacitor (inside the module)		1uF	

5.5 RTC – Real Time Clock

The FE990B modules RTC does not have a dedicated RTC supply pin: the RTC block is powered through the VPH_PWR supply.

If VPH_PWR power is removed, the RTC is not maintained; thus, if the application is required to maintain an internal RTC, VPH_PWR must never be interrupted.

6 Digital Section

Unless otherwise specified, all FE990B interface circuits are 1.8V CMOS logic. Only a few specific interfaces support dual voltage I/O. The following tables show the specifications for the logic levels used in the FE990B interface circuits.

Warning: Do not connect FE990B digital logic signals directly to peripheral digital logic signals with a level higher than 2.1V for 1.8V CMOS signals. Additionally, do not connect 2.95V signals directly to levels exceeding 3.35V.

6.1 Logic Levels

Table 35: Absolute Minimum and Maximum – 1.8/2.9 V

Parameter	Min	Max
Absolute Maximum Ratings – 1.8 V		
	-0.3 V	2.134V
Absolute Maximum Ratings – 2.9 V		
	-0.3 V	3.344 V

Table 36: Standard GPIO – 1.8 V

Parameter	Min	Max
1.8 V – Standard GPIO		
High-level input voltage	1.17 V	2.1 V
Low-level input voltage	-0.3 V	0.63 V
High-level output voltage	1.35 V	1.8 V
Low-level output voltage	0 V	0.45 V

Table 37: UIM1 1.8/2.95 V

Parameter	Min	Max
1.8 V UIM		
Supply voltage	1.65 V	1.95 V
High-level input voltage	1.155 V	2.25 V
Low-level input voltage	-0.3 V	0.39 V
High-level output voltage	1.32 V	1.95 V
Low-level output voltage	0 V	0.4 V
2.95 V UIM		
Supply voltage	2.7 V	3.05 V
High-level input voltage	1.89 V	3.35 V
Low-level input voltage	-0.3 V	0.61 V
High-level output voltage	2.16 V	3.05 V
Low-level output voltage	0 V	0.4 V

Table 38: SIM2 1.8 V

Parameter	Min	Max
1.8 V UIM		
Supply voltage	1.65 V	1.95 V
High-level input voltage	1.27 V	2 V
Low-level input voltage	-0.3 V	0.58 V
High-level output voltage	1.4 V	-
Low-level output voltage	-	0.45 V

6.2 Power On

To turn on the FE990B module, the ON_OFF_N pad must be asserted low for at least 0.1 second and then released. It is recommend to use an open collector/drain configuration.

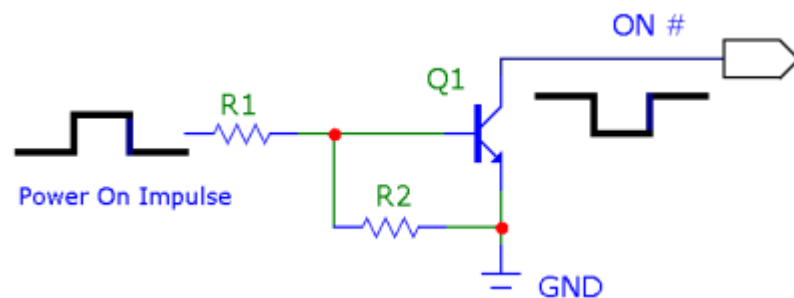


Figure 4: Power-on Circuit illustrates a simple circuit to power on the module using an inverted buffer output.

Note: Do not connect a pull-up resistor to the ON_OFF_N line, as it is internally pulled up. Adding an external pull-up resistor could cause latch-up issues with the FE990B power regulator, leading to improper power-on/off of the module. The ON_OFF_N line must be connected only in the open collector or open drain configuration.

6.2.1 Initialization and Activation State

After turning on the FE990B module, a predefined internal boot sequence performs module HW and SW initialization: this takes some time to complete. During this process, FE990B interfaces are not accessible.

As shown in the diagram below, the FE990B becomes operational at least 20 seconds after the assertion of ON_OFF.

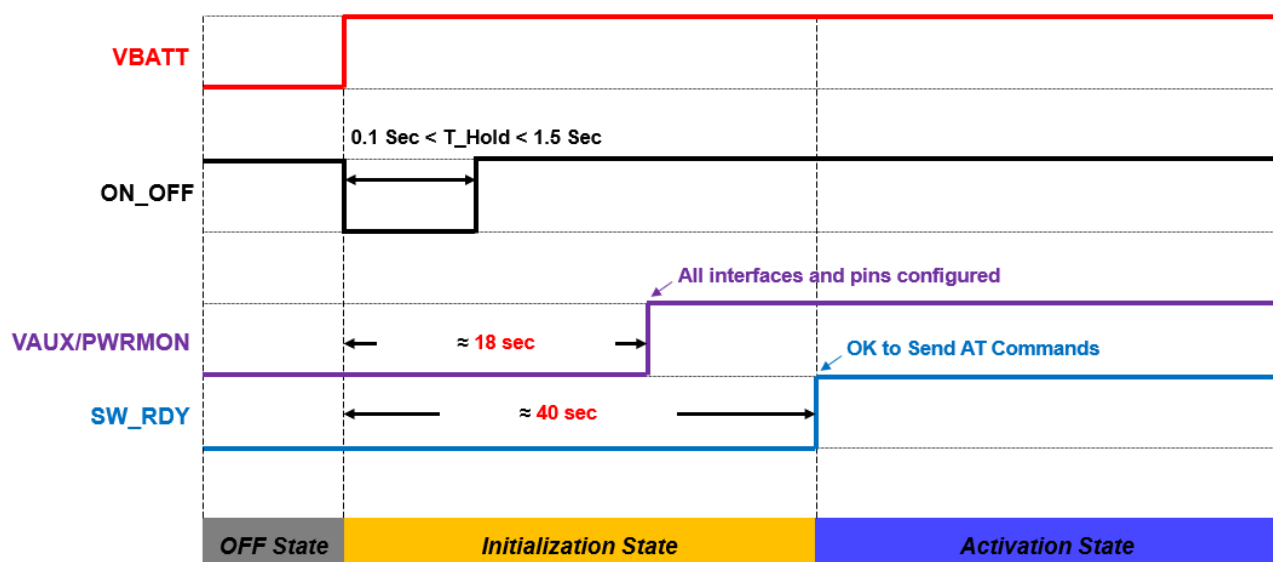


Figure 5: FE990B Initialization and Activation

A flow chart showing the proper Power-On procedure is displayed below:

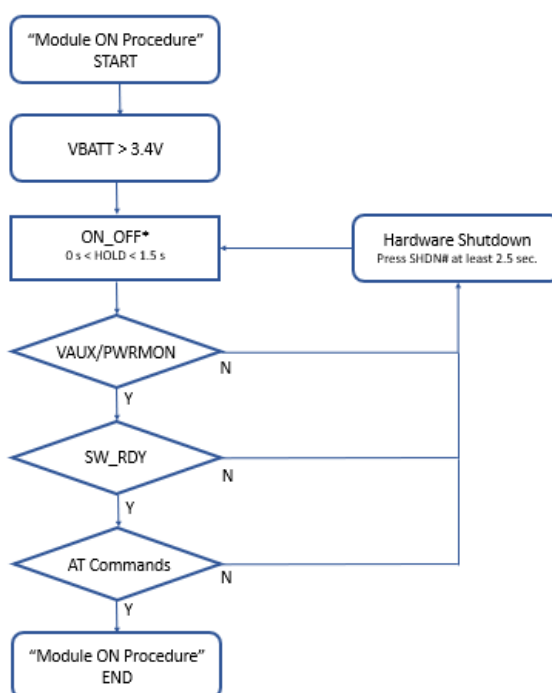


Figure 6: Power On Procedure Flow Chart

A flow chart showing the AT commands managing procedure is displayed below:

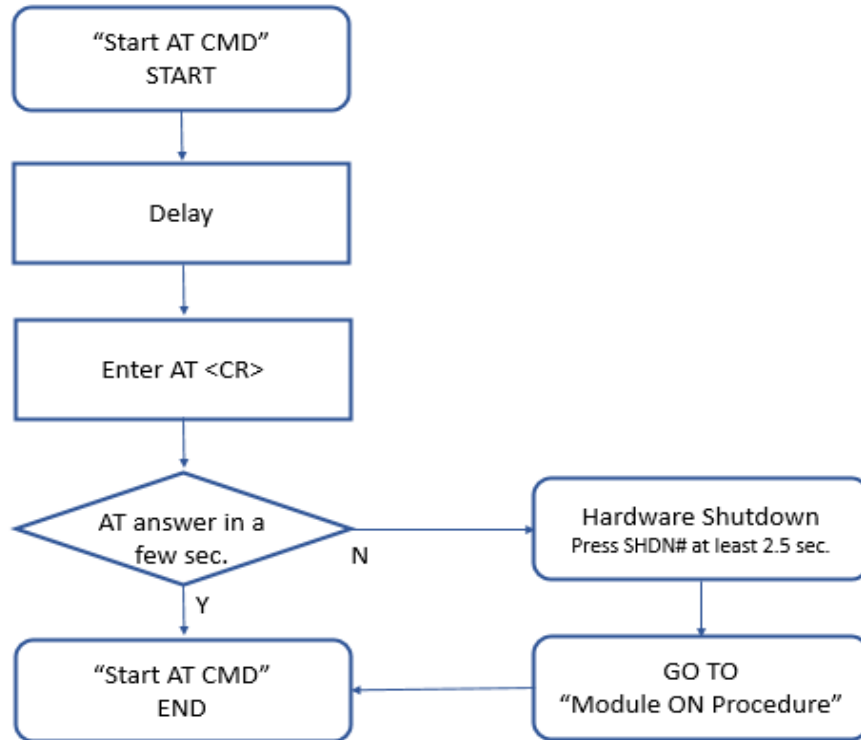


Figure 7: AT commands Managing Procedure Flow Chart

Note: To avoid back-powering effect, it is recommended to prevent any HIGH logic level signal from being applied to the FE990B digital pins when the module is powered off or during an ON-OFF transition.

- Note:**
- During initialization state, AT commands interface is not available. The DTE host must wait for the Activation state before communicating with the FE990B.
 - To check whether the FE990B has completely powered on, SW_RDY hardware line should be monitored. When SW_RDY becomes high, the module is completely powered on and is ready to accept AT commands.
 - During FE990B SW initialization, the SW configures all pads and interfaces to the desired mode. When PWRMON goes high, this indicates that the initialization of all I/O pads is completed.
 - For systems not requiring controlled power ON/OFF, automatic power on can be supported by AUTO_ON_N.
 - In this case, the module will initiate power on sequence immediately after the VBATT supply is applied.
 - Active low signals are labeled with a name that ends with "#" or with "_N "

6.2.2 AUTO_ON_N

If the module needs to turn on automatically, AUTO_ON_N (C41) should be low directly to GND.

Note: AUTO_ON_N is only for power-on, so it cannot be used for power-off. To power-off, require to remove VPH_PWR.
This feature can be useful during testing, and when using this feature, there's no need to use ON_OFF_N separately.

6.3 Power Off

Turning off the device can be done in the following different ways:

- Shutdown by software using the AT#SHDN command.
- Hardware shutdown using ON_OFF_N
- Hardware unconditional shutdown using the SHDN_N

When the device is powered off through a software command or hardware shutdown, it issues a detach request to the network, informing the network that the device will no longer be reachable.

Note:

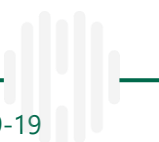
- To check if the device has powered off, monitor the PWRMON/SW_RDY hardware line. When PWRMON/SW_RDY goes low, it means the device has powered off.
- To avoid a back-powering effect it is recommended to prevent any HIGH logic level signal from being applied to the digital pins of the FE990B when the module is powered off or during an ON-OFF transition.

Warning: Not following the recommended shut-down procedures might damage the device and consequently void the warranty.

6.3.1 Shutdown via Software Command

The FE990B module can be powered down using a software command. Upon receiving a shutdown command, the FE990B transitions into a finalization state. Once the finalization process is complete, the module will deactivate the PWRMON/SW_RDY signal, indicating shutdown.

The duration of the finalization state depends on the module's current status, making it difficult to specify an exact time. Usually, it will take more than 15 seconds to send a shutdown command until a complete shutdown is achieved. The DTE host should monitor the status of PWRMON/SW_RDY to observe the actual power-off.



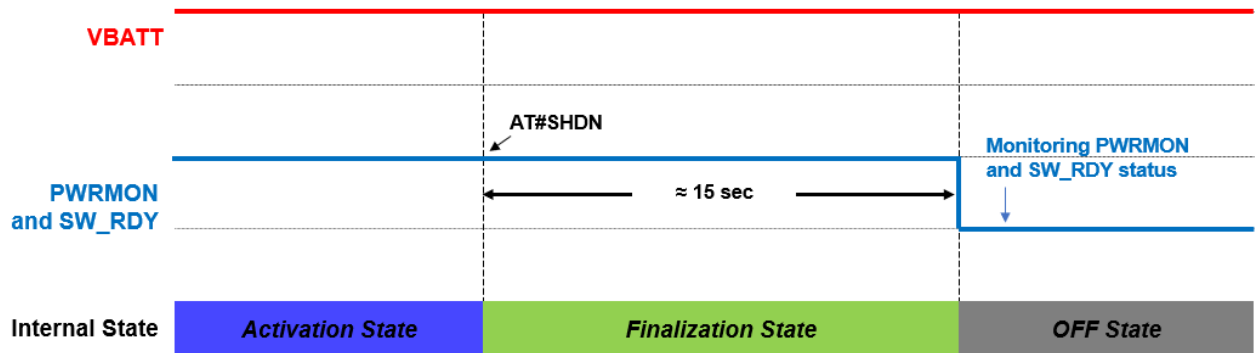


Figure 8: Shutdown by Software Command

Note: To check whether the device has completed powered off sequence, monitor the PWRMON/SW_RDY hardware line. When PWRMON/SW_RDY is low, the device is powered off.

6.3.2 Hardware Shutdown

To turn off the FE990B module, the ON_OFF_N pad must be asserted low for at least 2.5 seconds and then released. Use the same circuitry and timing for power-on.

When the ON/OFF# hold time is above 2.5 seconds, the FE990B enters the Finalization state and eventually shuts down PWRMON/SW_RDY.

Finalization state duration can vary according to the module state at power down, thus value cannot be defined.

Usually, it will take more than 15 seconds until a complete shutdown is achieved. The DTE host should monitor the status of PWRMON/SW_RDY to observe the actual power-off.

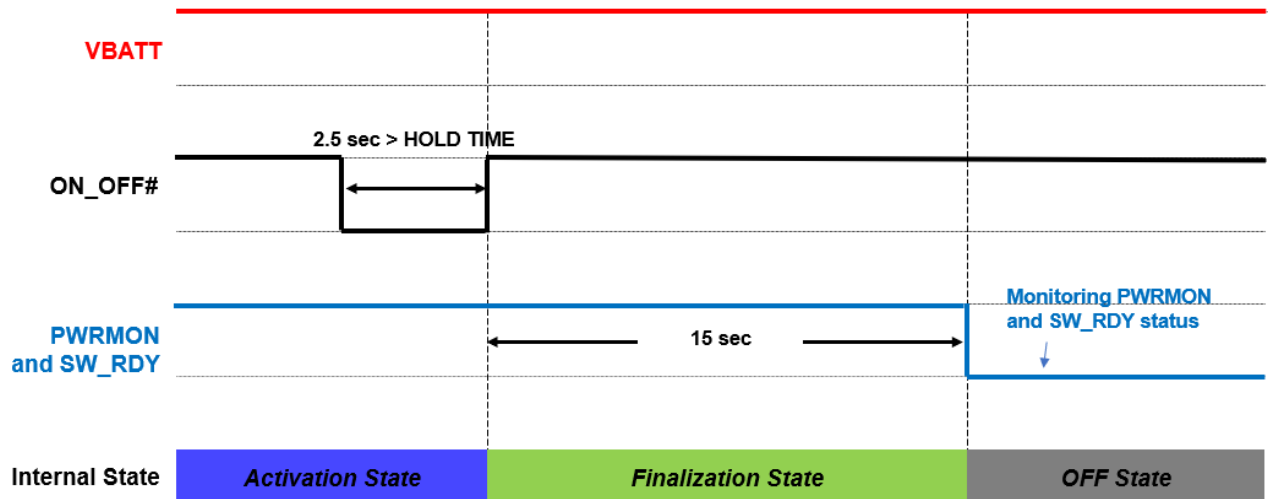


Figure 9: Hardware Shutdown

Note: To check whether the device has powered off, monitor the PWRMON/SW_RDY hardware line. When PWRMON/SW_RDY goes low, the device is powered off.

6.3.3 Unconditional Hardware Shutdown

To unconditionally shut down the FE990B module, the HW_SHUTDOWN_N pad must be tied low for at least 2.5 seconds and then released.

The figure below shows a simple circuit for applying an unconditional shutdown.

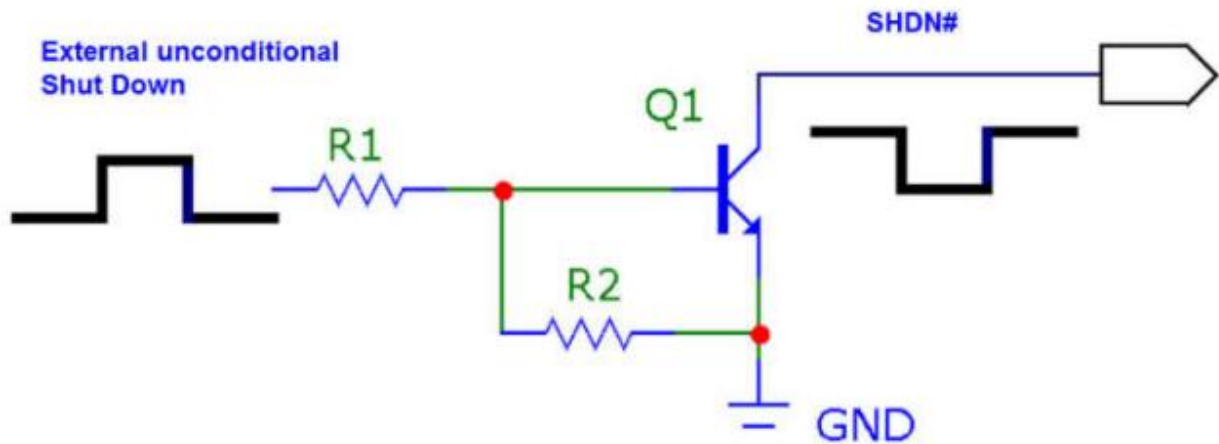


Figure 10: Circuit for Unconditional Hardware Shutdown

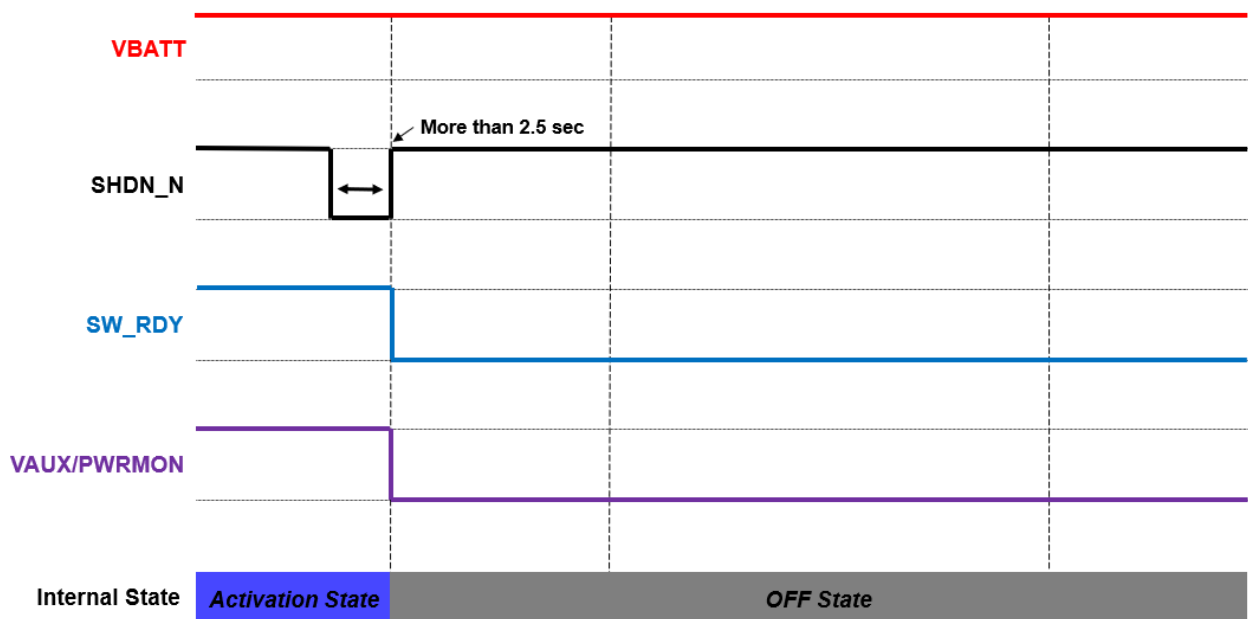


Figure 11: Power down timing using HW_SHUTDOWN_N

Note: Do not use any pull-up resistor on the HW_SHUTDOWN_N line or any totem pole digital output. Using a pull-up resistor may cause latch-up problems on the FE990B power regulator and improper functioning of the module. The HW_SHUTDOWN_N line must be connected only in an open-collector configuration.

The Unconditional Hardware Shutdown must always be implemented on the boards. However, this function should only be used as an emergency exit procedure, not for routine power-off operations.

6.3.4 RESET_N Function

The FE990B40 provides a reset function; however, its use is not recommended during normal operation. Since activating the reset function may lead to unexpected behavior, it should be used with caution and only when absolutely necessary.

Warning: When the reset function is triggered during module operation, it may lead to memory bit corruption. Therefore, the reset function is recommended only for internal debugging or development purposes.

If it is unavoidable to use the reset function, a software reset is recommended.

The AT command is as follows:

- AT#REBOOT
-

6.4 Powering OFF the Module

Powering OFF the module should be performed gracefully, allowing the module to complete all ongoing and pending tasks while properly handling all memory buffers.

If a complete power supply shutdown is needed, the procedure below must be followed:

- 1 Perform a HW shutdown as described in the previous section.
- 2 Wait for the HW shutdown procedure to complete (monitor the PWRMON/SW_RDY pin).
- 3 Turn OFF the power supply to the module.

Warning: Carefully follow the recommended procedure for shutdown and power-off.

Failure to follow the recommended shut-down and power-off procedures may damage the device and consequently void the warranty.

6.5 Fast Power Down

The gentle power-down procedure is described in Chapter 6.3. Usually, it takes more than 4.5 seconds to detach from the network and properly close the FE990B internal filesystem.

In the event of an unwanted power supply loss, FE990B can be switched off without any risk of filesystem data corruption by implementing the Fast Power Down feature.

The Fast Power Down feature permits to reduction current consumption and the time-to-power off to a minimum.

Note: Refer to the FE990B AT command reference guide (Fast power down - #FASTSHDN) for a detailed command description.

6.5.1 Fast Shut Down by Hardware

Fast Power Down can be triggered by a GPIO. Applications needing to implement Fast Shut Down should configure a GPIO as the trigger pin for the Fast Shut Down through the AT command. The high-to-low transition of a GPIO triggers the Fast Shut Down and then the FE990B module turns off within 50 ms.

Example circuit:

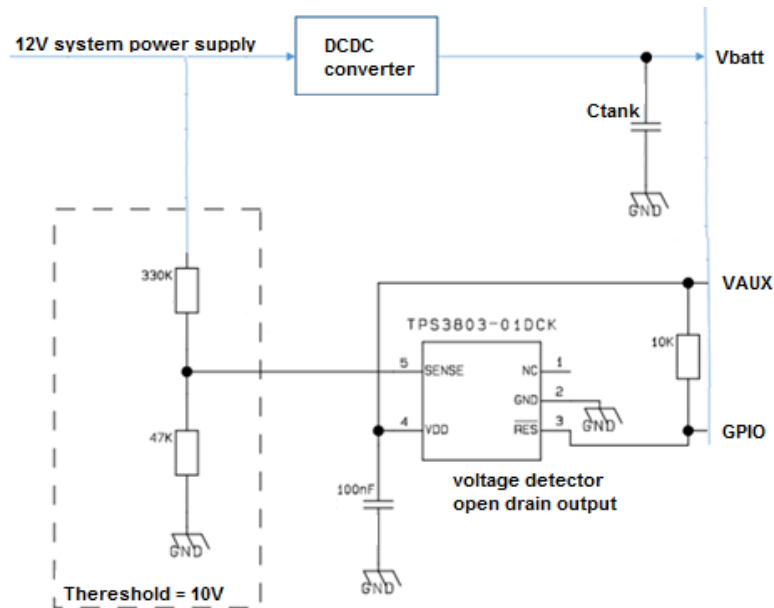


Figure 12: Example Circuit

Note: Consider voltage drop under maximum current conditions when defining the voltage detector threshold to avoid an unwanted shutdown.

The capacitor is rated with the following formula:

$$C = I \frac{\Delta t}{\Delta V}$$

Note: Make the same plot during system verification to check timings and voltage levels.

6.5.2 Fast Shutdown by Software

The Fast Power Down can be triggered by the AT command.

6.6 Communication Ports

6.6.1 USB

The FE990B includes a super-speed USB 3.1 Gen 2 port with high-speed USB 2.0 backward compatibility. The interface with the Universal Serial Bus Specification, revision 3.1 can be used for control and data transfers as well as for diagnostic monitoring and firmware update. The USB port is typically the main interface between the FE990B module and application hardware. USB 3.1 needs AC coupling series capacitors on the TX lines in both directions. To interface USB 3.1 with the application board controlling the modem, it is necessary to install a 220 nF capacitor on the USB_SS_RX_P/M lines of the FE990B Family.

The series capacitors are already placed on USB_SS_TX_P/M lines inside the FE990B module.

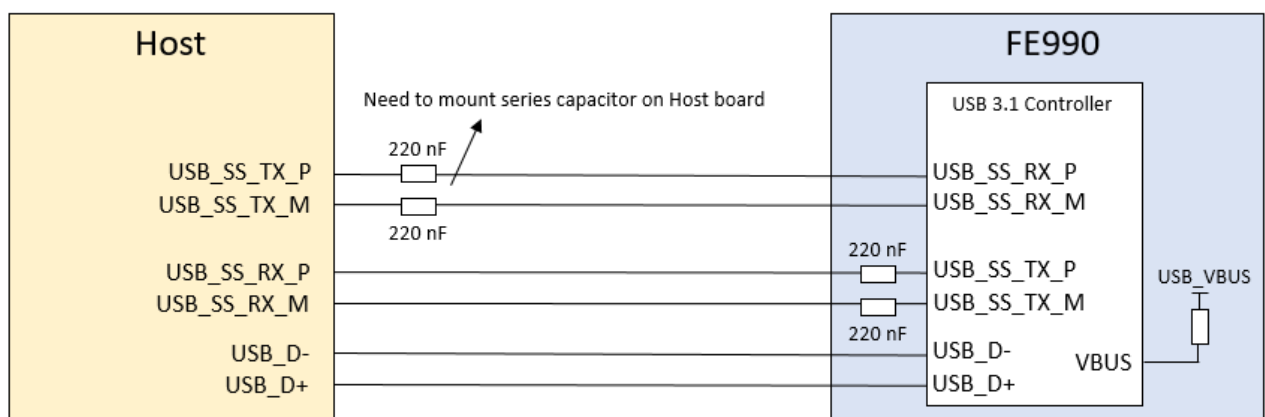


Figure 13: Connection for USB Interface

Note: The USB signal traces must be carefully routed: minimize trace lengths, number of vias, and capacitive loading. The impedance value should be as close as possible to the nominal 90 Ohm differential.

The following table lists the available signals:

Table 39: Available Signals

PAD	Signal	I/O	Function	NOTE
AC47	USB_D+	I/O	USB 2.0 differential Data – Plus	Float if USB 2.0 is unused.
AD45	USB_D-	I/O	USB 2.0 differential Data – Minus	
X45	USB_SS_RX_M	I	USB 3.1 super-speed receive – Minus	Float if USB 3.1 is unused.
W47	USB_SS_RX_P	I	USB 3.1 super-speed receive – Plus	
Z45	USB_SS_TX_M	O	USB 3.1 super-speed transmit – Minus	
Y47	USB_SS_TX_P	O	USB 3.1 super-speed transmit – Plus	
AF45	USB_VBUS	AI	Power and cable detection for the internal USB transceiver. (not for power supply) USB connection detect	Vmax: 5.5 V Vnom: 5.0 V VIH: Min. 1.3 V VIL: Max. 0.85 V Detection threshold (USB presence is detected)
AE47	USB_VBUS			

PAD	Signal	I/O	Function	NOTE
				VIH: Min.1.3 V. Detection threshold (USB presence is not detected) VIL: Max. 0.85 V
V45	USB_ID	I	Used for USB OTG to determine host or client mode	

Note: USB OTG feature is supported by default.
If the USB_ID pin asserted to 'low', USB OTG is enabled.
Please note that FE990Bxx doesn't supply 5V power to OTG devices therefore an external 5V power is required on application board to provide 5V power to OTG devices.

Note: Consider placing a low-capacitance ESD protection component to protect FE990B against ESD strikes.

6.6.1.1 USB Layout Guidelines

- If third-party components are required for signal improvement, place them closer to the USB connector.
- There are relatively fast edge rates, so must be routed away from sensitive circuits and signals (RF, audio, and XO).
- Maintain good isolation between the USB connector and RF antennas (especially 2.4 GHz).
- Route the RF signals operating at a 2.4 GHz frequency with the highest isolation possible from USB_SS_TX/RX traces.
- USB SS Tx AC coupling capacitors are better placed close to the source or the ESD/connector side to keep good SI of the main route on the PCB.
- Route differential pairs in the inner layers with a solid GND reference to have good impedance control and to minimize discontinuities.
- Keep isolation between the Tx pair, Rx pair, and DP/DM to avoid crosstalk.
- The SS-USB Tx and Rx differential pair maximum length is recommended to be less than 150 mm.
- For USB 2.0 signal, the maximum trace length should be less than 250 mm.

Table 40: USB Routing Constraints

Type of guidance	Guideline	Requirement	
		USB 3.1 Gen 2	USB 2.0
General	Data rate	10 Gbps	480 Mbps
	Insertion loss budget	-7 dB at 5 GHz	N/A
	Impedance	90 ohms differential	
	Maximum PCB trace length*	150 mm	250 mm
Length matching	Intra length match	< 0.7 mm	< 2 mm
Spacing	To all other signals	> 4 x line width	> 3 x line width
	Tx lane to Rx lane	> 4 x line width	N/A

Type of guidance	Guideline	Requirement	
		USB 3.1 Gen 2	USB 2.0
Component	AC capacitance	220 nF	N/A

Warning: *Please consider the Table 41: USB Trace Length

Table 41: USB Trace Length

PAD	Signal	Length (mm)	Difference	NOTE
AC47	USB_D+	7.35	0.014	90 ohm
AD45	USB_D-	7.364		
X45	USB_SS_RX_M	3.908	0.016	
W47	USB_SS_RX_P	3.892		
Z45	USB_SS_TX_M	12.929	0.178	
Y47	USB_SS_TX_P	12.751		

6.6.2 PCIe

The FE990B module includes a PCIe interface. PCIe needs AC coupling series capacitors on the TX lines in both directions. To interface PCIe with the application board that controls the modem, 220nF capacitors should be installed on PCIE_RX_P/M lines of the FE990B. The series capacitors are already placed on PCIE_TX_P/M lines inside the FE990B. Internally, a 1.8V level 4.7k pull-up resistor is already mounted on PCIE_WAKE_N and PCIE_CLKREQ_N.

For the host PCIe three lines (WAKE, RESET, CLKREQ) pull-up resistance value, refer to the PCIe documentation and apply. (PCI Express Card Electromechanical Specification)

The suggested PCIe interface connection is shown in the diagram below:

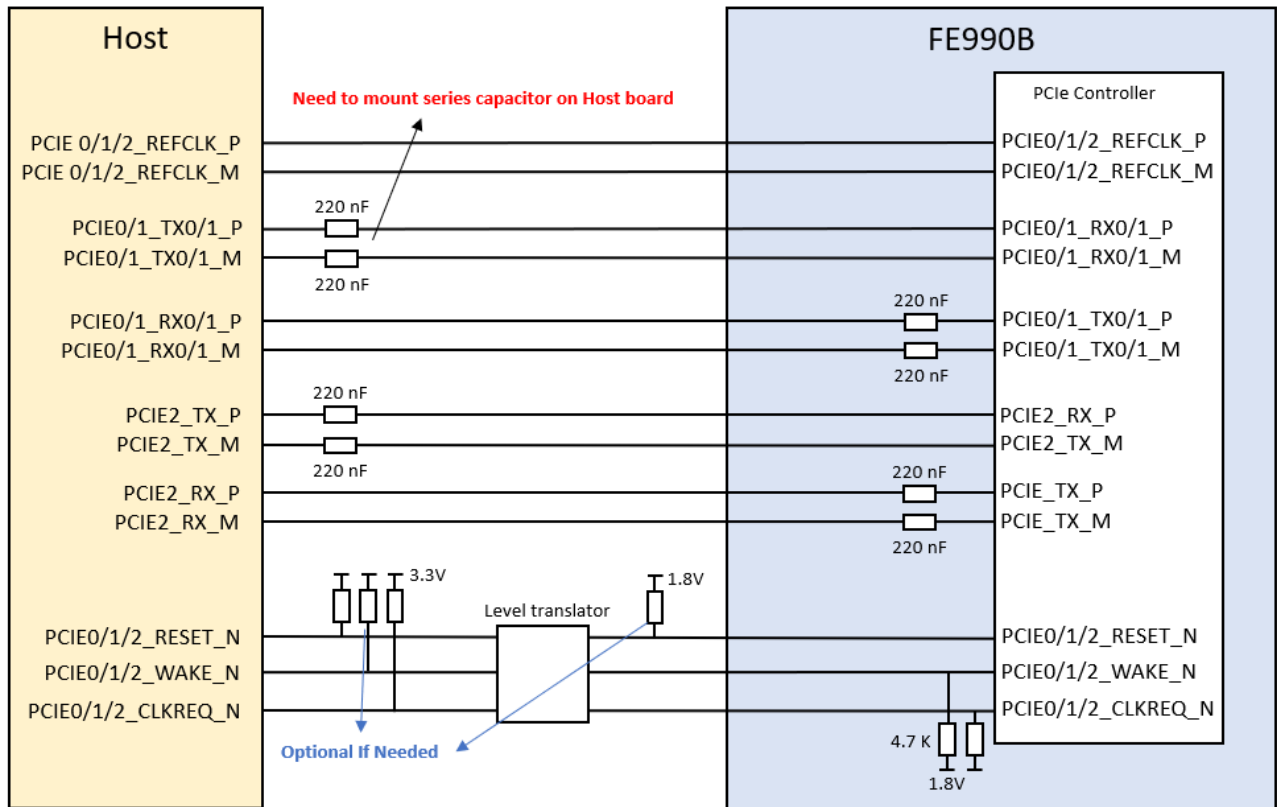


Figure 14: Connection for PCIe Interface

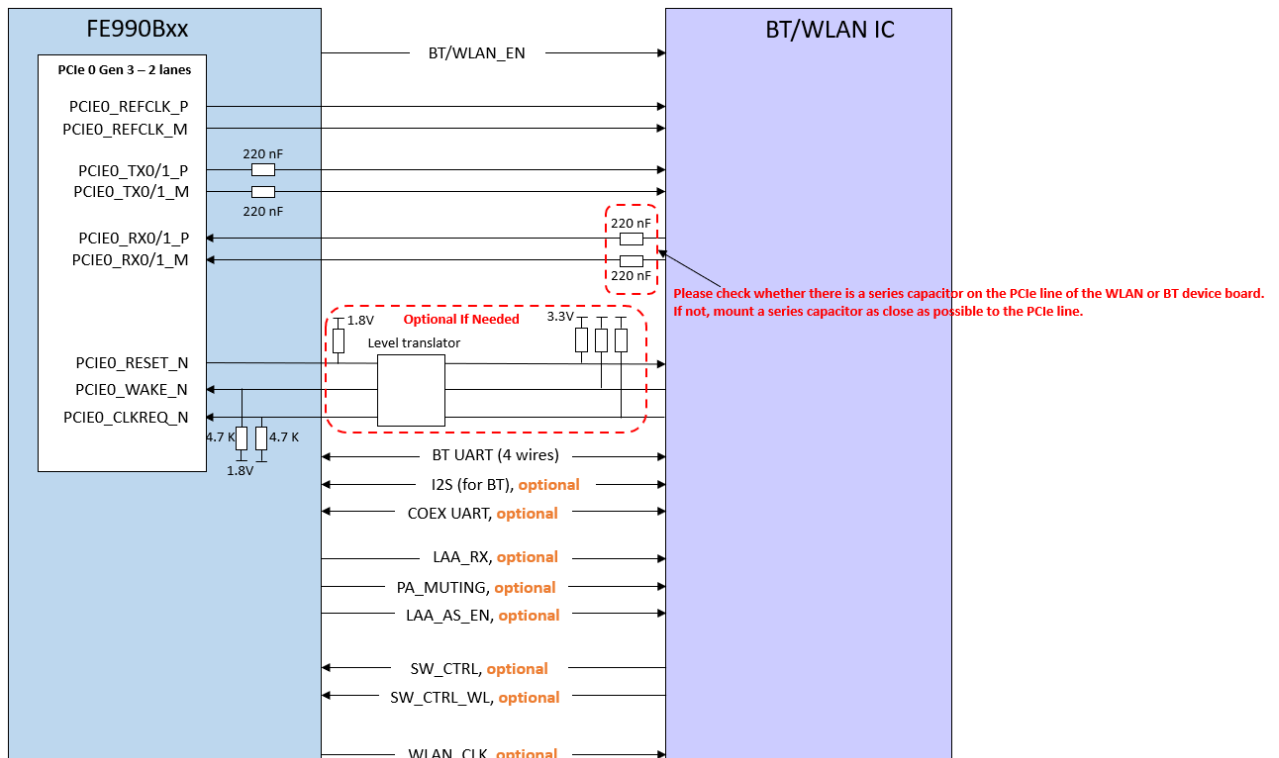


Figure 15: Example of PCIe RC connection using PCIe 0 Gen 3, 2-lane

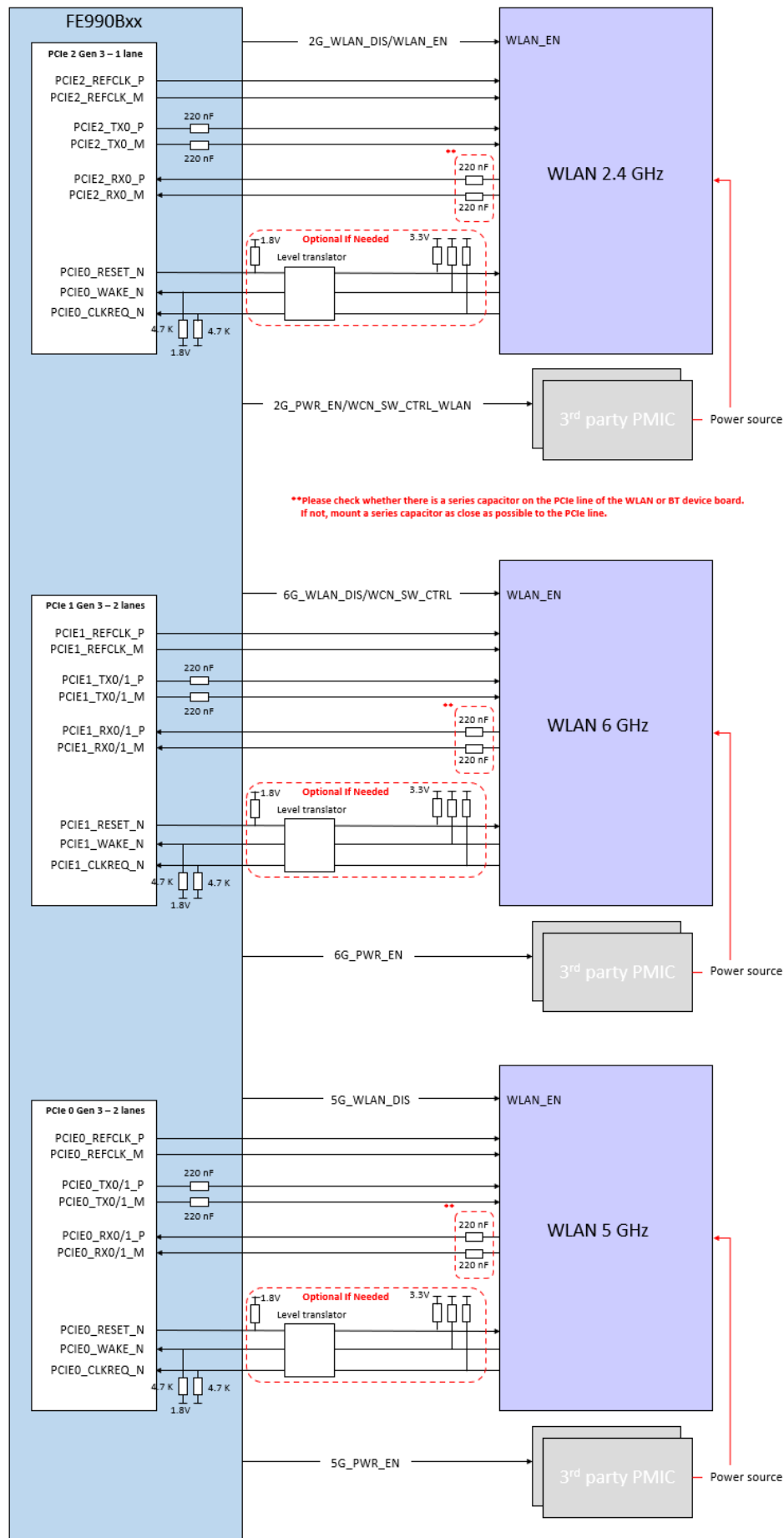


Figure 16: Example of PCIe RC connection using all PCIe interfaces

Note: PCIe 0: Gen 4 – One lane or Gen 3 – Two lanes (RC and EP)
 PCIe 1: Gen 3 – Two lanes (only RC)
 PCIe 2: Gen 3 – One lane (only RC)

Note: The PCIe signal traces must be carefully routed: minimize trace lengths, number of vias, and capacitive loading. The impedance value should be as close as possible to the 85-ohm differential.

Table 42: PCIe Communication Port

Pin	Signal	I/O	Function	Type	Comment
PCIe Communication Port					
X49	PCIE0_CLKREQ_N	OD	PCIe0 reference clock request signal	OD	Internal PU (4.7 K) Input: Master Output: Slave
Z49	PCIE0_RST_N	I/O	PCIe0 reset	I/O	Input: Slave Output: Master
T49	PCIE0_WAKE_N	OD	PCIe0 wake up	OD	Internal PU (4.7 K) Input: Master Output: Slave
V51	PCIE0_REFCLK_P	I/O	PCIe0 differential reference clock - Plus	Analog Input/Output	Float if PCIe0 is unused. Connected during one lane operation.
W50	PCIE0_REFCLK_M	I/O	PCIe0 differential reference clock - Minus	Analog Input/Output	
R51	PCIE0_TX0_P	O	PCIe0 transmit 0 - Plus	Analog Output	Float all signals if PCIe0 is unused. If using only one lane, connect PCIe0_TX0_M/P and float PCIe0_TX1_M/P.
S50	PCIE0_TX0_M	O	PCIe0 transmit 0 - Minus	Analog Output	
T51	PCIE0_TX1_P	O	PCIe0 transmit 1 - Plus	Analog Output	
U50	PCIE0_TX1_M	O	PCIe0 transmit 1 - Minus	Analog Output	
X51	PCIE0_RX0_P	I	PCIe0 receive 0 - Plus	Analog Input	Float all signals if PCIe 0 is unused. If using only one lane, connect PCIe0_RX0_M/P and float PCIe0_RX1_M/P.
Y50	PCIE0_RX0_M	I	PCIe0 receive 0 - Minus	Analog Input	
Z51	PCIE0_RX1_P	I	PCIe0 receive 1 - Plus	Analog Input	
AA50	PCIE0_RX1_M	I	PCIe0 receive 1 - Minus	Analog Input	
AH49	PCIE1_CLKREQ_N	I	PCIe1 reference clock request signal	DI	Internal PU (4.7 K) RC only
AK49	PCIE1_RST_N	O	PCIe1 reset	DO	RC only
AD49	PCIE1_WAKE_N	I	PCIe1 wake up	DI	Internal PU (4.7 K)

Pin	Signal	I/O	Function	Type	Comment
					RC only
AH51	PCIE1_REFCLK_P	I/O	PCle1 differential reference clock - Plus	Analog Input/Output	Float if PCle1 is unused.
AJ50	PCIE1_REFCLK_M	I/O	PCle1 differential reference clock - Minus	Analog Input/Output	Connected during one lane operation.
AD51	PCIE1_TX0_P	O	PCle1 transmit 0 - Plus	Analog Output	Float all signals if PCle1 is unused.
AE50	PCIE1_TX0_M	O	PCle1 transmit 0 - Minus	Analog Output	If using only one lane, connect PCIE1_TX0_M/P and float PCIE1_TX1_M/P.
AF51	PCIE1_TX1_P	O	PCle1 transmit 1 - Plus	Analog Output	
AG50	PCIE1_TX1_M	O	PCle1 transmit 1 - Minus	Analog Output	
AK51	PCIE1_RX0_P	I	PCle1 receive 0 - Plus	Analog Input	Float all signals if PCle1 is unused.
AL50	PCIE1_RX0_M	I	PCle1 receive 0 - Minus	Analog Input	If using only one lane, connect PCIE1_RX0_M/P and float PCIE1_RX1_M/P.
AM51	PCIE1_RX1_P	I	PCle1 receive 1 - Plus	Analog Input	
AN50	PCIE1_RX1_M	I	PCle1 receive 1 - Minus	Analog Input	
AU49	PCIE2_CLKREQ_N	I	PCle2 reference clock request signal	DI	Internal PU (4.7 k) RC only
AW49	PCIE2_RST_N	O	PCle2 reset	DO	RC only
AP49	PCIE2_WAKE_N	I	PCle2 wake up	DI	Internal PU (4.7 k) RC only
AU51	PCIE2_REFCLK_P	I/O	PCle2 reference clock request signal	Analog Input/Output	Float all signals if PCle2 is unused.
AV50	PCIE2_REFCLK_M	I/O	PCle2 differential reference clock - Minus	Analog Input/Output	
AX50	PCIE2_RX0_M	I	PCle2 receive 0 - Minus	Analog Input	
AW51	PCIE2_RX0_P	I	PCle2 receive 0 - Plus	Analog Input	
AT50	PCIE2_TX0_M	O	PCle2 transmit 0 - Minus	Analog Output	
AS51	PCIE2_TX0_P	O	PCle2 transmit 0 - Plus	Analog Output	

Note: PCIE_RESET_N operates as digital input in PCIe EP mode, and open drain in PCIe RC mode. PCIE_CLKREQ_N and PCIE_WAKE_N operates as open drain in PCIe EP mode, and digital input in PCIe RC mode.

Note: Consider placing a low-capacitance ESD protection component to protect the FE990B against ESD spikes.

Warning: In the case of PCIe EP mode, FE990B modems are not designed or intended to support Hot-Swap or Hot-Plug connection. Performing How-Swap or Hot-Plug may pose danger to the FE990B module, to the host device, and to the person handling the device.

6.6.2.1 PCIe Layout Guidelines

The following guidelines will provide general guidelines for the PCIe interface to improve signal integrity.

- All other sensitive/high-speed signals and circuits must be protected from PCIe corruption.
- PCIe signals must be protected from noisy signals (clocks, SMPS, and so forth)
- Pay extra attention to crosstalk, ISI, and intraplane skew and impedance discontinuities.
- PCIe Tx AC coupling capacitors are better placed close to the source or receiver side to keep good SI of route on PCB.
- To maintain impedance balance, maintain positive and negative traces as balanced as possible in terms of the signal and its return path.
- Trace length matching between the reference clock, Tx, and Rx pairs are not required.
- External capacitors also should keep differential traces. Ensure not to stagger the capacitors. This can affect the differential integrity of the design and can create EMI.

Table 43: PCIe Gen 3.0 Routing Constraints

Type of guidance	Guideline	Requirement
General	Data rate	8 Gbps*
	Insertion loss at 4 GHz (dB)	-10 dB
	Impedance	85 ohms differential
	Bus length**	300 mm
Length matching	Intra length match	< 0.7 mm
Spacing	To all other signals	> 4 x line width
	Tx lane to Rx lane	> 4 x line width
Component	AC capacitance	220 nF

Note: *Actual throughput at the system level could be lower due to overheads.

Table 44: PCIe Gen 4.0 (1-lane) Routing Constraints (only PCIe 0)

Type of guidance	Guideline	Requirement
General	Data rate	16 Gbps*
	Insertion loss at 4 GHz (dB)	-13.5 dB
	Impedance	85 ohms differential
	Bus length**	216 mm
Length matching	Intra length match	< 0.7 mm
Spacing	To all other signals	> 4 x line width
	Tx lane to Rx lane	> 4 x line width
Component	AC capacitance	220 nF

Note:

*Link speed is described as supported PCIe Generation standard. Actual throughput at the system level could be lower due to overheads.

Warning:

**Please consider Table 45: PCIe Trace Length

Table 45: PCIe Trace Length

PAD	Signal	Length (mm)	Difference (mm)	Note
PCIe 0				
V51	PCIE0_REFCLK_P	4.208	0.303	85 ohm
W50	PCIE0_REFCLK_M	3.905		
R51	PCIE0_TX0_P	6.708	0.134	
S50	PCIE0_TX0_M	6.842		
T51	PCIE0_TX1_P	5.115	0.27	
U50	PCIE0_TX1_M	4.845		
X51	PCIE0_RX0_P	4.198	0.045	
Y50	PCIE0_RX0_M	4.153		
Z51	PCIE0_RX1_P	4.941	0.137	
AA50	PCIE0_RX1_M	5.078		
PCIe 1				
AH51	PCIE1_REFCLK_P	10.885	0.103	85 ohm
AJ50	PCIE1_REFCLK_M	10.988		
AD51	PCIE1_TX0_P	10.813	0.046	
AE50	PCIE1_TX0_M	10.859		
AF51	PCIE1_TX1_P	11.408	0.068	
AG50	PCIE1_TX1_M	11.476		
AK51	PCIE1_RX0_P	10.468	0.058	
AL50	PCIE1_RX0_M	10.526		
AM51	PCIE1_RX1_P	11.427	0.025	
AN50	PCIE1_RX1_M	11.402		
PCIe 2				

PAD	Signal	Length (mm)	Difference (mm)	Note
AU51	PCIE2_REFCLK_P	17.516	0.102	85 ohm
AV50	PCIE2_REFCLK_M	17.414		
AX50	PCIE2_RX0_M	19.649	0.017	
AW51	PCIE2_RX0_P	19.632		
AT50	PCIE2_TX0_M	19.12	0.104	
AS51	PCIE2_TX0_P	19.016		

6.6.2.2 Host Interface Switch Function

This section describes the host interface switch functions.

Note: The meaning of the name host interface switch implies which interface provides the main function. Please refer to the FE990B Software User Guide, regarding each function.

Table 46: Host Interface Switch Pin

Pin	Signal	I/O	Function	Type	Comment	
Host Interface						
A43	USB_PCIE_SWITCH	I	PCIe/USB interface switch	1.8 V		
USB/PCIE Switch			Mode	USB	PCIe EP	PCIe RC
High			USB	Available	Not Support	Available**
Low			PCIe	Available*	Available	Not Support

FE990B determines the host interface by checking the status of the USB_PCIE_SWITCH pin at the beginning of the power-on sequences.

Note: *When using PCIe EP, PCIe RC cannot be used, and basic functions such as mobile data and AT commands are provided through PCIe EP, while USB is provided only for debugging and specific purposes.
For more details, please refer to the 1VW0301969, FE990B Software User Guide.

Note: **FE990B supports the following devices as EP for data interface:

- Realtek RTL8261 Ethernet Controller

Please consult Telit if a different EP device is used as a data interface since the EP device kernel driver needs to be modified to use the FE990B network hardware accelerator

Warning: Since the **USB_PCIE_SWITCH pin is set to Low by default**, an external pull-up resistor with a 1.8 V supply is required in order to use the USB interface.

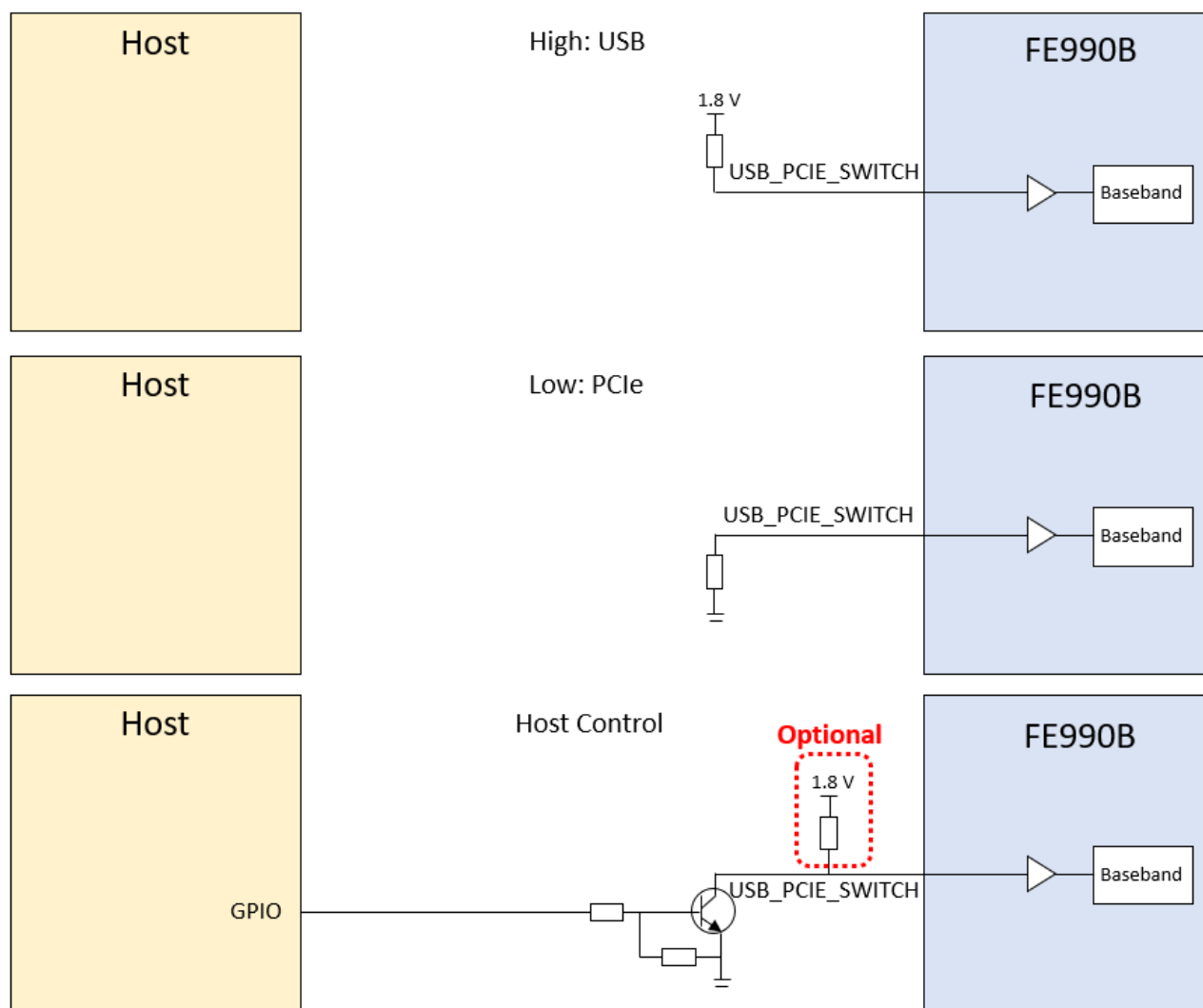


Figure 17: Example Circuit for Host Interface Switch Function

6.6.3 SIM

The FE990B supports an external SIM interface. (1.8 V or 2.95 V).

Note: UIM2 can be assigned as an optional eSIM. In case eSIM is mounted, UIM2 can't be used as an external SIM interface.

Table 47: SIM Card 1 Interface

Pin	Signal	I/O	Function	Type	Comment
SIM Card 1 Interface					
BE17	UIM1_VCC	-	Power supply for the SIM 1	1.8/2.95 V	
BD18	UIM1_IO	O	SIM 1 Data I/O	1.8/2.95 V	
BC19	UIM1_DET	I	SIM 1 presence detection	1.8V	
BD20	UIM1_RST	O	SIM 1 reset	1.8/2.95 V	
BE19	UIM1_CLK	O	SIM 1 clock	1.8/2.95 V	

Table 48: SIM Card 2 Interface

Pin	Signal	I/O	Function	Type	Comment
SIM Card 2 Interface					

Pin	Signal	I/O	Function	Type	Comment
BE13	UIM2_VCC	-	Power supply for the SIM 2	1.8 V	
BD14	UIM2_IO	O	SIM 2 Data I/O	1.8 V	
BC17	UIM2_DET	I	SIM 2 presence detection	1.8 V	
BD16	UIM2_RST	O	SIM 2 reset	1.8 V	
BE15	UIM2_CLK	O	SIM 2 clock	1.8 V	
BC15	RFU	-	-	-	

Note:

- The UIM_DET pin is set to active low (inserted) by default.
- So, FE990B will detect the SIM card insertion when UIM_DET input is changed from logic 1 to a logic 0.
- If it is required to change UIM_DET pin to active high (inserted), please refer to AT#SIMINCFG of FE990B AT commands reference guide.
- To change the default value stored within the firmware without sending AT commands at each power up, please contact Telit technical support.

6.6.3.1 SIM Schematic Example

The diagram below shows how the SIM part of the application interface should be designed.

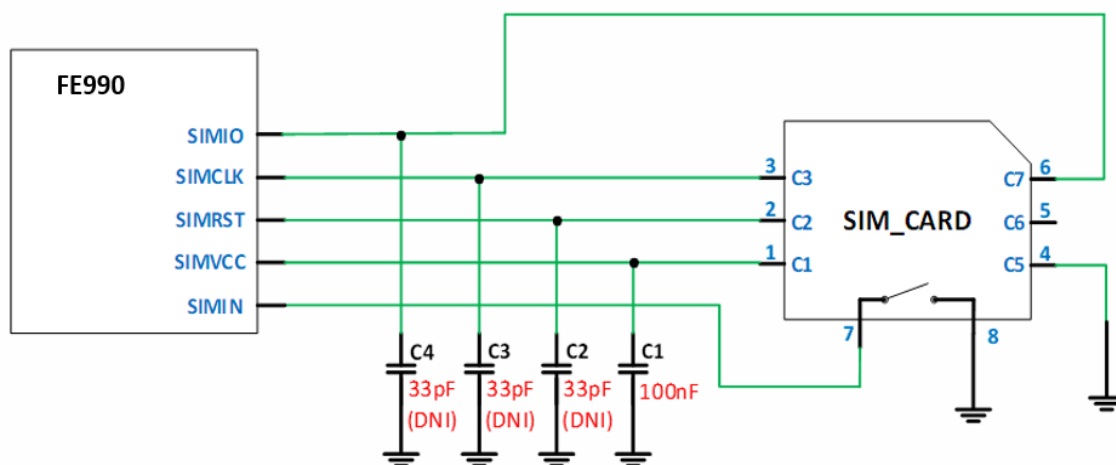


Figure 18: SIM Schematic Example

Note:

The FE990B module contains an internal pull-up resistor on SIMIO. It is not necessary to install an external pull-up resistor.

6.6.3.2 eSIM

FE990B module includes a pad for an optional embedded SIM (MFF-XS, DFN-8 package). Customers interested in using an embedded SIM mounted on the FE990B can contact Telit Technical Support, refer to section [2.3 Contact Information, Support](#).

6.6.4 UART

The serial port generally serves as a secondary interface between the FE990B module and OEM hardware. The module offers the following serial ports:

- **Main UART Interface:** Supports a baud rate of 115200 bps and is used for AT command communication. It also supports RTS and CTS hardware flow control.
- **Debug UART Interface:** Supports a baud rate of 115200 bps and is used for console logging.
- **COEX UART Interface:** Facilitates WWAN/WLAN coexistence.

Table 49: Main UART

Pin	Signal	I/O	Function	Type	Comment
Main UART					
G13	UART1_TX	I	UART1 transmit	1.8 V	
E12	UART1_RX	O	UART1 receive	1.8 V	
C13	UART1_CTS	O	UART1 Clear to Send (CTS)	1.8 V	
E14	UART1_RTS	I	UART1 Request to Send (RTS)	1.8 V	
C9	UART1_DTR	I	UART Input for Data terminal ready (DTR)	1.8 V	
C11	UART1_DCD	O	UART Output for Data Carrier Detect (DCD)	1.8 V	
E10	UART1_DSR	O	UART Output for Data Set Ready (DSR)	1.8 V	
G11	UART1_RI	O	UART Output for Ring Indication (RI)	1.8 V	

Table 50: Debug UART

Pin	Signal	I/O	Function	Type	Comment
DBG UART					
BA10	DEBUG_UART_TX	O	Debug UART transmit	1.8 V	
AY11	DEBUG_UART_RX	I	Debug UART receive	1.8 V	

Table 51: Bluetooth UART (TBD)

Pin	Signal	I/O	Function	Type	Comment
BT UART					
G17	BT_UART_TXD	I	Bluetooth UART Output for Transmit	1.8 V	
E16	BT_UART_RXD	O	Bluetooth UART Input for Receive	1.8 V	
G19	BT_UART_CTS_N	O	Bluetooth UART Output for Clear to Send	1.8 V	
E18	BT_UART_RTS_N	I	Bluetooth UART Input for Request to Send	1.8 V	

Table 52: COEX UART

Pin	Signal	I/O	Function	Type	Comment
COEX UART					
G25	COEX_UART_RX	I	Coexistence UART receive	1.8 V	TBD
E26	COEX_UART_TX	O	Coexistence UART transmit	1.8 V	TBD

Note: The Debug UART is used as the SW main debug console. It is required to place test points on this interface, even if not used.

Note: The DTR pin is used to control the UART and system sleep. Pulling the DTR pin down prevents the UART and the entire module from entering low-power mode. DTR can be left floating if not used (DTR is internally pulled high).

Note: The FE990Bxx series supports BT/Wi-Fi and is only compatible with Qualcomm's QFW71x4 and WCN785x chipsets.

Note: For minimal implementations, only the TXD and RXD lines need be connected, while other lines can be left open provided a software flow control is implemented.

Warning: When using the I2C2 interface, the BT_UART interface is not available. When using the BT_UART interface, the I2C2 interface is not available.

The FE990B provides 1.8 V UART interfaces. If the application uses a 3.3 V UART interface, a level shifter must be used.

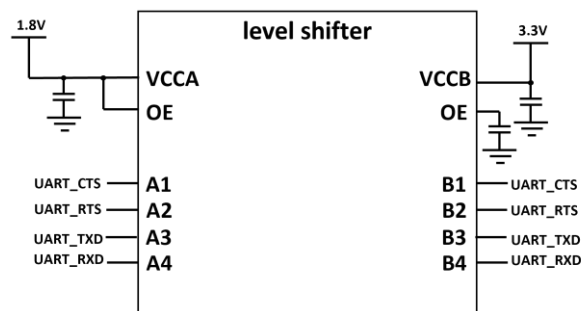


Figure 19: Level Shifter Schematic Example for UART

6.6.4.1 RS232 Level Translation

To interface the FE990B with a PC COM port or an RS232 (EIA/TIA-232) application, a level translator is required. This level translator must perform the following actions:

- Invert the electrical signal in both directions.
- Change the level from 0/1.8 V to ± 15 V.

The RS232 UART 16450, 16550, 16650 and 16750 chipsets accept signals with lower levels on the RS232 side (EIA/TIA-562), allowing a lower voltage-multiplying ratio on the level translator. Note that the negative signal voltage must be less than 0 V and hence some sort of level translation is always required.

The easiest way to translate levels and invert the signal is by using a single chip-level translator. There are different translator chips available on the market, differing in the number of drivers and receivers and in the levels. Please make sure to integrate a true RS232 level translator, not a RS485 or other standards.

By convention, the driver is the level translator from the 0 – 1.8 V UART to the RS232 level. The receiver is the translator from the RS232 level to 0 – 1.8 V UART. To translate the whole set of control lines of the UART, the following is required:

- 2 drivers
- 2 receivers

Warning: The digital input lines, operating at 1.8 V CMOS levels, have an absolute maximum input voltage of 2.0 V. The level translator IC outputs on the module side (i.e. FE990B inputs) will damage module inputs if the level translator is powered with +3.8 V power.

So, the level translator IC must be powered by a dedicated +1.8 V power supply.

As an example, RS232 level adaption circuitry could use a MAXIM transceiver (MAX218).

In this case, the chip can translate directly from 1.8 V to the RS232 levels (example on 4 signals only).

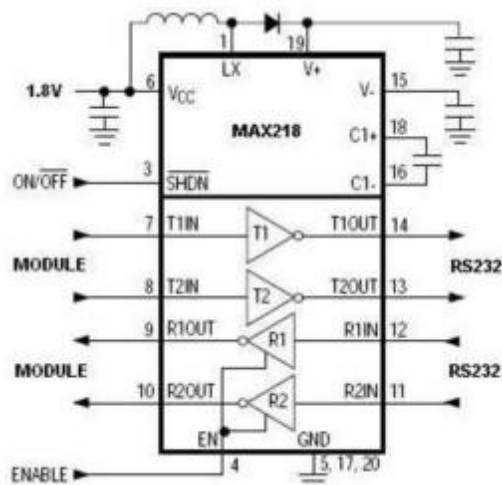


Figure 20: RS232 Level Adaptation Circuitry Example

Note: In this case, the length of the lines on the application must be taken into account to avoid problems in the case of high-speed rates on RS232.

The RS232 serial port lines are usually connected to a DB9 connector as shown in the below figure. Signal names and directions are named and defined from the DTE point of view.

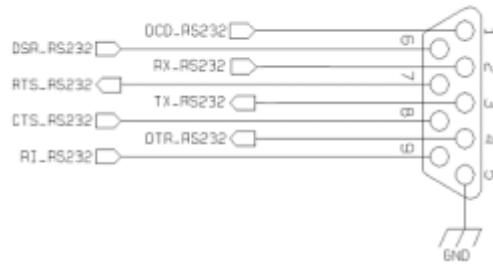


Figure 21: RS232 Serial Port Lines Connection Layout

6.6.5 USXGMII

The FE990 family supports the following functions.

- Support two ethernet media access controllers (EMAC).
- USXGMII, OC-SGMII and SGMII interfaces are supported on each EMAC
 - USXGMII: 10G mode
 - OC-SGMII: 2.5G/1G/100M speeds support
 - SGMII: 1G/100M speeds support
- RTL8261B PHY chip can be connected on USXGMII_0 (EMAC0).
- QEP8121 PHY chip can be connected on USXGMII_1 (EMAC1).
- If HW design has only one ethernet transceiver PHY, the PHY chip should be connected to USXGMII_0 (EMAC0)
- If HW design has two ethernet transceiver PHY's, High data rate (10G) PHY should be connected on USXGMII_0 (EMAC0), and lower data rate PHY should be connected on USXGMII_1 (EMAC1).

Note: #ETHEN should be set to 1 for EMAC activation, and Manual reboot is required.
If different PHY chip is used, please consult Telit Cinterion.



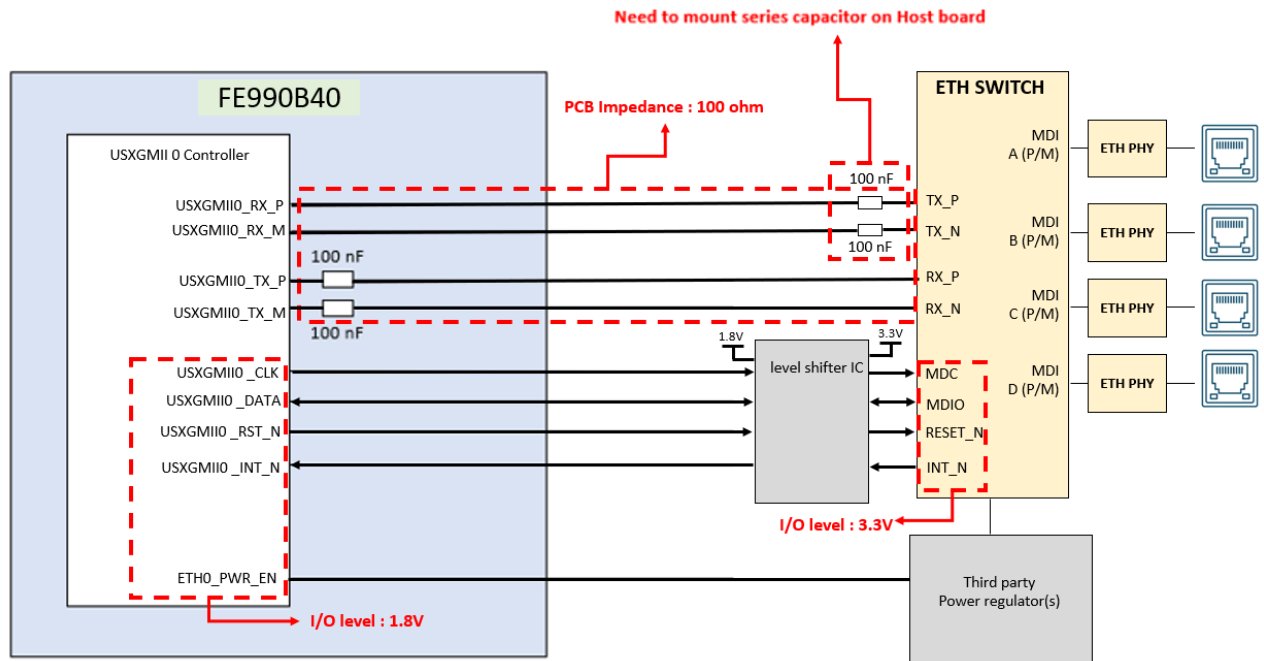


Figure 22: Connection for Ethernet Interface

Note:

* 1.8 V pull-up resistors are required on lines ETH_MDIO, ETH_RST, and ETH_INT.

Regarding the pull-up resistors value, please follow the ethernet PHY chipset guidelines.

Warning:

ETH0_MDC, ETH0_MDIO, ETH0_RST, and ETH0_INT are dedicated to USXGMII0/Ethernet 0 interface. They cannot be used for the USXGMII1/Ethernet 1 interface.

ETH1_MDC, ETH1_MDIO, ETH1_RST, and ETH1_INT are dedicated to USXGMII1/Ethernet 1 interface. They cannot be used for the USXGMII0/Ethernet 0 interface.

Table 53: Ethernet MAC

Pin	Signal	I/O	Function	Type	Comment
USXGMII					
BA30	USXGMII_0_CLK	O	MDIO Interface Clock for ETH0 PHY		
AY33	USXGMII_0_INT_N	I	Interrupts input from Ethernet PHY 0		
BE33	USXGMII_0_RX_P	I	USXGMII 0 receive – plus	AI	Float all signals if USXGMII is unused.
BD34	USXGMII_0_RX_M	I	USXGMII 0 receive – minus	AI	
BE31	USXGMII_0_TX_P	O	USXGMII 0 transmit – plus	AO	
BD32	USXGMII_0_TX_M	O	USXGMII 0 transmit – minus	AO	
AY31	USXGMII_0_RST_N	O	Reset for ETH0 PHY		
BA32	USXGMII_0_DATA	I/O	MDIO data for ETH0 PHY		
BA34	USXGMII_1_CLK	O	MDIO Interface Clock for ETH1 PHY		

Pin	Signal	I/O	Function	Type	Comment
AY37	USXGMII_1_INT_N	I	Interrupts input from Ethernet PHY 1		
BE37	USXGMII_1_RX_P	I	USXGMII 1 receive – plus	AI	Float all signals if USXGMII is unused.
BD38	USXGMII_1_RX_M	I	USXGMII 1 receive – minus	AI	
BE35	USXGMII_1_TX_P	O	USXGMII 1 transmit – plus	AO	
BD36	USXGMII_1_TX_M	O	USXGMII 1 transmit – minus	AO	
AY35	USXGMII_1_RST_N	O	Reset for ETH1 PHY		
BA36	USXGMII_1_DATA	I/O	MDIO data for ETH1 PHY		
BC31	ETH0_PWR_EN	O	Enables the power regulators for ethernet PHY 0	1.8 V	Ethernet PHY Control
BC35	ETH1_PWR_EN	O	Enables the power regulators for ethernet PHY 1	1.8 V	Ethernet PHY Control
BA38	PPS_ETH_PHY	O	Pulse per second (PPS) signal for Ethernet PHY	1.8 V	

6.6.5.1 Ethernet Layout Guidelines

The following guidelines will provide general guidelines for the Ethernet interface to improve signal integrity.

- SGMII/OC-SGMII/USXGMII signals must be protected from noisy signals (clocks, SMPS, and so forth)
- Pay extra attention to crosstalk, ISI, and intraplane skew and impedance discontinuities.
- SGMII/OC-SGMII/USXGMII Tx AC coupling capacitors are better placed close to the source or receiver side to keep good SI of route on PCB. (It should be 100 nF.)
- To maintain impedance balance, maintain positive and negative traces as balanced as possible in terms of the signal and its return path.
- Trace length matching between the reference clock, Tx, and Rx pairs are not required.

External capacitors should also keep differential traces. Ensure not to stagger the capacitors. This can affect the differential integrity of the design and can create EMI.

Table 54: SGMII Layout Constraints

Type of guidance	Guideline	
General	Data rate	1.25 Gbps
	Insertion loss at 625 MHz	-4.375 dB (no equalization)
	Impedance*	75-100 ohms ($\pm 10\%$)
	Max bus length	Appr. 508 mm
Length matching	Intra length match	< 0.7 mm
Isolation	Tx to Rx at 625 MHz	-30 dB
Spacing	To all other signals	Stripline: 3 x line width
	Tx lane to Rx lane	Stripline: 2 x line width
Component	DC Blocking Capacitor	100 nF

Table 55: OC-SGMII Layout Constraints

Type of guidance	Guideline	
General	Data rate	3.125 Gbps
	Insertion loss at 1.56 GHz	-2.3 dB (no equalization)
	Impedance*	75-100 ohms ($\pm 10\%$)
	Max bus length	Appr. 203.2 mm
Length matching	Intra length match	< 0.7 mm
Spacing	To all other signals	Stripline: 3 x line width Microstrip: 4.5 x line width
	Tx lane to Rx lane	Stripline: 2 x line width Microstrip: 4.5 x line width
Component	DC Blocking Capacitor	100 nF

Table 56: USXGMII Layout Constraints

Type of guidance	Guideline	
General	Data rate	10.3125 Gbps
	Insertion loss at 5.5 GHz	-6 dB (Equalization)
	Impedance*	90-110 ohms ($\pm 10\%$)
	Max bus length	Appr. 144 mm
Length matching	Intra length match	< 0.7 mm
Spacing	To all other signals	4 x line width
	Tx lane to Rx lane	4 x line width
Component	DC Blocking Capacitor	100 nF

Note: * FE990Bxx module has 100 ohm impedance.

Table 57: USXGMII Trace Length

PAD	Signal	Length (mm)	Difference (mm)	Note
USXGMII 0				
BE33	USXGMII_0_RX_P	30.737	0.14	100 ohm
BD34	USXGMII_0_RX_M	30.597		
BE31	USXGMII_0_TX_P	30.736	0.04	
BD32	USXGMII_0_TX_M	30.696		
USXGMII 1				
BE37	USXGMII_1_RX_P	32.033	0.077	100 ohm
BD38	USXGMII_1_RX_M	32.11		
BE35	USXGMII_1_TX_P	30.911	0.005	
BD36	USXGMII_1_TX_M	30.906		

6.7 Peripheral Ports

In addition to the FE990B serial ports, the FE990B supports the following peripheral ports:

- SPI – Serial Peripheral Interface
- I2C – Inter – integrated circuit
- SD/MMC Card Interface
- SDIO Interface

6.7.1 SPI

The FE990B SPI supports the following:

- Master mode only
- 1.8 V CMOS level
- Up to 50 MHz clock rate

Note: The FE990B module supports master mode only and cannot be configured as slave mode.

Table 58: SPI

Pin	Signal	I/O	Function	Type	Comment
SPI					
M5	SPI_CLK	O	SPI Clock output	1.8V	
K5	SPI_CS_N	O	SPI Chip select output	1.8V	
N7	SPI_MISO	I	SPI data Master Input Slave Output	1.8V	
L7	SPI_MOSI	O	SPI data Master Output Slave Input	1.8V	

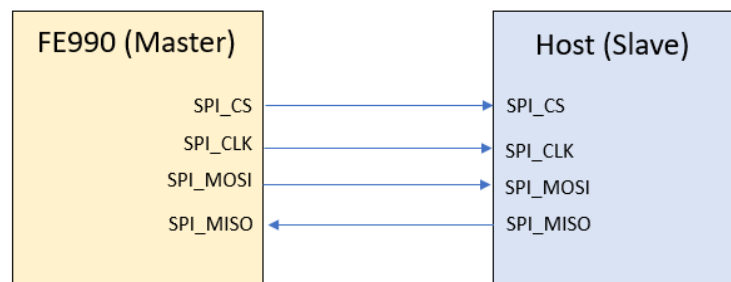


Figure 23: SPI Signal Connectivity

Regarding the 3.3 V, please use a level translator.

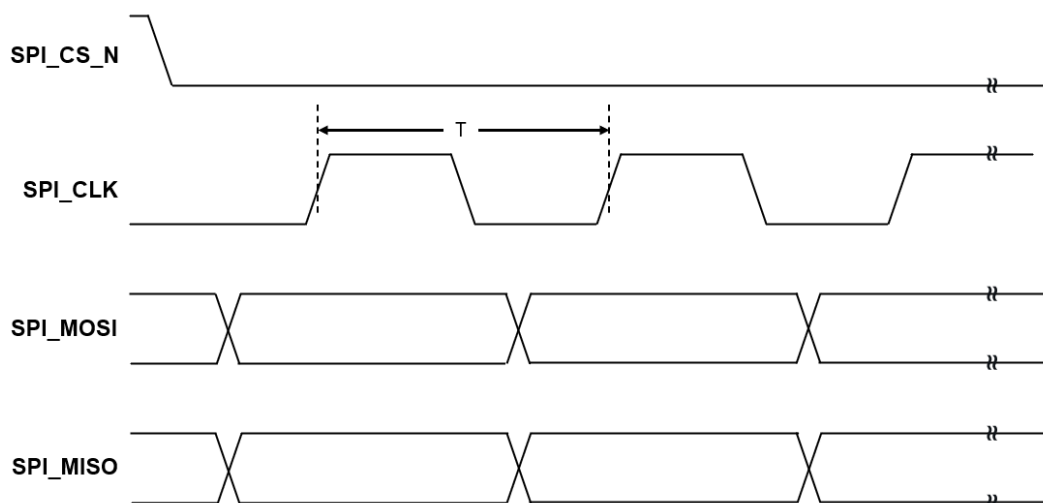


Figure 24: SPI master timing

Table 59: SPI master timing

Parameter	Description	Comment
T	SPI clock period 50 MHz maximum	The maximum clock period includes 1% jitter of maximum frequency

6.7.2 I2C

FE990B supports an I2C interface; the table below lists the I2C signals.

Table 60: I2C

Pin	Signal	I/O	Function	Type	Comment
I2C					
T7	I2C1_SCL	OD	I2C1 serial clock	1.8V	Internal PU (2.2 K)
S5	I2C1_SDA	OD	I2C1 serial data	1.8V	Internal PU (2.2 K)
R7	I2C2_SCL	OD	I2C2 serial clock	1.8V	Internal PU (2.2 K)
P5	I2C2_SDA	OD	I2C2 serial data	1.8V	Internal PU (2.2 K)

Warning: When using the I2C2 interface, the BT_UART interface is not available.
When using the BT_UART interface, the I2C2 interface is not available.

6.7.3 SDC/eMMC 5.1

The FE990B provides an SD port supporting SD 3.0 specification, which can be used to support standard SD/eMMC 5.1 memory cards with the following features:

- Clock output up to 200 MHz for SD card; up to 100 MHz for eMMC 5.1.
- 1.8 V or 2.95 V dual-voltage operation.
- Support for SDIO host mode.

Table 61: SD Card

Pin	Signal	I/O	Function	Type	Comment
SDC					
N49	SDC_CLK	O	Secure digital controller clock	1.8 V	If unused, keep it open.
M50	SDC_CMD	I/O	Secure digital controller command	1.8 V	If unused, keep it open.
G51	SDC_DATA_0	I/O	Secure digital controller data bit 0	1.8 V	If unused, keep it open.
H50	SDC_DATA_1	I/O	Secure digital controller data bit 1	1.8 V	If unused, keep it open.
J51	SDC_DATA_2	I/O	Secure digital controller data bit 2	1.8 V	If unused, keep it open.
K50	SDC_DATA_3	I/O	Secure digital controller data bit 3	1.8 V	If unused, keep it open.
N45	SDC_DET	I	SD card detect	1.8 V	Internal PU (470 K)
P47	SDC_VSEL	O	Selects the voltage of the LDO that powers the VCCB pin of the SD card level shifter	1.8 V	If unused, keep it open.
R45	SDC_VDD	I	Power supply for SDC	1.8 V	2.95 V needs an external Level shifter. If unused, connect to VDD_IO
L45	SDC_PWR_EN	O	SDC power enable	1.8 V	

FE990

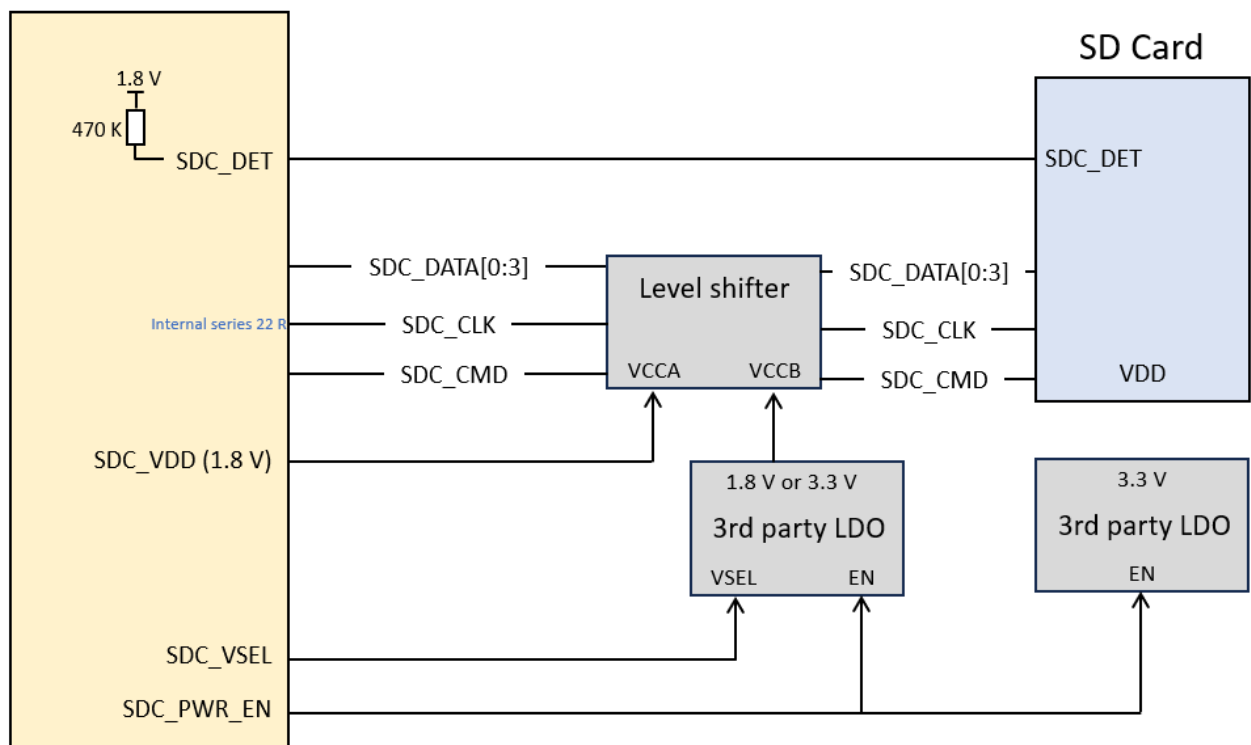


Figure 25: SDC Connectivity

Note: The card detection input has a built-in pull-up resistor, and the clock line has an internal series resistor.

For ESD protection, add a TVS diode to each pin, considering parasitic capacitance.

SDC and eMMC cannot be used simultaneously.

Table 62: eMMC 5.1

Pin	Signal	I/O	Function	Type	Comment
SDC					
N49	SDC_CLK	O	Secure digital controller clock	1.8 V	If unused, keep it open.
M50	SDC_CMD	I/O	Secure digital controller command	1.8 V	If unused, keep it open.
L51	SDC_RCLK	I	SDC return clock	1.8 V	If unused, keep it open.
BD10	RESOUT_N	O	Reset output	1.8 V	Do not populate any pull-up/down resistor.
G51	SDC_DATA_0	I/O	Secure digital controller data bit 0	1.8 V	If unused, keep it open.
H50	SDC_DATA_1	I/O	Secure digital controller data bit 1	1.8 V	If unused, keep it open.
J51	SDC_DATA_2	I/O	Secure digital controller data bit 2	1.8 V	If unused, keep it open.
K50	SDC_DATA_3	I/O	Secure digital controller data bit 3	1.8 V	If unused, keep it open.
J49	SDC_DATA4	I/O	Secure digital controller data bit 4	1.8/2.95 V	If unused, keep it open.
K47	SDC_DATA5	I/O	Secure digital controller data bit 5	1.8/2.95 V	If unused, keep it open.
L49	SDC_DATA6	I/O	Secure digital controller data bit 6	1.8/2.95 V	If unused, keep it open.
M47	SDC_DATA7	I/O	Secure digital controller data bit 7	1.8/2.95 V	If unused, keep it open.

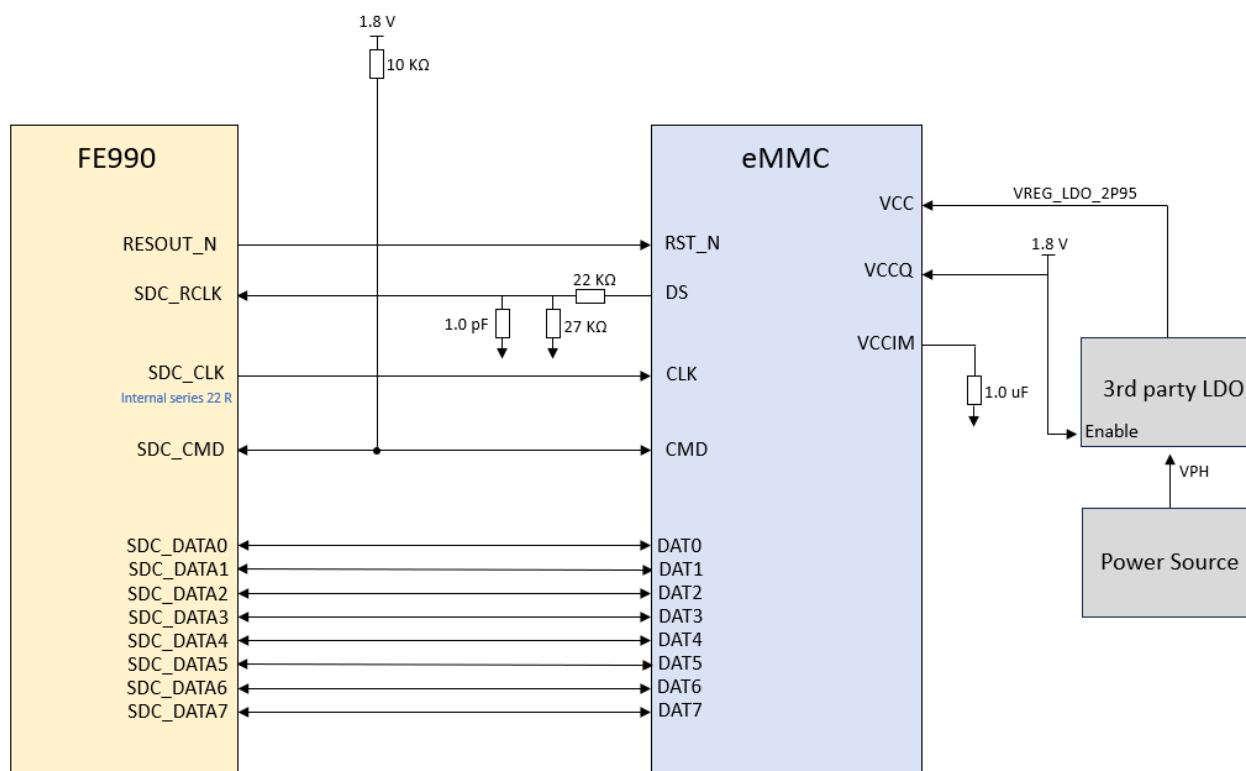


Figure 26: eMMC Connectivity

Danger: Do NOT populate any pull-up/down resistor on RESOUT_N.

6.7.3.1 SDC/eMMC 5.1 Layout Guidelines

The following guidelines will provide general guidelines for the SD/eMMC interface to improve signal integrity.

- SD/eMMC signals must be protected from noisy signals (clocks, SMPS, and so forth)
- Keep the trace length between SDC_CLK and SDC_DATA [0:3]/SDC_CMD less than 6 mm (50 MHz DDR) / 2mm (100 MHz SDR).

Table 63: SDC External SD Card Routing Constraints

Type of guidance	Guideline		
Clock frequency	50 MHz DDR / 100 MHz SDR	208 MHz	
Data rate	50 MBps	104 Mbps	
SD card capacitive load	10 pF	5 pF*	*For UHS104 modes, if card capacitance is > 5 nF, then trace length must be reduced accordingly.
Impedance	45 ohm		
Clock to data length matching	6 mm	2 mm	
Bus length*	< 150 mm	< 50 mm	
Spacing	1.5 x line width		

Note: *Guidance of bus length is based on the SD card I/O driver capability and maximum load capacitance per SD card specifications.

Table 64: SDC Trace Length

PAD	Signal	Length (mm)	Difference (mm)	NOTE
N49	SDC_CLK	8.203	N/A	45 ohm
M50	SDC_CMD	6.592		
G51	SDC_DATA_0	8.13		
H50	SDC_DATA_1	8.225		
J51	SDC_DATA_2	8.319		
K50	SDC_DATA_3	8.104		

Table 65: eMMC 5.1 Routing Constraints

Type of guidance	Guideline
Clock frequency	200 MHz
Data rate	400 MBps
Max bus length	100 mm
Impedance	45 ohm
Clock to data / CMD length matching	6 mm
Spacing	2.5 x line width

Table 66: eMMC Trace Length

PAD	Signal	Length (mm)	Difference (mm)	NOTE
N49	SDC_CLK	8.203	N/A	45 ohm
M50	SDC_CMD	6.592		
L51	SDC_RCLK	6.513		
BD10	RESOUT_N	N/A		
G51	SDC_DATA_0	8.13		
H50	SDC_DATA_1	8.225		
J51	SDC_DATA_2	8.319		
K50	SDC_DATA_3	8.104		
J49	SDC_DATA4	8.272		
K47	SDC_DATA5	8.161		
L49	SDC_DATA6	8.144		
M47	SDC_DATA7	8.192		

6.7.4 I2S/PCM

The FE990B module supports a digital audio interface.

Table 67: Codec I2S/PCM

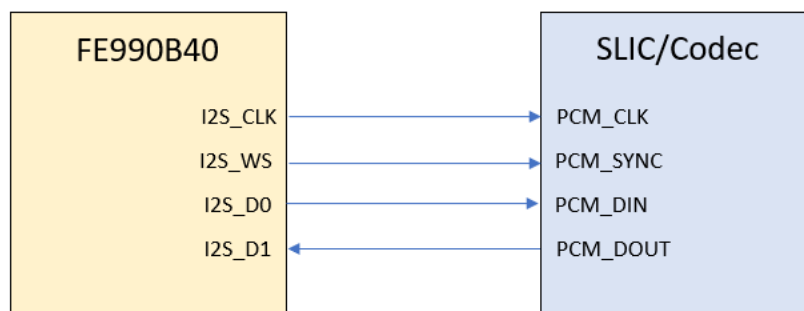
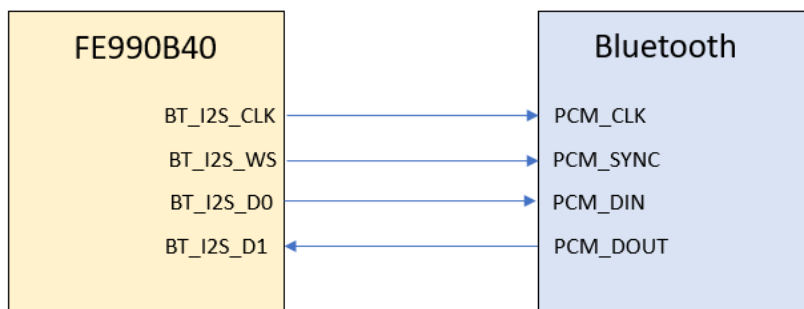
Pin	Signal	I/O	Function	Type	Comment
I2S					
AF7	I2S_D0	O	I2S Data Input	1.8 V	PCM_DOUT

Pin	Signal	I/O	Function	Type	Comment
AE5	I2S_D1	I	I2S Data Output	1.8 V	PCM_DIN
AD7	I2S_SCK	I/O	I2S clock	1.8 V	PCM_CLK
AC5	I2S_WS	I/O	I2S word select	1.8 V	PCM_SYNC

Table 68: Bluetooth I2S/PCM (TBD)

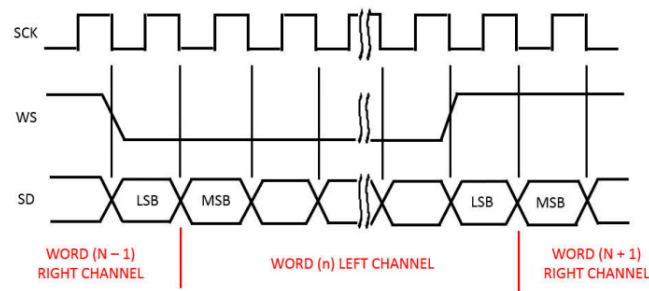
Pin	Signal	I/O	Function	Type	Comment
BT I2S					
AH3	BT_EN	O	Bluetooth enable	1.8 V	
C23	BT_I2S_WS (BT_PCM_SYNC)	I/O	Bluetooth I2S word select	1.8 V	
E22	BT_I2S_D0 (BT_PCM_DOUT)	O	Bluetooth I2S DATA Input	1.8 V	
C21	BT_I2S_D1 (BT_PCM_DIN)	I	Bluetooth I2S DATA Output	1.8 V	
E24	BT_I2S_SCK (BT_PCM_CLK)	I/O	Bluetooth I2S continuous serial clock	1.8 V	

Note: In master mode, SYNC and CLK are output signal.
In slave mode, SYNC and CLK are an input signal.


Figure 27: PCM interface for Codec

Figure 28: PCM interface for BT

6.7.4.1 I2S Digital Audio Diagram

High-level I2S timing



I2S timing details – Tx & Rx

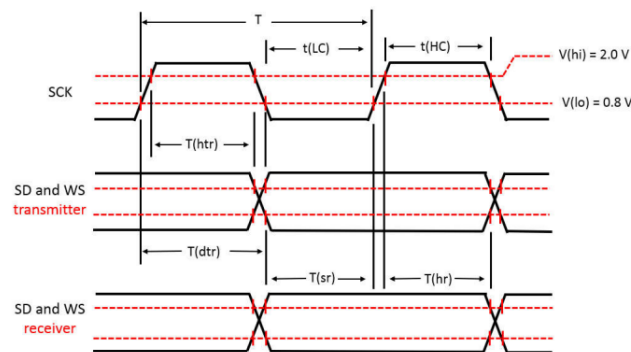


Figure 29: I2S Timing Diagram

Table 69: I2S Interface Timing

Parameter	Description	Min	Typ	Max	Unit
Using internal SCK					
f	Frequency	-	-	12.288	MHz
T	Clock period	81.380	-	-	ns
t(HC)	Clock high	0.45*T	-	0.55*T	ns
t(LC)	Clock low	0.45*T	-	0.55*T	ns
t(sr)	SD and WS input setup time	16.276	-	-	ns
t(hr)	SD and WS input hold time	0	-	-	ns
t(dtr)	SD and WS output delay	-	-	20.34	ns

6.7.4.2 PCM Digital Audio Diagram

The PCM interface is configured as master or slave. In each case, the PCM_IN pin is the data receive terminal (an input), and the PCM_OUT pin is the data transmit terminal (an output). The clock and sync pins function as input or output, depending on whether the FE990B PCM interface is configured as a master or slave:

When the FE990B PCM interface is the master, PCM_CLK and PCM_SYNC are outputs from the FE990B to the PCM bus slave(s).

When the FE990B PCM interface is the slave, PCM_CLK and PCM_SYNC are inputs to the FE990Bxx from the PCM bus master.

FE990Bxx supports 16-bit linear PCM format.

2048 kHz (default)

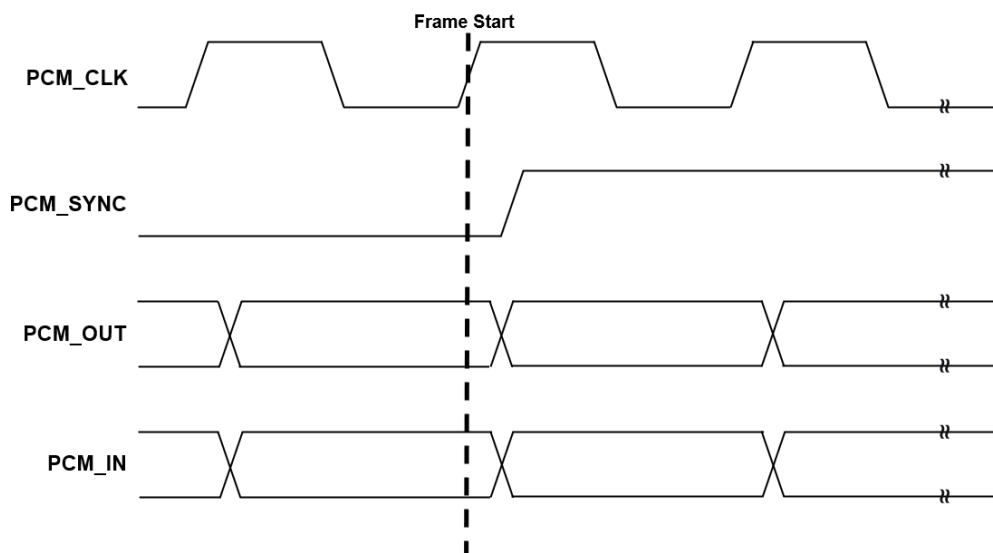


Figure 30: PCM interface timing (master)

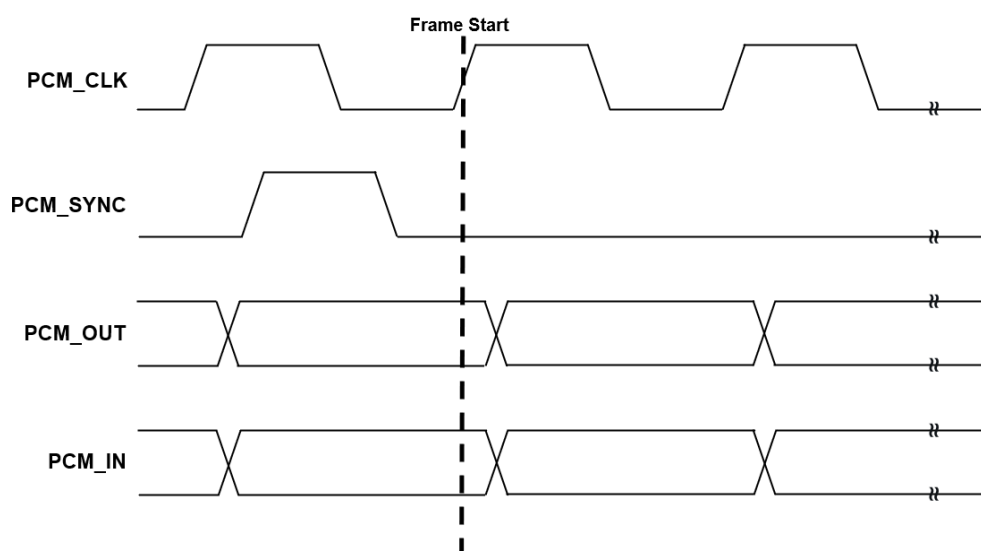


Figure 31: PCM interface timing (slave)

6.8 General Purpose I/O

The general-purpose I/O pins can be configured to act in three different ways:

- Input
- Output
- Dedicated function (Customer requirement)

Input pins can only report digital values (high or low) present on the pin at the read time. Output pins can only be set or the pin level can be queried.

Table 70: FE990B Available GPIO

PAD	Signal	I/O	Description	Type	NOTE
X3	TGPIO1	I/O	General Purpose I/O	1.8V	
Y5	TGPIO2	I/O	General Purpose I/O	1.8V	
X7	TGPIO3	I/O	General Purpose I/O	1.8V	
BD12	TGPIO4	I/O	General Purpose I/O	1.8V	

PAD	Signal	I/O	Description	Type	NOTE
BC13	TGPIO5	I/O	General Purpose I/O	1.8V	
BA16	TGPIO6	I/O	General Purpose I/O	1.8V	

6.8.1 Using a GPIO pad as Input

GPIO pins, when used as inputs, can be tied to a digital output of another device and report its status, provided the device interface levels are compatible with the GPIO 1.8V CMOS levels. If a digital output of a device is tied to GPIO input, the pin has interface levels different than 1.8V CMOS. It can be buffered with an open-collector transistor with a 47K ohm pull-up resistor to 1.8V.

6.8.2 Using a GPIO as Output

GPIO pins, when used as output, can drive 1.8V CMOS digital devices or compatible hardware. When set as outputs, the pins have a push-pull output, and therefore, the pull-up resistor can be omitted.

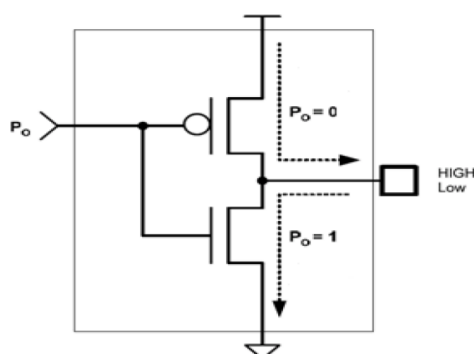


Figure 32: GPIO Output Pad Equivalent Circuit

6.9 Miscellaneous Functions

6.9.1 DPR

This signal is an input directly to the FE990B module from a suitable SAR sensor. Then the FE990B module will reduce the output tx power. DPR function is not available yet: specific implementation will be determined on customer request. For further information on the DPR function on the FE990B module, contact Telit Technical Support.

Refer to the section 2.3 Contact Information, Support

6.9.2 LED

The LED signal drives the LED output. The recommended LED connection is the following:

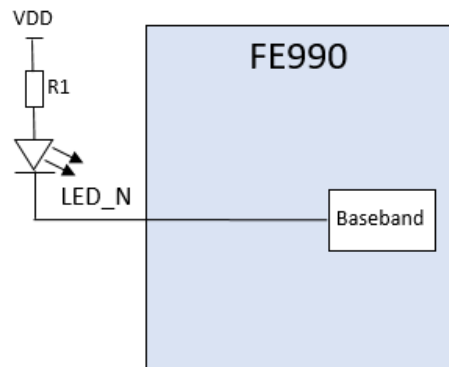


Figure 33: Recommended LED Connection

R1 and VDD determine the LED brightness and forward current.

When VDD is 3.8 V and the LED's forward voltage is 2.0 V, the recommended R1 value ranges from 66 to 250 ohms.

However, the resistor value must be calculated considering the LED specifications. It is recommended to use VDD below the VPH_PWR level.

Note: If the LED function is enabled and an LED is connected to the LED_N pin, current consumption may be slightly increased. And the current sinking mode (up to 10 mA) can be supported.

6.9.3 ADC Converter

The FE990B module provides two on-board 16-bit Analog to Digital Converters. Each ADC reads the voltage level applied on the relevant pin, converts it and stores it into an 16-bit word.

Table 71: ADC

Pin	Signal	I/O	Function	Type	Comment
ADC					
E34	ADC1	A/I	Analog Digital Converter 1 Input	Analog Input	
E36	ADC2	A/I	Analog Digital Converter 2 Input	Analog Input	

Table 72: Characteristics of ADC

Parameter	Min	Typ	Max	Units
Input voltage range	0.1	-	1.875	V
ADC Resolution	-	64.879	-	uV
ADC Sample clock	-	4.8	-	MHz

6.9.3.1 Using the ADC

AT command is available to use the ADC function.

The command is AT#ADC?. The read value is expressed in mV.

Please refer to FE990B AT command user guide for the full description of this function.

6.9.4 DAC Converter (TBD)

The FE990B module provides a Digital to Analog Converter. The DAC_OUT is available on pad C39 of the FE990B module.

The onboard DAC is in the range from 0 to 1023.
However, an external low-pass filter is necessary.

Table 73: DAC

Parameter	Min	Max	Units
Voltage range (filtered)	0	1.8	Volts
Range	0	1023	Steps

The precision is 1023 steps, so if we consider that the maximum voltage is 1.8 V, the integrated voltage could be calculated with the following formula:

Integrated output voltage = $1.8 * \text{value} / 1023$

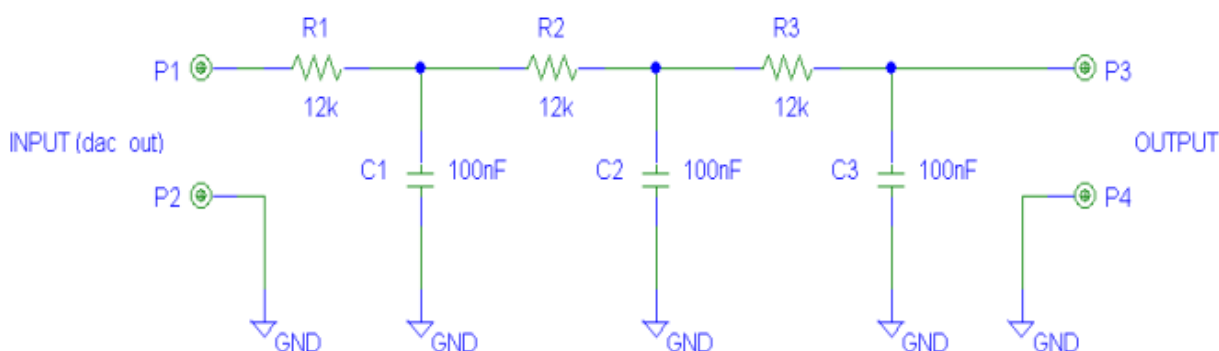
DAC line must be integrated (for example with a low band pass filter) to obtain an analog voltage.

6.9.4.1 Enabling DAC

AT command is available to use the DAC function.

Please refer to FE990B AT command user guide for the full description of this function.

6.9.4.2 Low Pass Filter Example


Figure 34: Low Pass Filter Example

6.10 Forced USB Boot

Emergency boot download mode is case of corrupted boot image has been flashed into the device or in case all other recovery modes failed to work.

The emergency download mode is triggered by FORCED_USB_BOOT signal (Pad AA47). Asserting this signal high (1.8 V) during boot will force the system into emergency download.

In certain cases, when firmware upgrade is performed FORCED_USB_BOOT pin must be set to 1.8V during power-on of FE990B.

Table 74: Miscellaneous Functions

Pin	Signal	I/O	Function	Type	Comment
Miscellaneous Functions					
AA47	USB_BOOT	I	Forced USB BOOT – emergency download	1.8 V	

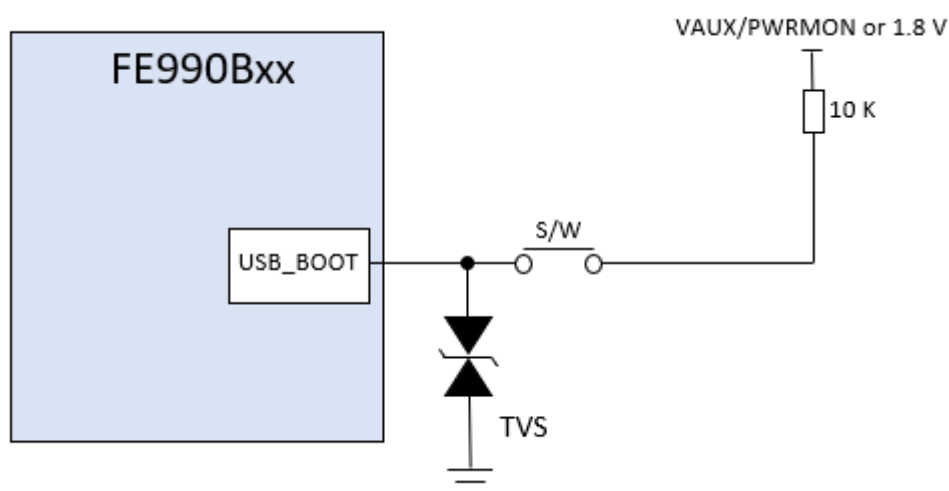


Figure 35: Example of Forced USB BOOT

6.11 VAUX Power Output

A regulated power supply output is provided to supply small peripherals from the module.

This output is active when the module is ON and turns OFF when the module is shut down.

The operating range characteristics of the supply are as follows:

Table 75: Operating Range – VAUX Power Supply

Parameter	Min	Typical	Max	Units
Output voltage	1.75	1.80	1.85	Volts
Output current			200	mA
Output bypass capacitor(within the module)			1	uF

6.12 Temperature Monitor Function

The temperature monitor supports temperature monitoring by providing periodic temperature indications. When properly set (see the #TEMPSENS command in FE990B AT command user guide), it raises a GPIO to a high logic level when the maximum temperature is reached.

7 RF Section

7.1 Frequency Bands

Operating frequencies in 5G, LTE, and WCDMA modes conform to 3GPP specifications. The table below lists the FE990B operating frequencies on 5G, LTE, and WCDMA modes.

Table 76: 5G NR Sub-6 Bands

NR BAND	Duplex Mode	Uplink Frequency (MHz)	Downlink Frequency (MHz)	Channels	SCS (KHz)
n1 - 2100	FDD	1920 - 1980	2110 - 2170	Tx: 384000 - 396000 Rx: 422000 - 434000	15
n2 - 1900	FDD	1850 - 1910	1930 - 1990	Tx: 370000 - 382000 Rx: 386000 - 398000	15
n3 - 1800	FDD	1710 - 1785	1805 - 1880	Tx: 342000 - 357000 Rx: 361000 - 376000	15
n5 - 850	FDD	824 - 849	869 - 894	Tx: 164800 - 169800 Rx: 173800 - 178800	15
n7 - 2600	FDD	2500 - 2570	2620 - 2690	Tx: 500000 - 514000 Rx: 524000 - 538000	15
n8 - 900	FDD	880 - 915	925 - 960	Tx: 176000 - 183000 Rx: 185000 - 192000	15
n12 - 700a	FDD	699 - 716	729 - 746	Tx: 139800 - 143200 Rx: 145800 - 149200	15
n13 - 700c	FDD	777 - 787	746 - 756	Tx: 155400 - 157400 Rx: 149200 - 151200	15
n14 - 700PS	FDD	788 - 798	758 - 768	Tx: 157600 - 159600 Rx: 151600 - 153600	15
n20 - 800	FDD	832 - 862	791 - 821	Tx: 166400 - 172400 Rx: 158200 - 164200	15
n25 - 1900+	FDD	1850 - 1915	1930 - 1995	Tx: 370000 - 383000 Rx: 386000 - 399000	15
n26 - 850+	FDD	814 - 849	859 - 894	Tx: 162800 - 169800 Rx: 171800 - 178800	15
n28 - 700 APT	FDD	703 - 748	758 - 803	Tx: 140600 - 149600 Rx: 151600 - 160600	15
n29 - 700d	SDL	N/A	717 - 728	Rx: 143400 - 145600	15
n30 - 2300WCS	FDD	2305 - 2315	2350 - 2360	Tx: 461000 - 463000 Rx: 470000 - 472000	15
n38 - 2600	TDD	2570 - 2620		T/Rx: 514000 - 524000	30
n40 - 2300	TDD	2300 - 2400		T/Rx: 460000 - 480000	30
n41 - 2600+	TDD	2496 - 2690		T/Rx: 499200 - 537996	30
n48 - 3600	TDD	3550 - 3700		T/Rx: 636668 - 646666	30
n66 - AWS-3	FDD	1710 - 1780	2110 - 2200	Tx: 342000 - 356000	15

NR BAND	Duplex Mode	Uplink Frequency (MHz)	Downlink Frequency (MHz)	Channels	SCS (KHz)
				Rx: 422000 - 440000	
n70 – AWS-2	FDD	1695 – 1710	1995 – 2020	Tx: 339000 - 342000 Rx: 399000 - 404000	15
n71 - 600	FDD	663 – 698	617 – 652	Tx: 132600 - 139600 Rx: 123400 - 130400	15
n75 - DL 1500+	SDL	-	1432 - 1517	Rx: 286400 - 303400	15
n76 - DL 1500-	SDL	-	1427 - 1432	Rx: 285400 - 286400	15
n77 - 3700	TDD	3300 - 4200		T/Rx: 620000 - 680000	30
n78 - 3500	TDD	3300 - 3800		T/Rx: 620000 - 653332	30
n79 - 4700	TDD	4400 - 5000		T/Rx: 693334 - 733332	30

Table 77: LTE Bands

E-UTRA BAND	Duplex Mode	Uplink Frequency (MHz)	Downlink Frequency (MHz)	Channels
B1 - 2100	FDD	1920 - 1980	2110 - 2170	Tx: 18000 - 18599 Rx: 0 - 599
B2 - 1900	FDD	1850 – 1910	1930 – 1990	Tx: 18600 - 19199 Rx: 600 - 1199
B3 - 1800+	FDD	1710 - 1785	1805 - 1880	Tx: 19200 - 19949 Rx: 1200 - 1949
B4 - AWS	FDD	1710 – 1755	2110 – 2155	Tx: 19950 - 20399 Rx: 1950 - 2399
B5 - 850	FDD	824 - 849	869 - 894	Tx: 20400 - 20649 Rx: 2400 - 2649
B7 - 2600	FDD	2500 - 2570	2620 - 2690	Tx: 20750 - 21449 Rx: 2750 - 3449
B8 - 900	FDD	880 - 915	925 - 960	Tx: 21450 - 21799 Rx: 3450 - 3799
B12 – 700a	FDD	699 – 716	729 – 746	Tx: 23010 - 23179 Rx: 5010 - 5179
B13 – 700c	FDD	777 – 787	746 – 756	Tx: 23180 - 23279 Rx: 5180 - 5279
B14 – 700PS	FDD	788 – 798	758 – 768	Tx: 23280 - 23379 Rx: 5280 - 5379
B17 – 700b	FDD	704 – 716	734 – 746	Tx: 23730 - 23849 Rx: 5730 - 5849
B18 - 800 Lower	FDD	815 - 830	860 - 875	Tx: 23850 - 23999 Rx: 5850 - 5999
B19 - 800 Upper	FDD	830 - 845	875 - 890	Tx: 24000 - 24149 Rx: 6000 - 6149
B20 - 800 DD	FDD	832 - 862	791 - 821	Tx: 24150 - 24449 Rx: 6150 - 6449
B25 – 1900+	FDD	1850 – 1915	1930 – 1995	Tx: 26040 - 26689

E-UTRA BAND	Duplex Mode	Uplink Frequency (MHz)	Downlink Frequency (MHz)	Channels
				Rx: 8040 - 8689
B26 - 850+	FDD	814 - 849	859 - 894	Tx: 26690 - 27039 Rx: 8690 - 9039
B28 - 700 APT	FDD	703 - 748	758 - 803	Tx: 27210 - 27659 Rx: 9210 - 9659
B29 - 700d	SDL	-	717 - 728	Rx: 9660 - 9769
B30 - 2300WCS	FDD	2305 - 2315	2350 - 2360	Tx: 27660 - 27759 Rx: 9770 - 9869
B32 - 1500 L	SDL	-	1452 - 1496	Rx: 9920 - 10359
B38 - 2600	TDD	2570 - 2620		T/Rx: 37750 - 38249
B40 - 2300	TDD	2300 - 2400		T/Rx: 38650 - 39649
B41 - 2600+	TDD	2496 - 2690		T/Rx: 39650 - 41589
B42 - 3500	TDD	3400 - 3600		T/Rx: 41590 - 43589
B43 - 3700	TDD	3600 - 3800		T/Rx: 43590 - 45589
B48 - 3600	TDD	3550 - 3700		T/Rx: 55240 - 56739
B66 - AWS-3	FDD	1710 - 1780	2110 - 2200	Tx: 131972 - 132671 Rx: 66436 - 67335
B68- 700	FDD	698 - 728	753 - 783	Tx: 132672 - 132971 Rx: 67536 - 67835
B71 - 600	FDD	663 - 698	617 - 652	Tx: 133122 - 133471 Rx: 68586 - 68935

Table 78: WCDMA Bands

UTRA BAND	Duplex Mode	Uplink Frequency (MHz)	Downlink Frequency (MHz)	Channels
B1 - 2100	FDD	1920 - 1980	2110 - 2170	Tx: 9612 - 9888 Rx: 10562 - 10838
B5 - 850	FDD	824 - 849	869 - 894	Tx: 4132 - 4233 Rx: 4357 - 4458
B6 - 850 Japan	FDD	830 - 840	875 - 885	Tx: 4162 - 4188 Rx: 4387 - 4413
B8 - 900	FDD	880 - 915	925 - 960	Tx: 2712 - 2863 Rx: 2937 - 3088
B19 - 800 Japan	FDD	830 - 845	875 - 890	Tx: 312 - 363 Rx: 712 - 763

7.2 CA/MIMO/EN-DC (TBD)

Note: Refer to the FE990B family CA/EN-DC list, XXXXXNTXXXXA (TBD) for detailed combinations of CA and EN-DC.

7.3 RF Performance

The RF performance in 5G, LTE, and WCDMA modes conform to the 3GPP specifications.

7.3.1 Conducted Transmit Output Power

TX power follows the measurement conditions and specifications defined in 3GPP.

Table 79: Conducted Transmit Output Power

Band	Class	RF Power (dBm) Nominal ¹⁾
5G NR Sub-6 n1/n2/n3/n5/n7/n8/n12/n13/n14/n20/n25/n26/n28/n30 ³⁾ /n38/n40/n41/ n48 ²⁾ /n66/n70/n71/n77/n78/n79	3 (0.2 W)	23
5G NR Sub-6 n41/n77/n78/n79/n2 ⁴⁾ /n25 ⁴⁾ /n66 ⁴⁾ /n71 ⁴⁾	2 (0.4 W)	26
5G NR Sub-6 n41 ⁴⁾ /n77 ⁴⁾ /n78 ⁴⁾ /n79 ⁴⁾	1.5 (0.8W)	29
LTE All Bands B1/B2/B3/B4/B5/B7/B8/B12/B13/B14/B17/B18/B19/B20/B25/B26/B28/ B30 ³⁾ /B38/B40/B41/B42 ²⁾ /B43 ²⁾ /B48 ²⁾ /B66/B68/B71	3 (0.2 W)	23
LTE B38/B41/B42/B43	2 (0.4W)	26
3G WCDMA B1/B5/B6/B8/B19	3 (0.2 W)	23

- Note:**
- 1 RF Power Nominal: Max output power tolerance according to 3GPP TS 38.521-1, 3GPP TS 36.521-1 and 3GPP TS 34.121-1 or better.
 - 2 LTE B42, B43, B48 / NR n48 : PC 3 Nominal RF Power 22dBm
These bands may show lower power due to Country-type approval constraints.
 - 3 LTE B30 / NR n30 : PC 3 Nominal RF Power 22dBm
These bands may show lower power due to Country-type approval constraints.
 - 4 n2/n25/n66/n71 PC2 and n41/n77/n78/n79 PC1.5 are achieved via dual Tx.

7.3.2 Conducted Receiver Sensitivity

The sensitivity of the receiver follows the measurement conditions and specifications defined in 3GPP.

Table 80: 3GPP compliance for conducted receiver sensitivity

Mode	3GPP Compliance
5G NR Sub-6	Throughput >95%, According to 3GPP 38.521-1
4G LTE	Throughput >95%, According to 3GPP 36.521-1
3G WCDMA	BER <0.1%, According to 3GPP 34.121-1

Table 81: Typical Conducted Receiver Sensitivity - NR Bands

NR Band	Typical Conducted Rx Sensitivity (dBm) *						
	SCS(kHz)	BW(MHz)	PRx	DRx	MIMO0	MIMO1	Combined
NR FDD n1	15	20	-93.0	-94.0	-93.0	-94.0	-99.5
NR FDD n2	15	20	-95.0	-95.5	-93.0	-94.0	-100.0
NR FDD n3	15	20	-94.0	-94.0	-94.5	-95.0	-100.0
NR FDD n5	15	20	-96.0	-96.0	-97.0	-97.0	-102.5
NR FDD n7	15	20	-94.0	-93.0	-92.0	-91.0	-98.0
NR FDD n8	15	20	-96.5	-96.5	-97.0	-96.5	-102.5
NR FDD n12	15	10	-99.0	-99.0	-99.0	-99.0	-105.0
NR FDD n13	15	10	-99.0	-99.0	-99.0	-99.0	-105.0
NR FDD n14	15	10	-99.0	-99.0	-99.0	-99.0	-105.0
NR FDD n20	15	20	-96.0	-96.5	-96.5	-96.0	-102.5
NR FDD n25	15	20	-95.0	-95.0	-93.0	-94.0	-100.0
NR FDD n26	15	20	-96.0	-96.0	-97.0	-97.0	-102.5
NR FDD n28	15	20	-96.0	-96.0	-96.0	-96.0	-102.0
NR FDD n29	15	10	-99.0	-99.0	-99.0	-98.0	-104.5
NR FDD n30	15	10	-92	-96.0	-96.0	-96.0	-100.5
NR TDD n38	30	20	-93.0	-94.0	-95.0	-92.0	-98.0
NR TDD n40	30	20	-93.0	-92.5	-94.0	-92.0	-98.0
NR TDD n41	30	20	-92.0	-92.0	-94.0	-90.0	-97.0
NR TDD n48	30	20	-95.0	-95.0	-96.0	-94.0	-100.0
NR FDD n66	15	20	-94.0	-93.0	-91.0	-93.0	-98.5
NR FDD n70	15	10	-98.0	-99.0	-96.0	-96.0	-102.5
NR FDD n71	15	20	-96.0	-96.0	-96.0	-94.0	-101.5
NR SDL n75	15	20	-93.0	-94.5	-93.5	-93	-99.5
NR SDL n76	30	5	TBD	TBD	TBD	TBD	TBD
NR TDD n77	30	20	-95.0	-93.0	-93.0	-92.0	-99.0
NR TDD n78	30	20	-96.0	-95.0	-95.0	-94.0	-100.0
NR TDD n79	30	40	-92.5	-92.0	-90.0	-89.0	-96.0

***3.8 Voltage / Room temperature**

Table 82: Typical Conducted Receiver Sensitivity - LTE Bands

E-UTRA Band	Typical Conducted Rx Sensitivity (dBm) *				
	PRX	DRX	MIMO0	MOMO1	Combined
LTE FDD B1	-98.5	-98.5	-97.0	-97.5	-103.5
LTE FDD B2	-97.0	-97.0	-97.0	-97.0	-103.0
LTE FDD B3	-98.5	-98.5	-98.5	-99.0	-104.0
LTE FDD B4	-96.0	-96	-96.0	-96.0	-102.0
LTE FDD B5	-98.5	-98.5	-98.0	-99.0	-104.5
LTE FDD B7	-96.0	-96.0	-94.0	-97.0	-102.0
LTE FDD B8	-99.5	-100.0	-99.5	-100	-105.0
LTE FDD B12	-99.0	-98.5	-97.5	-98.0	-104.0
LTE FDD B13	-99.0	-99.5	-98.0	-99.5	-105.0
LTE FDD B14	-99.0	-99.0	-97.5	-98.5	-104.5
LTE FDD B17	-99.0	-98.5	-97.5	-98.5	-104.0
LTE FDD B18	-99.5	-100	-99.5	-100	-105.5
LTE FDD B19	-99.5	-100	-99.5	-100	-105.5
LTE FDD B20	-99.5	-99.5	-100	-100	-105.5
LTE FDD B25	-97.0	-97.0	-96.0	-96.0	-102.5
LTE FDD B26	-98.5	-98.5	-98.0	-99.5	-105.0
LTE FDD B28	-99.0	-99.5	-99.5	-100	-105.0
LTE SDL B29 ¹⁾	-102.0	-102.0	-100.0	-102.0	-107.0
LTE FDD B30	-95.0	-96.0	-95.0	-96.0	-101.5
LTE SDL B32	-97.5	-97.5	-96.0	-97.0	-103.0
LTE TDD B38	-95.0	-94.0	-94.0	-96	-101.0
LTE TDD B40	-96.5	-96.0	-95.0	-97.0	-101.5
LTE TDD B41	-94.5	-94.0	-92.5	-95.5	-100.0
LTE TDD B42	-97.5	-96.0	-97.0	-96.0	-103.0
LTE TDD B43	-97.0	-95.5	-96.5	-96.5	-102.5
LTE TDD B48	-97.5	-96.0	-97.0	-96.5	-103.0
LTE FDD B66	-96.0	-96.0	-96.0	-96.0	-102.0
LTE FDD B68	-99.5	-99.0	-99.0	-99.5	-105.0
LTE FDD B71	-99.0	-99.0	-97.0	-98.5	-104.5

***3.8 Voltage / Room temperature**

1. B29 DL ONLY 5MBW.

Table 83: Typical Conducted Receiver Sensitivity - WCDMA Bands

UTRA Band	Typical Conducted Rx Sensitivity (dBm) *				
	PRX	DRX	MIMO0	MIMO1	Combined
WCDMA B1	-110	-110	NA	NA	-113
WCDMA B5	-111	-111	NA	NA	-114
WCDMA B6	-111	-111	NA	NA	-114
WCDMA B8	-111	-111	NA	NA	-114
WCDMA B19	-111	-111	NA	NA	-114

*3.8 Voltage / Room temperature

Note: The sensitivity level has a deviation of approximately +/- <2dB, device, and channel because the level shows a typical value.

The sensitivity level of the NR bands has a deviation of approximately +/- <3dB depending on the EN-DC combinations, but the combined sensitivity performance meets the 3GPP requirements.

LTE level is measured at BW 10 MHz.

7.4 Antenna Interface

The antenna connection and board layout design are one of the most important aspects of the whole application design as they strongly affect the overall radio performance. Hence, please read and follow the requirements and the guidelines as carefully as possible.

7.4.1 Antenna Configuration

The FE990B family modules have 4 RF ports for cellular antenna connection and 1 port for GNSS antenna connection.

Please refer to the following for the frequency bands allocation of each port.

Refer to the following antenna configuration assigned.

Table 84: Antenna Configuration

Antenna port	Technology	Tx	Rx	GNSS
ANT 0	WCDMA	B1, B5, B6, B8, B19	B1, B5, B6, B8, B19	-
	LTE	B1/B2/B3/B4/B5/B7/B8/B12/B13/B14/B17/B18/B19/B20/B25/B26/B28/B30/B38/B40/B41/B66/B68/B71	B1/B2/B3/B4/B5/B7/B8/B12/B13/B14/B17/B18/B19/B20/B25/B26/B28/B29(SDL)/B30/B32(SDL)/B38/B40/B41/B42/B43/B48/B66/B68/B71	
	5G NR FR1	n1/n2/n3/n5/n7/n8/n12/n13/n14/n20/n25/n26/n28/n30/n38/n40/n41/n48/n66/n70/n71/n77/n78/n79	n1/n2/n3/n5/n7/n8/n12/n13/n14/n20/n25/n26/n28/n29(SDL)/n30/n38/n40/n41/n48/n66/n70/n71/n75(SDL)/n77/n78/n79	
ANT 1	WCDMA	-	-	GPS L1/L5,
	LTE	-	B1/B2/B3/B4/B5/B7/B8/B12/B13/B14/B17/B18/B19/B20/B25/	

Antenna port	Technology	Tx	Rx	GNSS
			B26/B28/B29(SDL)/B30/B32(SD L)/B38/B40/B41/B42/B43/B48/B66/B68/B71	Galileo E1, Beidou B1, Glonass G1
	5G NR FR1	-	n1/n2/n3/n5/n7/n8/n12/n13/n14/n20/n25/n26/n28/n29(SDL)/n30/n38/n40/n41/n48/n66/n70/n71/n75(SDL)/n77/n78/n79	QZSS,SBAS
ANT 2	WCDMA	-	B1, B5, B6, B8, B19	-
	LTE	B1/B2/B3/B4/B5/B7/B8/B12/B13/B14/B17/B18/B19/B20/B25/B26/B28/B30/B38/B40/B41/B42/B43/B48/B66/B68/B71	B1/B2/B3/B4/B5/B7/B8/B12/B13/B14/B17/B18/B19/B20/B25/B26/B28/B29(SDL)/B30/B32(SD L)/B38/B40/B41/B42/B43/B48/B66/B68/B71	
	5G NR FR1	n1/n2/n3/n5/n7/n8/n12/n13/n14/n20/n25/n26/n28/n30/n38/n40/n41/n48/n66/n70/n71/n77/n78/n79	n1/n2/n3/n5/n7/n8/n12/n13/n14/n20/n25/n26/n28/n29(SDL)/n30/n38/n40/n41/n48/n66/n70/n71/n75(SDL)/n77/n78/n79	
ANT 3	WCDMA	-	-	-
	LTE	-	B1/B2/B3/B4/B5/B7/B8/B12/B13/B14/B17/B18/B19/B20/B25/B26/B28/B29(SDL)/B30/B32(SD L)/B38/B40/B41/B42/B43/B48/B66/B68/B71	
	5G NR FR1	-	n1/n2/n3/n5/n7/n8/n12/n13/n14/n20/n25/n26/n28/n29(SDL)/n30/n38/n40/n41/n48/n66/n70/n71/n75(SDL)/n77/n78/n79	
ANT 4	GNSS	-	-	GPS L1/L5, Galileo E1, Beidou B1, Glonass G1 QZSS,SBAS

Table 85: Antenna Configuration for nR

NR Band				
	ANT0	ANT1	ANT2	ANT3
NR FDD n1	DRX/TX1	MOMO1	PRX/TX0	MOMO0
NR FDD n2	DRX/TX1	MOMO1	PRX/TX0	MOMO0
NR FDD n3	DRX/TX1	MOMO1	PRX/TX0	MOMO0
NR FDD n5	DRX/TX1	MOMO1	PRX/TX0	MOMO0
NR FDD n7	DRX/TX1	MOMO1	PRX/TX0	MOMO0
NR FDD n8	DRX/TX1	MOMO1	PRX/TX0	MOMO0
NR FDD n12	DRX/TX1	MOMO1	PRX/TX0	MOMO0
NR FDD n13	DRX/TX1	MOMO1	PRX/TX0	MOMO0
NR FDD n14	DRX/TX1	MOMO1	PRX/TX0	MOMO0

NR Band				
NR FDD n20	DRX/TX1	MOMO1	PRX/TX0	MOMO0
NR FDD n25	DRX/TX1	MOMO1	PRX/TX0	MOMO0
NR FDD n26	DRX/TX1	MOMO1	PRX/TX0	MOMO0
NR FDD n28	DRX/TX1	MOMO1	PRX/TX0	MOMO0
NR FDD n29	DRX	MOMO1	PRX	MOMO0
NR FDD n30	DRX/TX1	MOMO1	PRX/TX0	MOMO0
NR TDD n38	DRX/TX1	MOMO1	PRX/TX0	MOMO0
NR TDD n40	DRX/TX1	MOMO1	PRX/TX0	MOMO0
NR TDD n41	DRX/TX1	MOMO1	PRX/TX0	MOMO0
NR TDD n48	DRX/TX1	MOMO1	PRX/TX0	MOMO0
NR FDD n66	DRX/TX1	MOMO1	PRX/TX0	MOMO0
NR FDD n70	DRX/TX1	MOMO1	PRX/TX0	MOMO0
NR FDD n71	DRX/TX1	MOMO1	PRX/TX0	MOMO0
NR SDL n75	DRX	MOMO1	PRX	MOMO0
NR SDL n76	DRX	MOMO1	PRX	MOMO0
NR TDD n77	DRX/TX1	MOMO1	PRX/TX0	MOMO0
NR TDD n78	DRX/TX1	MOMO1	PRX/TX0	MOMO0
NR TDD n79	DRX/TX1	MOMO1	PRX/TX0	MOMO0

Table 86: Antenna Configuration for E-UTRA

E-UTRA Band				
	ANT0	ANT1	ANT2	ANT3
LTE FDD B1	PRX/TX0	MOMO0	DRX/TX1	MOMO1
LTE FDD B2	PRX/TX0	MOMO0	DRX/TX1	MOMO1
LTE FDD B3	PRX/TX0	MOMO0	DRX/TX1	MOMO1
LTE FDD B4	PRX/TX0	MOMO0	DRX/TX1	MOMO1
LTE FDD B5	PRX/TX0	MOMO0	DRX/TX1	MOMO1
LTE FDD B7	PRX/TX0	MOMO0	DRX/TX1	MOMO1
LTE FDD B8	PRX/TX0	MOMO0	DRX/TX1	MOMO1
LTE FDD B12	PRX/TX0	MOMO0	DRX/TX1	MOMO1
LTE FDD B13	PRX/TX0	MOMO0	DRX/TX1	MOMO1
LTE FDD B14	PRX/TX0	MOMO0	DRX/TX1	MOMO1
LTE FDD B17	PRX/TX0	MOMO0	DRX/TX1	MOMO1
LTE FDD B18	PRX/TX0	MOMO0	DRX/TX1	MOMO1

E-UTRA Band				
LTE FDD B19	PRX/TX0	MOMO0	DRX/TX1	MOMO1
LTE FDD B20	PRX/TX0	MOMO0	DRX/TX1	MOMO1
LTE FDD B25	PRX/TX0	MOMO0	DRX/TX1	MOMO1
LTE FDD B26	PRX/TX0	MOMO0	DRX/TX1	MOMO1
LTE FDD B28	PRX/TX0	MOMO0	DRX/TX1	MOMO1
LTE SDL B29	PRX	MOMO0	DRX	MOMO1
LTE FDD B30	PRX/TX0	MOMO0	DRX/TX1	MOMO1
LTE SDL B32	PRX	MOMO0	DRX	MOMO1
LTE TDD B38	PRX/TX0	MOMO0	DRX/TX1	MOMO1
LTE TDD B40	PRX/TX0	MOMO0	DRX/TX1	MOMO1
LTE TDD B41	PRX/TX0	MOMO0	DRX/TX1	MOMO1
LTE TDD B42	DRX/TX1	MOMO1	PRX/TX0	MOMO0
LTE TDD B43	DRX/TX1	MOMO1	PRX/TX0	MOMO0
LTE TDD B48	DRX/TX1	MOMO1	PRX/TX0	MOMO0
LTE FDD B66	PRX/TX0	MOMO0	DRX/TX1	MOMO1
LTE FDD B68	PRX/TX0	MOMO0	DRX/TX1	MOMO1
LTE FDD B71	PRX/TX0	MOMO0	DRX/TX1	MOMO1

Table 87: Antenna Configuration for UTRA

UTRA Band				
	ANT0	ANT1	ANT2	ANT3
WCDMA B1	PRX/TX0	NA	DRX	NA
WCDMA B5	PRX/TX0	NA	DRX	NA
WCDMA B6	PRX/TX0	NA	DRX	NA
WCDMA B8	PRX/TX0	NA	DRX	NA
WCDMA B19	PRX/TX0	NA	DRX	NA

7.5 Antenna Requirements

Antennas for FE990B Family modules must meet the requirements listed in the table below.

Table 88: WCDMA/LTE/5G Sub-6 Antenna Requirements

Item	Value
Frequency range	Depending on the frequency band(s) provided by the network operator, the customer must use the most suitable antenna for that/those band(s). The bands supported by the FE990B Family are provided in Section Frequency Bands and CA/MIMO/EN-DC .
Impedance	50 Ohm

Item	Value
Input power	> 24 dBm average power in WCDMA & LTE & 5G Sub-6
VSWR absolute max	$\leq 10:1$
VSWR recommended	$\leq 2:1$

7.5.1 Antenna Connection

FE990B modules do not mount RF connectors: antennas must be connected to the modem antenna pads using a transmission line implemented on the PCB.

The transmission line must meet the following requirements:

Table 89: Antenna line on PCB Requirements

Item	Value
Characteristic Impedance	50 ohm
Max Attenuation	0.3 dB
Avoid coupling with other signals.	
Cold End (Ground Plane) of the antenna must be equipotential to the FE990B ground pads.	

Warning: The impedance of the antenna RF line (and connectors, if mounted) must be matched to 50 Ohm: any mismatch will affect RF performance.

Warning: The FE990B should be located away from noise sources. Antennas should be installed away from noise sources such as SMPS, USB/PCIe interfaces, and so on.

7.5.2 PCB Guidelines in Case of FCC Certification

In the case FCC certification is required for an application using FE990B, according to FCC KDB 996369 for modular approval requirements, the transmission line should be similar to those implemented on FE990B interface board described in the following chapter.

7.5.2.1 Transmission Line Design

When designing the FE990B interface board, trace loss was minimized by properly selecting the component layout and keeping the line length as short as possible.

A Grounded Coplanar Waveguide (G-CPW) line has been chosen, since this kind of transmission line ensures good impedance control and can be implemented in an outer PCB layer as needed in this case. A SMA female connector has been used to feed the line. The interface board is realized on a FR4, 8-layers PCB. Substrate material is characterized by relative permittivity $\epsilon_r = 3.9 @ 2 \text{ GHz}$, $\text{TanD} = 0.008 @ 2 \text{ GHz}$.

A characteristic impedance of nearly 50Ω is achieved using trace width = 0.36 mm, clearance from coplanar ground plane = 0.1mm each side. The line uses a reference ground plane on layer 6, while copper is removed from layer 2 underneath the line. The Height of trace above ground plane is 1.36 mm. Calculated characteristic impedance is 51.6Ω , estimated line loss is less than 0.3dB. The line geometry is shown below:

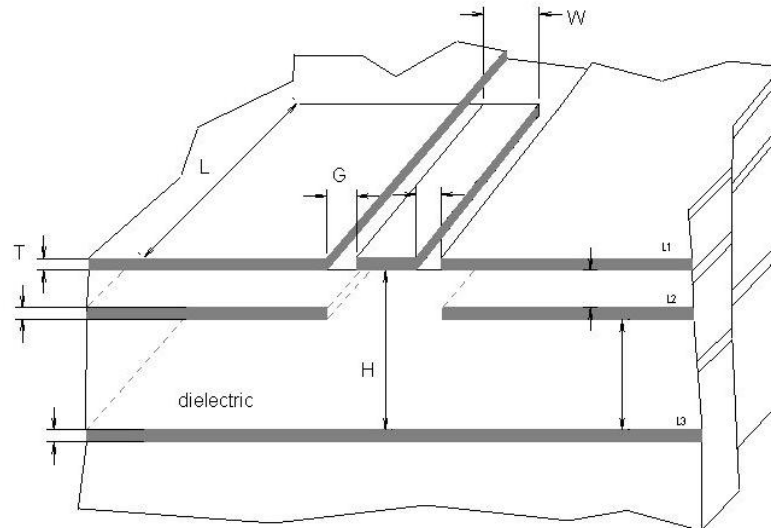


Figure 37: Line Geometry

7.5.3 Antenna Installation Guidelines

- Each antenna must be installed with 20dB isolation.
- Install the antenna in a location with access to the network radio signal.
- The Antenna must not be installed inside metal cases.
- The Antenna must be installed according to the Antenna manufacturer's instructions.
- Antenna integration should optimize Radiation Efficiency. Efficiency values > 50% are recommended on all frequency bands.
- Antenna integration should not perturb the radiation pattern described in the Antenna manufacturer's documentation.
- It is preferable to get an omnidirectional radiation pattern.
- To meet the related EIRP limitations, antenna gain must not exceed the values indicated in regulatory requirements, where applicable. The Typical antenna Gain in most M2M applications does not exceed 2dBi.
- If the device antenna is located farther than 20 cm from the human body and there are no co-located transmitters, then the Telit FCC/IC approvals can be reused by the product.
- If the device antenna is closer to 20 cm from the human body or there are co-located transmitters, then additional FCC/IC testing may be required for the product (Telit FCC/IC approvals cannot be reused).

Note: GNSS receive path uses either the dedicated GNSS connector or the shared Secondary AUX antenna connector.

7.6 GNSS Receiver

The FE990B Family modems integrate a GNSS receiver that can be used either in Standalone or in A-GPS (assisted GPS) mode.

FE990B modems support active GNSS antennas.

Table 90: GNSS Receiver

Item	Value
Frequency range	- Wide-band GNSS: 1559 – 1606 MHz recommended. - GPS L1: 2.046 MHz BW NB GPS (centered on 1575.42 MHz) - GPS L5 24 MHz BW (centered on 1176.45 MHz) - Glonass (GLO): ~ 8.3 MHz BW (1597.05 ~ 1606 MHz) - BeiDou (BDS): 4.092 MHz BW (1559.05 ~ 1563.14 MHz) - Galileo (GAL): 4.092 MHz BW (centered on 1575.42 MHz) - Quasi-Zenith (QZSS): 12 MHz L1 GPS (centered on 1575.42 MHz) - SBAS: 12 MHz L1 GPS (centered on 1575.42 MHz)
Passive Antenna Gain	1.5 dBi < Gain < 3dBi ¹
Impedance	50 Ohm
External Amplification Gain	7.5 dB < Gain < 26 dB for nominal performance ^{2,3}
Supply Voltage	3.1V

- Note:**
- 1 Configured as AT\$GPSANTPORT= 1 (Internal LNA Active).
 - 2 Configured as AT\$GPSANTPORT= 2 (Internal LNA bypassed)
Must not exceed 26 dB.
 - 3 Total gain applied at FE990B RF input connector (Passive Antenna gain + External LNA gain-losses).

7.6.1 GNSS RF Front End Design

The FE990B Family contains an integrated LNA and front-end SAW filter.

This allows the module to operate properly with a passive GNSS antenna. If the antenna cannot be located near the FE990B, then an active antenna (that is, an antenna with a built-in low noise amplifier) can be used with an external dedicated power supply circuit. GNSS receive path uses either the dedicated GNSS connector #4 or the shared antenna connector #1.

- Note:** Refer to the FE990B Family AT Commands Reference Guide, for detailed information about GNSS operating modes and GNSS antenna selection.

7.7 GNSS Characteristics

The table below specifies the GNSS characteristics and expected performance.

Table 91: GNSS Characteristics

Parameters		Typical Measurement	Notes
Sensitivity	Tracking Sensitivity	-161 dBm	Standalone or MS-based
	Acquisition	-157 dBm	
	Cold Start	-148 dBm	
TTFF	Hot	1 sec	Open Sky, mean TTFF
	Warm	21 sec	Open Sky, mean TTFF
	Cold	25 sec	Open Sky, mean TTFF

Parameters		Typical Measurement	Notes
Min update rate		1 Hz	
2D positioning error meters (50%, 68%, 95%)		< 1.2m, <1.5m, <3 m	Open sky conditions. Good quality antenna, L1+L5
Speed accuracy (68%, 95%)		0.05ms , 0.1ms	30ms with all signals 130 dBm



8 Mechanical Design

8.1 General

The FE990B module is designed to be compliant with a standard lead-free SMT process.

8.2 Drawing

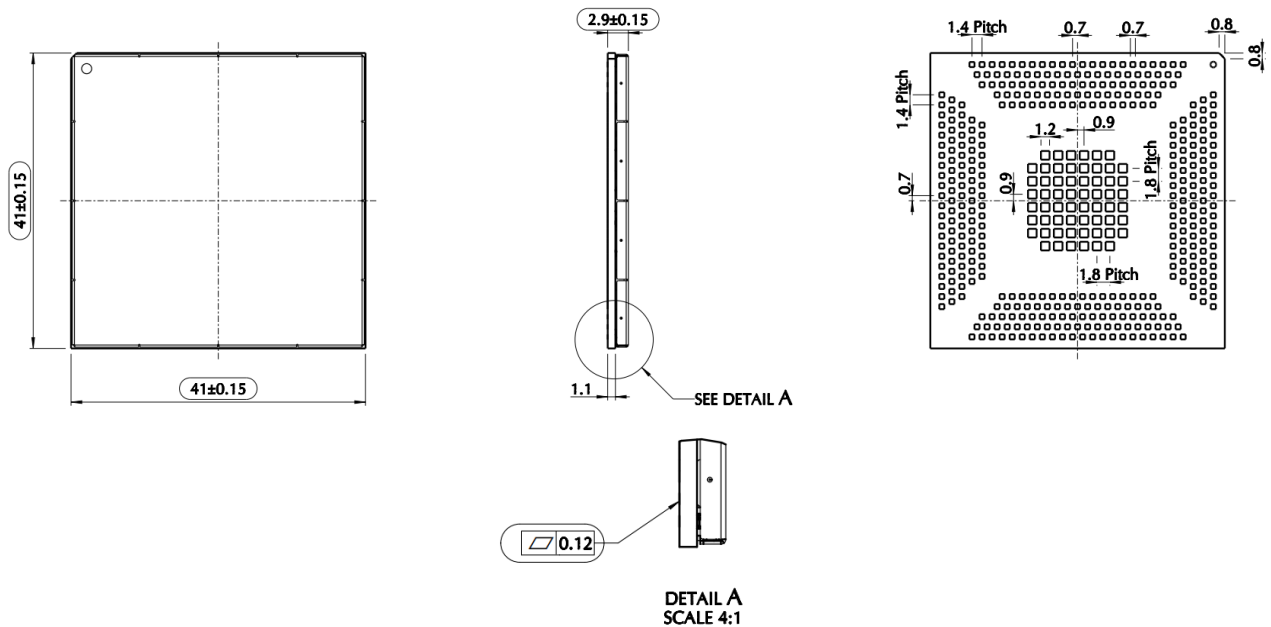


Figure 40: FE990B Module Mechanical Dimensions

9 Application PCB Design

9.1 Recommended Footprint for the Application

The recommended footprint for the application board is shown below (dimensions in mm). To facilitate module replacement should it ever be required, it is suggested to design the application board with a 1.5 mm placement inhibit area around the module. It is also suggested, as a common rule for an SMT component, to avoid having a mechanical part of the application board in direct contact with the module.

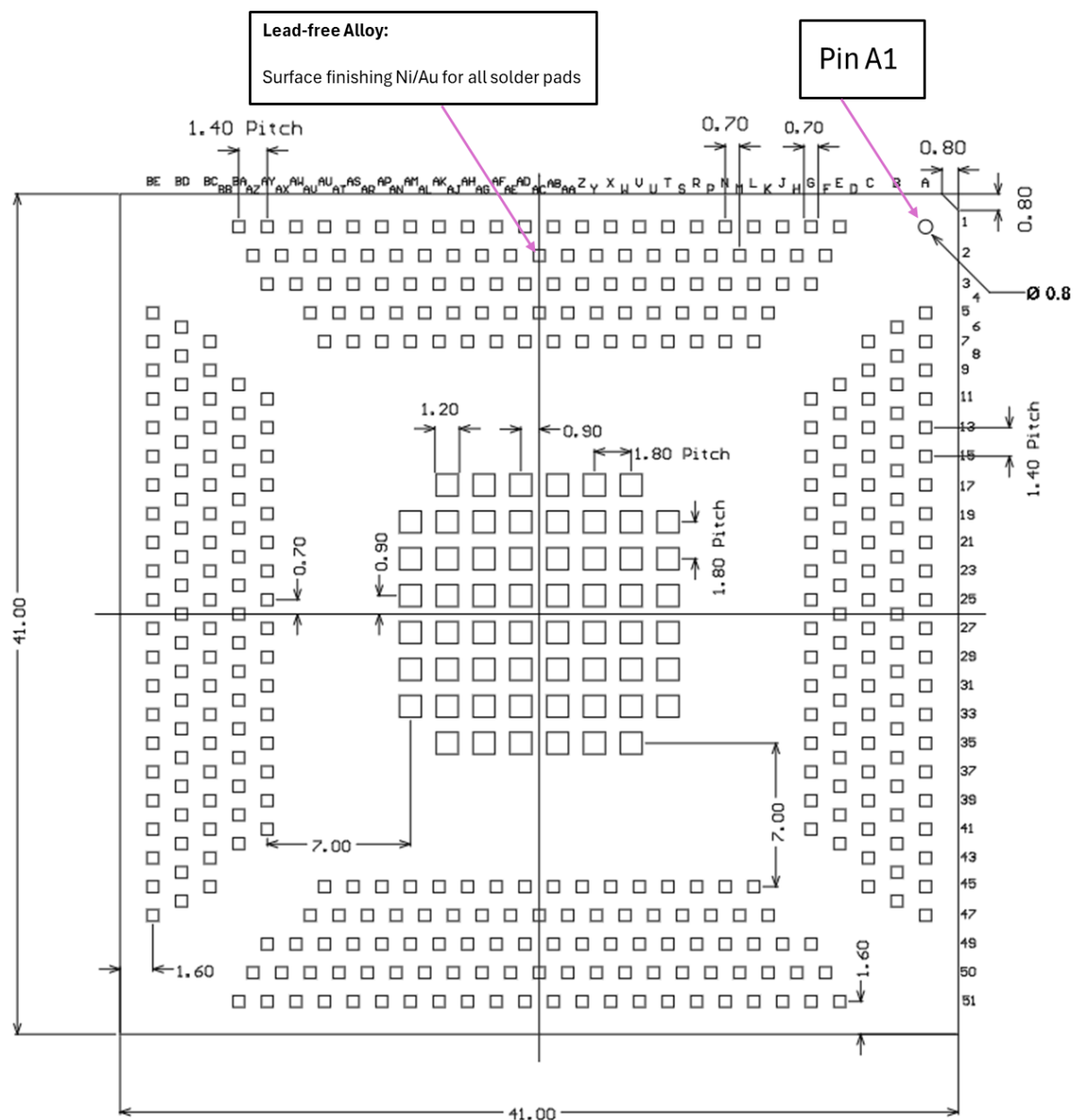


Figure 41: Footprint (Bottom View)

9.2 PCB Pad Design

The solder pads on the PCB are recommended to be of the Non-Solder Mask Defined (NSMD) type.

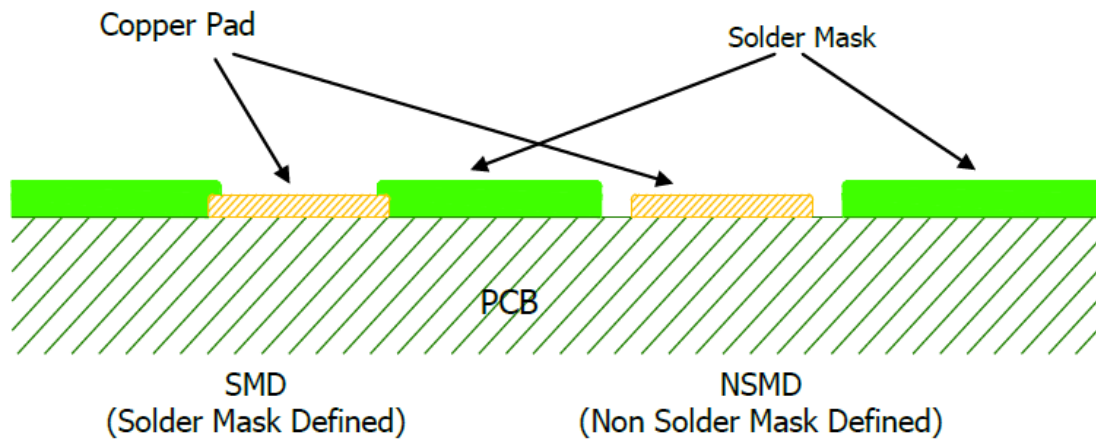


Figure 42: PCB Pad Design

9.3 Recommendations for PCB Pad Dimensions

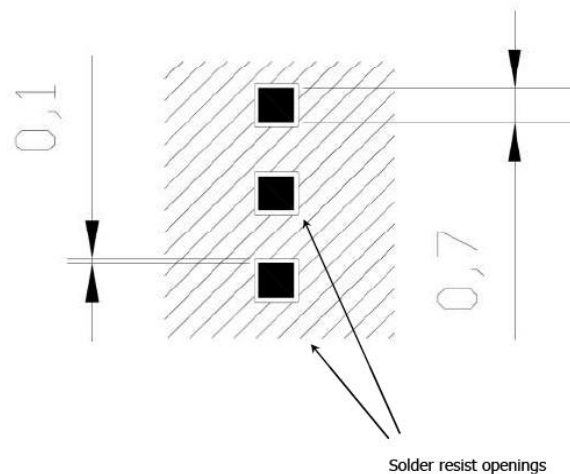


Figure 43: PCB Pad Dimensions

It is not recommended to place a via or micro-via not covered by the solder resist around the pads in an area of 0.15 mm unless it carries the same signal as the pad itself. Micro vias inside the pads are allowed.

Holes in the pad are only allowed for blind holes and not for through holes.

Table 92: Recommendations for PCB Pad Surfaces

Finish	Layer Thickness (um)	Properties
Electroless Ni/Immersion Au	3 - 7/0.05 - 0.15	Good solder ability protection, high shear force values

The PCB must be able to resist the higher temperatures, which occur during the lead-free process. This issue should be discussed with the PCB-supplier. In general, the wettability of tin-lead solder paste on the described surface plating is better compared to lead-free solder paste.

9.4 Cleaning

In general, cleaning the module mounted on the carrier board is not recommended.

- Residues between the module and the host board cannot be easily removed with any cleaning method.
- Cleaning with water or any organic solvent can lead to capillary effects where the cleaning solvent is absorbed into the gap between the module and the host board or even leaks inside the module (due to the gap between the module shield and PCB). The combination of soldering flux residues and encapsulated solvent could lead to short circuits between conductive parts. The solvent could also damage the module label.
- Ultrasonic cleaning could damage the module permanently. Especially for crystal oscillators, where the risk of damage is very high.

9.5 Stencil

The layout of the stencil openings can be the same as the recommended footprint (1:1). The suggested thickness of stencil foil is greater than 120 μm .

9.6 Solder Paste

It is recommended to use only “no clean” solder paste to avoid modules cleaning after assembly.

9.7 Solder Reflow

Recommended solder reflow profile:

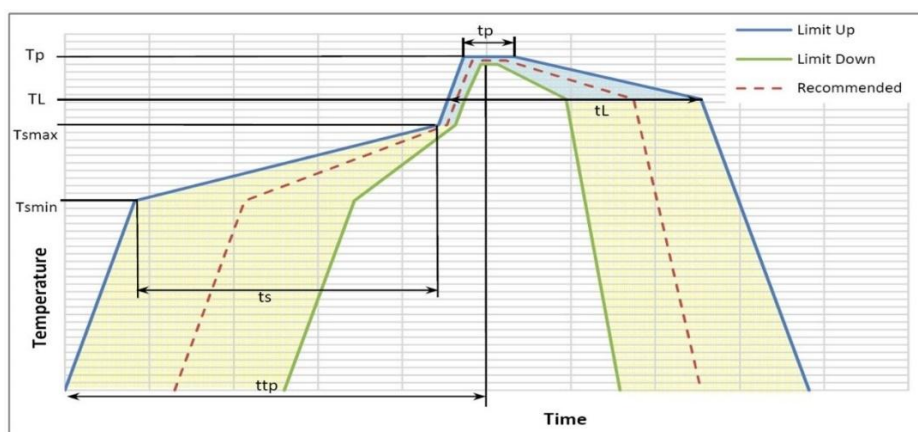


Figure 44: Recommended Solder Reflow Profile

Table 93: Profile Feature Recommendations

Profile Feature	Pb-Free Assembly Free
Average ramp-up rate (TL to TP)	3°C/second max
Preheat • Temperature Min (Tmin) • Temperature Max (Tsmax) • Time (min to max) (ts)	150°C 200°C 60-180 seconds
Tsmax to TL Ramp-up Rate	3°C/second max
Time maintained above:	

Profile Feature	Pb-Free Assembly Free
• Temperature (TL) • Time (tL)	217°C 60-150 seconds
Peak Temperature (Tp)	245 +0/-5°C
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds
Ramp-down Rate	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

Note: All temperatures refer to the topside of the package, measured on the package body surface.

Warning: THE FE990B MODULE WITHSTANDS ONE REFLOW PROCESS ONLY.

Warning: The above solder reflow profile represents the typical SAC reflow limits and does not guarantee adequate adherence of the module to the customer application throughout the temperature range. Customers must optimize the reflow profile depending on the overall system taking into account such factors as thermal mass and warpage.



10 Application Guide

10.1 Debug of the FE990B Module in Production

To test and debug the FE990B module integration, it is recommended to add test pins on the host PCB for the following purposes:

- Checking the connection between the FE990B itself and the application
- Testing the performance of the module by connecting it with an external computer

Depending on the customer application these test pins include, but are not limited to, the following signals:

- ON_OFF_N, RESET_N, SHDN_N
- PCIe lines
- VDD_IO
- USB lines
- VAUX/PWRMON

10.2 Bypass Capacitor on Power Supplies

When a sudden voltage step is asserted to or removed from the power supplies, the step transition causes effects such as overshoot and undershoot. These abrupt voltage transitions can cause the device to fail or malfunction. To mitigate this behavior, bypass capacitors are essential. The specific impact may vary across different applications, so integrators must pay close attention to this issue when designing their application boards.

The power line length and width must be considered carefully, and the capacitor value must be selected accordingly.

The capacitor will also prevent power supply ripple and the switching noise caused in TDMA systems, such as GSM.

Most importantly, a suitable bypass capacitor must be mounted on the following lines on the application board:

- VPH_PWR

Recommended value:

- 100 uF for VPH_PWR

The required capacitance primarily depends on the application board. Generally, additional capacitance is required when the power line is longer.

Furthermore, if the fast power-down function is used, an additional bypass capacitor should be mounted on the application board.

10.3 EMC Recommendations

EMC protection on all FE990B pins should be designed on the application side according to customer's requirements.

ESD Ratings for FE990B Pins:

- Human Body Model (HBM): ± 1000 V
- Charged Device Model (CDM): ± 250 V

- Antenna Pins: Up to ± 4 kV

Warning: Do not touch without proper electrostatic protective equipment. The product must be handled with care, avoiding any contact with the pins as electrostatic discharge may damage the product itself.

11 Packaging

11.1 Tray

The FE990B modules are packaged on trays that can be used in SMT processes for pick & place handling. The first Marketing and Engineering samples of the FE990B series will be shipped with the current packaging of the FE990B modules (on trays of 12 pieces each). The mass production units of FE990B will be shipped according to the following drawings:

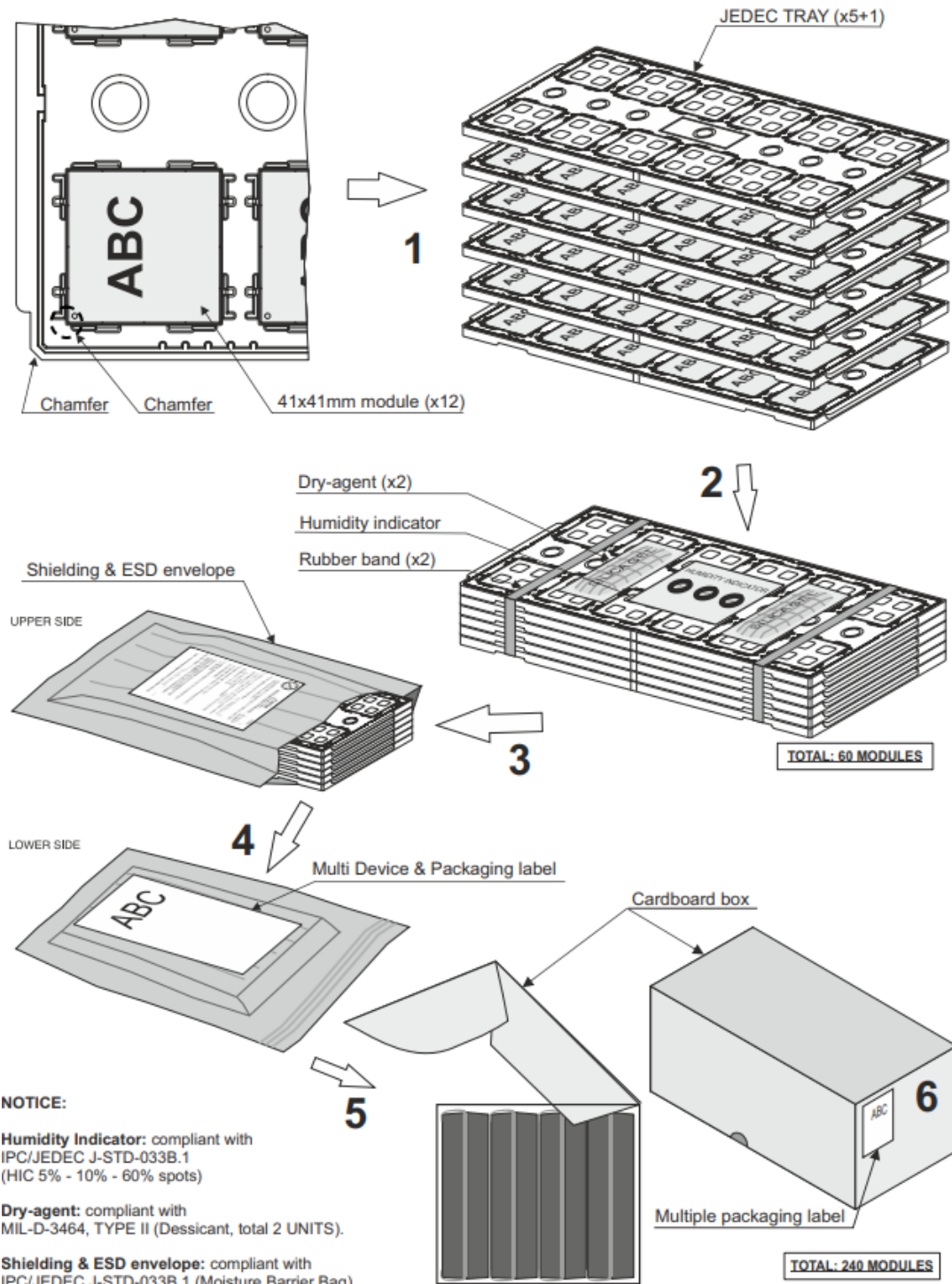


Figure 45: Tray Packaging

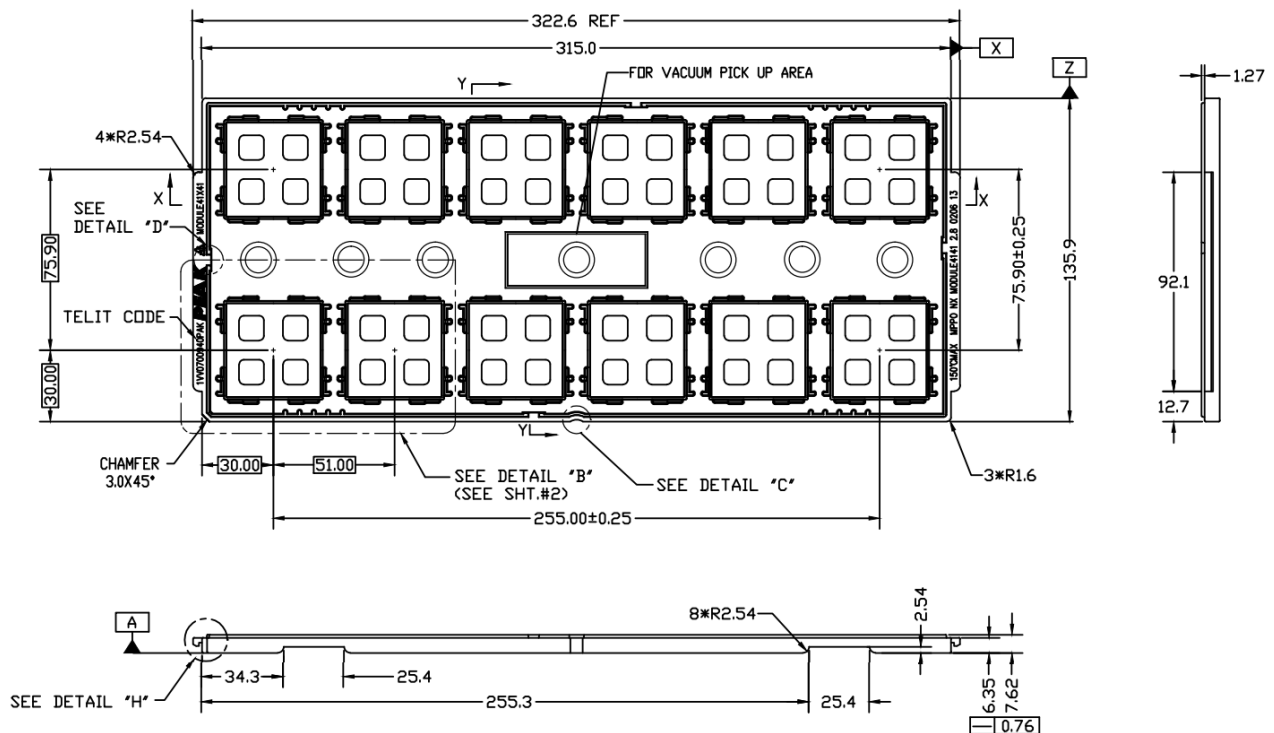


Figure 46: Tray Dimensions

11.2 Moisture Sensitivity

The FE990B is a Moisture Sensitive Device level 3, according to standard IPC/JEDEC J-STD-020, and takes care of all the relative requirements for using this kind of component.

Moreover, the customer has to take care of the following conditions:

- a** Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH).
- b** An environmental condition during the production: 30°C/60% RH according to IPC/JEDEC J STD-033A paragraph 5.
- c** The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition b) "IPC/JEDEC J-STD-033D paragraph 5.2" is respected.
- d** Baking is required if conditions b) or c) are not respected.
- e** Baking is required if the humidity indicator inside the bag indicates 10% RH or more.

12 Conformity Assessment Issues

12.1 Approvals Compliance Summary

Table 94: Legend Description

Legend	Description
	The equipment is compliant
	Type approval is in progress
	The equipment is not compliant

Table 95: Americas Approvals Compliance Summary

Region	Americas						
Country & Type Approval	AR ENACOM	BR ANATEL	CA ISED	CO CRC	MX IFETEL	PE MTC	US FCC
FE990B40-NA(D)							
FE990B34-NA(D)							

Table 96: APAC Approvals Compliance Summary

Region	APAC					
Country & Type Approval	AU RCM	CH CCC	JP JRL / JTBL	SG IMDA	TW NCC	KR KC
FE990B40-RW(D)						
FE990B34-RW(D)						

Table 97: EMEA Approvals Compliance Summary

Region	EMEA	
Country & Type Approval	EU RED	UK UKCA
FE990B40-RW(D)		
FE990B34-RW(D)		

12.2 Americas Approvals

12.2.1 USA FCC

12.2.1.1 FCC Certificates

The FCC Grants can be found here: <https://www.fcc.gov/oet/ea/fccid>

12.2.1.2 Applicable FCC Rules

Table 98: Applicable FCC Rules

Model	Applicable FCC Rules
FE990B40-NA(D)	47 CFR Part 2, 22, 24, 27, 90

12.2.1.3 FCC Regulatory Notices

Modification Statement

Telit has not approved any changes or modifications to this device by the user. Any changes or modifications could void the user's authority to operate the equipment.

Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Wireless Notice

This device complies with FCC radiation exposure limits set forth for an uncontrolled environment and meets the FCC radio frequency (RF) Exposure Guidelines. This transmitter must not be co-located or operate in conjunction with any other antenna or transmitter. The antenna should be installed and operated with a minimum distance of 20 cm between the radiator and your body.

FCC Class B digital device notice

This equipment has been tested and found to comply with the limits for a Class B digital device, according to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.

This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used per the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by taking one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment to an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Information for the OEMs and Integrators

The following statement must be included with all versions of this document supplied to an OEM or integrator but should not be distributed to the end user.

- 1 This device is intended for OEM integrators only.
- 2 Please see the full Grant of Equipment document for other restrictions

Note EMI Considerations

Note that a host manufacture is recommended to use KDB996369 D04 Module Integration Guide recommending as "best practice" RF design engineering testing and evaluation in case non-linear interactions generate additional non-compliant limits due to module placement to host components or properties. For standalone mode, reference the guidance in KDB996369 D04 Module Integration Guide and for simultaneous mode;

see KDB996369 D02 Module Q&A Question 12, which permits the host manufacturer to confirm compliance.

How to make changes

Only Grantees are permitted to make permissive changes, if the module will be used differently than granted conditions, please contact us to ensure modifications will not affect compliance at the following contact points.

Grantee code:	RI7	Grantee name:	Telit Communications S.p.A.
Mailing address:	Viale Stazione di Prosecco 5/b, 34010 Sgonico – Trieste, Italy		
Website:	https://www.telit.com/	Support contact:	TS-EMEA@telit.com

Manual Information to the End User

The OEM integrator should be aware not to provide information to the end-user on how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as shown in this manual

Information on test modes and additional testing requirements

The module has been evaluated in mobile stand-alone conditions. For operational conditions other than a stand-alone modular transmitter in a host (multiple, simultaneously transmitting modules or other transmitters in a host), additional testing may be required (collocation, retesting...). If this module is intended for use in a portable device, you are responsible for separate approval to satisfy the SAR requirements of FCC Part 2.1093.

Additional testing, Part 15 Subpart B disclaimer

The modular transmitter is only authorized by the FCC for the specific rule parts (for example, FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance with any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuitry), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed. The end product with an embedded module may also need to pass the FCC Part 15 unintentional emission testing requirements and be properly authorized per FCC Part 15.

12.2.1.4 FCC Antenna Info

This radio transmitter has been approved by FCC to operate with the antenna types listed below with the maximum allowable gain indicated. Antenna types not included in this list, with a gain greater than the maximum gain indicated for that type, are strictly prohibited from use with this device.

Table 99: Max Antenna Gain for FCC in dBi

Max Gain for FCC (dBi)				
Band	FE990B40-NA(D)			
LTE B2	7.5			

Max Gain for FCC (dBi)				
LTE B4	4.5			
LTE B5	9.9			
LTE B7	8.5			
LTE B12	9.6			
LTE B13	10.1			
LTE B14	10.2			
LTE B17	9.6			
LTE B25	7.5			
LTE B26	9.9			
LTE B30	0.0			
LTE B38 PC3	8.5			
LTE B38 PC2	5.5			
LTE B41 PC3	8.5			
LTE B41 PC2	5.5			
LTE B42	0.5			
LTE B43	0.5			
LTE B48	0.0			
LTE B66	4.5			
LTE B71	8.4			
NR N2	7.5			
NR N5	9.9			
NR N7	8.5			
NR N12	9.6			
NR N13	10.1			
NR N14	10.2			
NR N25	7.5			
NR N26	9.9			
NR N30	0.0			
NR N38	8.5			
NR N41 PC3	8.5			
NR N41 PC2	5.5			
NR N48	0.0			
NR N66	4.5			
NR N70	5.5			
NR N71	8.4			
NR N77 PC3	5.5			
NR N77 PC2	2.5			
NR N78 PC3	5.5			
NR N78 PC2	2.5			
N2 UL MIMO PC3	7.5			

Max Gain for FCC (dBi)				
N2 UL MIMO PC2	4.5			
N5 UL MIMO	9.9			
N7 UL MIMO	8.5			
N25 UL MIMO PC3	7.5			
N25 UL MIMO PC2	4.5			
N30 UL MIMO	0.0			
N38 UL MIMO	8.5			
N41 UL MIMO PC3	8.5			
N41 UL MIMO PC2	5.5			
N41 UL MIMO PC1.5	3.0			
N48 UL MIMO	0.0			
N66 UL MIMO PC3	4.5			
N66 UL MIMO PC2	1.5			
N70 UL MIMO	5.5			
N71 UL MIMO PC3	8.4			
N71 UL MIMO PC2	5.4			
N77 UL MIMO PC3	5.5			
N77 UL MIMO PC2	2.5			
N77 UL MIMO PC1.5	0.5			
N78 UL MIMO PC3	5.5			
N78 UL MIMO PC2	2.5			
N78 UL MIMO PC1.5	0.5			

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Labelling requirements for the host device

The host device shall be properly labelled to identify the modules within the host device. The certification label of the module shall be clearly visible at all times when installed in the host device, otherwise, the host device must be labelled to display the FCC ID of the module, preceded by the words "Contains transmitter module", or the word "Contains", or similar wording expressing the same meaning, as in the below table.

Table 100: Host device FCC Label

Model	Host device FCC label
FE990B40-NA(D)	Contains FCC ID: RI7FE990B40NA

12.2.2 Canada ISED

12.2.2.1 ISED Database

The products ISED certified can be found here:

Les produits certifiés ISED peuvent être trouvés ici :

<https://sms-sgs.ic.gc.ca/equipmentSearch/searchRadioEquipments?execution=e1s1&lang=en>

12.2.2.2 Applicable ISED Rules

Table 101: Applicable ISED rules / Règles ISDE applicable

Model	Applicable ISED rules / Règles ISDE applicables
FE990B40-NA(D)	RSS: 132 Issue 4, 133 Issue 7, 130 Issue 2, 139 Issue 4, 195 Issue 2, 199 Issue 4, 140 Issue 1, 192 Issue 5, 198 Issue 1; RSS-Gen Issue 5

12.2.2.3 ISED Regulatory Notices

Modification Statement / Déclaration de modification

Telit has not approved any changes or modifications to this device by the user. Any changes or modifications could void the user's authority to operate the equipment.

Telit n'approuve aucune modification apportée à l'appareil par l'utilisateur, quelle qu'en soit la nature. Tout changement ou modification peuvent annuler le droit d'utilisation de l'appareil par l'utilisateur.

Interference Statement / Déclaration d'interférence

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux applicables RSS standards d'Industrie Canada. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Radio Exposure Notice / Avis d'exposition radio

This device complies with ISED radiation exposure limits set forth for an uncontrolled environment and meets the RSS-102 of the ISED radio frequency (RF) Exposure rules. Antenna gain must be less than the values reported in the table below:

Le présent appareil est conforme à l'exposition aux radiations FCC / ISED définies pour un environnement non contrôlé et répond aux directives d'exposition de la fréquence de la FCC radiofréquence (RF) et RSS-102 de la fréquence radio (RF) ISED règles d'exposition. Gain de l'antenne doit être ci-dessous:

Table 102: Max antenna gain for ISED in dBi / Gain d'antenne max pour ISED en dBi

Gain maximum pour ISED (dBi) / Gain maximum pour ISDE (dBi)				
Band	FE990B40-NA(D)			
LTE B2	7.5			
LTE B4	4.5			
LTE B5	6.6			
LTE B7	8.5			
LTE B12	6.6			
LTE B13	6.9			
LTE B14	6.9			

Gain maximum pour ISED (dBi) / Gain maximum pour ISDE (dBi)				
LTE B17	6.6			
LTE B25	7.5			
LTE B26	6.6			
LTE B30	0.0			
LTE B38 PC3	8.5			
LTE B38 PC2	5.5			
LTE B41 PC3	8.5			
LTE B41 PC2	5.5			
LTE B42 PC3	7.5			
LTE B42 PC2	3.0			
LTE B43 PC3	7.5			
LTE B43 PC2	3.0			
LTE B48	7.0			
LTE B66	4.5			
LTE B71	5.4			
NR N2	7.5			
NR N5	6.6			
NR N7	8.5			
NR N12	6.6			
NR N13	6.9			
NR N14	6.9			
NR N25	7.5			
NR N26	6.6			
N30	0.0			
N38	8.5			
N41 PC3	8.5			
N41 PC2	5.5			
N48	7.0			
N66	4.5			
N71	5.4			
N77 PC3	5.5			
N77 PC2	2.5			
N78 PC3	5.5			
N78 PC2	2.5			
N2 UL MIMO PC3	7.5			
N2 UL MIMO PC2	4.5			
N5 UL MIMO	6.6			
N7 UL MIMO	8.5			
N25 UL MIMO PC3	7.5			
N25 UL MIMO PC2	4.5			

Gain maximum pour ISED (dBi) / Gain maximum pour ISDE (dBi)				
N30 UL MIMO	0.0			
N38 UL MIMO	8.5			
N41 UL MIMO PC3	8.5			
N41 UL MIMO PC2	5.5			
N41 UL MIMO PC1.5	3.0			
N48 UL MIMO	7.0			
N66 UL MIMO PC3	4.5			
N66 UL MIMO PC2	1.5			
N71 UL MIMO PC3	5.4			
N71 UL MIMO PC2	2.4			
N77 UL MIMO PC3	5.5			
N77 UL MIMO PC2	2.5			
N77 UL MIMO PC1.5	0.5			
N78 UL MIMO PC3	5.5			
N78 UL MIMO PC2	2.5			
N78 UL MIMO PC1.5	0.5			

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

L'émetteur ne doit pas être colocalisé ni fonctionner conjointement avec à autre antenne ou autre émetteur.

This equipment must be installed and operated in accordance with provided instructions and the antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter. End-users and installers must be provided with antenna installation instructions and consider removing the no-collocation statement.

Cet équipement doit être installé et utilisé conformément aux instructions fournies et la ou les antennes utilisées pour cet émetteur doivent être installées pour fournir une distance de séparation d'au moins 20 cm de toutes les personnes et ne doivent pas être co-localisées ou fonctionner en conjonction avec toute autre antenne ou émetteur.

Les utilisateurs finaux et les installateurs doivent recevoir les instructions d'installation de l'antenne et envisager de supprimer la déclaration de non-collocation.

Information on test modes and additional testing requirement / Informations sur les modes de test et exigences de test supplémentaires

The module has been evaluated in mobile stand-alone conditions. For operational conditions other than a stand-alone modular transmitter in a host (multiple, simultaneously transmitting modules or other transmitters in a host), additional testing may be required (collocation, retesting...) If this module is intended for use in a portable device, you are responsible for separate approval to satisfy the SAR requirements IC RSS-102.

Le module a été évalué dans des conditions mobiles autonomes. Pour des conditions de fonctionnement autres qu'un émetteur modulaire autonome dans un hôte (plusieurs modules

transmettant simultanément ou d'autres émetteurs dans un hôte), des tests supplémentaires peuvent être nécessaires (colocalisation, retest...) Si ce module est destiné à être utilisé dans un appareil portable, vous êtes responsable de l'approbation séparée pour satisfaire aux exigences SAR IC RSS-102.

Labelling requirements for the host device / Exigences d'étiquetage pour le périphérique hôte

The host device shall be properly labelled to identify the modules within the host device. The certification label of the module shall be clearly visible at all times when installed in the host device, otherwise the host device must be labelled to display the IC of the module, preceded by the words "Contains transmitter module", or the word "Contains", or similar wording expressing the same meaning, as in the following table.

L'appareil hôte doit être étiqueté comme il faut pour permettre l'identification des modules qui s'y trouvent. L'étiquette de certification du module donné doit être posée sur l'appareil hôte à un endroit bien en vue en tout temps. En l'absence d'étiquette, l'appareil hôte doit porter une étiquette donnant le IC du module, précédé des mots « Contient un module d'émission », du mot « Contient » ou d'une formulation similaire exprimant le même sens, comme en tableau suivant.

Table 103: Host device IC label / Étiquette IC du dispositif hôte

Model / HVIN	Host device IC label / Étiquette IC du dispositif hôte
FE990B40-NA(D)	Contains IC: 5131A-FE990B40NA

CAN ICES-3 (B) / NMB-3 (B)

This Class B digital apparatus complies with Canadian ICES-003.

Cet appareil numérique de classe B est conforme à la norme canadienne ICES-003.

12.2.3 Brazil ANATEL

12.2.3.1 ANATEL Regulatory Notices

The FE990B module is certified in Brazil by Anatel.



"Este equipamento não tem direito à proteção contra interferência prejudicial e não pode causar interferência em sistemas devidamente autorizados"

"This equipment is not entitled to protection against harmful interference and must not cause interference in duly authorized systems"

FE990B40-NA(D) Homologation # XXXXX-XX-XXXXX

FE990B34-NA(D) Homologation # XXXXX-XX-XXXXX

12.3 APAC Approvals

12.3.1 Japan Approvals

Telit strongly recommends to customers, deploying the module to Japan, the usage of AT#FWSWITCH command to select the right Japanese carrier profile. The carrier profile

has been designed to enable the right LTE and WCDMA bands and also the required carrier settings.

12.3.2 JRL/JTBL Regulatory Notices

Antenna info

According to Japan regulatory rule, module certification is valid only with the specific antennas registered to and approved by Japan Radio Law (JRL) certified body in relation to module certification. Customers who are going to use modules under JRL are responsible to contact Telit technical support or sales to get the list of these antennas.

12.3.3 Taiwan NCC

12.3.3.1 NCC Regulatory Notices

According to National Communication Commission (NCC) Taiwan requirements, the module, and the packaging shall be identified as described in the following lines. Shall be added also the specified safety warning statement.

- 「減少電磁波影響，請妥適使用」

「此模組於取得認證後將依規定於模組本體標示審驗合格標籤，並要求平台廠商於平台上標示『本產品內含發射器模組： ☐

CCXXxxLPyyyZzW」字樣。」

FE990B40-RW: ☐ CCXXxxLPyyyZzW

FE990B34-RW: ☐ CCXXxxLPyyyZzW

- 「本產品 FE990B40-RW / FE990B34-RW 支持 WCDMA Bx, LTE Bx. 」

12.4 EMEA Approvals

12.4.1 EU RED

12.4.1.1 EU Declaration of Conformity

Following the above Approval Compliance Summary table, where applicable (green dot), hereby, Telit Communications S.p.A declares that the equipment complies with Directive 2014/53/EU.

The full text of the EU Declaration of Conformity is available at the following internet address: <https://www.telit.com/red>

Text of 2014/53/EU Directive (RED) requirements can be found here:

12.4.1.2 RED Antennas

This radio transmitter has been approved under RED to operate with the antenna types listed below with the maximum permissible gain indicated. The usage of a different antenna in the final hosting device may need a new assessment of host conformity to RED.

Table 104: Max Antenna Gain for RED in dBi

Max Gain for RED (dBi)			
Band	FE990B40-RW(D)		
UMTS B1	12.3		
UMTS B5	8.7		
UMTS B8	8.9		
LTE B1	12.3		
LTE B3	11.8		
LTE B5	8.7		
LTE B7	12.5		
LTE B8	8.9		
LTE B20	9.2		
LTE B28	8.0		
LTE B38	12.5		
LTE B38 PC2	10.0		
LTE B40	12.5		
LTE B41	13.0		
LTE B41 PC2	10.0		
LTE B42	13.0		
LTE B42 PC2	10.0		
LTE B43	13.0		
LTE B43 PC2	10.0		
LTE B68	8.4		
n1	12.3		
n3	11.8		
n5	8.7		
n7	12.5		
n8	8.9		
n20	9.2		
n28	8.0		
n38	12.5		
n40	12.5		
n41	13.0		
n41 PC2	10.0		
n77	13.0		
n77 PC2	10.0		
n78	13.0		
n78 PC2	10.0		
n1 UL MIMO	12.3		
n3 UL MIMO	11.8		
n5 UL MIMO	8.7		

Max Gain for RED (dBi)			
n7 UL MIMO	12.5		
n8 UL MIMO	8.9		
n28 UL MIMO	8.0		
n38 UL MIMO	12.5		
n40 UL MIMO	12.5		
n41 UL MIMO PC1.5	7.0		
n77 UL MIMO PC1.5	7.0		
n78 UL MIMO PC1.5	7.0		

12.4.2 UK UKCA

12.4.2.1 UKCA Declaration of Conformity

Following the above Approval Compliance Summary table, where applicable (green dot), hereby, Telit Communications S.p.A declares that the equipment complies with the Radio Equipment Regulations 2017 for UKCA.

The full text of the UKCA declaration of conformity is available at the following internet address: <https://www.telit.com/ukca>

The UKCA requirements can be found here:

<https://www.gov.uk/guidance/using-the-ukca-marking>

12.5 RoHS and REACH Info

12.5.1 RoHS Info

Any requests for information related to RoHS certifications can be addressed to Chemical.Certifications@telit.com.

12.5.2 REACH Info

Any requests for information related to REACH certifications can be addressed to Chemical.Certifications@telit.com.

13 Acronyms and Abbreviations

Table 105: Acronyms and Abbreviations

Acronym	Definition
CA	Carrier aggregation
CLK	Clock
CMOS	Complementary Metal – Oxide Semiconductor
DTE	Data Terminal Equipment
EN-DC	E-UTRA – NR Dual Connectivity
ESR	Equivalent Series Resistance
E-UTRA	Evolved UMTS Terrestrial Radio Access
FDD	Frequency Division Duplex
GPIO	General Purpose Input Output
HCI	Host Controller Interface
HS	High Speed
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
I/O	Input Output
I2C	Inter-integrated Circuit
I2S	Inter-IC Sound
LTE	Long Term Evolution
NR	New Radio
OD	Open Drain
PCB	Printed Circuit Board
PCIE	Peripheral Component Interconnect Express
PCM	Pulse-code modulation
RTC	Real Time Clock
SDL	Supplementary Down Link
SIM	Subscriber Identification Module
SOC	System-on-Chip
SMPS	Switching Mode Power Supply
TDD	Time Division Duplex
UART	Universal Asynchronous Receiver Transmitter
UMTS	Universal Mobile Telecommunication System
USB	Universal Serial Bus
VSWR	Voltage Standing Wave Ratio

14 Related Documents

For current documentation and downloads, refer to <https://dz.telit.com/>.

Table 106: Related Documents

S.no	Doc Code	Document Title
1	1VW0301249	Generic EVB Hardware User Guide
2	1VW0301732	Telit EVB 2.0 Hardware User Guide
3	1VW0302018	FE990B TLB Hardware User Guide

15 Document History

Table 107: Document History

Revision	Date	Changes
5	2025-09-19	Added SBAS function in Main Features and GNSS Receiver section Added Band 68 in Table 82 and Table 86 Updated section 12.1 Approvals Compliance Summary Added Product FE990B40-RWD Updated section 3.4. Block Diagram Updated Section 4.1. Pin-out for USB_PCIE_SWITCH Added Warning for USB_PCIE_SWITCH at Section 6.6.6.2 Updated Figure 18. Example Circuit for Host Interface Switch Function
4	2025-08-18	Updated Table 85, 86, 87 Antenna Configuration Updated Table 104. Max Antenna Gain for RED Updated Section 7.5.2 PCB Guidelines in Case of FCC Certification Updated Table 28: SFP+ Added Section 6.3.4. RESET_N Function.
3	2025-07-07	Numerous updates were made to this document revision; it should be read in its entirety Template Update
2	2025-04-09	Updated Template. Updated Section 12 Conformity Assessment Issues Updated Section 7.3 RF Performance Updated Section 7.4.1 Antenna Configuration Updated Table 3: Functional Features - Support band and UL-MIMO n70/n71 Updated Pin-out Updated Table 39: Available Signals Updated Table 42: PCIe Communication Port Updated Table 46: Host Interface Switch Pin Updated Table 47: SIM Card 1 Interface Updated Table 48: SIM Card 2 Interface Updated Table 49: Main UART Updated Table 50: Debug UART Updated Table 58: SPI Updated Table 61: SD Card Updated Table 70: FE990B Available GPIO Updated Table 71: ADC Updated Table 72: Characteristics of ADC Updated Table 74: Miscellaneous Functions Updated Section 6.9.4 DAC Converter Updated Table 2: Product Variants and their Frequency Bands - VoLTE/NR Feature updated Updated Table 32: Idle Mode Updated 6.7.3 SD/MMC Note Updated 6.6.5 USXGMII Section

Revision	Date	Changes
		Updated 6.6.4 UART
1	2025-03-12	Template upgrade. Updated Section 3.2 Product Variants and Frequency Bands Updated Section 3.3 Main Features Updated Section 5.2 Power Consumption Updated Section 6.6.1. USB - NOTE for USB OTG Updated Section 7.3 RF Performance Updated Section 7.6 GNSS Receiver Updated Section 7.7 GNSS Characteristics Updated Section 11 Packaging Updated Tables 36, 37, and 45
0	2024-09-04	Initial release

From Mod.0809 Rev.11

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