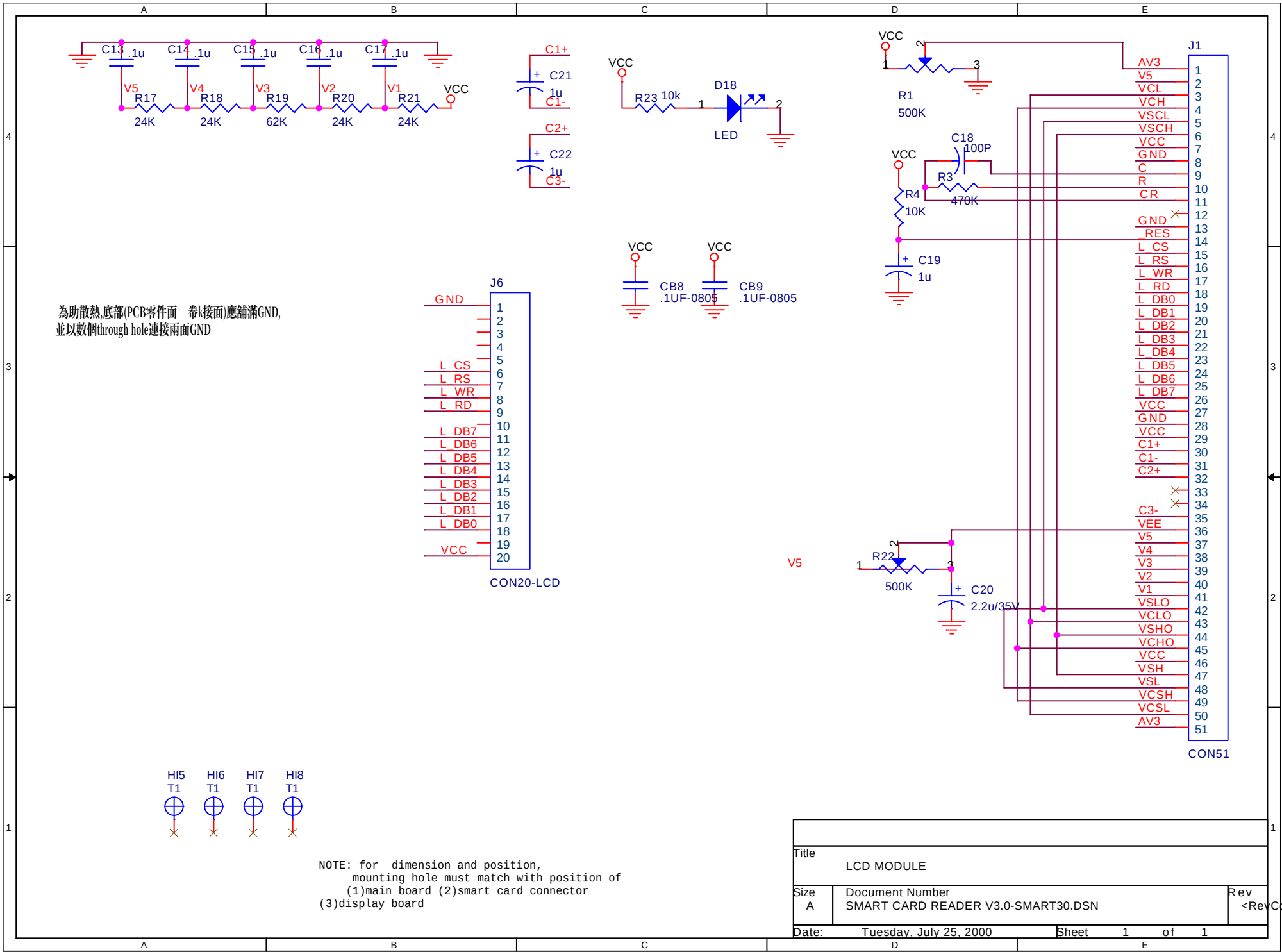
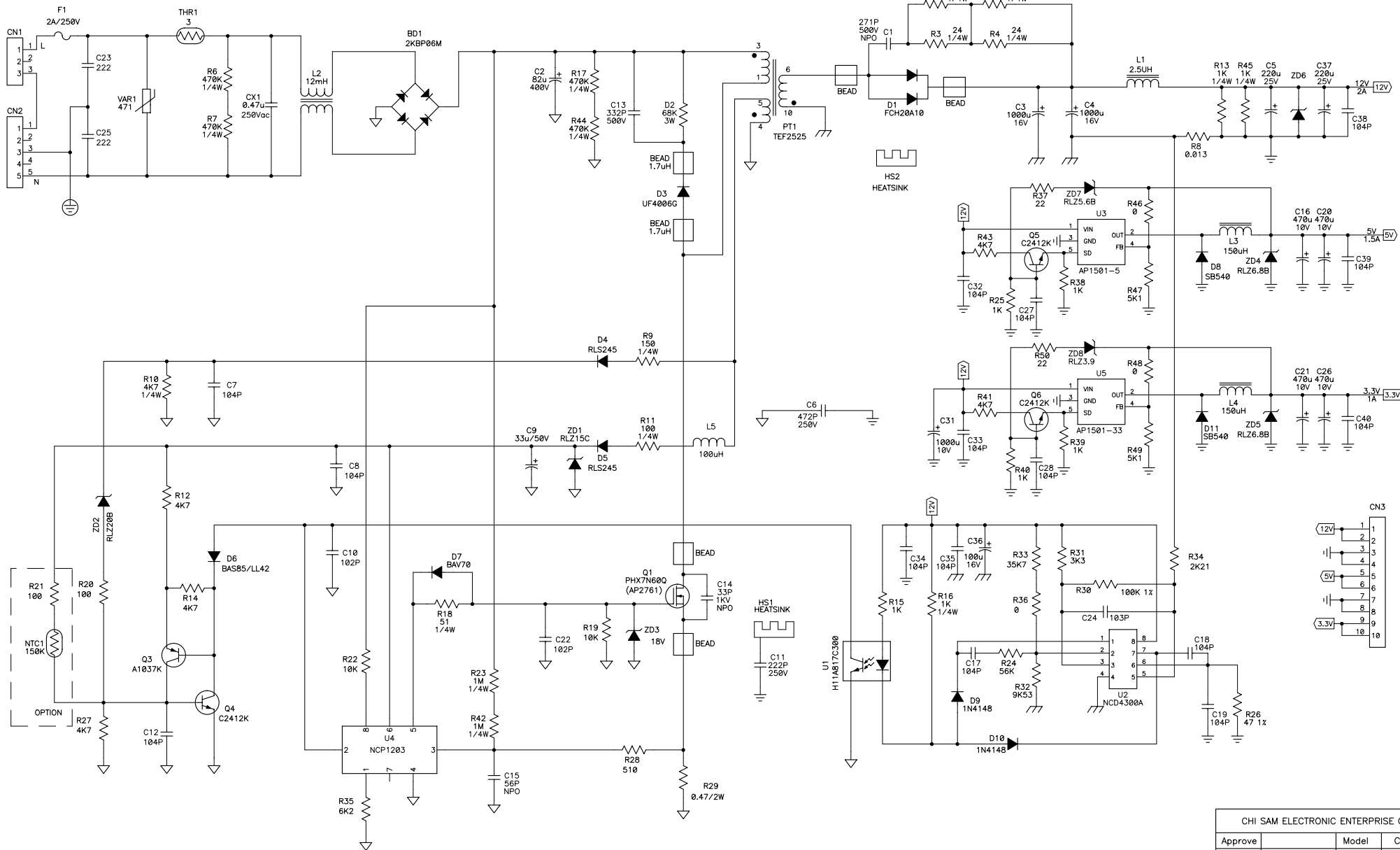
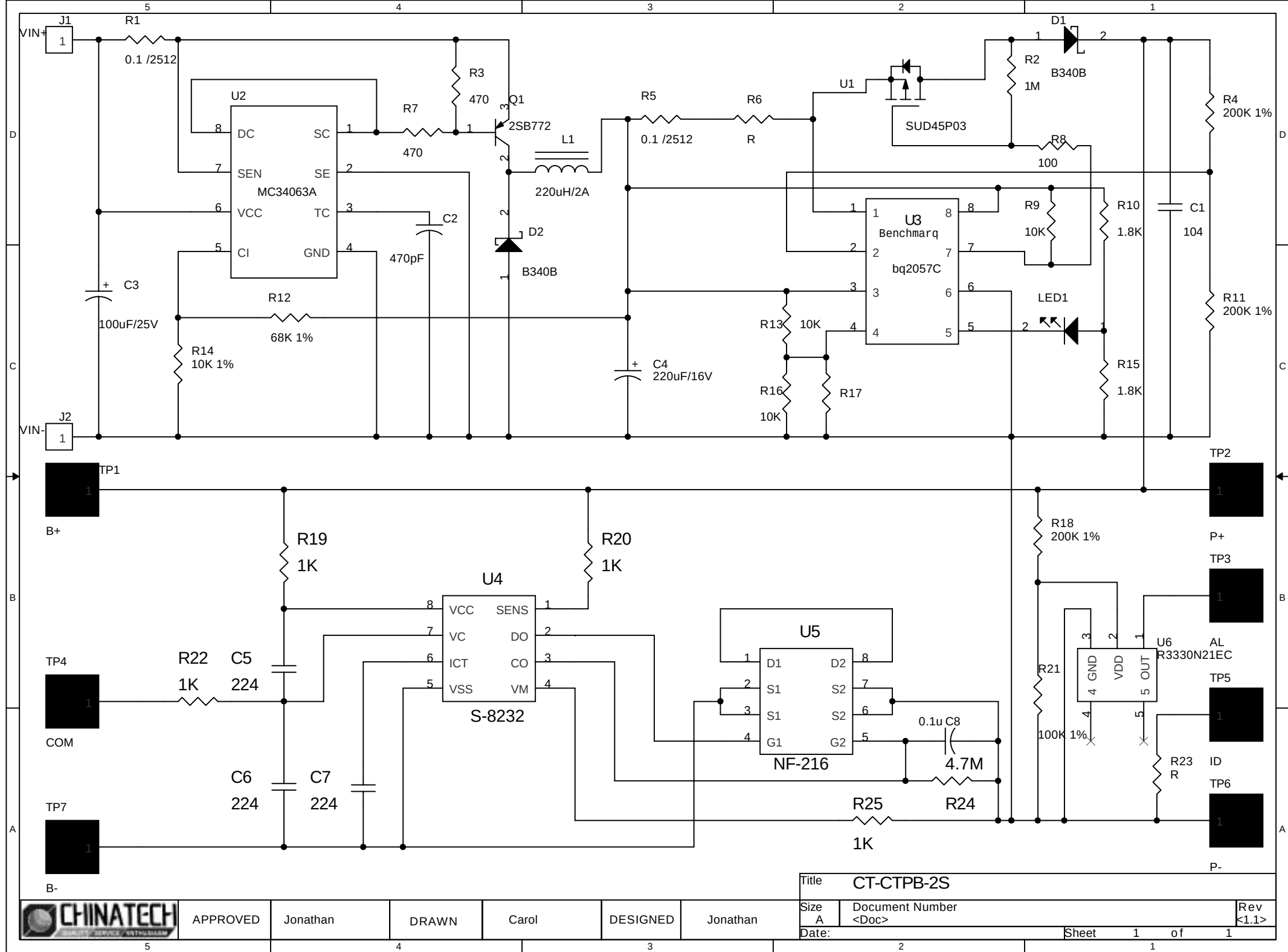


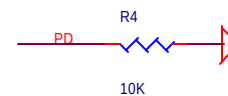
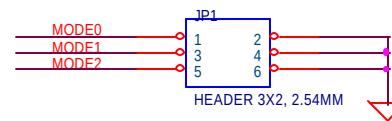
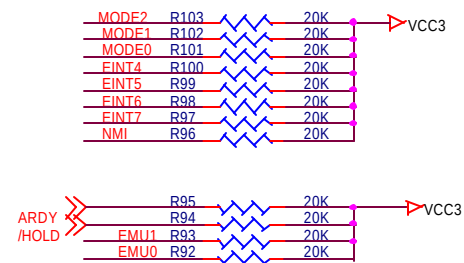
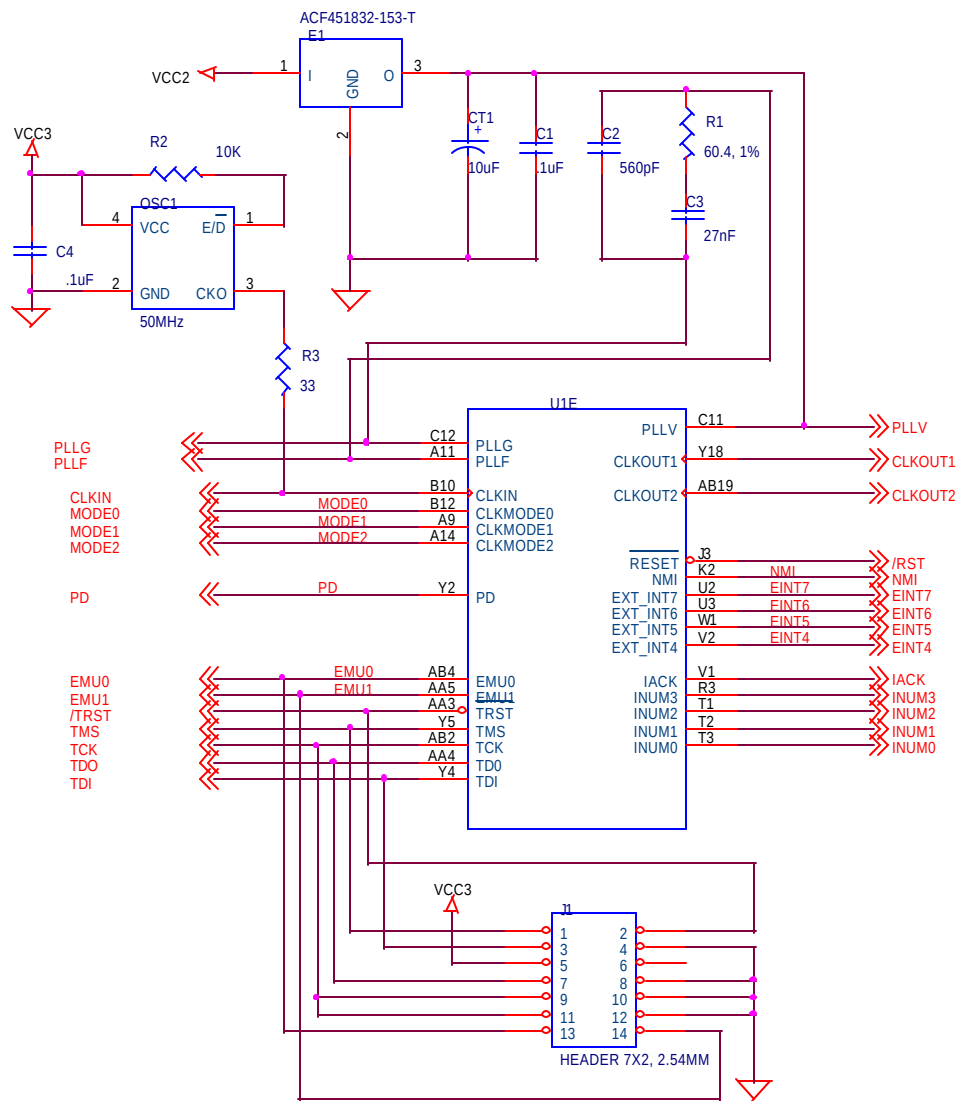




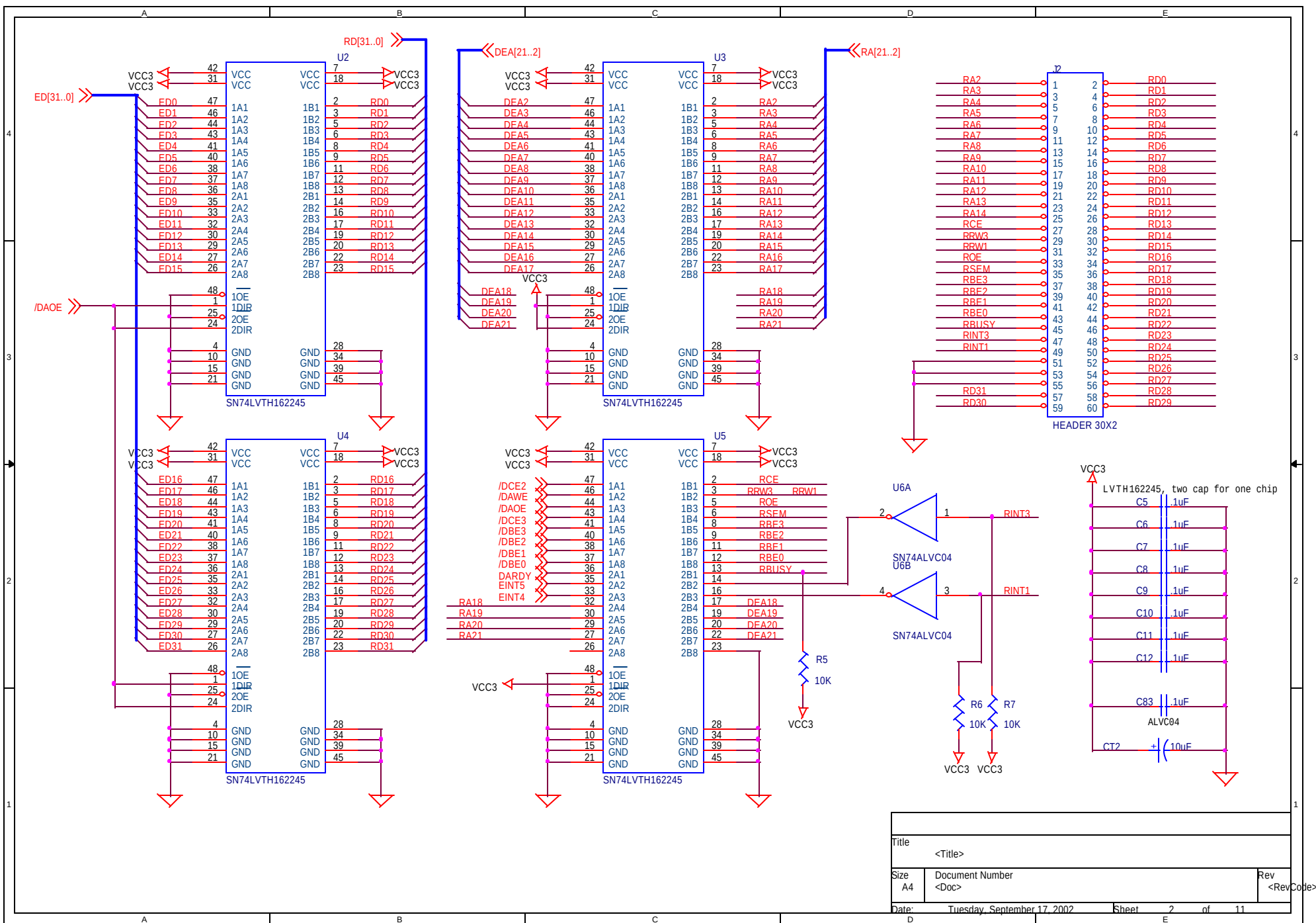
CHI SAM ELECTRONIC ENTERPRISE CO.,LTD.

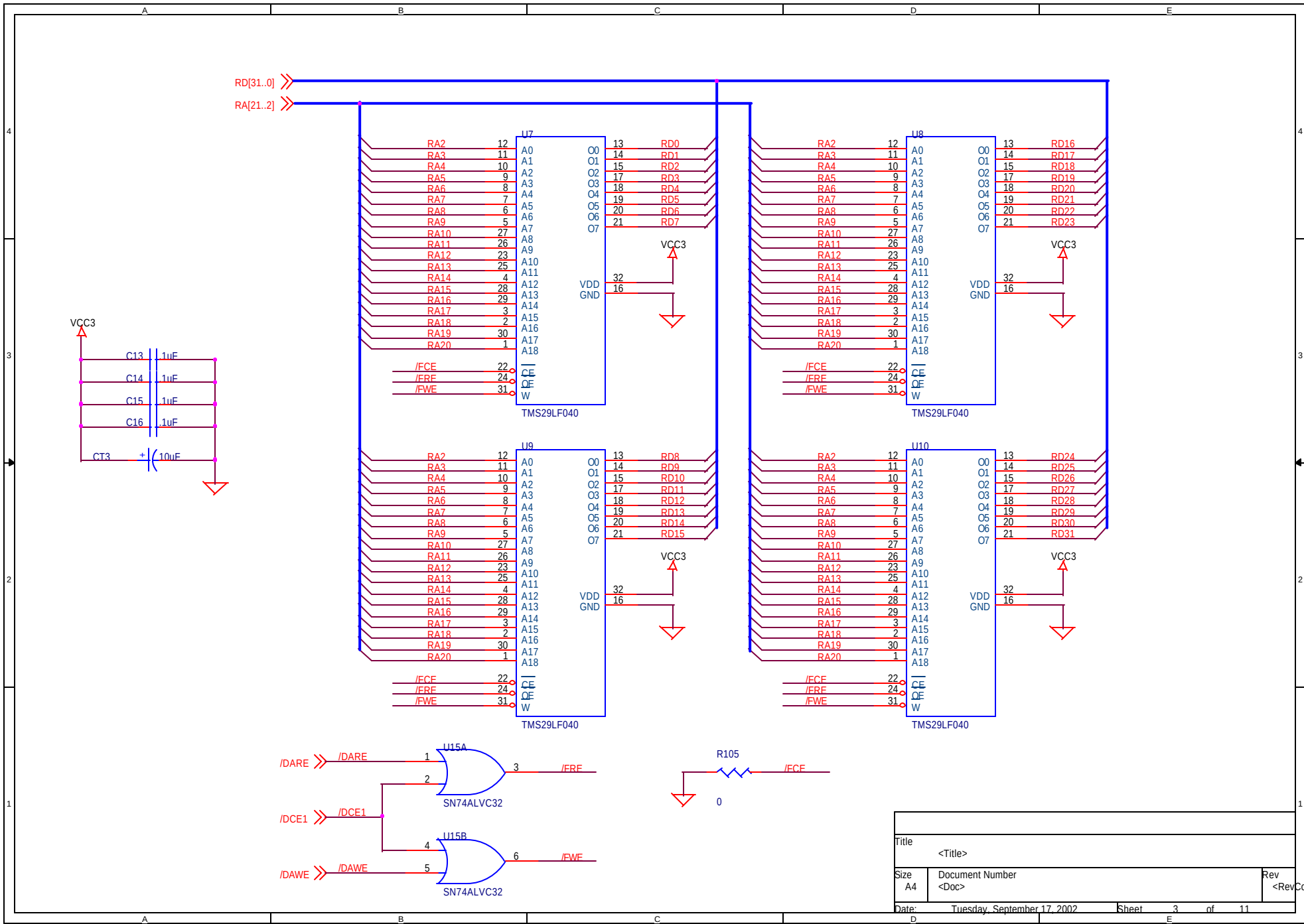
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Check		Number	
Drawn		Rev	B
Date	2003-12-05	Sheet	1 of 1

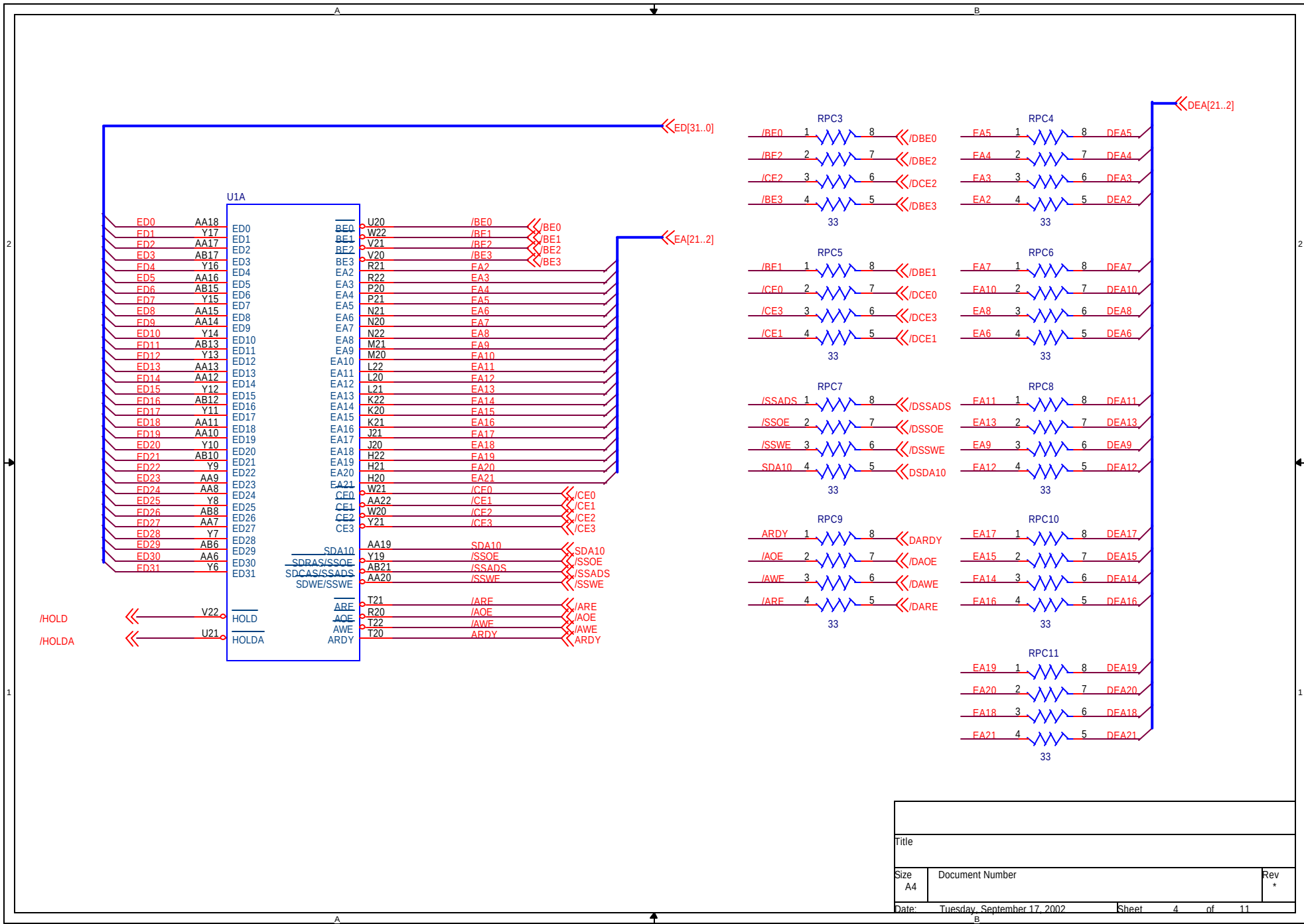


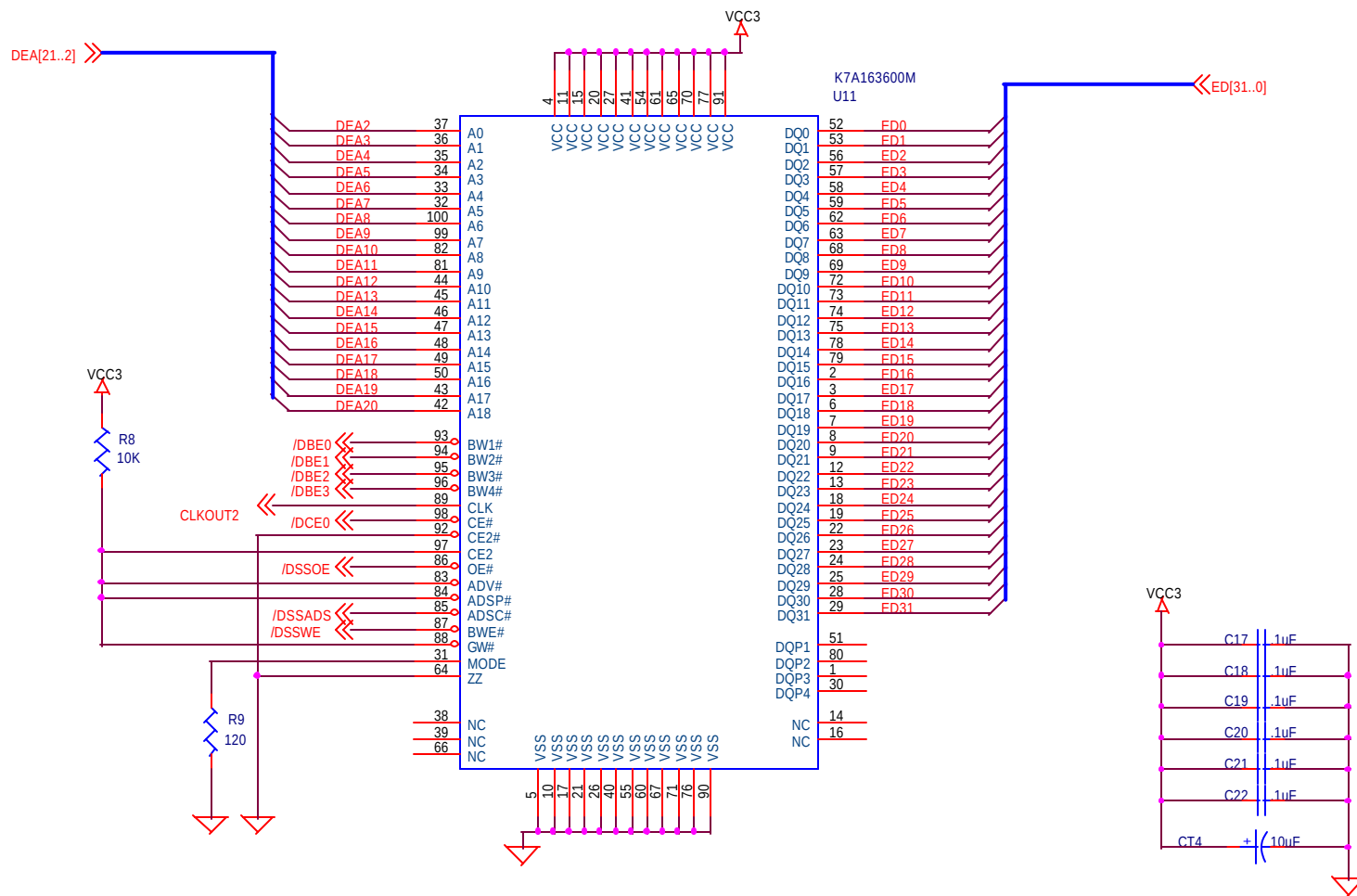


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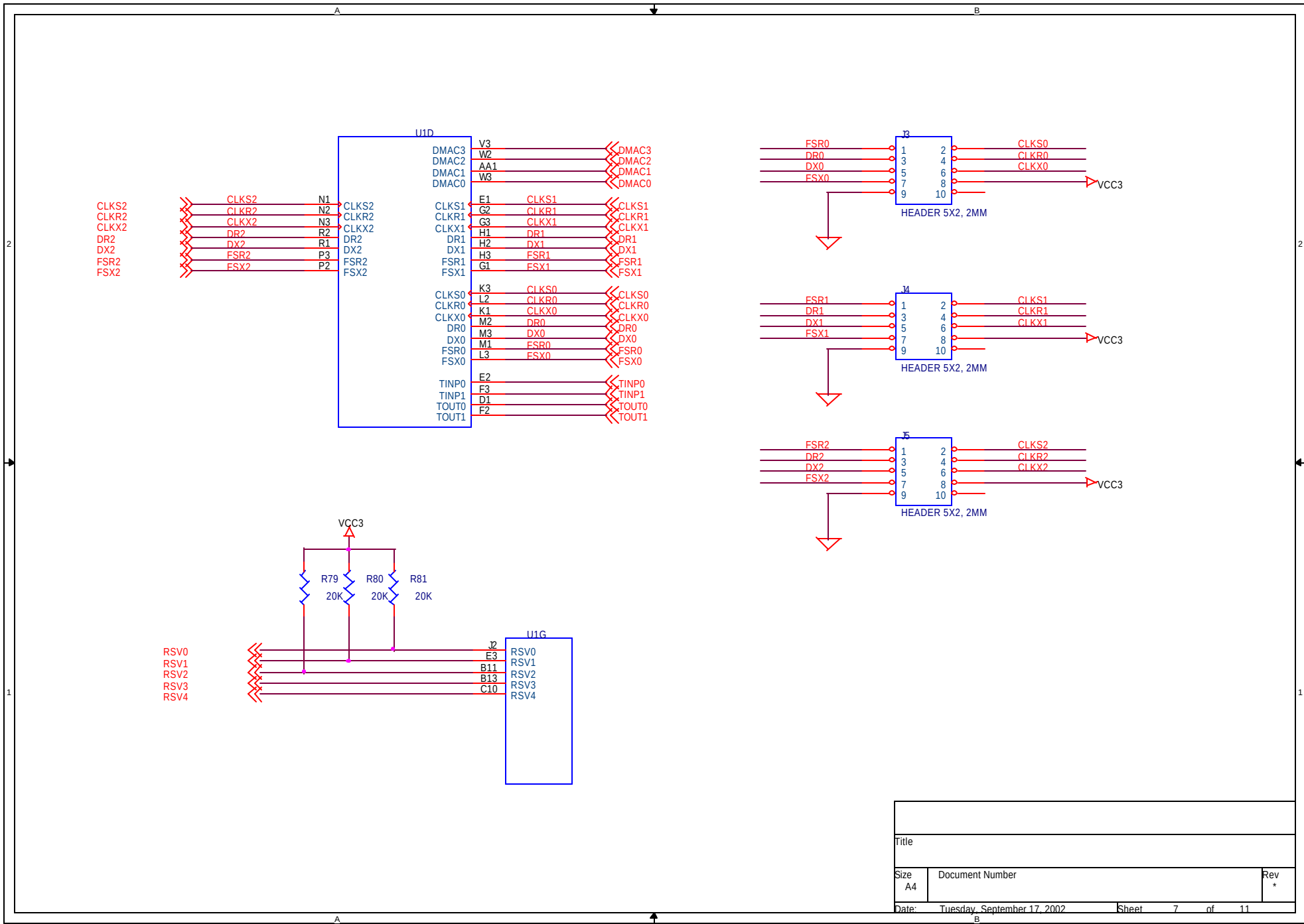




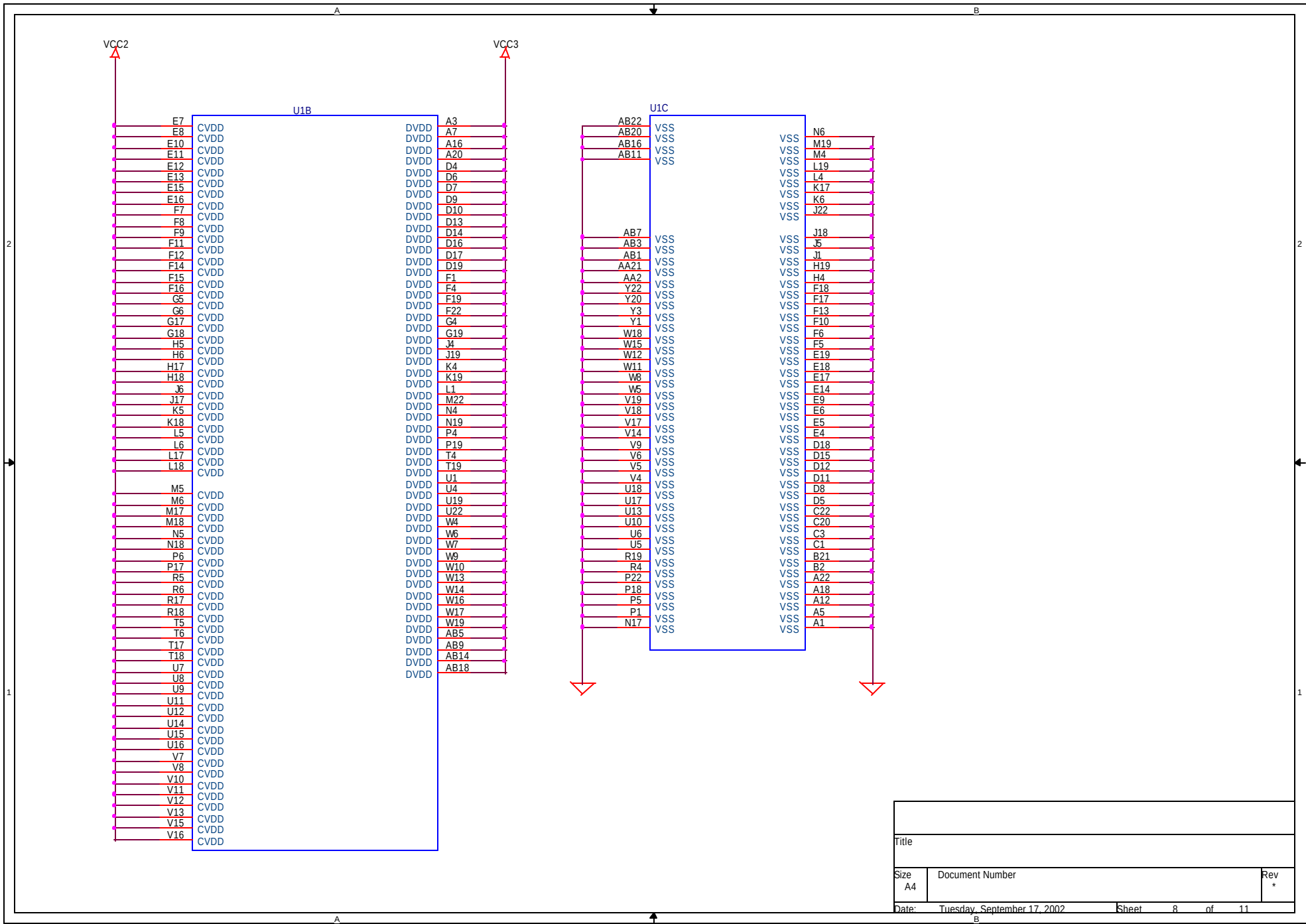


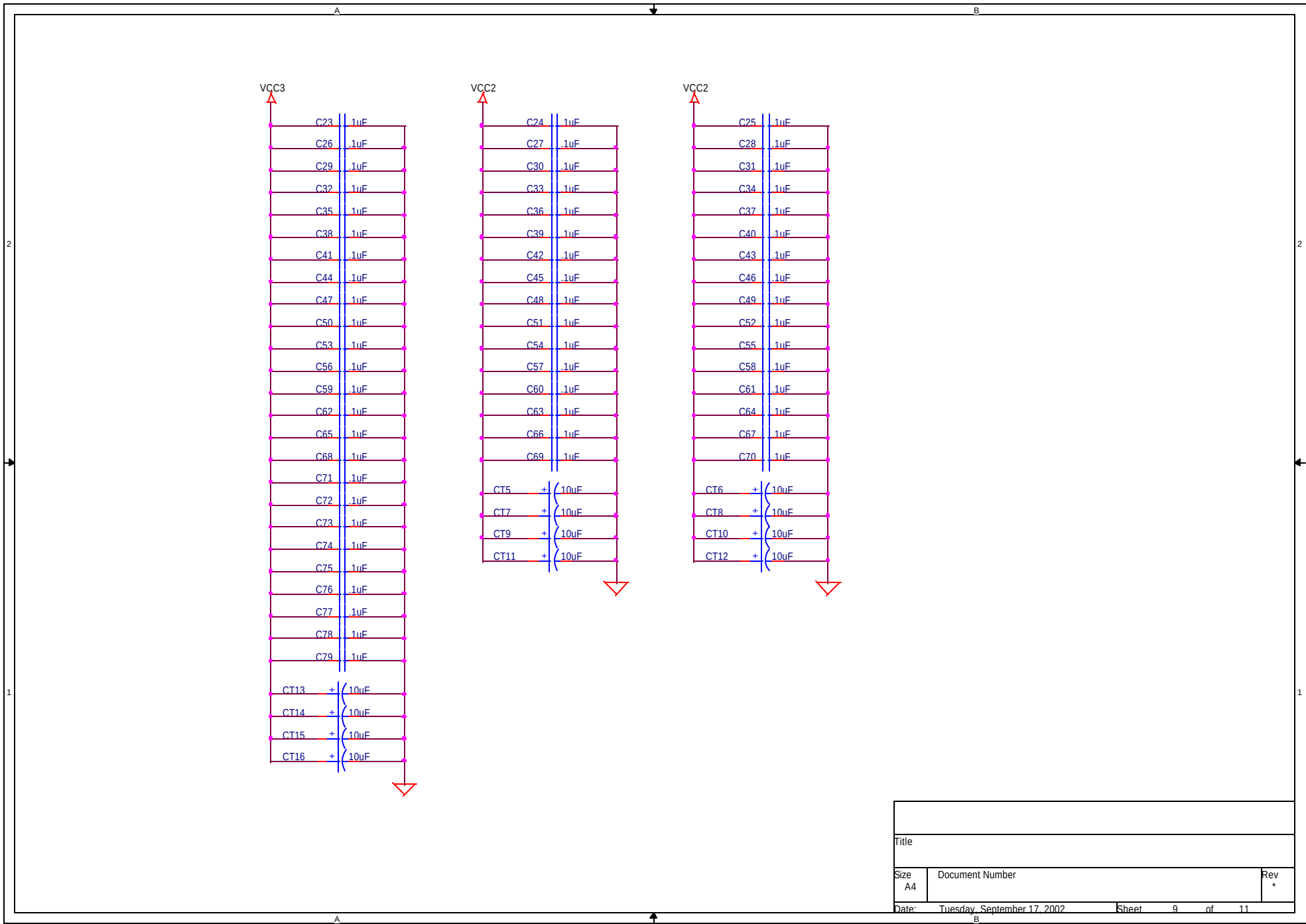
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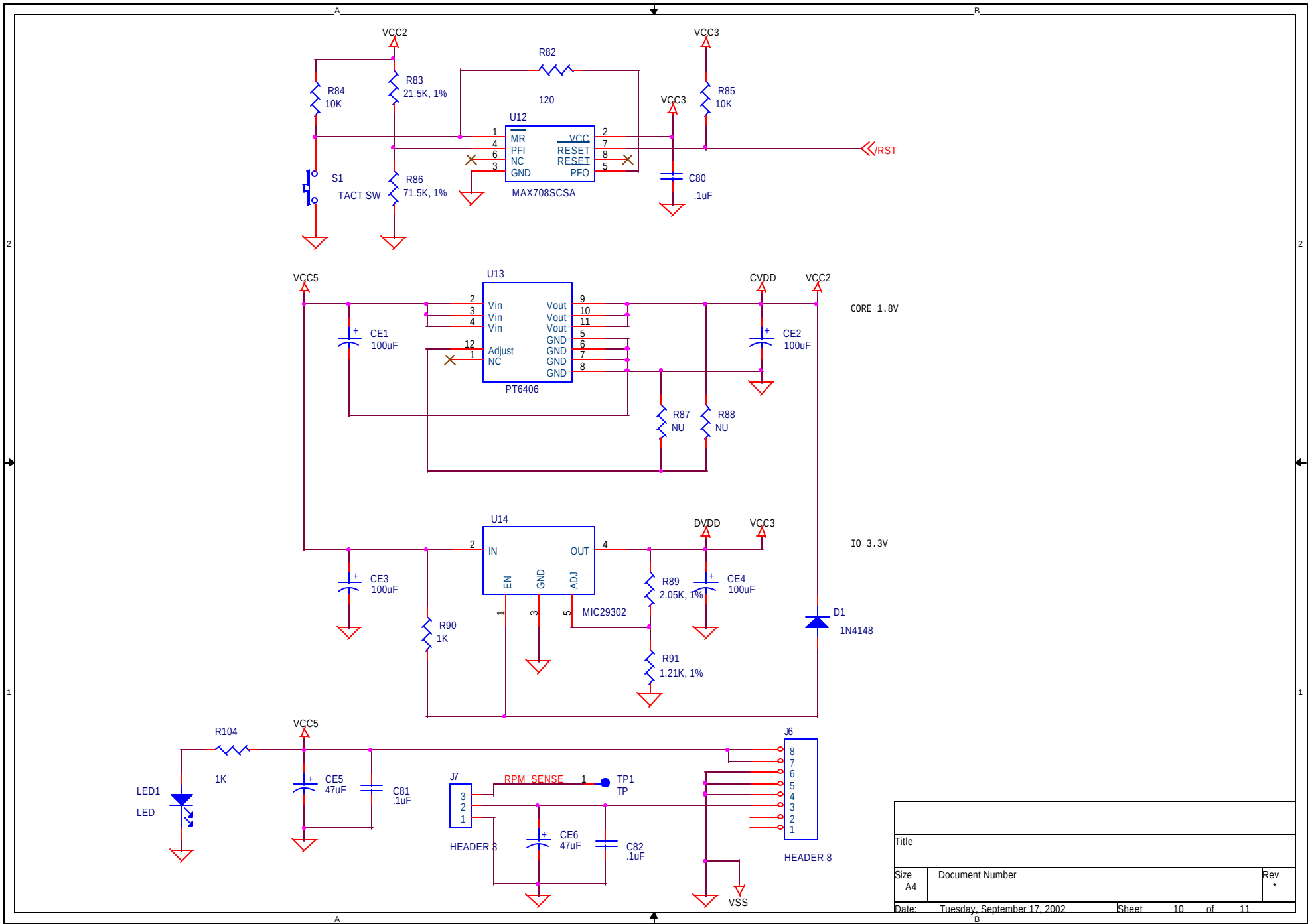


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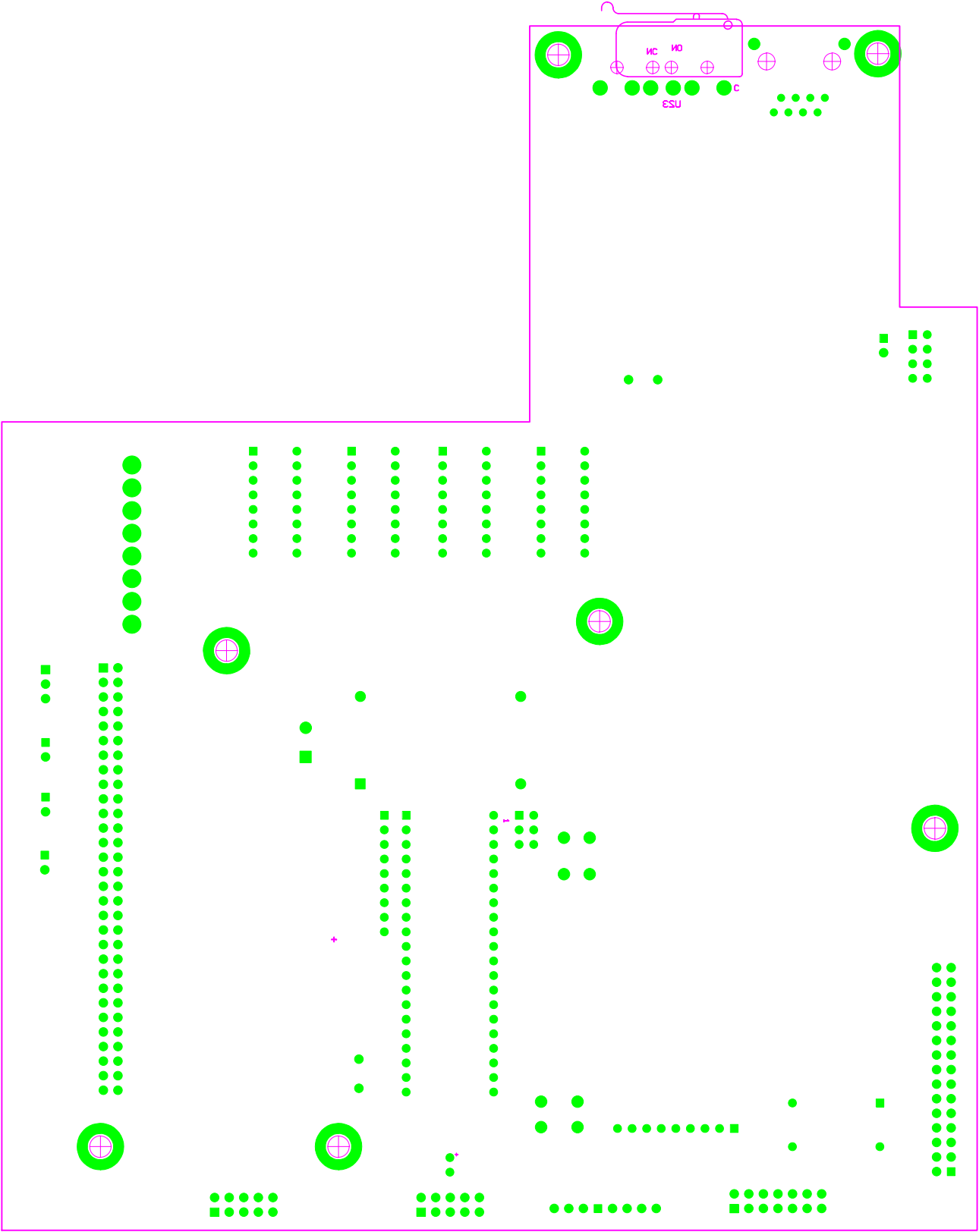




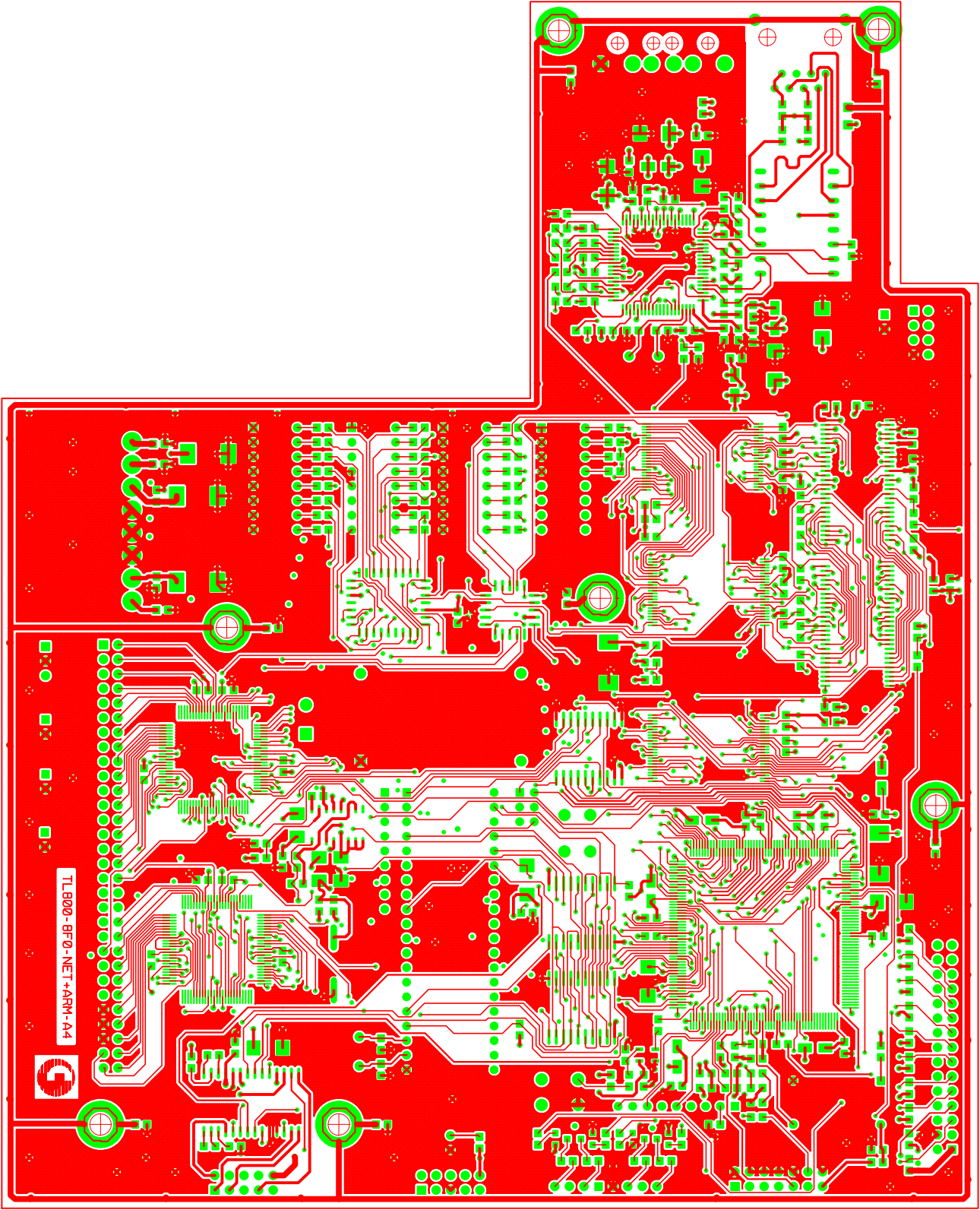
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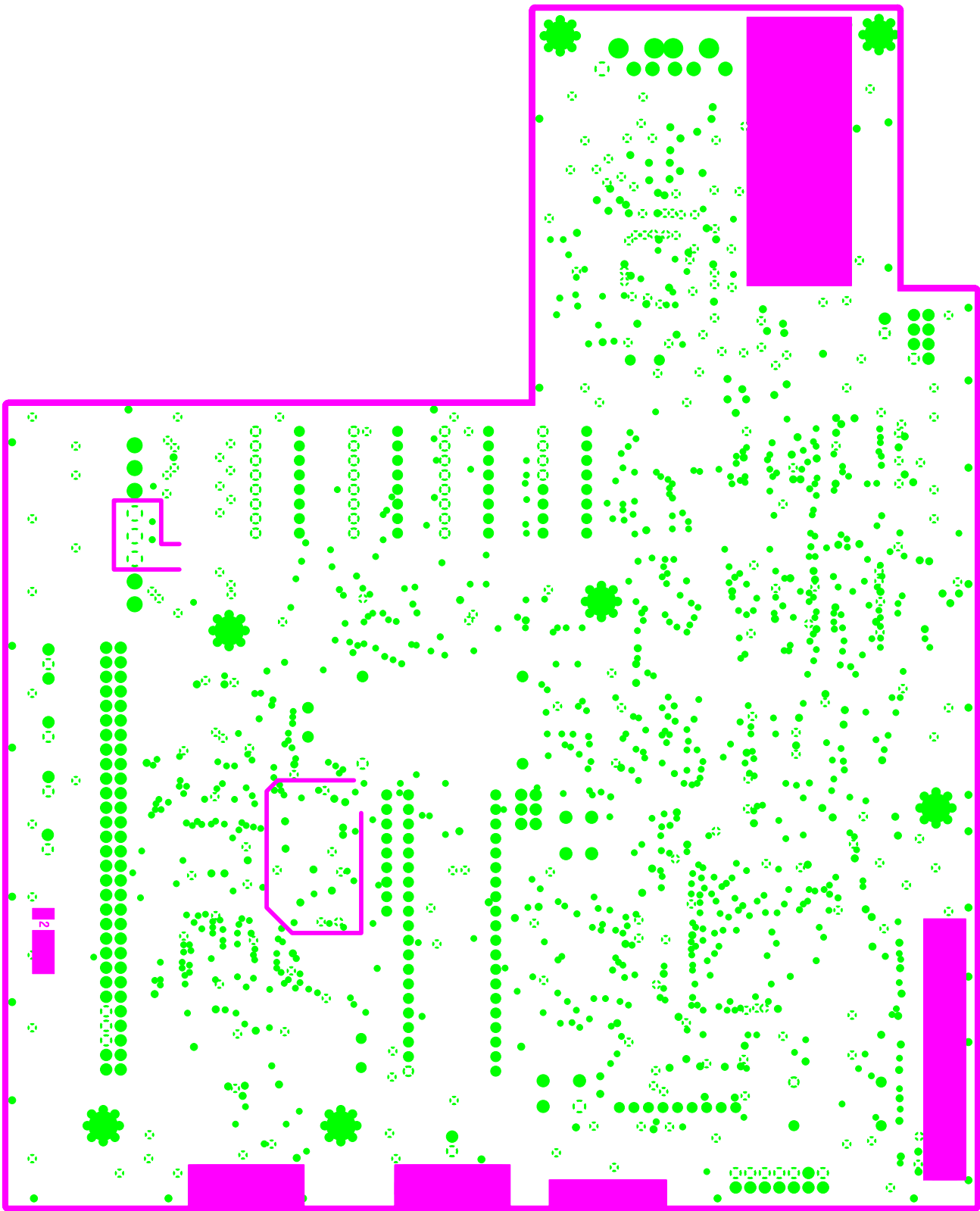
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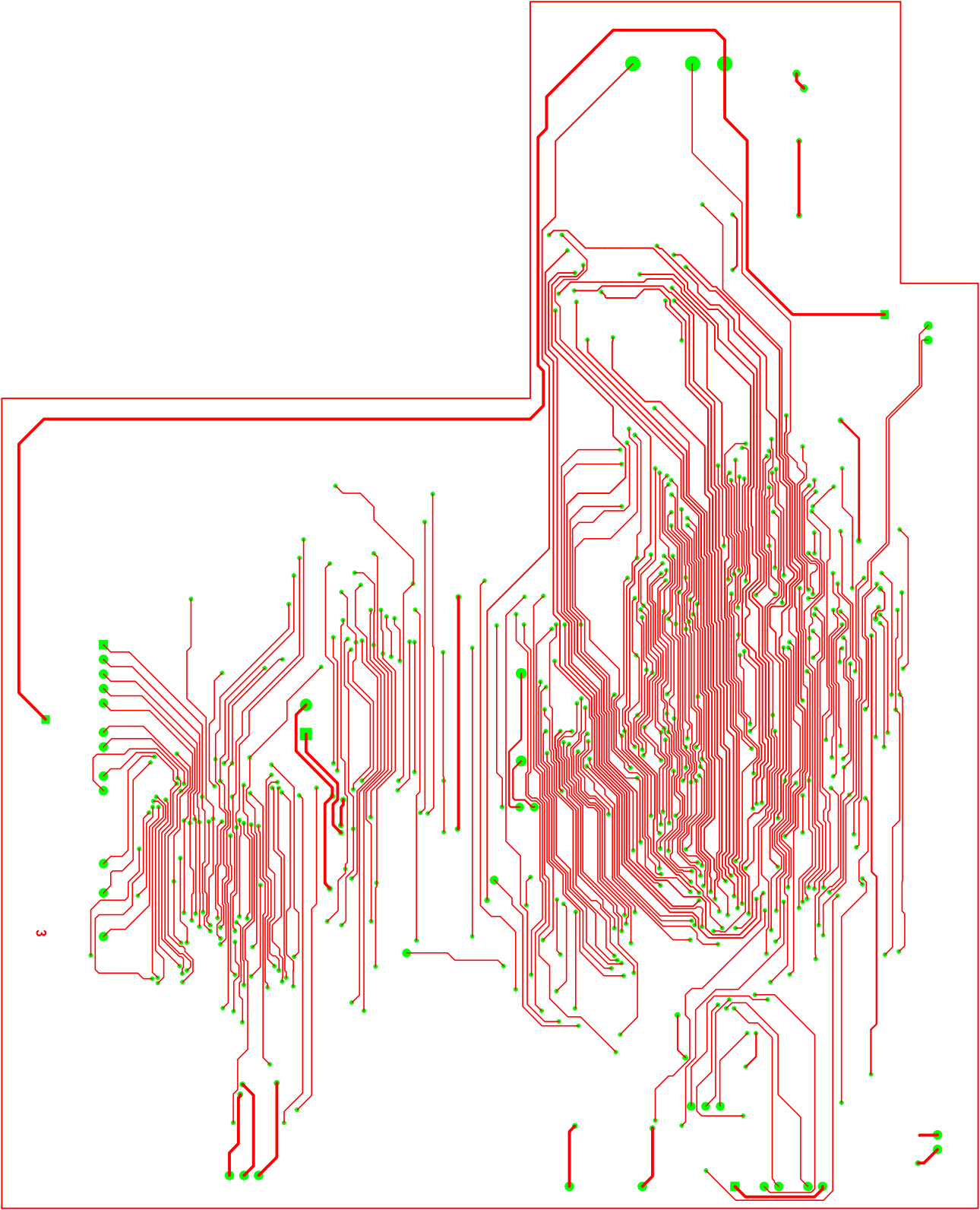
TL800-8F0-NET+ARM-A4(2003-10-23 suyo)



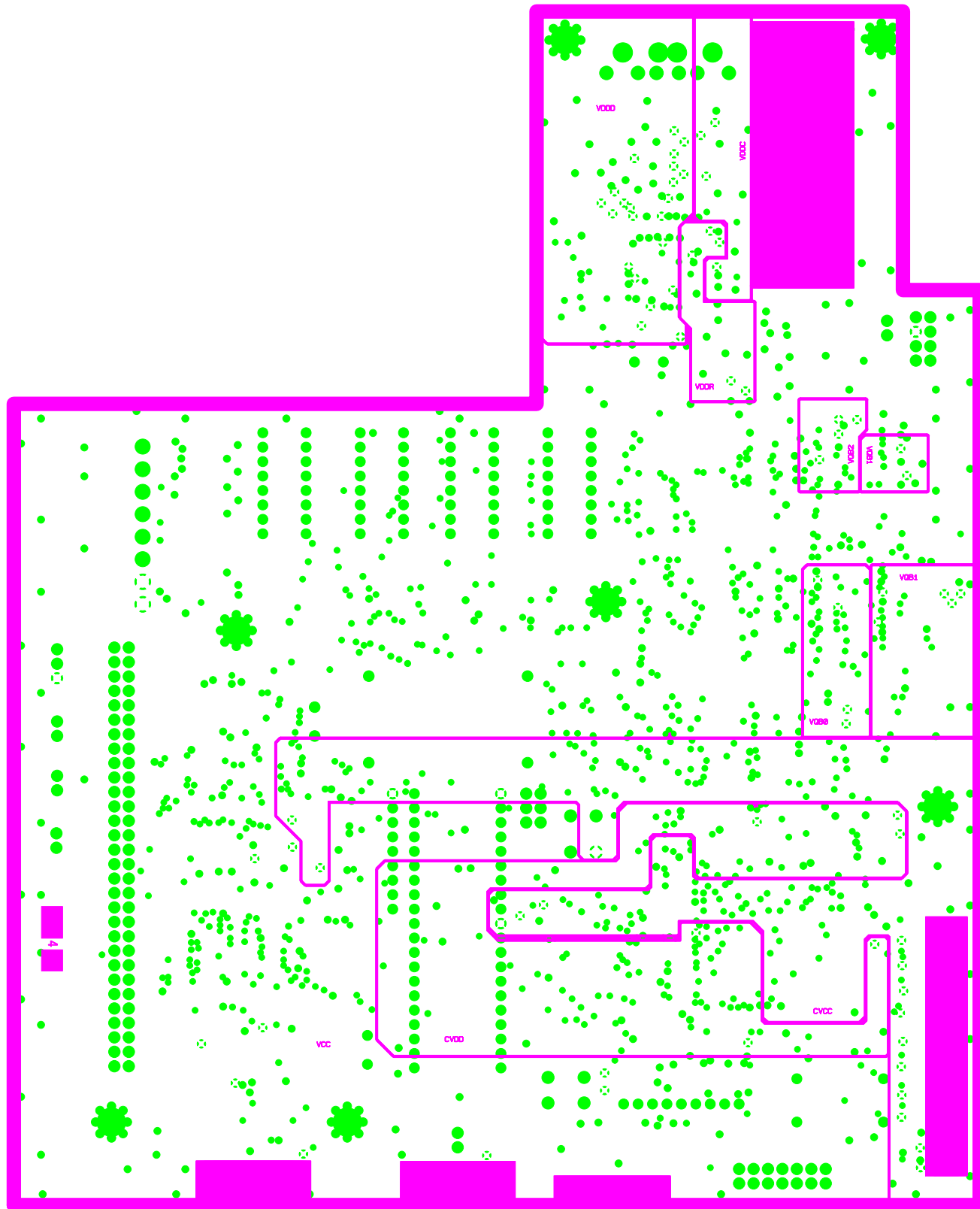
TLB00-BF0-NET+ARM-A4(2003-10-23 suyo) LAYER 1 (COMP)



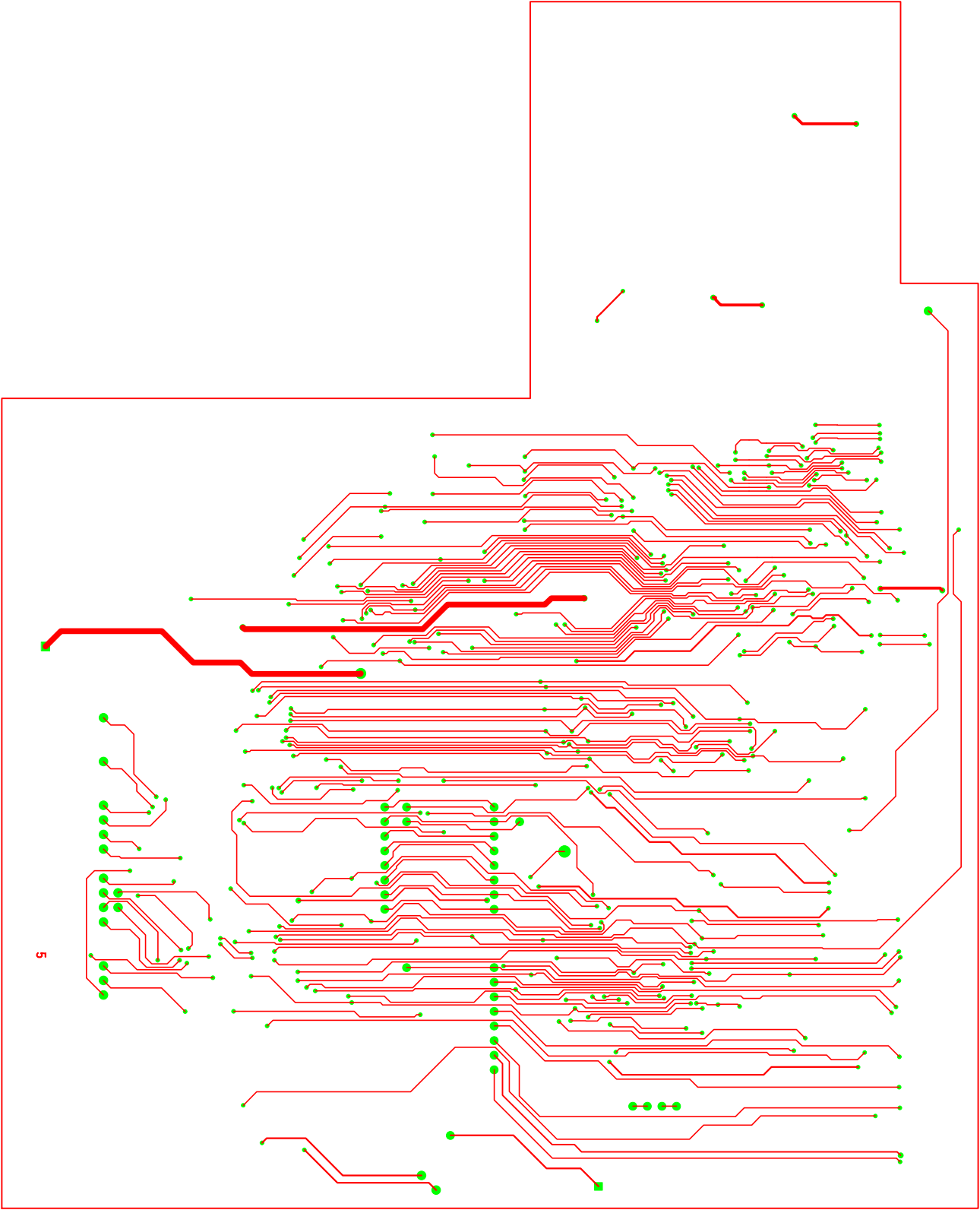
TLB00-8F0-NET+ARM-A4(2003-10-23 suyo) LAYER 2 (GND)



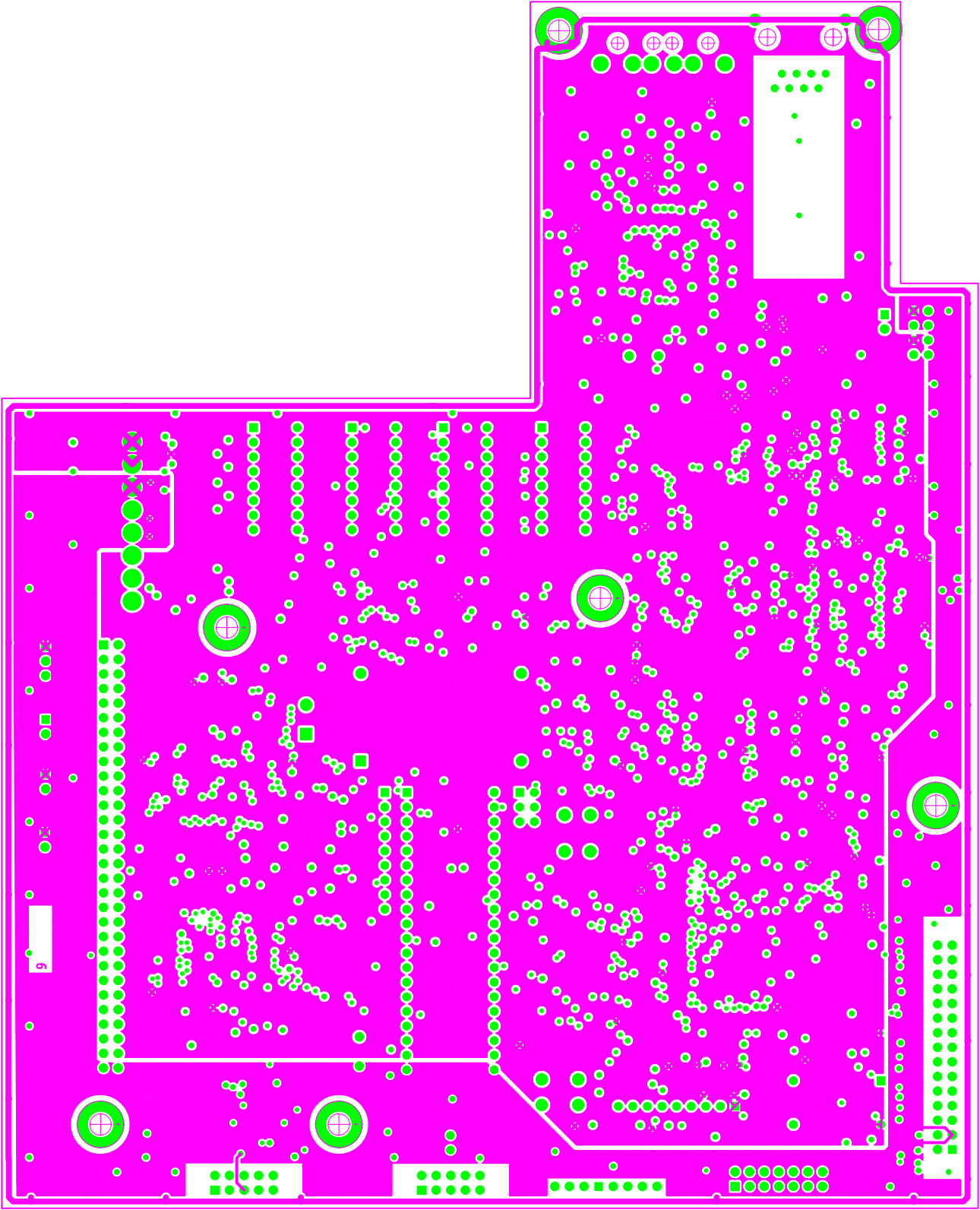
TL800-8F0-NET+ARM-A4(2003-10-23 suyo) LAYER 3



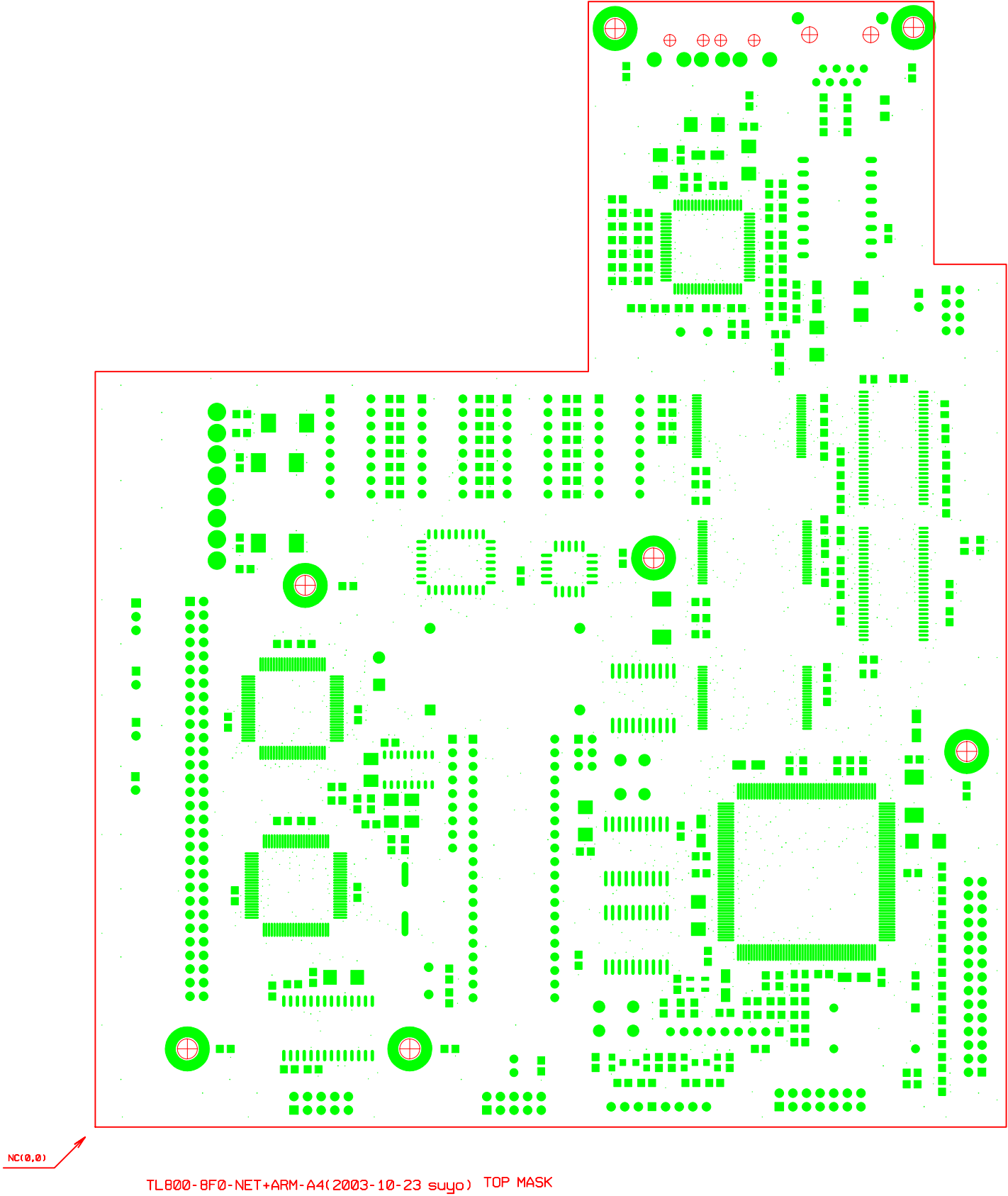
TLB00-8F0-NET+ARM-A4(2003-10-23 suyo) LAYER 4 (CVCC,CVDD,VCC,VDDC,VDDD,VDDR,VQB0,VQB1,VQB2,VQB3)

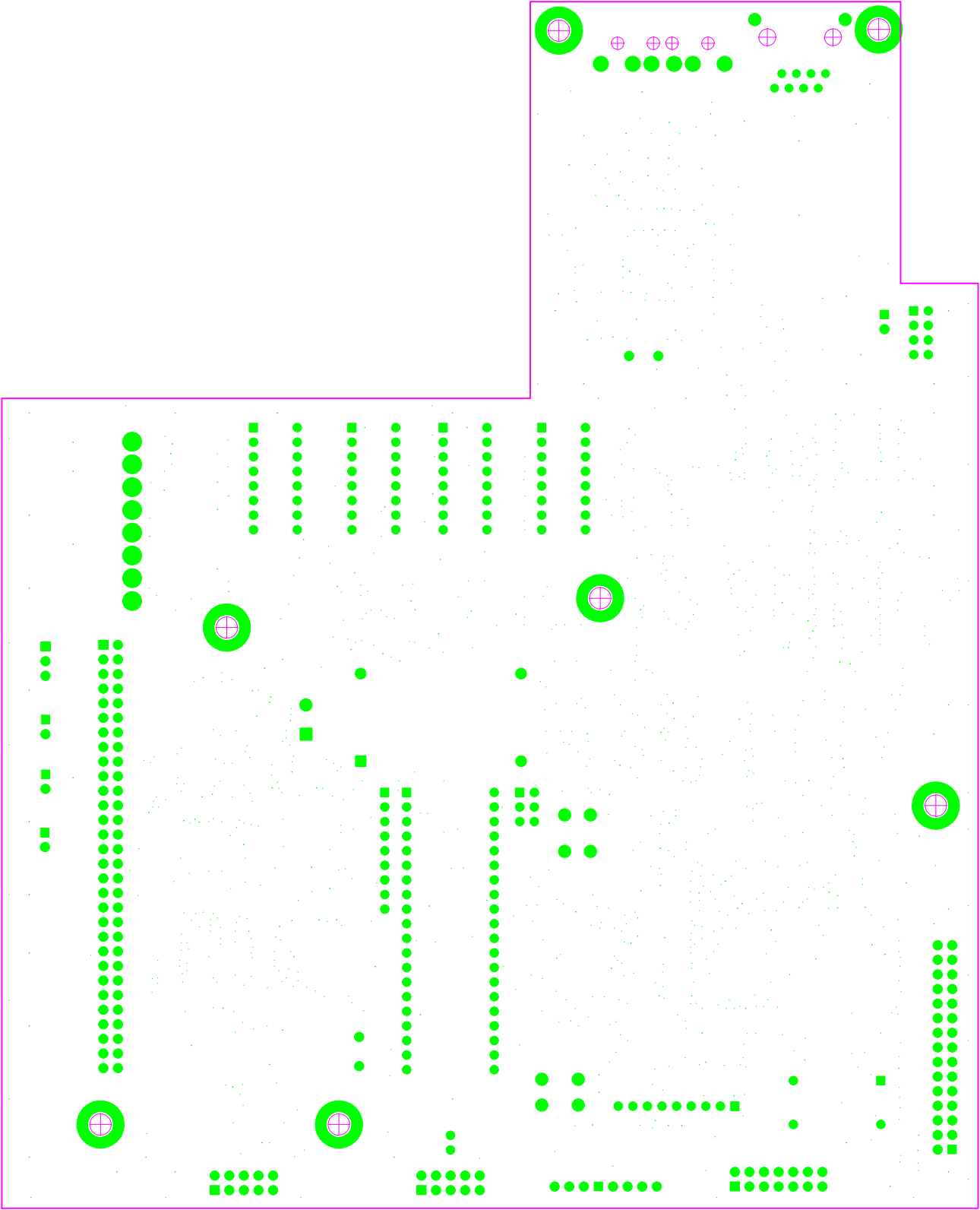


TL800-8F0-NET+ARM-A4(2003-10-23 sugo) LAYER 5

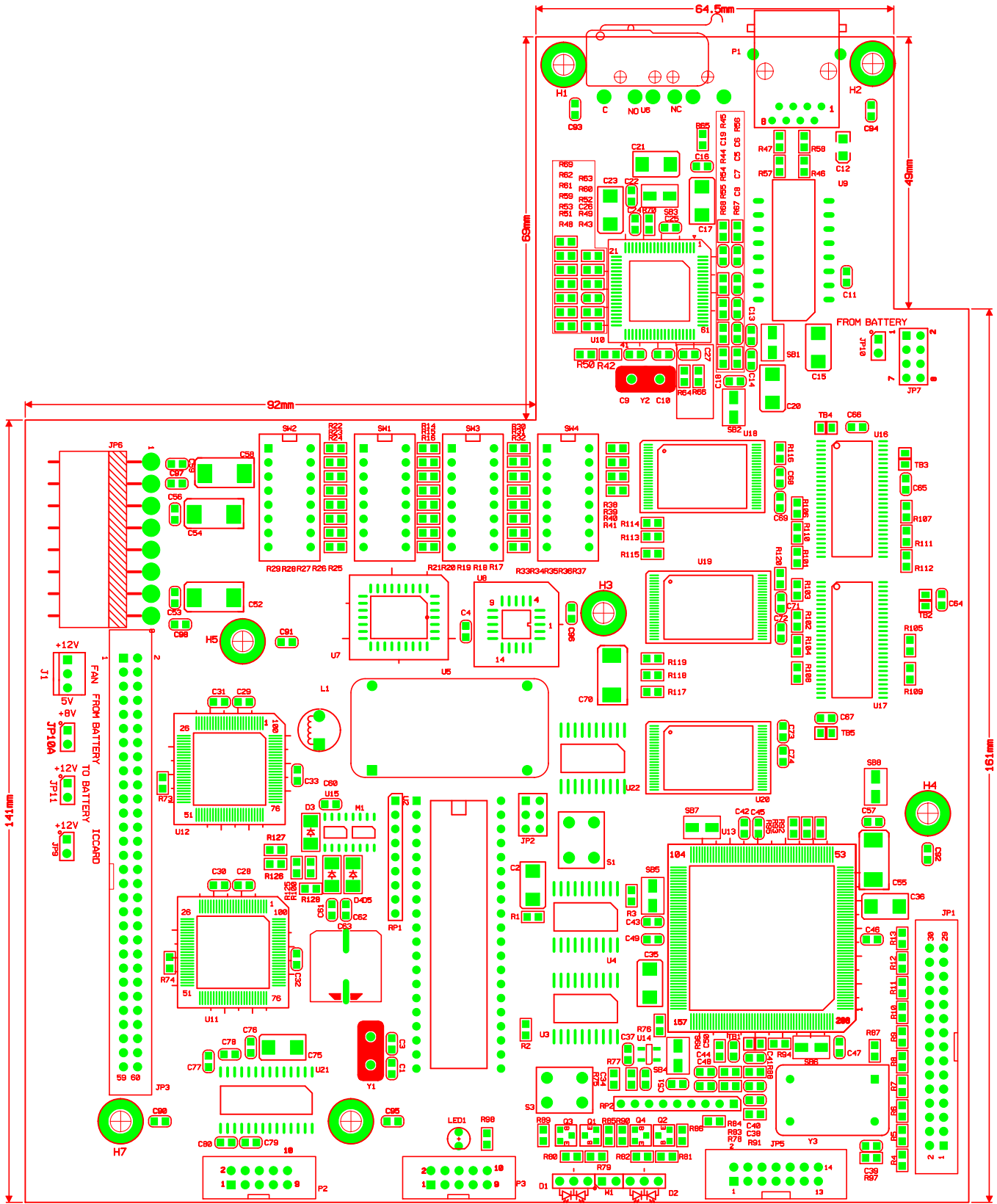


TLB00-8F0-NET+ARM-A4(2003-10-23 suyo) LAYER 6 (3.3V,12V)

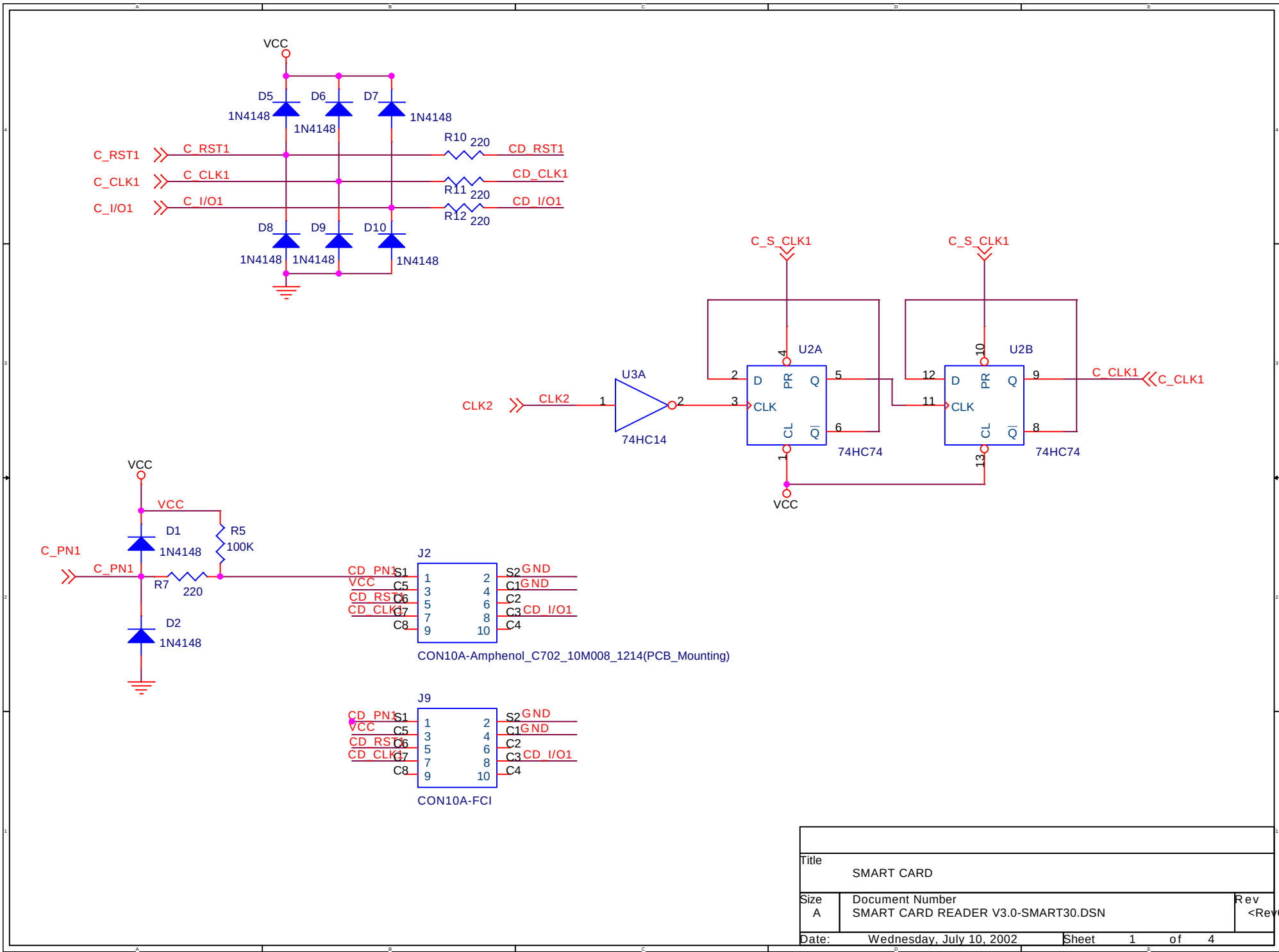




TL800-8F0-NET+ARM-A4(2003-10-23 suyo) BOT MASK

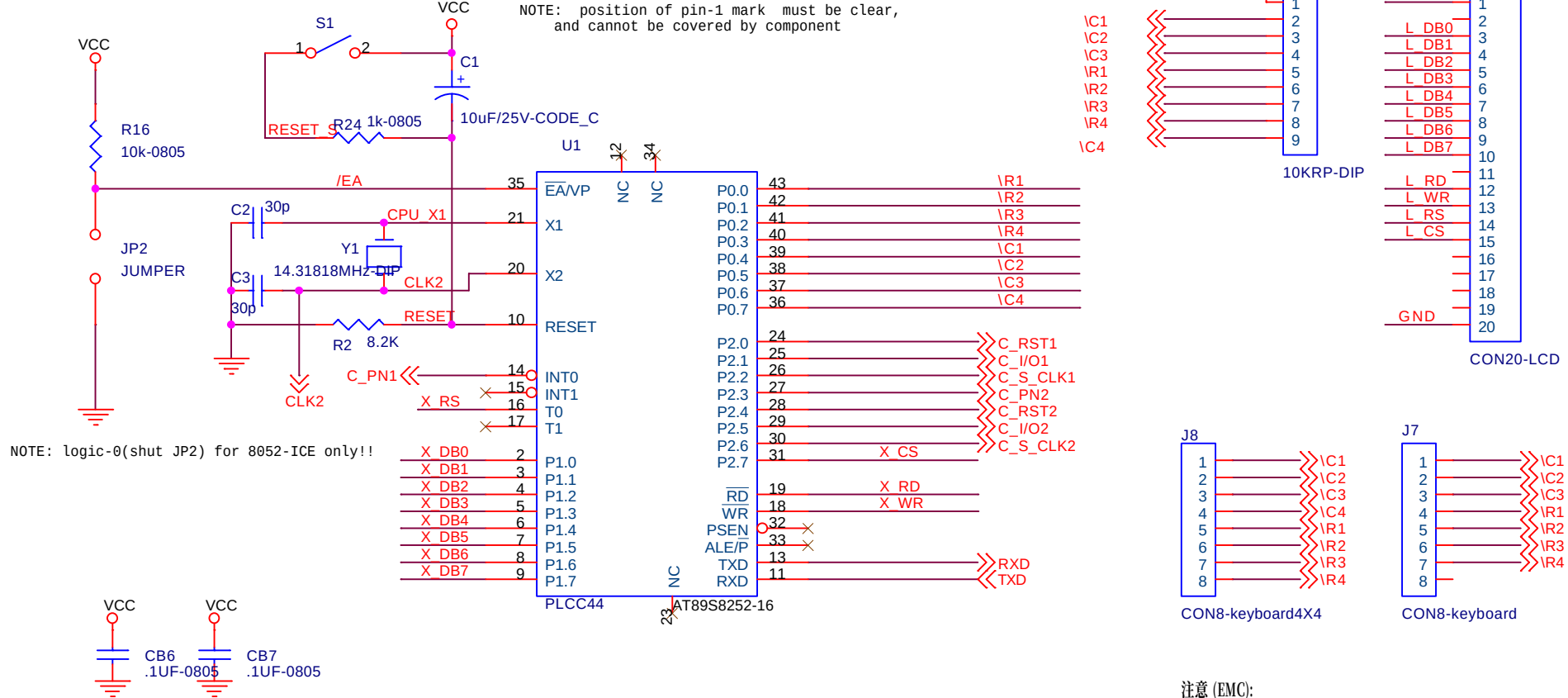


TL800-8F0-NET+ARM-A4(2003-10-23 suyo) COMP SIDE



NOTE: check netlist for VCC & GND

NOTE: position of pin-1 mark must be clear,
and cannot be covered by component



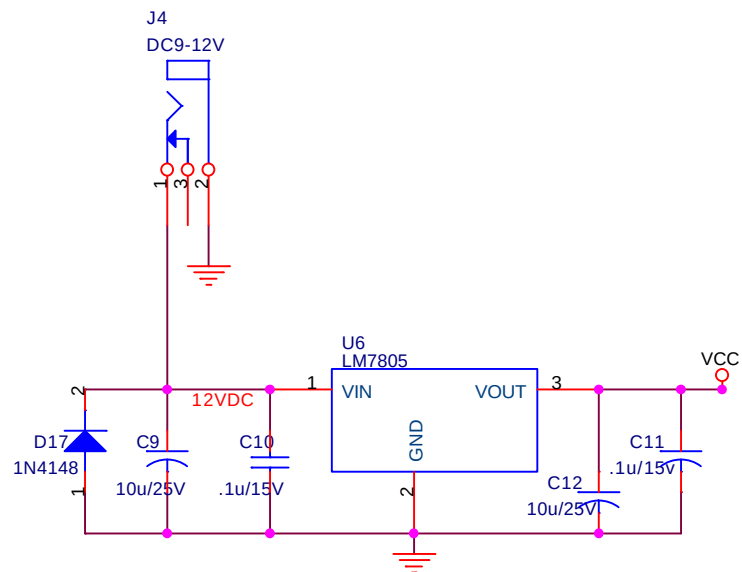
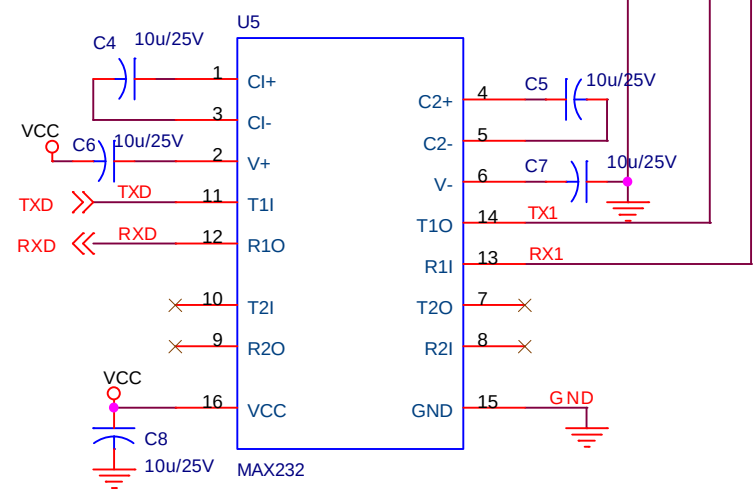
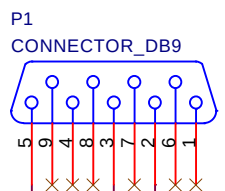
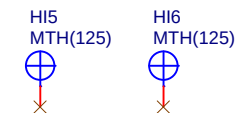
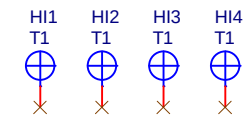
NOTE: logic-0(shut JP2) for 8052-ICE only!!

注意 (EMC):

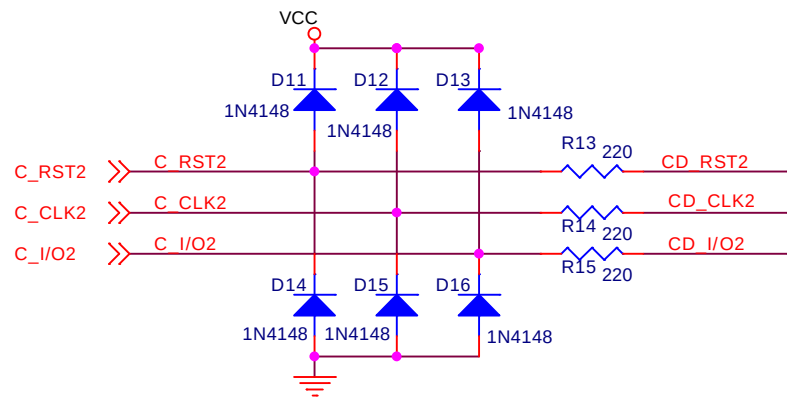
滤波电容器儘量靠 儲結構件



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CPU			
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POWER & RS232C		
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CLK2

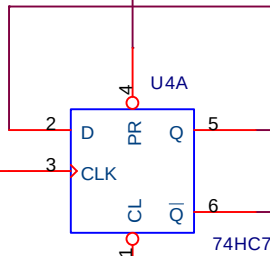
CLK2

U3C

74HC14

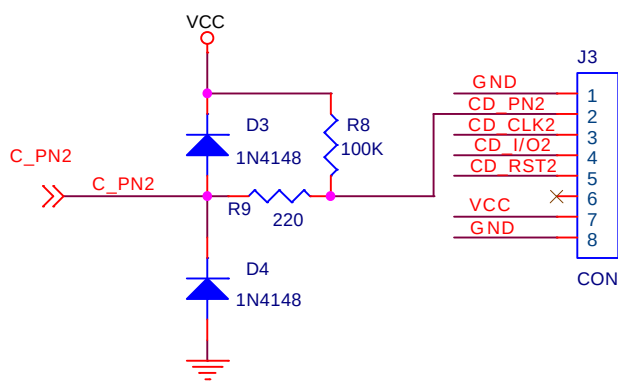
C_S_CLK2

C_S_CLK2



註: CLK2 = 14.31818 MHz
C_CLK = 3.579545 MHz
...almost =3.5712 MHz

3571200/372=9600...baud-rate



CON8-Amphenol_C707_10M006_0002(SIM-LOCK)

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SAM I/F		
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