DPAC TECHNOLOGIES®
Products & Services for the Integration Age™

WIRELESS PRODUCTS

Airborne™ Wireless LAN Node Module Data Book

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FCC STATEMENT

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio / TV technician for assistance.

FCC RF EXPOSURE STATEMENT

To satisfy RF expose requirements, this device and its antenna must operate with a separation distance of a least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

INFORMATION FOR CANADIAN USERS (IC NOTICE)

This device has been designed to operate with an antenna having a maximum gain of 5 dBi. Antenna having a higher gain is strictly prohibited per regulations of Industry Canada. The required antenna impedance is 50 ohms.

To Reduce potential radio interference to other users, the antenna type and its gain should be so chosen than the equivalent isotropically radiated power (EIRP) is not more than the required for successful communication.

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CHAPTER 1
INTRODUCTION

1.1 OVERVIEW

Airborne™ is a line of highly integrated 802.11 wireless products based on the Airborne Wireless LAN Node Module. The Airborne Wireless LAN Node Module includes a radio, a baseband processor, an application processor, and firmware for a "drop-in" Web-enabled Wi-Fi solution. Since there is no need to develop driver software or to develop the RF and communications expertise in-house, original equipment manufacturers (OEMs) can realize reduced product-development costs and a quick time-to-market. Airborne™ modules provide instant Local Area Network (LAN) and Internet connectivity, and connect through simple standard interfaces to a wide variety of applications.

1.2 CONFIGURATIONS

The Airborne Wireless LAN Node (WLN) Module consists of a fully integrated 802.11 radio and application processor available in two models (see Table 1).

Table 1. Airborne WLN Module Configurations

Configuration	Description	DPAC Model Number
Airborne 802.11b Wireless LAN Node Module – UART Version	Module with UART firmware and UART interface	WLNB-AN-DP101
Airborne 802.11b Wireless LAN Node Module – SPI Version	Module with SPI (Serial Peripheral Interface) firmware and SPI interface	WLNB-AN-DP102

1.3 FEATURES

The following list describes the key features of the Airborne WLN Module.

- 802.11b wireless LAN (Wi-Fi) standards-based technology
- Highly integrated module includes radio, baseband and MAC processor, and application processor
- Built-in TCP/IP and UDP features provide flexible LAN connectivity options
- Built-in Web server enables drop-in LAN and Internet connectivity
- Simplified data communication interface speeds development and time-to-market with reduced development costs
- Simplified antenna connections reduce the need for RF communications expertise
- Powerful integrated command interface eliminates the need to develop complicated software drivers

- Configurable serial, digital, analog I/O, I^2C (master), and SPI (slave) ports
- UART or SPI interface

1.4 APPLICATIONS

The Airborne WLN Module's small physical footprint makes the Module easy to embed into new or existing designs. The Module is interoperable with industry-standard IEEE 802.11 Access Points that provide a low-cost infrastructure for connection to a LAN and to the Internet.

The built-in TCP/IP stack, Real Time Operating System (RTOS), and application firmware provide embedded devices with instant LAN and Internet connectivity, without requiring special WLN Module programming. Only a simple configuration procedure is required using either DPAC's built-in Web-page interface or the WLN Module's powerful Command Line Interface. An integrated Web server makes it easy to monitor and control any device remotely using a standard browser. Additionally, OEMs can create custom Web pages that deliver content from their application.

The Airborne WLN Module has been designed specifically to provide wireless LAN and Internet connectivity in industrial, scientific, medical, automotive, and other OEM applications. It is an excellent solution for remote sensing and data collection. Equipment with an embedded Airborne WLN Module can be monitored and controlled by a handheld device, by a personal computer in a central location, or over the Internet. This eliminates cabling and allows the equipment to be moved. Additionally, e-mail or text messages can be sent, advising appropriate personnel of alarm conditions or equipment status.

1.5 USING THIS DOCUMENT

In addition to this chapter, this book contains the following chapters and appendixes:

- *Chapter 2, Airborne Wireless LAN Node Module* — describes the hardware and software characteristics of the Airborne WLN Module.
- *Chapter 3, Recommended Layout Practices* — provides suggested layout practices for the Airborne WLN Module.
- *Chapter 4, Serial Peripheral Interface (SPI)* — describes the Airborne WLN Module's SPI interface.
- *Chapter 5, Web Interface* — describes how to use the Web-based console to configure, manage, and view the status of the Airborne WLN Module.
- *Appendix A, Command Line Interface* — describes the Airborne WLN Module command line interface.
- *Appendix B, Power Control* — describes a suggested power supply design.
- *Appendix C, Radio Frequency Channels* — lists radio-frequency channels.
- *Appendix D, Glossary* — defines the terms associated with the Airborne WLN Module and wireless networks in general.

For convenience, an Index appears at the end of this book.

1.6 CONVENTIONS

The following conventions are used in this book:

1.6.1 Terminology

In the following chapters, these terms are used:

- "Airborne Wireless LAN Node Module" (abbreviated Airborne WLN Module) is used to identify the Module the first time in a chapter. Thereafter, the term "Module" is used.
- "Serial Host" refers to a device, such as an embedded microcontroller, that communicates with the Airborne WLN Module via the Module's serial UART interface.
- "LAN Host" refers to a LAN-based application such as a Web Browser or TCP client that communicates with the Airborne WLN Module via a wireless network connection.

1.6.2 Notes

A note is information that requires special attention. The following convention is used for notes.

Note: A note contains information that deserves special attention.

1.6.3 Cautions

A caution contains information that, if not followed, can cause adverse consequences or damage to the product. The following convention is used for cautions.

Caution: A caution contains information that, if not followed, can cause damage to the product or adverse consequences to the user.

1.6.4 Courier Typeface

Commands and other input that a user is to provide are indicated with `Courier` typeface. For example, typing the following command and pressing the Enter key displays the result of a command:

```
wl-scan <cr>


 SSID:            FirstAccessPoint
 BSSID:           0006255D537D
 signal (dBm):    -56
 noise (dBm):     -92
 rate (KB/s):     0x0014
 capabilities:    0x0005
 channel:         0x0007
```

1.7 RELATED DOCUMENTATION

In addition to this book, the following documents are provided on the Evaluation Kit or Developer's Kit CD:

- Airborne™ DLL Programmer's Guide
- Airborne™ Wireless LAN Node Module Evaluation and Development Kit Product Brief
- Airborne™ Wireless LAN Node Module Evaluation and Development Kit Quick Start Guide
- Airborne™ Wireless LAN Node Module Evaluation and Development Kit User's Guide
- Airborne™ Wireless LAN Node Module Firmware Release Notes
- Airborne™ Wireless LAN Node Module Industrial Control Applications
- Airborne™ Wireless LAN Node Module Medical Applications
- Airborne™ Wireless LAN Node Module Product Brief
- Airborne™ Wireless LAN Node Module Transportation-Trucking Applications
- End User License Agreement
- OEM Configuration Tool Release Notes
- VCOM Configuration Utility Release Notes
- VCOM Quick Start Guide
- Other Product Briefs, Release Notes, and Application Notes

These documents are provided as Portable Document Format (PDF) files. To read them, you need Adobe® Acrobat® Reader® 4.0.5 or higher. For your convenience, Adobe Reader is provided on Airborne distribution CDs. For the latest version of Adobe Acrobat Reader, go to the Adobe Web site: www.adobe.com.

Additional literature about AirborneDirect products and the Airborne WLN Module that powers them, such as application notes, product briefs, and white papers, can be found on the DPAC Technologies Web site: www.dpactech.com.

DPAC Technologies also offers developer documentation for its AirborneDirect products. Please contact DPAC Technologies for more information.

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CHAPTER 2
AIRBORNE WIRELESS LAN NODE MODULE

2.1 OVERVIEW

This chapter describes the hardware and software characteristics of the Airborne WLN Module. Topics in this chapter include:

- 2.2 Specifications (page 8)
- 2.3 Block Diagram (page 9)
- 2.4 Hardware Description (page 9)
- 2.5 Host Pin Assignments and Signal Descriptions (page 11)
- 2.6 Antenna Pin Assignments and Descriptions (page 15)
- 2.7 Reset (page 15)
- 2.8 Airborne WLN Module Operation (page 17)
- 2.9 Design Guidelines (page 18)
- 2.10 Package Configuration (page 21)
- 2.11 Electrical Characteristics (page 22)

Note: Unless otherwise noted, the information in this chapter applies to both the UART WLN Module and SPI WLN Module.

2.2 SPECIFICATIONS

Table 2. Airborne WLN Module Specifications

Specification	Description
Technology	IEEE 802.11b DSSS, Wi-Fi compliant
Frequency	2.400 – 2.4835 GHz (US/Can/Japan/Europe) 2.471 – 2.497 GHz (Japan)
Modulation	DBPSK (1 Mbps), DQPSK (2 Mbps), and CCK (5.5 and 11 Mbps)
Clock Frequencies	4.8 MHz – CPU reference clock 32.768 KHz – real-time clock
Channels	USA/Canada: 11 channels (1 – 11) Europe: 13 channels (1 – 13) Japan: 14 channels (1 – 14) France: 4 channels (10 – 13)
Data Rate	11, 5.5, 2, 1 Mbps (raw wireless rate)
MAC	CSMA/CA with ACK, RTS, CTS
RF Power	+15 dBm (typical) Approx.32 mW
Sensitivity	-82 dBm for 11 Mbps -86 dBm for 5.5 Mbps -88 dBm for 2 Mbps -90 dBm for 1 Mbps
Security	WEP standard encryption, 64 or 128 bits
Antenna	Two U.FL coaxial connectors, 50Ω, supports receive diversity
Supply	3.3 VDC
Current Consumption	420 mA – transmit mode (typical) 350 mA – receive mode (typical) 250 mA – doze mode (typical – see Note 1 and Note 5 below) 235 mA – snooze mode (typical – see Note 1 and Note 5 below) 50 mA – sleep mode (typical – see Note 5 below)
Power Up Inrush Current	1900 mA (max)
Operating Temperature	Industrial: -40°C – +85°C (see Note 2 below) (Meets IEEE 802.11 industrial temperature range)
Application Processor	16-bit, 120 MIPS @ 120 MHz
Serial Interface	UART: Up to 460,800 bps SPI (slave): Can be clocked up to 20 MHz
Data Throughput	UART-to-LAN – 320 Kbps (max) (see Note 5 below) LAN-to-UART – 70 Kbps (max) (see Note 3 and Note 5 below)
Memory	Flash: 64 Kbytes onboard, 512 Kbytes expansion (see Note 4 below) SRAM:20 Kbytes onboard, 128 Kbytes expansion
Digital I/O	Up to 8 digital I/O ports and status
Analog Inputs	Up to 8 channels, 10-bit resolution, single ended, 0 – 2.5 V
Connector	36 pin (pn: HRS DF12-36DS-0.5 V) 4-mm height

Note 1: The doze, snooze, and sleep mode current consumption depends on an Access Point's low power support implementation. Some Access Points do not include support for low-power stations.
Note 2: Temperatures above +80°C reduce wireless performance. Module operates from -40°C cold start.
Note 3: Rates are based on operation at maximum wireless data rate, with escape checking set off, serial buffer size set to maximum, minimum wireless interference, and no other LAN traffic.
Note 4: Flash and SRAM are not available to external applications.
Note 5: WLN UART model only.

2.3 BLOCK DIAGRAM

Figure 1 shows the block diagram of the Module hardware.

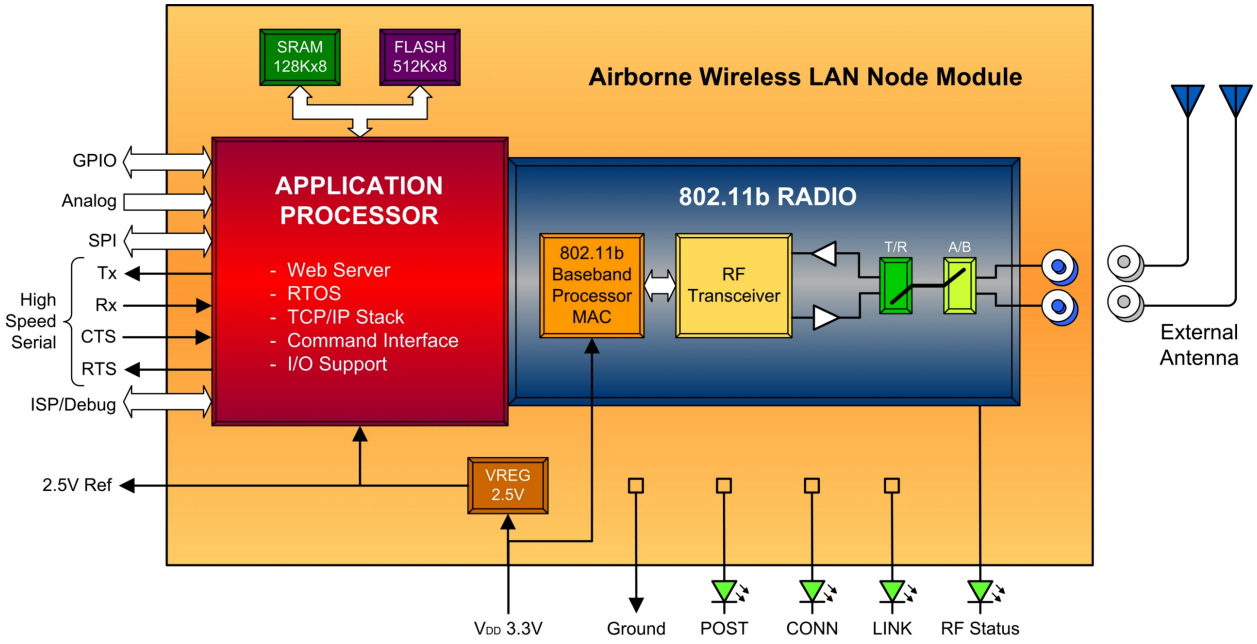

Figure 1. Airborne WLN Module Hardware Block Diagram

Note: The SPI and UART are not available in the same model.

2.4 HARDWARE DESCRIPTION

The Module contains all of the hardware and firmware components required to implement a full Wireless Fidelity (Wi-Fi)-compatible IEEE 802.11b network interface. It includes two antenna connections, along with all required RF, baseband, and application-processor circuitry. Depending on the configuration of the application firmware, the Module can operate as an embedded communication module under the control of a Host application, or as an application Host. The following sections describe the hardware associated with the Module.

2.4.1 Application Processor

The application processor interfaces to the radio module and is the link between the wireless LAN and the embedded Host application. A TCP/IP stack with TCP server, TCP client and Web server capabilities, an RTOS kernel, a radio Link Layer interface, and a Host application layer Command Line Interface all support features required for flexible LAN connectivity.

The application processor contains its own memory, Flash, and RAM, which are used exclusively to support the Module's application functionality.

2.4.2 General Purpose Input/Output

A set of General Purpose Input/Output (GPIO) ports is provided for control, sensing, and data exchange with the Host system or interface. These ports include digital input/output, analog input, and serial interfaces.

2.4.2.1 Digital Inputs

All digital ports are configurable as digital inputs. The ports use 3.3 V signal levels and are 5.0 V tolerant.

2.4.2.2 Analog Inputs

The analog input ports accept analog signals from 0 - 2.5 V levels and are 3.3 V tolerant. These ports can be alternatively used as digital inputs and can be set for use as digital outputs.

2.4.2.3 Serial Ports

The High Speed serial port can be used as a serial UART or as an SPI Slave. An I^2C Master interface is also available. The serial ports use 3.3 V signal levels and are 5.0 V tolerant.

2.4.3 Static Random Access Memory

The Module includes up to 128 KB Static Random Access Memory (SRAM) to support its functions and features. SRAM is built-in and is used exclusively by the application processor.

2.4.4 Flash Memory

The Module includes up to 512 KB Flash memory to support its functions and features. Flash memory is built-in and used exclusively by the application processor.

2.4.5 IEEE 802.11 Media Access Control

The IEEE 802.11 Media Access Control (MAC) provides for, and manages, all time-critical wireless media control.

2.4.6 IEEE 802.11 Baseband/RF

The IEEE 802.11 Baseband RF device provides the appropriate baseband signal processing, as well as the appropriate RF modulation for the wireless connection.

2.4.7 Transmit/Receive Switch

The Transmit/Receive (T/R) Switch selects the appropriate signal path for the antenna during transmit and receive operations. The IEEE 802.11 MAC controls the T/R Switch automatically.

2.4.8 A/B Diversity Switch

The A/B Diversity Switch controls whether Antenna 1 (J1) or Antenna 2 (J2) is selected. The IEEE 802.11 MAC controls the A/B Diversity Switch automatically when diversity is enabled. Diversity is limited to receive only (no transmit).

2.4.9 External Antenna Connections

The Module provides two U.FL-style connectors for connection to external antennas. The two external antenna connectors provide 50 Ω impedance RF signals at 2.4 GHz and offer receive diversity support for OEM system implementations.

2.4.10 Power Supply

The Module requires a single 3.3 V power source. The power source must provide sufficient current for peak startup inrush and peak transmit burst in accordance with the Module's specifications (see page 8).

The Module includes an on-board regulator that derives 2.5 V for the Analog Converter. The 2.5 V is provided as a reference source for analog input signals.

Caution: The 2.5 V source is for reference only and must not be used to power devices.

2.4.11 High Speed UART Configurations

- Baud rate parameters: 300, 600, 1200, 2400, 4800, 9600, 14400, 19200, 28800, 38400, 57600, 115200, 230400, 460800 bps
- Flow control parameters:
  - Hardware handshake: supports CTS and RTS
  - Software handshake: supports XON and XOFF
  - No flow control

2.4.12 SPI Configurations

There are no user-configurable parameters.

2.5 HOST PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

The interconnect between the Module and the Host system is a 4 mm high, 36-pin, Hirose DF12-36DS-0.5 V(80) connector.

The part number for the 4-mm high mating connector is Hirose DF12-36DP-0.5 V(80). Table 3 lists the Module's Host pin assignments.

Table 3. Airborne WLN Module Pin Assignments

Pin	Signal	Sink	Source	Description
1	GND			Ground
2	TSI			ISP Serial Data In (see Note 1)
3	DV_{DD}			Power, +3.3 V
4	DV_{DD}			Power, +3.3 V
5	V2.5			2.5 V Reference output (for reference only)
6	RFU			Reserved (see Note 1)
7	/RESET			Reset – active low. A transition to high releases the reset condition (see "Reset" on page 15). There is a weak pull-up on this pin, but floating this pin does not guarantee a logic high.
8	/TSS			ISP Slave Select (active low) (see Note 1)
9	G6	4 mA	4 mA	Used as analog input or digital output (see Table 6). Provides 3.3 V CMOS-compatible digital output (V_{OL}≤0.4, 2.4 V≤ V_{OH}).
10	TSO			ISP Serial Data Out (see Note 1)
11	G3	4 mA	4 mA	Used as analog input or digital output (see Table 6). Provides 3.3 V CMOS-compatible digital output (V_{OL}≤0.4, 2.4 V≤ V_{OH}). Port can be used at bootup to reset the Module to factory defaults – see Section 2.8.2, Factory Restart on page 17 for more information.
12	F5	8 mA	8 mA	Used as high-speed UART or high-speed SPI Slave (see Table 5). Signal is TTL-compatible and 5 V tolerant.
13	G5	4 mA	4 mA	Used as analog input or digital output (see Table 6). Provides 3.3 V CMOS-compatible digital output (V_{OL}≤0.4, 2.4 V≤ V_{OH}).
14	G4	4 mA	4 mA	Used as analog input or digital output (see Table 6). Provides 3.3 V CMOS-compatible digital output (V_{OL}≤0.4, 2.4 V≤ V_{OH}).
15	V_{SS}			Ground
16	V_{SS}			Ground
17	G2	4 mA	4 mA	Used as analog input or digital output (see Table 6). Provides 3.3 V CMOS-compatible digital output (V_{OL}≤0.4, 2.4 V≤ V_{OH}).
18	F4	8 mA	8 mA	Used as high-speed UART or high-speed SPI Slave (see Table 5). Signal is TTL-compatible and 5 V tolerant.
19	G1	4 mA	4 mA	Used as analog input or digital output (see Table 6). Provides 3.3 V CMOS-compatible digital output (V_{OL}≤0.4, 2.4 V≤ V_{OH}).
20	TSCK			ISP Serial Clock (see Note 1)
21	G7	4 mA	4 mA	Used as analog input or digital output (see Table 6). Provides 3.3 V CMOS-compatible digital output (V_{OL}≤0.4, 2.4 V≤ V_{OH}). Used as digital output for SPI firmware as Slave data ready interrupt.
22	G0	4 mA	4 mA	UART: Used as analog input or digital output (see Table 6). Provides 3.3 V CMOS-compatible digital output (V_{OL}≤0.4, 2.4 V≤ V_{OH}). SPI: Used as system interrupt (see Table 5). Signal is 3.3 V TTL-compatible and 5 V tolerant.

Table 3. Airborne WLN Module Pin Assignments

Pin	Signal	Sink	Source	Description
23	F6	8 mA	8 mA	Used for digital I/O and Status (see Table 4). Pre-configured as a digital output in firmware and represents the CONNECT status.
24	F7	8 mA	8 mA	Used as high-speed UART or high-speed SPI Slave (see Table 5). Signal is 3.3 V TTL-compatible and 5 V tolerant.
25	F0	8 mA	8 mA	Used for digital I/O and status (see Table 4). Pre-configured as a digital output in firmware and represents the POST status.
26	F3	8 mA	8 mA	Used for digital I/O and status (see Table 4). Pre-configured as a digital output in firmware and represents the WLAN CFG status.
27	F2	24 mA	24 mA	Used for digital I/O and status (see Table 4). Pre-configured as a digital output in firmware and represents the RF LINK status.
28	F1	24 mA	24 mA	Used as high-speed UART or high-speed SPI Slave (see Table 5). Signal is TTL-compatible and 5 V tolerant.
29	E6	24 mA	24 mA	General Purpose Digital I/O, 5 V tolerant.
30	E5	24 mA	24 mA	General Purpose Digital I/O, 5 V tolerant
31	E7	8 mA	8 mA	General Purpose Digital I/O, 5 V tolerant. Optional I^2C SDA (Data) input/output (see Table 7).
32	E4	8 mA	8 mA	General Purpose Digital I/O, 5 V tolerant. Optional I^2C SCL (Clock) output (see Table 7).
33	DV_{DD}			Power, +3.3 V
34	DV_{DD}			Power, +3.3 V
35	/RF_LED	2 mA		RF Status output, active low, represents RADIO ACTIVITY (see Table 4)
36	V_{SS}			Ground

Note 1: The ISP pins should be left as no connects and are tied high internally. ISP pins are reserved for factory loading firmware.

ISP = in-system programming port
V_{OL} = low-output voltage
V_{OH} = high-output voltage

Table 4. F0, F2, F3, F6 and RF_LED Signal Assignments

Port	Direction	
	Status*	Status Description
F0	POST	Indicates that the Module has passed its Power On Self Test (POST).
F2	RF LINK	Indicates that the Module has associated with an Access Point or peer.
F3	WLAN CFG LINK	Indicates that the Module has a Dynamic Host Configuration Protocol (DHCP) or static IP configuration.
F6	CONNECT	Indicates that the Module has made an IP connection with a device on the LAN.
/RF_LED	RADIO ACTIVITY	Blinks when radio is on and scanning for an Access Point. Solid ON when radio is on and associated.

* Status I/O is pre-assigned and controlled by the Airborne firmware.

Table 5. F1, F4, F5, and F7 Signal Assignments

Port	High Speed UART		High Speed SPI Slave	
	Signal*	Direction	Signal*	Direction
F4	HS.RTS	Out	HS.SCLK	In
F5	HS.CTS	In	HS.SS	Out
F7	HS.RXD	In	HS.SDI	In
F1	HS.TXD	Out	HS.SDO	Out
G0	(see Table 6)	(see Table 6)	HS.INT	Out

* I/O is pre-assigned and controlled by the Airborne firmware.

Table 6. G0 through G7 Signal Assignments

Port	Direction	
	Digital	Analog
G0	Out	In
G1	Out	In
G2	Out	In
G3	Out	In
G4	Out	In
G5	Out	In
G6	Out	In
G7	Out	In

Table 7. E4, E5, E6, E7 Signal Assignments

		I^2C Master	
Port	Digital	Signal	Direction
E4	Digital In/Out	SCL - Clock	Out
E5	Digital In/Out	—	—
E6	Digital In/Out	—	—
E7	Digital In/Out	SDA – Bidirectional Data	In/Out

2.6 ANTENNA PIN ASSIGNMENTS AND DESCRIPTIONS

Figure 2 shows the Module antenna connectors and Table 8 describes their pin assignments.

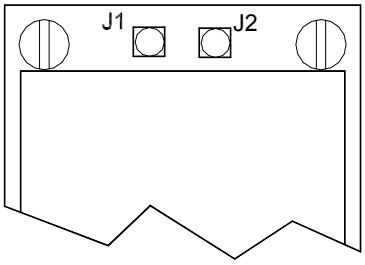

Figure 2. Antenna Connectors

Table 8. Airborne WLN Module Antenna Pin Assignments

Pin	Description
J1 (left connector)	Antenna 1
J2 (right connector)	Antenna 2

2.7 RESET

The Module incorporates a Power-On Reset (POR) detector that generates an internal reset as DV_{dd} rises during power-up. An internal startup timer together with a reset latch control the reset timeout delay. On power-up, the reset latch is cleared (CPU held in reset), and the startup timer starts counting when it detects a valid logic high signal on the /RESET pin (pin 7). When the startup timer reaches the end of the timeout period, the reset latch is cleared, releasing the CPU from reset.

Note: CPU operation does not start until the CPU is released from reset and valid core clocks are received past the system clock suspend circuit. The Module's POR is set to 1 millisecond.

Figure 3 shows a power-up sequence in which /RESET is not tied to the DV_{dd} pin, and the DV_{dd} signal is allowed to rise and stabilize before the /RESET pin is brought high. WUDX specifies the length of time from the rising edge of /RESET until the device leaves reset. For the Module, this length of time is set to 1 millisecond. In this case, the CPU receives a reliable reset.

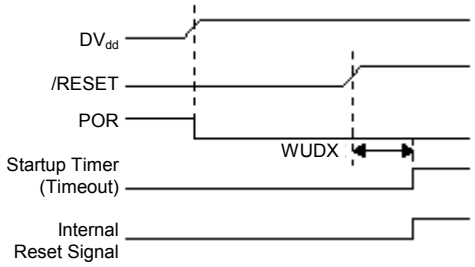

Figure 3. Power-up Sequence (Separate /RESET Signal)

Figure 4 shows the on-chip POR sequence in which the /RESET and DV_{DD} pins are tied together. The DV_{DD} signal is stable before the startup timer expires. In this case, the CPU receives a reliable reset.

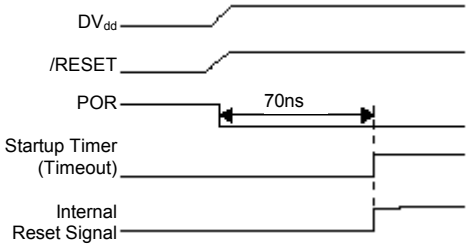

Figure 4. Power-up Sequence (/RESET Tied to DV_{DD})

Figure 5 shows a situation where DV_{DD} rises too slowly. In this scenario, the startup timer times-out before DV_{DD} reaches a valid operating voltage level (DV_{DD} min). As a result, the CPU comes out of reset and starts operating with the supply voltage below the level required for reliable performance. In this situation, an external RC circuit is recommended for driving /RESET. The RC delay should exceed five times the time period required for DV_{DD} to reach a valid operating voltage.

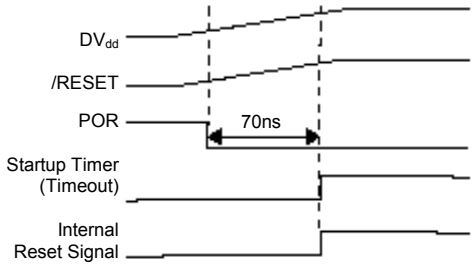

Figure 5. DV_{DD} Rise Time Exceeds Tstartup

Figure 6 shows the recommended external reset circuit. The external reset circuit is required only if the DV_{DD} rise time has the possibility of being too slow (refer to Table 11 on page 23).

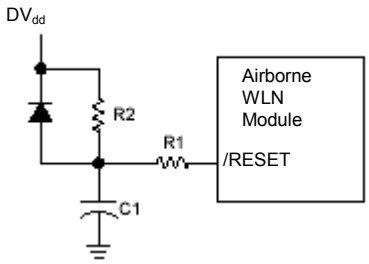

Figure 6. External Reset Circuit

In Figure 6:

- The diode D discharges the capacitor when DV_{DD} is powered down.
- R1 = 100 Ω to 1K Ω limits any current flowing into /RESET from external capacitor C1. This protects the /RESET pin from breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).
- R2 < 40K Ω is recommended to ensure that voltage drop across R2 leaves the /RESET pin above a V_{IHGP} level.

Choose C1 to have R2 ∞ C1 exceed five times the time period required for DV_{DD} to reach a valid operating voltage. V_{DD} must start rising from V_{ss} to ensure proper Power-On-Reset when relying on the internal Power-On-Reset circuitry. If power supply takes more than 50 ms to rise from 0 to 2.5 V, use RCs on /RESET pin (see Figure 6).

2.8 AIRBORNE WLN MODULE OPERATION

2.8.1 Power-up

When the Module powers-up, it performs a Power On Self Test (POST). The POST procedure checks that RAM, Flash memory, real-time clock, and radio are operating as expected. If the Module passes the POST, the POST line is set high (POST). Any failures cause the Module to reset.

2.8.2 Factory Restart

The Module provides a factory-restart function that returns the Module to its original factory default settings. There are three ways to activate this feature:

- Use the **Reset** page in the Web interface (see page **Error! Bookmark not defined.**).
- Use the CLI command `reset` (see page **Error! Bookmark not defined.**).
- Hold Port G3 low during Module startup.

To ensure proper operation, a resistor (4.7 K Ω to 47 K Ω) should be used to pull up Port G3 to +2.5 V (use the Module's 2.5 V reference). This signal can be pulled low using either a push-button switch to GND or an open-drain output signal from the Host. For proper factory-reset operation, Port G3 must be held low for 100 ms before /RESET goes high and kept low until 750 ms after /RESET goes high.

Caution: Port G3 must be tied high to no more than 2.5 V. Higher voltages may cause latch-up or damage to the application processor.

2.9 DESIGN GUIDELINES

2.9.1 General Design Guidelines

The Module is designed to be implemented into a variety of applications. Any design must meet the following guidelines:

- Provide 3.3 V to all DV_{dd} power pins.
- Provide ground connections to all V_{ss} pins.
- Tie port G3 to the Module's 2.5 V V_{ref} through a 10 KΩ resistor to prevent the Module from resetting itself to factory defaults at startup.
- Tie all unused I/O to ground via 10 KΩ resistors. If the state of the I/O can be controlled, set all unused I/O as outputs.
- Do not exceed 2.5 V on any port G pins configured as analog inputs.
- Provide a connection to a suitable antenna.
- TSI, TSS, TSO, TSCK, and RFU should be left as No Connects (they are pulled up internally).
- Carefully follow the Hirose DF12 connector placement, mounting, and precautions for use to avoid shorts due to an incorrect soldering profile.

2.9.2 SPI Design Guidelines

The Module with the SPI interface is designed to be implemented into a variety of applications. Any design must meet the following guidelines:

- Data transfer from master to slave is carried out across the MOSI (Master-Out/Slave-In) line.
- Data transfer from slave to master is carried out across the MISO (Master-In/Slave-Out) line.
- All data transfers are synchronized by the Master's serial clock (SCK). One bit of data is transferred every clock pulse, and one octet can be exchanged in eight (8) clock cycles.
- Communication is enabled when the /SS (Slave Select) line is pulled low.
- An Interrupt Master (INT) line is used by the Slave to signal the Master that data is available.

- This protocol is completely octet (8 bits) aligned. Octets used for commands and returned status are in Intel ("little-endian") format.
- A frame is defined as those octets that are bounded by the Slave Select assertion (from the time /SS goes low, until it returns high). SPI requires that commands be framed, so a frame can be of varying sizes, especially for the read and write command sequences. This puts a timing strain on the system to quickly deal with the data. With the SCK running at 2MHz, the system has 4 microseconds to deal with an octet transferred (read or write) between the driver and the buffer.
- If a frame is prematurely terminated (before the octet count is completed), the driver must ensure that the data is properly accounted for and the pointers managed with the actual number of octets transferred, not the number of initially defined.
- The Configuration Status must be available to be shifted out of the MISO port at the beginning of each command, requiring its update immediately at the end of a frame to be prepared for the next frame.
- A pre-defined data frame has to be agreed upon by both the master and slave for the exchange of data. The data frame is described by two parameters, the clock polarity and the clock phase. These parameters have four possible states that correspond to four SPI Modes.

Table 9. SPI Modes

SPI Mode	Clock Polarity (CPOL)	Clock Phase (CPHA)	Clock (SCK) Idle Low: Output on rising, sample on falling High: Output on falling, sample on rising	Output Sample Edge	Input Sample Edge
0	0	0	Low	Falling	Rising
*1	0	1	Low	Rising	Falling
2	1	0	High	Rising	Falling
3	1	1	High	Falling	Rising

- ***The WLN SPI Slave shall run in Mode 1 ***only***.
- The Slave's MOSI needs to be setup by the Master on the first-edge (rising if Idle = Low, falling if Idle = High) following the assertion of /SS. Therefore, the Slave will sample its MOSI on the second-edge (transition).
- The bit ordering of data coming into the SPI Slave is MSB-first for both transmit and receive.

2.9.3 WLN UART Connections

For embedded applications that will communicate with the serial UART interface, the following guidelines are also recommended:

- Connect HS.TXD (port F1) to the receive line of the embedded processor UART.
- Connect HS.RXD (port F7) to the transmit line of the embedded processor UART.
- Connect HS.RTS (port F4) and HS.CTS (port F5) if hardware handshaking is desired.

- Connect the CONNECT status line (port F6) to a digital input on the embedded processor. This line indicates whether a TCP connection is active.
- Connection to the other status lines — POST, RF LINK, WLAN CFG LINK — is optional.
- If HS.RTS and HS.CTS (Ports F4 and F5) are not used, tie them to ground via 10 kΩ resistors.

2.9.4 WLN SPI Connections

- Connect the application's MOSI line to port F7 of the WLN to transfer data from the Master.
- Connect the application's MISO line to port F1 of the WLN to receive data from the Slave.
- Connect the application's SCK line to port F4 of the WLN to send the Master's serial clock.
- Connect the application's /SS line to port F5 of the WLN to select the WLN Module.
- Connection the application's INT line to port G0 of the WLN to receive interrupts from the Slave. This indicates that data is available on the WLN.

Caution: If the Module is connected to a circuit that is powered on while the Module is powered off, the design should ensure that no logic highs are present on the connections while the Module is powered off. Otherwise, the Module can be damaged beyond repair. If the state of the connections cannot be controlled, insert a tri-state buffer between the Module and its Host. For additional information, see Appendix B, Power Control.

Caution: The 3.3 V power supply should be a low-noise design, with less than 150 mV ripple at the maximum average transmit current. The power supply should also be designed to provide sufficient power to handle the Module's power-up inrush current. For additional information, see Appendix B, Power Control.

2.10 PACKAGE CONFIGURATION

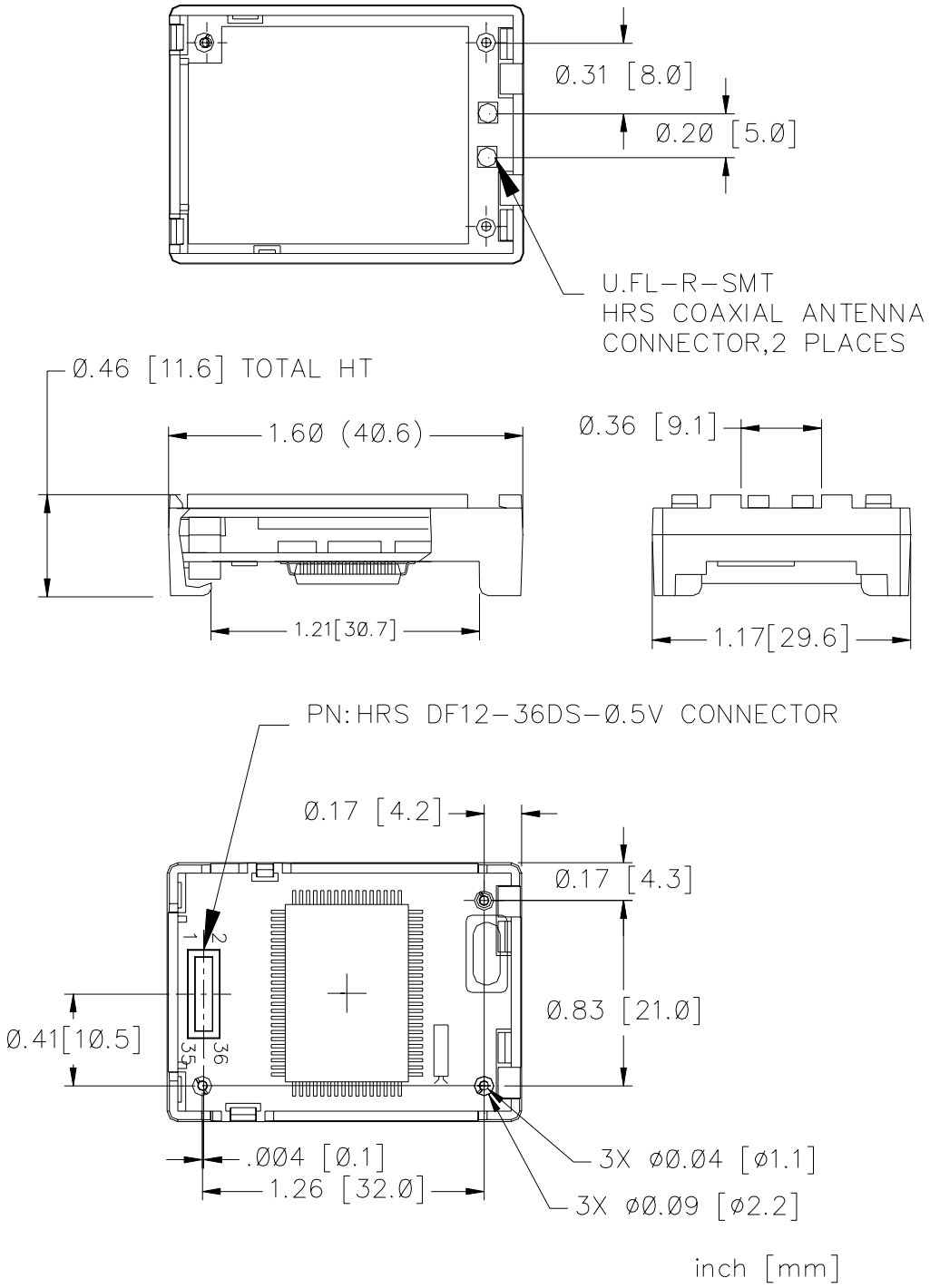

Figure 7. Mechanical Dimensions (Airborne WLN Module)

2.11 ELECTRICAL CHARACTERISTICS

2.11.1 Absolute Maximum Ratings

Table 10 shows the absolute maximum ratings for supply voltage and voltages on the Module's digital and analog pins. Exceeding these values will permanently damage the Module.

Table 10. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Peak instantaneous operating current		480	mA
Startup inrush current		1900	mA
Voltage at GPIO pins	-0.3	5.7	V
Voltage at Analog pins	-0.3	3.5	V
Voltage at V_{DD} pin	0	7	V
Operating temperature	-40	+85	°C
Storage temperature	-40	+100	°C

2.11.2 Electrical Characteristics

Table 11. Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage (3.3 V ±5%)	3.135	3.3	3.465	V
I_{DDTX}	Transmit Mode Current		400	480	mA
I_{DDRX}	Receive Mode Current		300	380	mA
$I_{DDSNOOZE}$	Snooze Mode Current (WLN UART only)		275	300	mA
$I_{IDDDOZE}$	Doze Mode Current (WLN UART only)		235	280	mA
$I_{DDSLEEP}$	Sleep Mode Current (WLN UART only)		50	80	mA
V_{IHGP}	GPIO Input High voltage	1.8		5.5	V
V_{ILGP}	GPIO Input Low voltage			1.0	V
V_{OHGP}	GPIO Output High voltage	2.4		V_{DD}	V
V_{OLGP}	GPIO Output Low voltage			0.4	V
I_{OHGP}	GPIO Output High Current Port E5 and Port E6 only			24 60	mA
I_{OLGP}	GPIO Output Low Current Port E5 and Port E6 only			16 40	mA
V_{IHAn}	Analog Input High voltage	1.8		$V_{2.5}$	V
V_{ILAN}	Analog Input Low voltage			1.0	V
V_{OHAn}	Analog Output High voltage	2.4		$V_{2.5}$	V
V_{OLAn}	Analog Output Low voltage			0.4	V
I_{OHAn}	Analog Output High Current			6	mA
I_{OLAn}	Analog Output Low Current			6	mA
$V_{2.5}$	Internal 2.5 V monitor and Reference	2.37	2.5	2.75	V
$I_{V2.5}$	Reference 2.5 V output current			25	mA
SV_{DD}	DV_{DD} slew rate to ensure Power-On Reset	0.05			V/ms

2.11.3 AC Electrical Characteristics – Receiver

Table 12. RF Performance Receive Sensitivity

Data Rate	Sensitivity
11.0 Mb/s	-82 dBm
5.5 Mb/s	-86 dBm
2.0 Mb/s	-88 dBm
1.0 Mb/s	-90 dBm

2.11.4 AC Electrical Characteristics – Transmitter

Transmit power is managed by the Module automatically. The maximum transmit output power is typically +15 dBm.

2.11.5 Performance/Range

Table 13 shows the typical data rates, performance, and range the Module can provide with an omnidirectional antenna.

Table 13. Performance/Range*

Wireless Data Rate	Indoor Distance	Outdoor Distance (Max)
11.0 Mb/s	30 – 100 m	300 m
5.5 Mb/s	32 – 107 m	330 m
2.0 Mb/s	35 – 115 m	375 m
1.0 Mb/s	40 – 130 m	400 m

* Ranges are based on signal-to-noise ratio and performance estimates.

Note:

- Wireless Data Rate is the raw rate provided over the wireless link and does not represent the throughput data rate of the Module.
- Indoor Distance is “Office Environment.”
- Outdoor Distance is “Open Field.”

CHAPTER 3
RECOMMENDED LAYOUT PRACTICES

3.1 OVERVIEW

This chapter contains recommended layout practices. Topics covered in this chapter include:

- 3.2 Module Mounting Guidelines (below)
- 3.3 Circuit Board Layout Practices (below)
- 3.4 EMI/RFI Guidelines (page 26)

3.2 MODULE MOUNTING GUIDELINES

Special care must be observed when placing the Airborne WLN Module. In particular:

- The antenna must not be mounted below any other printed circuit boards, components, or metallic housing.
- The proximity of the antenna to large metallic objects can affect the Module's range and performance.
- Packaging and enclosure designers must carefully review the placement of the Module in the enclosure and the placement of the antenna to minimize interference or blocking sources.
- For mechanical clearance, performance, and emissions reasons, there should be no components placed on the main printed circuit board facing the Module. This region should be clear of components, as indicated by the clear area in Figure 8 on the next page.

3.3 CIRCUIT BOARD LAYOUT PRACTICES

When considering capacitance, calculations must take into account all device loads and capacitances due to printed circuit board traces. Capacitance due to the traces depends on a number of factors, including the trace width, dielectric material from which the circuit board is made, and proximity to ground and power planes.

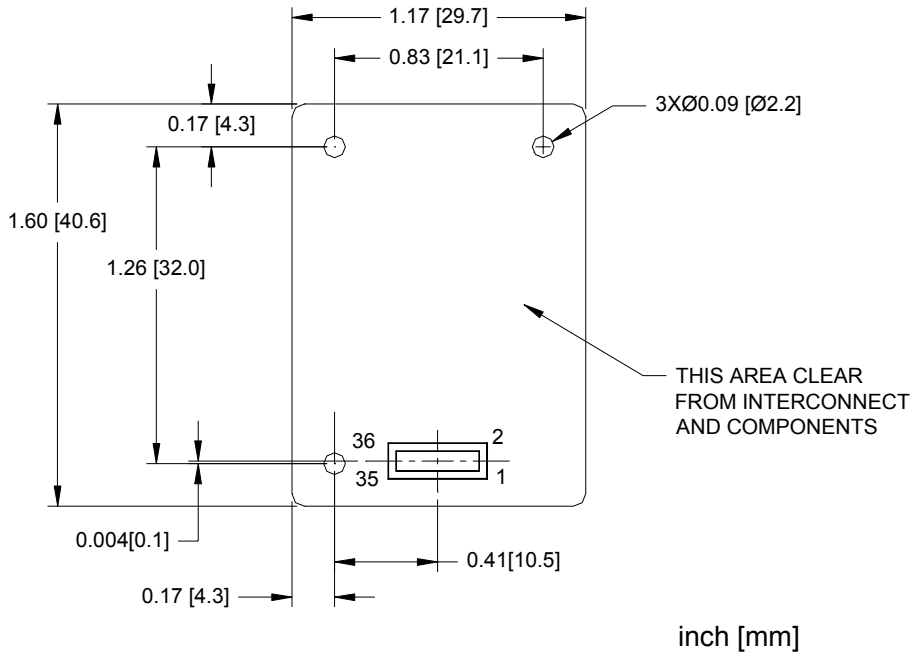

Figure 8. Guidelines for Mounting the Airborne WLN Module

3.4 EMI / RFI GUIDELINES

To minimize electromagnetic interference (EMI) and radio-frequency interference (RFI), pay strict attention to power and signal routing near the Module. As much as possible, the keep-clear area below the Module should be a solid copper ground plane. It is anticipated that the Module will be mounted on a board with a committed ground plane. Ensure that the interconnect has a designed impedance of 50-75 Ohms.

To keep signal impedance as low as possible, connect the ground plane to internal ground planes by several vias. Ground signals to the Module connector should connect directly to the ground plane below the Module. Individual ground connections to the Module should have a solid ground connection, preferably directly to the ground plane on the same surface side where the Module resides. Do not connect ground pins directly to an inside layer ground plane using vias.

Keep interconnects from the Module connector as short as possible on the mounting layer. All inboard signals must immediately transition to a different routing layer using a via as close to the connector as possible. Outboard signals (odd pin numbers) should also be kept to a minimum length.

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