# SPSGRFC

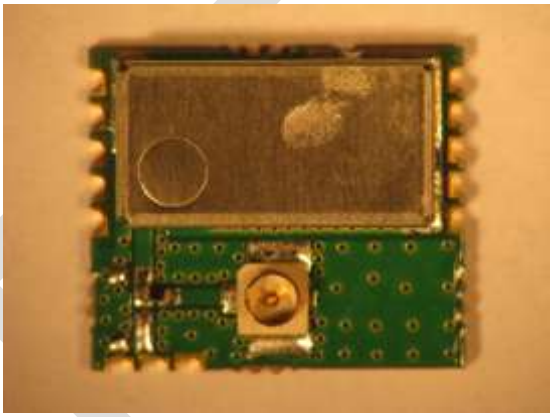
Sub1GHz (433 or 868 or 915 MHz) programmable transceiver module

Preliminary Datasheet

## Features

### Programmable Radio features

- Modulation schemes: 2-FSK, GFSK, MSK, GMSK, OOk, ASK
- Air data rate from 1 to 500 kbps
- On board UFL connector for external antenna
- Operating temperature range from -40 °C to 85°C



Preliminary module picture
11.5 mm x 13.5 mm x 2.0 mm

### RF features

- Receiver sensitivity: -118 dBm
- Programmable RF output power up to +16 dBm

### Host Interface

- SPI

### General I/O

- Up to 32 programmable I/O functions on 4 GPIO programmable module pins

### Three Carrier Frequency versions

- 433 MHz for externally tuned antenna
- 868 MHz for externally tuned antenna
- 915 MHz for externally tuned antenna

# 1 Description

The SPSGRFC is an easy to use Sub1GHz transceiver module, with many programmable features. The module provides a complete RF platform in a tiny form factor.

The SPSGRFC enables electronic devices with wireless connectivity, not requiring any RF experience or expertise for integration into the final product. The SPSGRFC, being a certified solution, optimizes the time to market of the final applications.

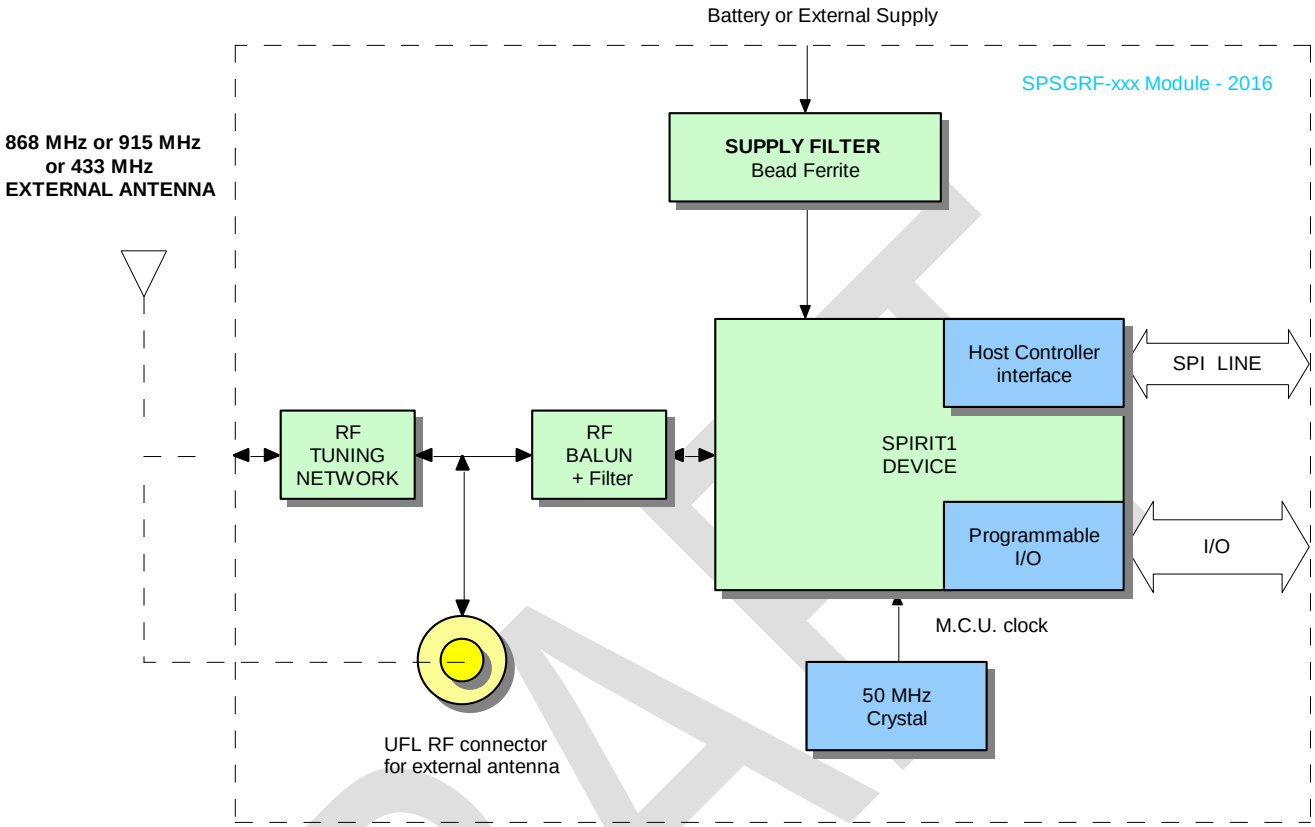
The module is designed for maximum performance in a minimal space including 4 programmable I/O pin and SPI serial interface.

# 2 Applications

- AMR (automatic meter reading)
- Home and building automation
- WSN (wireless sensors network)
- Industrial monitoring and control
- Wireless fire and security alarm systems
- Point-to-point wireless link

# 3 Block Diagram

**Figure 1 – Block Diagram**



# 4 Short description of the module functional behaviour

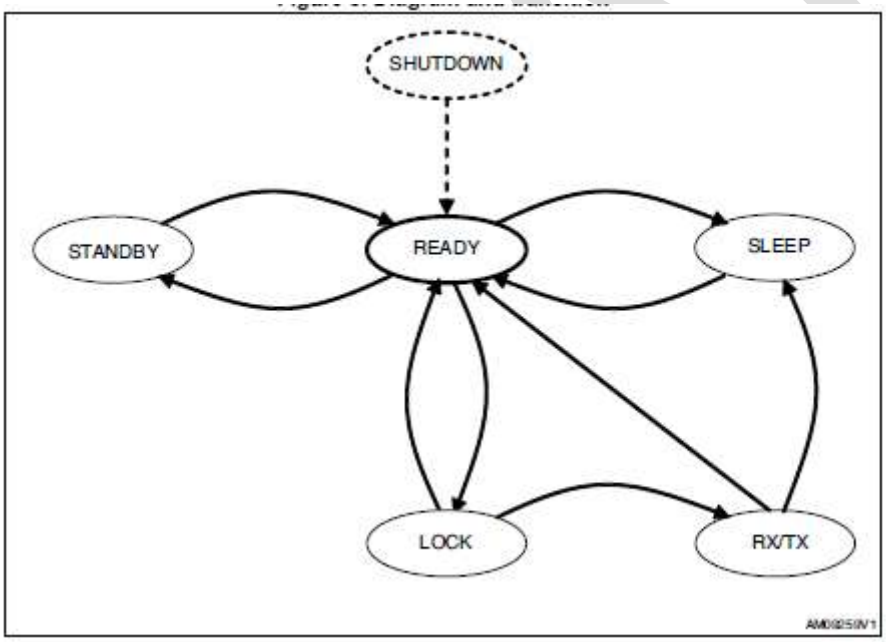
The SPIRIT1 device inside the SPSGRFC module is provided with a built-in main controller which controls the switching between the two main operating modes: transmit (TX) and receive (RX).
In shutdown condition the SPSGRFC module can be switched on/off with the external pin SDN, all other functions/registers/commands are available through the SPI interface and GPIOs. No internal supply is generated (in order to have minimum battery leakage), and hence, all stored data and configurations are lost.

The GPIO and SPI ports of the module during SHUTDOWN are in HiZ. From shutdown state, the SPSGRFC module can be switched on from the SDN pin and goes into READY state, which is the default, where the reference signal from XO is available.

From READY state, the SPSGRFC module can be moved to LOCK state to generate the high precision LO signal and/or TX or RX modes. Switching from RX to TX and vice versa can happen only by passing through the LOCK state. This operation is normally managed by radio control with a single user command (TX or RX).

At the end of the operations above, the SPSGRFC module can return to its default state (READY) and can then be put into a sleeping condition (SLEEP state), having very low power consumption.
If no timeout is required, the SPSGRFC module can be moved from READY to STANDBY state, which has the lowest possible current consumption while retaining FIFO, status and configuration registers. To manage the transitions towards and between these operating modes, the controller works as a state machine, whose state switching is driven by SPI commands.

**Figure 2 - Module functional states transitions diagram**



# 5 Hardware Specifications

General Conditions ($V_{IN}$= 3.3V and 25°C)

## 5.1 Absolute Maximum Ratings

Table 1 - Absolute Maximum Ratings

| Rating | Min | Typical | Max | Unit |
|---|---|---|---|---|
| Storage temperature range | -40 | - | +85 | °C |
| Supply voltage, $V_{IN}$ | -0.3 | - | + 3.9 | Volts |
| I/O pin Voltage | -0.3 | - | + 3.9 | Volts |
| RF saturation input power | - | 10 | - | dBm |

## 5.2 Recommended Operating Conditions

Table 2 - Recommended Operating Conditions

| Rating | Min | Typical | Max | Unit |
|---|---|---|---|---|
| Operating Temperature Range | -40 | - | 85 | °C |
| Supply Voltage $V_{IN}$ | 1.8 | 3.3 | 3.6 | Volts |
| Signals & I/O Pin Voltage (according Supply Voltage) | 1.8 | - | 3.6 | Volts |
| RF Frequency Bandwidth (SPSGRFC-433) | 433.050 | | 434.790 | MHz |
| RF Frequency Bandwidth (SPSGRFC-868) | 863 | | 870 | MHz |
| RF Frequency Bandwidth (SPSGRFC-915) | 902 | | 928 | MHz |

## 5.3 Module current consumption

Table 3 – SPSGRFC-433 module current consumption

| Symbol | Parameter | Test conditions | Max | Unit |
|---|---|---|---|---|
| Idd | Supply current | Operating mode Tx, +11.6 dBm, 2-FSK, 433 MHz | 22 | mA |
| | | Operating mode Tx, -7 dBm, 2-FSK, 433 MHz | 9 | mA |
| | | Operating mode Rx, 433 MHz | 10 | mA |
| | | Command mode | 0.6 | mA |
| | | Shutdown high level Vdd With other I/O in High impedance | 0.1 | µA |

Table 4 – SPSGRFC-868 module current consumption

| Symbol | Parameter | Test conditions | Max | Unit |
|---|---|---|---|---|
| Idd | Supply current | Operating mode Tx, +11.6 dBm, 2-FSK, 868 MHz | 22 | mA |
| | | Operating mode Tx, -7 dBm, 2-FSK, 868 MHz | 9 | mA |
| | | Operating mode Rx, 868 MHz | 10 | mA |
| | | Command mode | 0.6 | mA |
| | | Shutdown high level Vdd With other I/O in High impedance | 0.1 | µA |

Table 5 – SPSGRFC-915 module current consumption

| Symbol | Parameter | Test conditions | Max | Unit |
|---|---|---|---|---|
| Idd | Supply current | Operating mode Tx, +11.6 dBm, 2-FSK, 915 MHz | 22 | mA |
| | | Operating mode Tx, -7 dBm, 2-FSK, 915 MHz | 9 | mA |
| | | Operating mode Rx, 915 MHz | 10 | mA |
| | | Command mode | 0.6 | mA |
| | | Shutdown high level Vdd With other I/O in High impedance | 0.1 | µA |

## 5.4 Pin Assignement

**Figure 3 – Pin connection diagram**

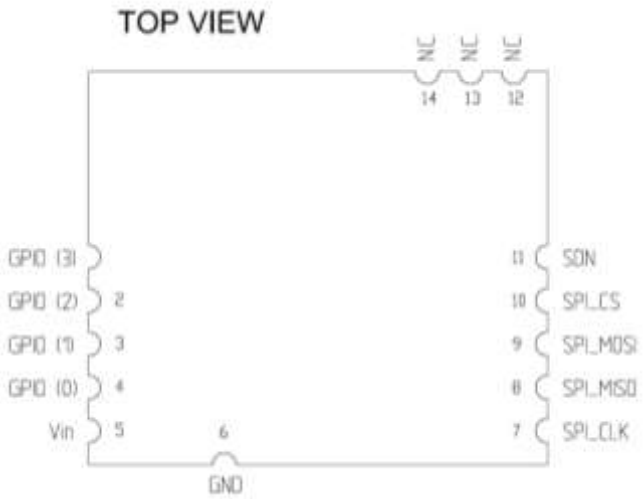



**Table 6 – Pin Assignment**

| Name | Type | Pin # | Description | ALT Function | V max. Tolerant | Initial State |
|---|---|---|---|---|---|---|
| **SPI Interface** | | | | | | |
| SPI_CLK | I | 7 | SPI CLOCK (Max. 8 MHz) | | $V_{in}$ | |
| SPI_MISO | O | 8 | SPI MISO (MASTER in / SLAVE out) | | $V_{in}$ | |
| SPI_MOSI | I | 9 | SPI MOSI (MASTER out SLAVE in) | | $V_{in}$ | |
| SPI_CS | I | 10 | SPI “Chip Select” (SPI slave select) | | $V_{in}$ | |
| **Power and Ground** | | | | | | |
| $V_{in}$ | | 5 | $V_{in}$ | | (1.8V + 3.6V max.) | |
| GND | | 6 | GND | | | |
| **Module SHUTDOWN** | | | | | | |
| SDN | I | 11 | SHUTDOWN input (active high) | | (1.8V + 3.6V max.). | |
| **GPIO – General Purpose Input/Output** | | | | | | |
| GPIO [0] | I/O | 4 | Programmable Input / Output & Analog Temperature output | | (1.8V + $V_{in}$ max.). | Digital Output. Low Power |
| GPIO [1] | I/O | 3 | Programmable Input / Output | | (1.8V + $V_{in}$ max.). | Digital Output. Low Power |
| GPIO [2] | I/O | 2 | Programmable Input / Output | | (1.8V + $V_{in}$ max.). | Digital Output. Low Power |
| GPIO [3] | I/O | 1 | Programmable Input / Output | | (1.8V + $V_{in}$ max.). | Digital Output. Low Power |
| **Optional External Antenna connections** (Not available on the standard SPSGRFC-xxx modules) | | | | | | |
| N.C. | N.C | 12 | Not connected | | | |
| N.C. | N.C. | 13 | Not connected | | | |
| N.C. | N.C. | 14 | Not connected | | | |

# 6 Mechanical dimensions

**Figure 4 – Mechanical Dimensions**

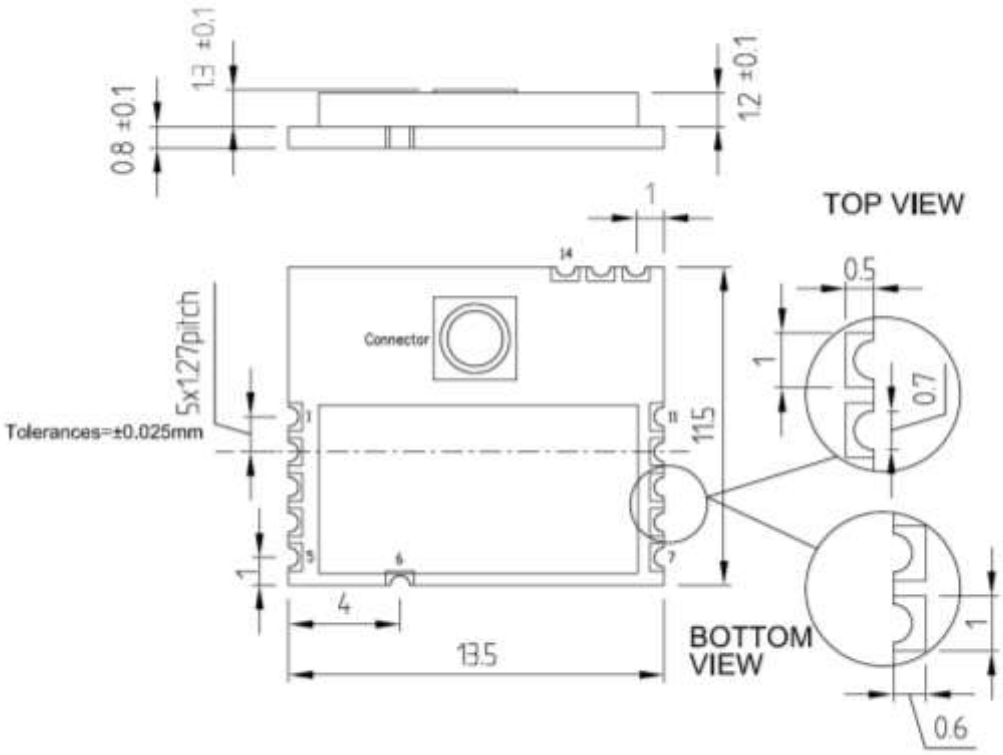
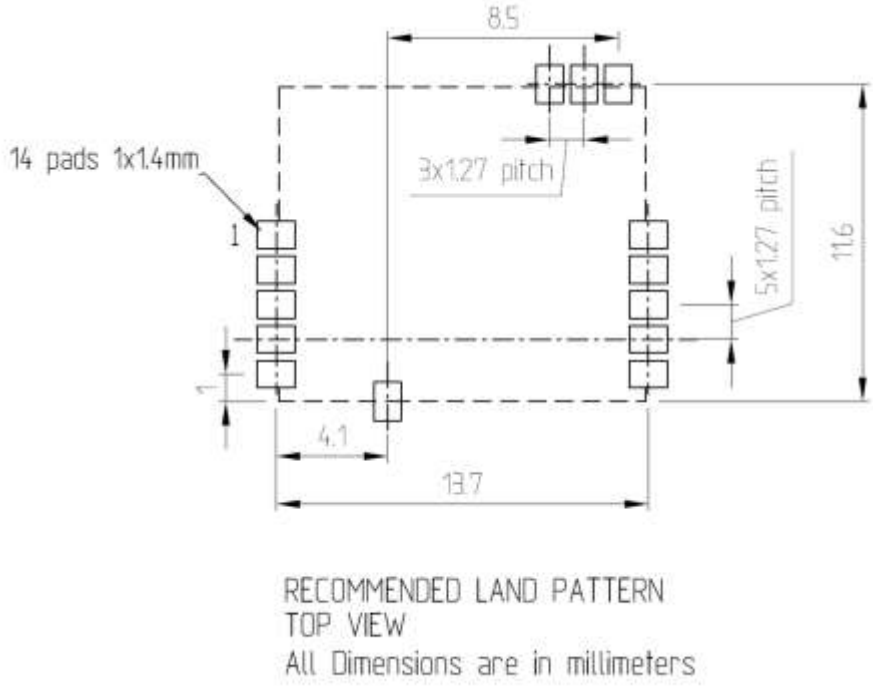



Figure 5 – Recommend land pattern



# 7 Hardware *design*

SPSGRFC module supports SPI hardware interfaces.

Notes

- All unused pins should be left floating; do not ground.
- All GND pins must be well grounded.
- The area around the module should be free of any ground planes, power planes, trace routings, or metal for 6 mm from the module antenna position, in all directions.
- Traces should not be routed underneath the module.

## *7.1* Modules RF compliance limits

The RF compliance limits are those tested for FCC, IC and CE certification using the dedicated dongle (PC92A.V01). These limits are enforced by the dongle firmware. Care must be taken with custom application firmware to ensure these limits are not exceeded, voiding the FCC, IC and CE certification.

**Table 7. RF compliance limits table**

| Modulation | Standards | Parameter | Max. | Unit |
|---|---|---|---|---|
| 2-FSK<br>GFSK<br>MSK | FCC Part 15.207 (1)<br>FCC Part 15.247 (1)<br>IC RSS-210 (1)<br>EN 300 220-2 V2.4.1<br>EN301 489-01 V1.9.2<br>EN301 489-03 V1.4.1 | Data Rate | 500 | kbps |
| | | Output power | +11.6 | dBm |
| OOK<br>ASK | FCC Part 15.207 (1)<br>FCC Part 15.247 (1)<br>IC RSS-210 (1) | Data Rate | 250 | kbps |
| | | Output power | +4 | dBm |

(1) FCC and IC standards are applicable only to the SPSGRFC-915 module.

# 8 Module user firmware short description

**For more user firmware information, please refer to the SPIRIT1 Datasheet - October 2016 DocID022758 Rev 10.**
**Downloadable at the following link:** *www.st.com/resource/en/datasheet/**bluenrg-1**.pdf*

The following are short firmware notes, useful to furnish to the user a condensed view of the many programming ways of the SPSGRFC-xxx module. (The following “Register table” refers the SPIRIT1 datasheet, so the table numbers and the links into the table are referred to the same document).

# Register table

This section describes all the registers used to configure the SPIRIT1 device, assembled into the module. The description is structured in sections according to the register usage.

SPIRIT1 has three types of registers:

- Read and write (R/W), which can be completely managed by SPI using READ and WRITE operations
- Read-only (R)
- Read-and-reset (RR), is automatically cleared after a READ operation.

A further category of special registers collects the ones which cannot be categorized in any of the three mentioned above R/W, R, or RR.

The fields named as “Reserved” must not be overridden by the user, otherwise, behavior is not guaranteed.

The memory map is shown in the following table:

**Table 41. General configuration registers**

| Register | Address | Bit | Field name | Reset | R/W | Description |
|---|---|---|---|---|---|---|
| ANA_FUNC_CONF[1] | 0x00 | 7:5 | Reserved | 000 | R/W | |
| | | 4:2 | GM_CONF[2:0] | 011 | | Sets the driver gm of the XO at startup |
| | | 1:0 | SET_BLD_LVL[1:0] | 00 | | Sets the BLD threshold<br>00: 2.7 V<br>01: 2.5 V<br>10: 2.3 V<br>11: 2.1 V |

**Table 41. General configuration registers (continued)**

| Register | Address | Bit | Field name | Reset | R/W | Description |
|---|---|---|---|---|---|---|
| ANA_FUNC_CONF[0] | 0x01 | 7 | Reserved | 1 | R/W | |
| | | 6 | 24_26MHz_SELECT | 1 | | 1: 26 MHz configuration<br>0: 24 MHz configuration<br>(impact only RCO calibration reference and loop filter tuning) |
| | | 5 | AES_ON | 0 | | 1: AES engine enabled |
| | | 4 | EXT_REF | 0 | | 0: reference signal from XO circuit<br>1: reference signal from XIN pin |
| | | 3 | Reserved | 0 | | |
| | | 2 | BROWN_OUT | 0 | | 1: enables accurate brownout detection |
| | | 1 | BATTERY_LEVEL | 0 | | 1: enables battery level detector circuit |
| | | 0 | TS | 0 | | 1: enables the “temperature sensor” function |
| GPIO3_CONF | 0x02 | 7:3 | GPIO_SELECT[4:0] | 10100 | R/W | GPIO3 configuration (default: digital GND) |
| | | 2 | Reserved | 0 | | |
| | | 1:0 | GPIO_MODE[1:0] | 10 | | GPIO3 mode:<br>01b: digital input<br>10b: digital output low power<br>11b: digital output high power<br>(default: digital output low power) |
| GPIO2_CONF | 0x03 | 7:3 | GPIO_SELECT[4:0] | 10100 | R/W | GPIO2 configuration (default: digital GND) |
| | | 2 | Reserved | 0 | | |
| | | 1:0 | GPIO_MODE | 10 | | GPIO2 mode:<br>01b: digital input<br>10b: digital output low power<br>11b: digital output high power<br>(default: digital output low power) |

Table 41. General configuration registers (continued)

| Register | Address | Bit | Field name | Reset | R/W | Description |
|---|---|---|---|---|---|---|
| GPIO1_CONF | 0x04 | 7:3 | GPIO_SELECT[4:0] | 10100 | R/W | GPIO1 configuration (default: digital GND) |
| | | 2 | Reserved | 0 | | |
| | | 1:0 | GPIO_MODE | 10 | | GPIO1 mode:<br>01b: digital input<br>10b: digital output low power<br>11b: digital output high power<br>(default: digital output low power) |
| GPIO0_CONF | 0x05 | 7:3 | GPIO_SELECT[4:0] | 00001 | R/W | GPIO0 configuration (default: power-on reset signal) |
| | | 2 | Reserved | 0 | | |
| | | 1:0 | GPIO_MODE | 10 | | GPIO0 mode:<br>00b: analog<br>01b: digital input<br>10b: digital output low power<br>11b: digital output high power<br>(default: digital output low power) |
| MCU_CK_CONF | 0x06 | 7 | EN_MCU_CLK | 0 | R/W | 1: The internal divider logic is running, so the MCU clock is available (but proper GPIO configuration is needed) |
| | | 6:5 | CLOCK_TAIL[1:0] | 0 | | Number of extra clock cycles provided to the MCU before switching to STANDBY state:<br>00: 0 extra clock cycle<br>01: 64 extra clock cycles<br>10: 256 extra clock cycles<br>11: 512 extra clock cycles |
| | | 4:1 | XO_RATIO[3:0] | 0 | | Divider for the XO clock output |
| | | 0 | RCO_RATIO | 0 | | Divider for the RCO clock output<br>0: 1<br>1: 1/128 |
| XO_RCO_TEST | 0xB4 | 7:4 | Reserved | 0010 | | |
| | | 3 | PD_CLKDIV | 0 | | 1: disable both dividers of the digital clock (and reference clock for the SMPS) and IF-ADC clock. |
| | | 2:0 | Reserved | 001 | | |

**Table 41. General configuration registers (continued)**

| Register | Address | Bit | Field name | Reset | R/W | Description |
|---|---|---|---|---|---|---|
| SYNTH_CONFIG[0] | 0x9F | 7 | SEL_TSPLIT | 0 | R/W | 0: split time: 1.75 ns<br>1: split time: 3.47 ns |
| | | 6:0 | Reserved | 0100000 | | |
| SYNTH_CONFIG[1] | 0x9E | 7 | REFDIV | 0 | R/W | Enable division by 2 on the reference clock:<br>0: $f_{REF} = f_{XO}$ frequency<br>1: $f_{REF} = f_{XO}$ frequency / 2 |
| | | 6:3 | Reserved | 1011 | | |
| | | 2 | VCO_L_SEL | 0 | | 1: enable VCO_L |
| | | 1 | VCO_H_SEL | 1 | | 1: enable VCO_H |
| | | 0 | Reserved | 1 | | |
| IF_OFFSET_ANA | 0x07 | 7:0 | IF_OFFSET_ANA | 0xA3 | R/W | Intermediate frequency setting for the analog RF synthesizer. (see *Section 9.4*) |

**Table 42. Radio configuration registers (analog blocks)**

| Register name | Address | Bit | Field Name | Reset | R/W | Description |
|---|---|---|---|---|---|---|
| SYNT3 | 0x08 | 7:5 | WCP[2:0] | 000 | R/W | Set the charge pump current according to the VCO frequency. See *Table 26*. |
| | | 4:0 | SYNT[25:21] | 01100 | | SYNT[25:21], highest 5 bits of the PLL programmable divider The valid range depends on $f_{XO}$ and REFDIV settings; for $f_{XO}$=26MHz. See *Equation 3* |
| SYNT2 | 0x09 | 7:0 | SYNT[20:13] | 0x84 | R/W | SYNT[20:13], intermediate bits of the PLL programmable divider. See *Equation 3* |
| SYNT1 | 0x0A | 7:0 | SYNT[12:5] | 0xEC | R/W | SYNT[12:5], intermediate bits of the PLL programmable divider. See *Equation 3* |

**Table 42. Radio configuration registers (analog blocks) (continued)**

| Register name | Address | Bit | Field Name | Reset | R/W | Description |
|---|---|---|---|---|---|---|
| SYNT0 | 0x0B | 7:3 | SYNT[4:0] | 01010 | R/W | SYNT[4:0], lowest bits of the PLL programmable divider. See *Equation 3* |
| | | 2:0 | BS | 001 | R/W | Synthesizer band select. This parameter selects the out-of-loop divide factor of the synthesizer (B in *Equation 3* ).<br>1: 6 Band select factor for high band<br>3: 12 Band select factor for middle band<br>4: 16 Band select factor for low band<br>5: 32 Band select factor for very low band |
| CHSPACE | 0x0C | 7:0 | CH_SPACING | 0xFC | R/W | Channel spacing in steps of $f_{XO}/2^{15}$ (~793 for $f_{XO}$ = 26 MHz, ~732 for $f_{XO}$ = 24 MHz). |
| IF_OFFSET_DIG | 0x0D | 7:0 | IF_OFFSET_DIG | 0xA3 | R/W | Intermediate frequency setting for the digital shift-to-baseband (see *Section 9.4*) |
| FC_OFFSET[1] | 0x0E | 7:4 | Reserved | 0 | R/W | Carrier offset in steps of $f_{XO}/2^{18}$ and represented as 12 bits 2-complement integer. It is added / subtracted to the carrier frequency set by the SYNTx register. This register can be used to set a fixed correction value obtained e.g. from crystal measurements. |
| | | 3:0 | FC_OFFSET[11:8] | 0 | | |
| FC_OFFSET[0] | 0x0F | 7:0 | FC_OFFSET[7:0] | 0 | R/W | |
| PA_POWER[8] | 0x10 | 7 | Reserved | 0 | R/W | Output power level for 8th slot (+12 dBm) |
| | | 6:0 | PA_LEVEL_7 | 0000011 | | |
| PA_POWER[7] | 0x11 | 7 | Reserved | 0 | R/W | Output power level for 7th slot (+6 dBm) |
| | | 6:0 | PA_LEVEL_6 | 0001110 | | |
| PA_POWER[6] | 0x12 | 7 | Reserved | 0 | R/W | Output power level for 6th slot (0 dBm) |
| | | 6:0 | PA_LEVEL_5 | 0011010 | | |
| PA_POWER[5] | 0x13 | 7 | Reserved | 0 | R/W | Output power level for 5th slot (-6 dBm) |
| | | 6:0 | PA_LEVEL_4 | 0100101 | | |
| PA_POWER[4] | 0x14 | 7 | Reserved | 0 | R/W | Output power level for 4th slot (-12 dBm) |
| | | 6:0 | PA_LEVEL_3 | 0110101 | | |

**Table 42. Radio configuration registers (analog blocks) (continued)**

| Register name | Address | Bit | Field Name | Reset | R/W | Description |
|---|---|---|---|---|---|---|
| PA_POWER[3] | 0x15 | 7 | Reserved | 0 | R/W | Output power level for 3rd slot (-18 dBm) |
| | | 6:0 | PA_LEVEL_2 | 1000000 | | |
| PA_POWER[2] | 0x16 | 7 | Reserved | 0 | R/W | Output power level for 2nd slot (-24 dBm) |
| | | 6:0 | PA_LEVEL_1 | 1001110 | | |
| PA_POWER[1] | 0x17 | 7 | Reserved | 0 | R/W | Output power level for first slot (-30 dBm) |
| | | 6:0 | PA_LEVEL_0 | 0000000 | | |
| PA_POWER[0] | 0x18 | 7:6 | CWC[1:0] | 00 | R/W | Output stage additional load capacitors bank (to be used to optimize the PA for different sub-bands):<br>00: 0 pF<br>01: 1.2 pF<br>10: 2.4 pF<br>11: 3.6 pF |
| | | 5 | PA_RAMP_ENABLE | 0 | | 1: enable the power ramping |
| | | 4:3 | PA_RAMP_STEP_WIDTH[1:0] | 00 | | Step width (unit: 1/8 of bit period) |
| | | 2:0 | PA_LEVEL_MAX_INDEX | 111 | | Final level for power ramping or selected output power index. |

**Table 43. Radio configuration registers (digital blocks)**

| Register name | Address | Bit | Field Name | Reset | R/W | Description |
|---|---|---|---|---|---|---|
| MOD1 | 0x1A | 7:0 | DATARATE_M | 0x83 | R/W | The mantissa value of the data rate equation (see *Equation 11*) |
| MOD0 | 0x1B | 7 | CW | 0 | R/W | 1: enable the CW transmit mode |
| | | 6 | BT_SEL | 0 | | Select BT value for GFSK<br>0: BT = 1<br>1: BT = 0.5 |
| | | 5:4 | MOD_TYPE[1:0] | 01 | | Modulation type<br>0: 2-FSK<br>1: GFSK<br>2: ASK/OOK<br>3: MSK |
| | | 3:0 | DATARATE_E | 1010 | | The exponent value of the data rate equation (see *Equation 11*) |

**Table 43. Radio configuration registers (digital blocks) (continued)**

| Register name | Address | Bit | Field Name | Reset | R/W | Description |
|---|---|---|---|---|---|---|
| FDEV0 | 0x1C | 7:4 | FDEV_E[3:0] | 0100 | R/W | The exponent value of the frequency deviation equation (see *Equation 10*) |
| | | 3 | CLOCK_REC_ALGO_SEL | 0 | | Select PLL or DLL mode for symbol timing recovery |
| | | 2:0 | FDEV_M | 101 | | The mantissa value of the frequency deviation equation (see *Equation 10*) |
| CHFLT | 0x1D | 7:4 | CHFLT_M[3:0] | 0010 | R/W | The mantissa value of the channel filter according to *Table 32* |
| | | 3:0 | CHFLT_E | 0011 | | The exponent value of the channel filter according to *Table 32* |
| AFC2 | 0x1E | 7 | AFC_FREEZE_ON_SYNC | 0 | R/W | 1: enable the freeze AFC correction upon sync word detection |
| | | 6 | AFC_ENABLE | 1 | | 1: enable AFC(see *Section 8.8: AFC*) |
| | | 5 | AFC_MODE | 0 | | Select AFC mode:<br>0: AFC loop closed on slicer<br>1: AFC loop closed on second conversion stage |
| | | 4:0 | AFC_PD_LEAKAGE | 01000 | | Peak detector leakage |
| AFC1 | 0x1F | 7:0 | AFC_FAST_PERIOD | 0x18 | R/W | Length of the AFC fast period |
| AFC0 | 0x20 | 7:4 | AFC_FAST_GAIN_LOG2[3:0] | 0010 | R/W | AFC loop gain in fast mode (log2) |
| | | 3:0 | AFC_SLOW_GAIN_LOG2 | 0101 | | AFC loop gain in slow mode (log2) |
| RSSI_FLT | 0x21 | 7:4 | RSSI_FLT[3:0] | 1110 | R/W | Gain of the RSSI filter |
| | | 3:2 | CS_MODE | 00 | | Carrier sense mode (see *Section 9.10.2*) |
| | | 1:0 | OOK_PEAK_DECAY | 11 | | Peak decay control for OOK: 3 slow decay; 0 fast decay |
| RSSI_TH | 0x22 | 7:0 | RSSI_THRESHOLD | 0x24 | R/W | Signal detect threshold in 0.5 dB steps,<br>-120 dBm corresponds to 0x14.<br>(see *Section 9.10.1*) |

**Table 43. Radio configuration registers (digital blocks) (continued)**

| Register name | Address | Bit | Field Name | Reset | R/W | Description |
|---|---|---|---|---|---|---|
| CLOCKREC | 0x23 | 7:5 | CLK_REC_P_GAIN[2:0] | 2 | R/W | Clock recovery loop gain (log2) |
| | | 4 | PSTFLT_LEN | 1 | | Post-filter:<br>0: 8 symbols,<br>1: 16 symbols |
| | | 3:0 | CLK_REC_I_GAIN | 8 | | Integral gain for the clock recovery loop (used in PLL mode) |
| AGCCTRL2 | 0x24 | 7:4 | Reserved | 0010 | R/W | |
| | | 3:0 | MEAS_TIME | 0010 | | Measure time |
| AGCCTRL1 | 0x25 | 7:4 | THRESHOLD_HIGH[3:0] | 0110 | R/W | High threshold for the AGC |
| | | 3:0 | THRESHOLD_LOW | 0101 | | Low threshold for the AGC |
| AGCCTRL0 | 0x26 | 7 | AGC ENABLE | 1 | R/W | 1: enable AGC. |
| | | 6:0 | Reserved | 0001010 | | |
| ANT_SELECT_CONF | 0x27 | 7:5 | Reserved | 000 | R/W | |
| | | 4 | CS_BLANKING | 0 | | 1: do not fill the RX FIFO with the data received if the signal is below the CS threshold |
| | | 3 | AS_ENABLE | 0 | | 1: enable antenna switching |
| | | 2:0 | AS_MEAS_TIME | 101 | | Measurement time |

**Table 44. Packet/protocol configuration registers**

| Register name | Address | Bit | Field Name | Reset | R/W | Description |
|---|---|---|---|---|---|---|
| PCKTCTRL4 | 0x30 | 7:5 | Reserved | 000 | R/W | |
| | | 4:3 | ADDRESS_LEN[1:0] | 00 | | Length of address field in bytes:<br>0 or 1: Basic<br>2: STack |
| | | 2:0 | CONTROL_LEN | 000 | | Length of control field in bytes |

**Table 44. Packet/protocol configuration registers (continued)**

| Register name | Address | Bit | Field Name | Reset | R/W | Description |
|---|---|---|---|---|---|---|
| PCKTCTRL3 | 0x31 | 7:6 | PCKT_FRMT[1:0] | 00 | R/W | Format of packet.<br>0: basic,<br>2: WM-Bus,<br>3: STack<br>(see *Section 9.7*) |
| | | 5:4 | RX_MODE[1:0] | 00 | | RX mode:<br>0: normal mode,<br>1: direct through FIFO,<br>2: direct through GPIO |
| | | 3:0 | LEN_WID | 0111 | | Size in number of binary digit of length field |
| PCKTCTRL2 | 0x32 | 7:3 | PREAMBLE_LENGTH[4:0] | 00011 | R/W | Length of preamble field in bytes (from 1 to 32) |
| | | 2:1 | SYNC_LENGTH[1:0] | 11 | | Length of sync field in bytes (from 1 to 4) |
| | | 0 | FIX_VAR_LEN | 0 | | Packet length mode.<br>0: fixed,<br>1: variable (in variable mode the field LEN_WID of PCKTCTRL3 register must be configured) |
| PCKTCTRL1 | 0x33 | 7:5 | CRC_MODE[2:0] | 001 | R/W | CRC:<br>0: No CRC,<br>1: 0x07,<br>2: 0x8005,<br>3: 0x1021,<br>4: 0x864CBF |
| | | 4 | WHIT_EN[0] | 0 | | 1: enable the whitening mode on the data<br>(see *Section 9.6.3*) |
| | | 3:2 | TXSOURCE[1:0] | 00 | | TX source data:<br>0: normal mode,<br>1: direct through FIFO,<br>2: direct through GPIO,<br>3: PN9 |
| | | 1 | Reserved | 0 | | |
| | | 0 | FEC_EN | 0 | | 1: enable the FEC encoding in TX or enable the Viterbi decoding in RX<br>(see *Section 9.6.1*) |
| PCKTLEN1 | 0x34 | 7:0 | PCKTLEN1 | 0 | R/W | Length of packet in bytes (MSB) |

**Table 44. Packet/protocol configuration registers (continued)**

| Register name | Address | Bit | Field Name | Reset | R/W | Description |
|---|---|---|---|---|---|---|
| PCKTLEN0 | 0x35 | 7:0 | PCKTLEN0 | 0x14 | R/W | Length of packet in bytes (LSB) |
| SYNC4 | 0x36 | 7:0 | SYNC4 | 0x88 | R/W | Sync word 4 |
| SYNC3 | 0x37 | 7:0 | SYNC3 | 0x88 | R/W | Sync word 3 |
| SYNC2 | 0x38 | 7:0 | SYNC2 | 0x88 | R/W | Sync word 2 |
| SYNC1 | 0x39 | 7:0 | SYNC1 | 0x88 | R/W | Sync word 1 |
| QI | 0x3A | 7:6 | SQI_TH[1:0] | 00 | R/W | SQI threshold (see *Section 9.10.4*) |
| | | 5:2 | PQI_TH[3:0] | 0000 | | PQI threshold (see *Section 9.10.3*) |
| | | 1 | SQI_EN[0] | 1 | | 1: enable SQI |
| | | 0 | PQI_EN[0] | 0 | | 1: enable PQI |
| MBUS_PRMBL | 0x3B | 7:0 | MBUS_PRMBL[7:0] | 0x20 | R/W | MBUS preamble length in chip sequence '01' |
| MBUS_PSTMBL | 0x3C | 7:0 | MBUS_PSTMBL[7:0] | 0x20 | R/W | MBUS postamble length in chip sequence '01' |
| MBUS_CTRL | 0x3D | 7:4 | Reserved | 00000 | R/W | |
| | | 3:1 | MBUS_SUBMODE[2:0] | 000 | | MBUS sub mode: allowed values are 0, 1, 3 and 5<br>WM-BUS sub mode:<br>0: S1 S2 long header,<br>1: S1m S2 T2 other to meter,<br>3: T1 T2 meter to other,<br>5: R2 short header |
| | | 0 | Reserved | 0 | | |
| FIFO_CONFIG[3] | 0x3E | 7 | Reserved | 0 | R/W | |
| | | 6:0 | RXAFTHR [6:0] | 110000 | R/W | FIFO almost full threshold for RX FIFO |
| FIFO_CONFIG[2] | 0x3F | 7 | Reserved | 0 | R/W | |
| | | 6:0 | RXAETHR [6:0] | 110000 | R/W | FIFO almost empty threshold for RX FIFO |
| FIFO_CONFIG[1] | 0x40 | 7 | Reserved | 0 | R/W | |
| | | 6:0 | TXAFTHR [6:0] | 110000 | R/W | FIFO almost full threshold for TX FIFO |
| FIFO_CONFIG[0] | 0x41 | 7 | Reserved | 0 | R/W | |
| | | 6:0 | TXAETHR [6:0] | 110000 | R/W | FIFO almost empty threshold for TX FIFO |
| PCKT_FLT_GOALS[12] | 0x42 | 7:0 | CONTROL0_MASK | 0 | R/W | For received packet only: all 0s: no filtering on control field |

Table 44. Packet/protocol configuration registers (continued)

| Register name | Address | Bit | Field Name | Reset | R/W | Description |
|---|---|---|---|---|---|---|
| PCKT_FLT_GOALS[11] | 0x43 | 7:0 | CONTROL1_MASK | 0 | R/W | For received packet only: all 0s: no filtering on control field |
| PCKT_FLT_GOALS[10] | 0x44 | 7:0 | CONTROL2_MASK | 0 | R/W | For received packet only: all 0s: no filtering on control field |
| PCKT_FLT_GOALS[9] | 0x45 | 7:0 | CONTROL3_MASK | 0 | R/W | For received packet only: all 0s: no filtering on control field |
| PCKT_FLT_GOALS[8] | 0x46 | 7:0 | CONTROL0_FIELD | 0 | R/W | Control field (byte 3) to be used as reference for receiver |
| PCKT_FLT_GOALS[7] | 0x47 | 7:0 | CONTROL1_FIELD | 0 | R/W | Control field (byte 2) to be used as reference for receiver |
| PCKT_FLT_GOALS[6] | 0x48 | 7:0 | CONTROL2_FIELD | 0 | R/W | Control field (byte 1) to be used as reference for receiver |
| PCKT_FLT_GOALS[5] | 0x49 | 7:0 | CONTROL3_FIELD | 0 | R/W | Control field (byte 0) to be used as reference for receiver |
| PCKT_FLT_GOALS[4] | 0x4A | 7:0 | RX_SOURCE_MASK | 0 | R/W | For received packet only: all 0s: no filtering |
| PCKT_FLT_GOALS[3] | 0x4B | 7:0 | RX_SOURCE_ADDR | 0 | R/W | RX packet source / TX packet destination fields |
| PCKT_FLT_GOALS[2] | 0x4C | 7:0 | BROADCAST | 0 | R/W | Broadcast address |
| PCKT_FLT_GOALS[1] | 0x4D | 7:0 | MULTICAST | 0 | R/W | Multicast address |
| PCKT_FLT_GOALS[0] | 0x4E | 7:0 | TX_SOURCE_ADDR | 0 | R/W | TX packet source / RX packet destination fields |

**Table 44. Packet/protocol configuration registers (continued)**

| Register name | Address | Bit | Field Name | Reset | R/W | Description |
|---|---|---|---|---|---|---|
| PCKT_FLT_OPTIONS | 0x4F | 7 | Reserved | 0 | R/W | |
| | | 6 | RX_TIMEOUT_AND_OR_SELECT | 1 | | 1: 'OR' logical function applied to CS/SQI/PQI values (masked by 7:5 bits in PROTOCOL register: CS_TIMEOUT_MASK, SQI_TIMEOUT_MASK, PQI_TIMEOUT_MASK) |
| | | 5 | CONTROL_FILTERING | 1 | | 1: RX packet accepted if its control fields match with masked CONTROLx_FIELD registers |
| | | 4 | SOURCE_FILTERING | 1 | | 1: RX packet accepted if its source field matches with masked RX_SOURCE_ADDR register |
| | | 3 | DEST_VS_SOURCE_ADDR | 0 | | 1: RX packet accepted if its destination address matches with TX_SOURCE_ADDR reg. |
| | | 2 | DEST_VS_MULTICAST_ADDR | 0 | | 1: RX packet accepted if its destination address matches with MULTICAST register |
| | | 1 | DEST_VS_BROADCAST_ADDR | 0 | | 1: RX packet accepted if its destination address matches with BROADCAST reg. |
| | | 0 | CRC_CHECK | 0 | | 1: packet discarded if CRC not valid. |
| PROTOCOL[2] | 0x50 | 23 | CS_TIMEOUT_MASK | 0 | R/W | 1: CS value contributes to timeout disabling |
| | | 22 | SQI_TIMEOUT_MASK | 0 | | 1: SQI value contributes to timeout disabling |
| | | 21 | PQI_TIMEOUT_MASK | 0 | | 1: PQI value contributes to timeout disabling |
| | | 20:19 | TX_SEQ_NUM_RELOAD[1:0] | 0 | | TX sequence number to be used when counting reset is required using the related command. |
| | | 18 | RCO_CALIBRATION | 0 | | 1: enable the automatic RCO calibration |
| | | 17 | VCO_CALIBRATION | 1 | | 1: enable the automatic VCO calibration |
| | | 16 | LDC_MODE | 0 | | 1: LDC mode on |

**Table 44. Packet/protocol configuration registers (continued)**

| Register name | Address | Bit | Field Name | Reset | R/W | Description |
|---|---|---|---|---|---|---|
| PROTOCOL[1] | 0x51 | 15 | LDC_RELOAD_ON_SYNC | 0 | R/W | 1: LDC timer is reloaded with the value stored in the LDC_RELOAD registers |
| | | 14 | PIGGYBACKING | 0 | | 1: PIGGYBACKING enabled |
| | | 13:12 | Reserved | 00 | | |
| | | 11 | SEED_RELOAD | 0 | | 1: reload the back-off random generator seed using the value written in the BU_COUNTER_SEED_MSBYTE / LSBYTE registers |
| | | 10 | CSMA_ON | 0 | | 1: CSMA channel access mode enabled |
| | | 9 | CSMA_PERS_ON | 0 | | 1: CSMA persistent (no back-off) enabled |
| | | 8 | AUTO_PCKT_FLT | 0 | | 1: automatic packet filtering mode enabled |
| PROTOCOL[0] | 0x52 | 7:4 | NMAX_RETX[3:0] | 0 | R/W | Max. number of re-TX (from 0 to 15).<br>0: re-transmission is not performed |
| | | 3 | NACK_TX | 1 | | 1: field NO_ACK=1 on transmitted packet |
| | | 2 | AUTO_ACK | 0 | | 1: automatic acknowledgement after correct packet reception |
| | | 1 | PERS_RX | 0 | | 1: persistent reception enabled |
| | | 0 | PERS_TX | 0 | | 1: persistent transmission enabled |
| TIMERS[5] | 0x53 | 47:40 | RX_TIMEOUT_PRESCALER[7:0] | 1 | R/W | Prescaler value of the RX TIMEOUT timer. When this timer expires the SPIRIT1 exits RX state. Can be controlled using the quality indicator (SQI, PQI, CS). |
| TIMERS[4] | 0x54 | 39:32 | RX_TIMEOUT_COUNTER[7:0] | 0 | R/W | Counter value of the RX TIMEOUT timer. When this timer expires the SPIRIT1 exits RX state. Can be controlled using the quality indicator (SQI, PQI, CS) |

**Table 44. Packet/protocol configuration registers (continued)**

| Register name | Address | Bit | Field Name | Reset | R/W | Description |
|---|---|---|---|---|---|---|
| TIMERS[3] | 0x55 | 31:24 | LDC_PRESCALER[7:0] | 1 | R/W | Prescaler value of the LDC wake-up timer. When this timer expires the SPIRIT1 exits SLEEP state. |
| TIMERS[2] | 0x56 | 23:16 | LDC_COUNTER[7:0] | 0 | R/W | Counter value of the LDC wake-up timer. When this timer expires the SPIRIT1 exits SLEEP state. |
| TIMERS[1] | 0x57 | 15:8 | LDC_RELOAD_PRESCALER[7:0] | 1 | R/W | Prescaler value of the LDC reload timer. When this timer expires the SPIRIT1 exits SLEEP state. The reload timer value is used if the SYNC word is detected (by the receiver) or if the LDC_RELOAD command is used. |
| TIMERS[0] | 0x58 | 7:0 | LDC_RELOAD_COUNTER[7:0] | 0 | R/W | Counter part of the LDC reload value timer. When this timer expires the SPIRIT1 exits SLEEP state. The reload timer value is used if the SYNC word is detected (by the receiver) or if the LDC_RELOAD command is used. |
| CSMA_CONFIG[3] | 0x64 | 7:0 | BU_COUNTER_SEED_MSBYTE | 0xFF | R/W | The MSB value of the counter of the seed of the random number generator used to apply the BBE algorithm during the CSMA algorithm |
| CSMA_CONFIG[2] | 0x65 | 7:0 | BU_COUNTER_SEED_LSBYTE | 0 | R/W | The LSB value of the counter seed of the random number generator used to apply the BBE algorithm during the CSMA algorithm |
| CSMA_CONFIG[1] | 0x66 | 7:2 | BU_PRESCALER[5:0] | 000001 | R/W | The prescaler value used to program the back-off unit BU |
| | | 1:0 | CCA_PERIOD | 00 | | Used to program the $T_{cca}$ time (64 / 128 / 256 / 512 × $T_{bit}$) |
| CSMA_CONFIG[0] | 0x67 | 7:4 | CCA_LENGTH[3:0] | 0000 | R/W | Used to program the $T_{listen}$ time |
| | | 3 | Reserved | 0 | | |
| | | 2:0 | NBACKOFF_MAX | 000 | | Max. number of back-off cycles |

**Table 44. Packet/protocol configuration registers (continued)**

| Register name | Address | Bit | Field Name | Reset | R/W | Description |
|---|---|---|---|---|---|---|
| TX_CTRL_FIELD[3] | 0x68 | 7:0 | TX_CTRL3 | 0 | R/W | Control field value to be used in TX packet as byte n.3 |
| TX_CTRL_FIELD[2] | 0x69 | 7:0 | TX_CTRL2 | 0 | R/W | Control field value to be used in TX packet as byte n.2 |
| TX_CTRL_FIELD[1] | 0x6A | 7:0 | TX_CTRL1 | 0 | R/W | Control field value to be used in TX packet as byte n.1 |
| TX_CTRL_FIELD[0] | 0x6B | 7:0 | TX_CTRL0 | 0 | R/W | Control field value to be used in TX packet as byte n.0 |
| PM_CONFIG[2] | 0xA4 | 7 | Reserved | 0 | R/W | |
| | | 6 | EN_TS_BUFFER | 0 | | 1: temperature sensor output is buffered |
| | | 5 | DISABLE_SMPS | 0 | | 0: enable internal SMPS<br>1: disable internal SMPS |
| | | 4 | Reserved | 0 | | |
| | | 3 | SET_SMPS_VTUNE | 1 | | Sets the SMPS Vtune voltage |
| | | 2 | SET_SMPS_PLLBW | 1 | | Sets the SMPS bandwidth |
| | | 1:0 | Reserved | 00 | | |
| PM_CONFIG[1] | 0xA5 | 7 | EN_RM | 0 | R/W | 0: divider by 4 enabled (SMPS' switching frequency is $F_{SW}$=FOSC/4)<br>1: rate multiplier enabled (SMPS' switching frequency is $F_{SW}$=KRM*FOSC/(2^15) |
| | | 6:0 | KRM[14:8] | 0100000 | | Sets the divider ration of the rate multiplier. |
| PM_CONFIG[0] | 0xA6 | 7:0 | KRM[7:0] | 0 | R/W | |
| XO_RCO_CONFIG | 0xA7 | 7:4 | Reserved | 1110 | R/W | |
| | | 3 | EXT_RCOSC | 0 | | 1: the 34.7kHz signal must be supplied from a GPIO pin |
| | | 2:0 | Reserved | 001 | | |
| TEST_SELECT | 0xA8 | 7:0 | Reserved | 0x00 | R/W | |
| PM_TEST | 0xB2 | 7:0 | Reserved | 0x42 | | |

**Table 45. Frequently used registers**

| Register name | Address | Bit | Field Name | Reset | R/W | Description |
|---|---|---|---|---|---|---|
| CHNUM | 0x6C | 7:0 | CH_NUM | 0 | R/W | Channel number. This value is multiplied by the channel spacing and added to the synthesizer base frequency to generate the actual RF carrier frequency. See *Equation 3* |
| VCO_CONFIG | 0xA1 | 7:6 | Reserved | 00 | R/W | |
| | | 5:0 | VCO_GEN_CURR | 010001 | | Set the VCO current |
| RCO_VCO_CALIBR_IN [2] | 0x6D | 7:4 | RWT_IN[3:0] | 0111 | R/W | RWT word value for the RCO |
| | | 3:0 | RFB_IN[4:1] | 0000 | | RFB word value for the RCO |
| RCO_VCO_CALIBR_IN [1] | 0x6E | 7 | RFB_IN[0] | 0 | R/W | |
| | | 6:0 | VCO_CALIBR_TX[6:0] | 1001000 | | Word value for the VCO to be used in TX mode |
| RCO_VCO_CALIBR_IN [0] | 0x6F | 7 | Reserved | 0 | R/W | |
| | | 6:0 | VCO_CALIBR_RX[6:0] | 1001000 | | Word value for the VCO to be used in RX mode |
| AES_KEY_IN[15] | 0x70 | 7:0 | AES_KEY15 | 0 | R/W | AES engine key input (128 bits) |
| AES_KEY_IN[14] | 0x71 | 7:0 | AES_ KEY14 | 0 | R/W | AES engine key input (128 bits) |
| | … | 7:0 | … | … | … | … |
| AES_KEY_IN[1] | 0x7E | 7:0 | AES_ KEY1 | 0 | R/W | AES engine key input (128 bits) |
| AES_KEY_IN[0] | 0x7F | 7:0 | AES_ KEY0 | 0 | R/W | AES engine key input (128 bits) |
| AES_DATA_IN[15] | 0x80 | 7:0 | AES_IN15 | 0 | R/W | AES engine data input (128 bits) |
| AES_DATA_IN[14] | 0x81 | 7:0 | AES_IN14 | 0 | R/W | AES engine data input (128 bits) |
| | … | … | … | … | … | … |
| AES_DATA_IN[1] | 0x8E | 7:0 | AES_IN1 | 0 | R/W | AES engine data input (128 bits) |
| AES_DATA_IN[0] | 0x8F | 7:0 | AES_IN0 | 0 | R/W | AES engine data input (128 bits) |
| IRQ_MASK[3] | 0x90 | 7:0 | INT_MASKT[31:24] | 0 | R/W | The IRQ mask register to route the IRQ information to a GPIO. See *Table 36*. |
| IRQ_MASK[2] | 0x91 | 7:0 | INT_MASK [23:16] | 0 | R/W | The IRQ mask register to route the IRQ information to a GPIO. See *Table 36*. |

Table 45. Frequently used registers (continued)

| Register name | Address | Bit | Field Name | Reset | R/W | Description |
|---|---|---|---|---|---|---|
| LINK_QUALIF[1] | 0xC6 | 7 | CS | 0 | R | Carrier sense indication |
| | | 6:0 | SQI[6:0] | 0 | | SQI value of the received packet |
| LINK_QUALIF[0] | 0xC7 | 7:4 | Reserved | 0 | R | |
| | | 3:0 | AGC_WORD | 0 | | AGC word of the received packet |
| RSSI_LEVEL | 0xC8 | 7:0 | RSSI_LEVEL | 0 | R | RSSI level of the received packet |
| RX_PCKT_LEN[1] | 0xC9 | 7:0 | RX_PCKT_LEN1 | 0 | R | Length (number of bytes) of the received packet: RX_PCKT_LEN=RX_PCKT_LEN1 × 256 + RX_PCKT_LEN0 |
| RX_PCKT_LEN[0] | 0xCA | 7:0 | RX_PCKT_LEN0 | 0 | R | |
| CRC_FIELD[2] | 0xCB | 7:0 | CRC2 | 0 | R | CRC field of the received packet, byte 2 |
| CRC_FIELD[1] | 0xCC | 7:0 | CRC1 | 0 | R | CRC field of the received packet, byte 1 |
| CRC_FIELD[0] | 0xCD | 7:0 | CRC0 | 0 | R | CRC field of the received packet, byte 0 |
| RX_CTRL_FIELD[3] | 0xCE | 7:0 | RX_CTRL0 | 0 | R | Control field(s) of the received packet, byte 0 |
| RX_CTRL_FIELD[2] | 0xCF | 7:0 | RX_CTRL1 | 0 | R | Control field(s) of the received packet, byte 1 |
| RX_CTRL_FIELD[1] | 0xD0 | 7:0 | RX_CTRL2 | 0 | R | Control field(s) of the received packet, byte 2 |
| RX_CTRL_FIELD[0] | 0xD1 | 7:0 | RX_CTRL3 | 0 | R | Control field(s) of the received packet, byte 3 |
| RX_ADDR_FIELD[1] | 0xD2 | 7:0 | ADDR1 | 0 | R | Source address field of the RX packet. |
| RX_ADDR_FIELD[0] | 0xD3 | 7:0 | ADDR0 | 0 | R | Destination address field of the RX packet. |
| AES_ DATA_OUT[15] | 0xD4 | 7:0 | AES_OUT15 | 0 | R | AES engine data output (128 bits) |
| AES_ DATA_OUT[14] | 0xD5 | 7:0 | AES_OUT14 | 0 | R | AES engine data output (128 bits) |
| | … | … | … | … | … | … |
| AES_ DATA_OUT[1] | 0xE2 | 7:0 | AES_OUT1 | 0 | R | AES engine data output (128 bits) |
| AES_ DATA_OUT[0] | 0xE3 | 7:0 | AES_OUT0 | 0 | R | AES engine data output (128 bits) |

**Table 45. Frequently used registers (continued)**

| Register name | Address | Bit | Field Name | Reset | R/W | Description |
|---|---|---|---|---|---|---|
| RCO_VCO_CALIBR_OUT[1] | 0xE4 | 7:4 | RWT_OUT[3:0] | 0 | R | RWT word from internal RCO calibrator |
| | | 3:0 | RFB_OUT[4:1] | 0 | | RFB word from internal RCO calibrator |
| RCO_VCO_CALIBR_OUT[0] | 0xE5 | 7 | RFB_OUT[0] | 0 | R | |
| | | 6:0 | VCO_CALIBR_DATA | 0 | | Output word from internal VCO calibrator |
| LINEAR_FIFO_STATUS[1] | 0xE6 | 7 | Reserved | 0 | R | |
| | | 6:0 | ELEM_TXFIFO | 0 | | Number of elements in the linear TX FIFO (from 0 to 96 bytes) |
| LINEAR_FIFO_STATUS[0] | 0xE7 | 7 | Reserved | 0 | R | |
| | | 6:0 | ELEM_RXFIFO | 0 | | Number of elements in the linear RX FIFO (from 0 to 96 bytes) |
| IRQ_STATUS[3] | 0xFA | 7:0 | INT_EVENT[31:24] | 0 | RR | The IRQ status register. See *Table 36*. |
| IRQ_STATUS[2] | 0xFB | 7:0 | INT_EVENT[23:16] | 0 | RR | The IRQ status register. See *Table 36*. |
| IRQ_STATUS[1] | 0xFC | 7:0 | INT_EVENT[15:8] | 0 | RR | The IRQ status register. See *Table 36*. |
| IRQ_STATUS[0] | 0xFD | 7:0 | INT_EVENT[7:0] | 0 | RR | The IRQ status register. See *Table 36*. |

**Table 46. General information**

| Register | Address | Bit | Field name | Reset | R/W | Description |
|---|---|---|---|---|---|---|
| DEVICE_INFO[1:0] | 0xF0 | 7:0 | PARTNUM[7:0] | 0x01 | R | Device part number |
| | 0xF1 | 7:0 | VERSION[7:0] | 0x30 | R | Device version number |

# 9 Regulatory compliance

## RF compliance

The RF certifications obtained are described in *Table 8* below.

**Table 8. RF certification summary**

| | | Comment |
|---|---|---|
| FCC ID | S9NSPSGRFC | With external “TAOGLASS” antenna and UFL to SMA connector RF cable version |
| IC ID | 8976C-SPSGRFC | With external “TAOGLASS” antenna and UFL to SMA connector RF cable version |
| ETSI | Compliant | Approved with external “LINX” antenna and UFL to SMA cable version |

This radio transmitter IC ID 8976-SPSGRFC has been approved by Industry Canada to operate with the antenna types listed below with the maximum permissible gain indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

*Note: The “TI.19.2113” antenna from “TAOGLASS” is the only approved antenna using the u.fl connector version.*

***(Please, see the A.1 at the bottom of this document for the French translation).***

The following are the main features of the antennas approved during the certification RF test procedures, dedicated to SPSGRFC modules.

**For the SPSGRFC-915 module the approved antenna is the TAOGLASS TI.19.2113**

TI.19 is a high performance 915MHz ISM band dipole omni-directional antenna. The hinged design enables the antenna to be positioned at its most suitable angle. This antenna features a SMA(M) Plug Connector.

For a lot of antenna applications, such as Wi-Fi Hotspot or cellular Pico-cell, the antenna of the operator's device and the antenna of the user's remote device are not on the same horizontal level. The TI.19 has been designed with a butterfly shape radiation pattern, to help counteract this effect.

## 2. Specification

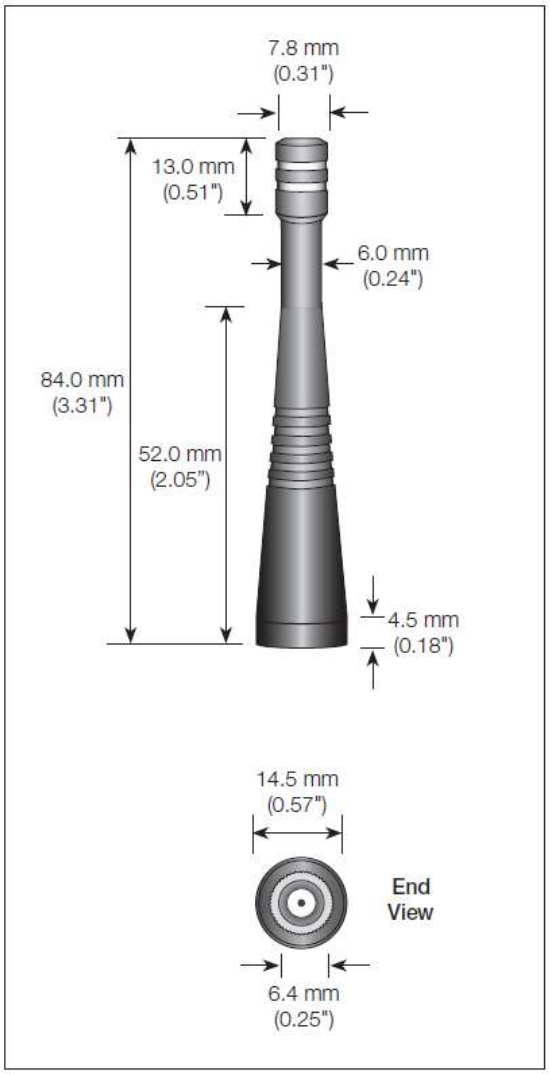
| ELECTRICAL | |
|---|---|
| Frequency | 902 ~ 928MHz |
| Peak Gain (bend) | 2.5dBi |
| Peak Gain (straight) | 2.4dBi |
| Average Gain (bend) | -1.0dBi |
| Average Gain (straight) | -0.9dBi |
| Efficiency (bend) | 81% |
| Efficiency (straight) | 82% |
| Impedance | 50Ω |
| VSWR | < 1.9 : 1 |
| Polarization | Linear |
| Radiation Pattern | Omni |
| Input Power | 10 W |
| MECHANICAL | |
| Antenna Length | 389 ± 5 mm |
| Antenna Diameter | 13 ± 0.5 mm |
| Casing | TPU |
| Connector | SMA Male |
| ENVIRONMENTAL | |
| Temperature Range | -40°C to 85°C |
| Humidity | Non-condensing 65°C 95% RH |

*Note all data provided in this table are based on the "TAOGLASS TI.19.2113" reference documentation.

## For the SPSGRFC-868 module the approved antenna is the LINX ANT-868-CW-QW

### Product Description

CW Series ¼-wave antennas deliver outstanding performance in a rugged and cosmetically attractive package. These antennas are available with standard SMA or FCC Part 15 compliant RP-SMA connectors. RP-SMA connectors allow for easy field replacement while complying with FCC requirements. A wide variety of matching connectors permit numerous mounting options.




### Features

- Low cost
- Excellent performance
- Omni-directional pattern
- Wide bandwidth
- Very low VSWR
- Fully weatherized
- Flexible main shaft
- Rugged & damage-resistant
- SMA or Part 15 compliant RP-SMA connector
- Use with plastic* or metal enclosures

*Requires proximity ground plane

### Electrical Specifications

| | |
|---|---|
| Center Frequency: | 868MHz |
| Recom. Freq. Range: | 750–950MHz |
| Wavelength: | ¼-wave |
| Peak Gain: | 1.6dBi |
| VSWR: | <1.9 typ. at center |
| Impedance: | 50-ohms |
| Connector: | RP-SMA or SMA |
| Oper. Temp. Range: | –40°C to +90°C |

Electrical specifications and plots measured on 10.16 cm x 10.16 cm (4.00" x 4.00") reference ground plane

### Ordering Information

ANT-868-CW-QW (with RP-SMA connector)
ANT-868-CW-QW-SMA (with SMA connector)

*Note all data provided in this table are based on the "LINX - ANT-868-CW-QW" reference ground plane.

**For the SPSGRFC-433 module the approved antenna is the LINX ANT-433-CW-QW**

## Product Description

HW Series antennas deliver outstanding performance in a rugged and cosmetically attractive package. The 315, 418 and 433MHz monopole versions have a straight whip ¼-wave element. The straight whip element delivers wide bandwidth and consistent performance. The antennas attach via a standard SMA or Part 15 compliant RP-SMA connector. Custom colors and connectors are available for volume OEM customers.

## Features

- Low cost
- Excellent performance
- Omni-directional pattern
- Outstanding VSWR
- Rugged & damage-resistant
- Standard SMA or Part 15 compliant RP-SMA connector
- Custom colors and terminators for volume OEMs
- Use with plastic* or metal enclosures
- Internal O-ring seal on connector

* Requires proximity ground plane

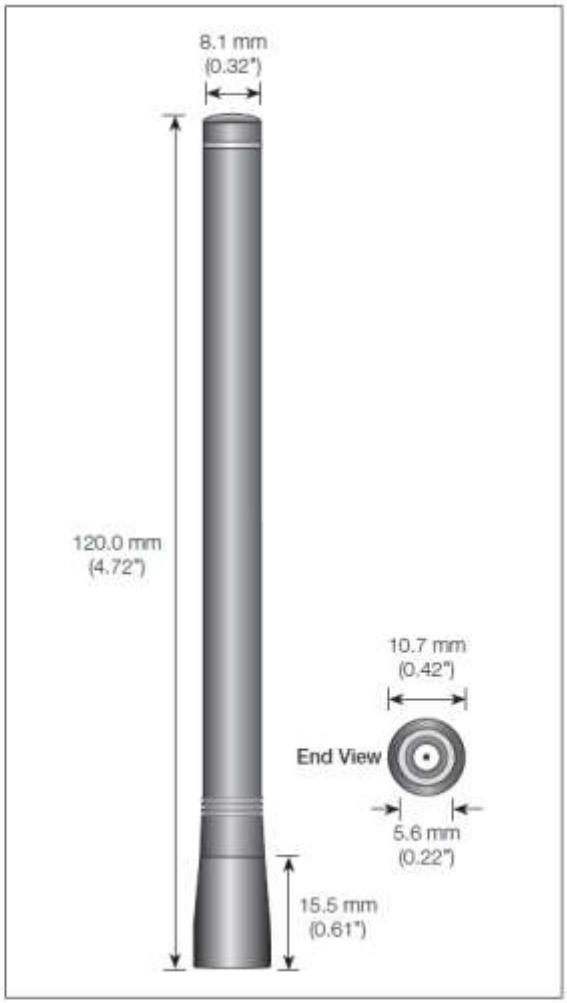
## Electrical Specifications

| | |
|---|---|
| Center Frequency: | 433MHz |
| Recmd. Freq. Range: | 418–448MHz |
| Wavelength: | ¼-wave |
| VSWR: | ≤ 2.0 typical at center |
| Peak Gain: | 0dBi |
| Impedance: | 50-ohms |
| Connection: | SMA or RP-SMA |
| Oper. Temp. Range: | –20°C to +85°C |

Electrical specifications and plots measured with a 10.16 cm x 10.16 cm (4.00" x 4.00") reference ground plane.

## Ordering Information

ANT-433-CW-HW (with RP-SMA connector)
ANT-433-CW-HW-SMA (with SMA connector)




*Note all data provided in this table are based on the "LINX - ANT-433-CW-QW" reference ground plane.

# FCC and IC

This module has been tested and complies with the FCC part 15 and IC RSS-247 regulations. These limits are designed to provide reasonable protection against harmful interference in approved installations. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.

However, there is no guarantee that interference will not occur in a particular installation.

This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions:

1. The device must not cause harmful interference.

and

2. The device must accept any interference received, including interference that may cause undesired operation.

Modifications or changes to this equipment not expressly approved by the party responsible for compliance may render void the user's authority to operate this equipment.

## Modular approval, FCC and IC

- FCC ID: S9NSPSGRFC
- IC: 8976C-SPSGRFC

In accordance with FCC part 15, the module SPSGRFC-915 is listed above as a modular transmitter device.
This module and the corresponding antenna are evaluated for stand-alone use only. Finished products incorporating multiple transmitters must comply with collocation and RF exposure requirements in accordance with FCC multi-transmitter product procedures. Collocated transmitters operating in portable RF exposure conditions (e.g. <20 cm from persons including but not limited to body worn and hand-held devices) may require separate approval.

### Labeling instructions

When integrating the SPSGRFC-915 into the final product, it must be ensured that the FCC and IC labeling requirements specified below are satisfied. Based on the Public Notice from FCC, the product into which the ST transmitter module is installed must display a label referring to the enclosed module. The label should use wording like the following:

Contains Transmitter Module

- FCC ID: S9NSPSGRFC
- IC: 8976C-SPSGRFC

Any similar wording that expresses the same meaning may also be used.

## *CE compliance*

This module complies with the following European EMI/EMC and safety directives and standards:

- ETSI EN 300 328 V1.8.1:2012
- EN 301 489-1 V1.9.2:2011 + EN 301 489-17 V2.2.1:2009
- EN 60950-1:2006 + A11:2009 + A1:2010 + A12:2011 + A2:2013
- EN 62479:2010

**Figure 3. CE certified**

# 10 Reflow soldering

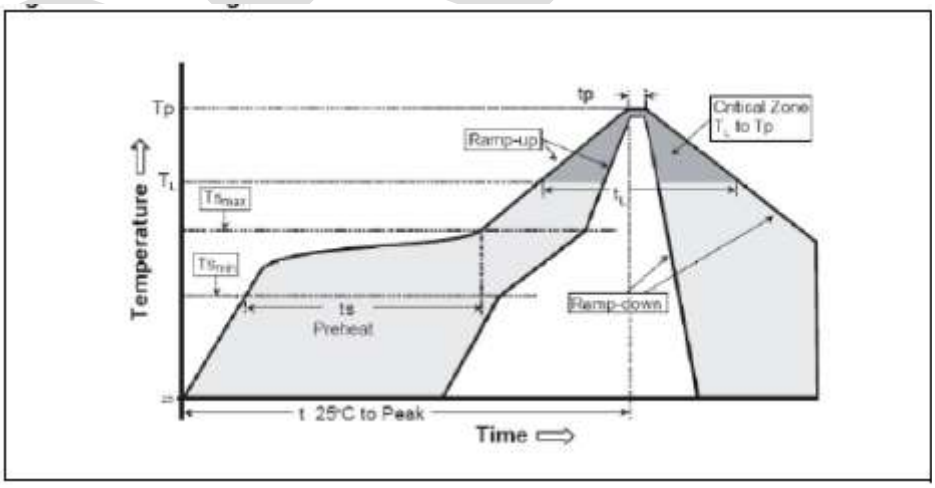
The SPSGRFC is a surface mount Sub1GHz Transceiver module supplied on a 11 pin, 4-layer PCB. The final assembly recommended reflow profiles are indicated here below.

Soldering phase has to be executed with care: In order to avoid undesired melting phenomenon, particular attention has to be taken on the set up of the peak temperature.
Here following some suggestions for the temperature profile based on IPC/JEDEC J-STD-020C, July 2004 recommendations.

**Table 4 – Soldering**

| Profile feature | PB-free assembly |
|---|---|
| Average ramp up rate ($T_{SMAX}$ to $T_P$) | 3°C / sec max |
| Preheat<br>Temperature min ($T_S$ min)<br>Temperature max ($T_S$ max)<br>Time ($t_S$ min to $t_S$ max) ($t_S$) | <br>150 °C<br>200 °C<br>60-100 sec |
| Time maintained above:<br>Temperature $T_L$<br>Time $t_L$ | <br>217 °C<br>60-70 sec |
| Peak temperature ($T_P$) | 240 + 0 °C |
| Time within 5 °C of actual peak temperature ($t_P$) | 10-20 sec |
| Ramp down rate | 6 °C / sec |
| Time from 25 °C to peak temperature | 8 minutes max |

**Figure 6 – Soldering profiles**



# 11 RoHS compliance

ST Bluetooth modules comply with the ECOPACK2 level of RoHS compliance grade.

# 12 Ordering Information

**Table 5 – Ordering Information**

| Order code | Description | Packing | MOQ |
|---|---|---|---|
| SPSGRFC-433 | 433 MHz Spirit1 transceiver module (Region 1,Europe) | Jedec tray | 2’448 pcs |
| SPSGRFC-868 | 868 MHz Spirit1 transceiver module (Region 1,Europe) | Jedec tray | 2’448 pcs |
| SPSGRFC-915 | 915 MHz Spirit1 transceiver module (Region 2,The Americas) | Jedec tray | 2’448 pcs |

# 13 Traceability

Each module is univocally identified by serial number stored in a 2D data matrix laser marked on the bottom side of the module itself.

The serial number has the following format:

WW YY D FF NNN

where

WW = week
YY = year
D = product ID family
FF = production panel coordinate identification
NNN = progressive serial number.

Each module bulk is identified by a bulk ID.

BULK ID and module 2D data matrix are linked by a reciprocal traceability link.
The module 2D data matrix traces the lot number of any raw material used.

# Déclaration de conformité

## A.1 Certification FCC

Le module SPSGRFC-915 a été testé et déclaré conforme avec la section 15 de la Règlementation FCC. Ces limitations sont stipulées afin de procurer une protection raisonnable contre les interférences gênantes dans les installations approuvées. Cet appareil génère, utilise et diffuse des ondes radio et, s'il n'est pas installé et utilisé en conformité avec les instructions dont il fait l'objet, peut causer des interférences gênantes sur les communications radio.

Il n'y a cependant pas de garantie qu'une interférence ne se produira pas dans une installation particulière.

Cet appareil est en conformité avec la section 15 des règlements FCC. L'utilisation est soumise aux deux conditions suivantes: (1) cet appareil ne doit pas causer d'interférences nocives, et (2) Cet appareil doit supporter toute interférence reçue, y compris des interférences qui peuvent provoquer un fonctionnement non désiré.

Tout changement ou modification fait(e) à cet appareil et non expressément approuvé(e) par STMicroelectronics peut annuler l'autorisation pour l'utilisateur de faire fonctionner l'appareil.

### Approbation du module

FCC ID: S9NSPSGRFC

Conformément à la section 15 des règlements FCC, le module SPSGRFC-915 est répertorié comme un dispositif émetteur modulaire.

Ce module n'est évalué que pour une utilisation autonome. Les produits finis incorporant plusieurs émetteurs doivent être conformes à la colocation et aux exigences d'exposition RF en concordance avec les procédures FCC multi-émetteurs. D'autres émetteurs fonctionnant dans des dispositifs portables exposés aux RF (par exemple, situés à moins de 20 cm des personnes avec dispositifs portatifs ou portés contre le corps) peuvent nécessiter d'une approbation séparée.

### A.1.1 Instructions d'étiquetage

Lors de l'intégration du module SPSGRFC-915 dans le produit final, le fabricant doit s'assurer que les exigences en matière d'étiquetage de la FCC sont satisfaites. Une déclaration doit être placée sur l'étiquette extérieure du produit final indiquant que le produit comprend un module certifié. L'étiquette doit comporter les informations suivantes (ou une mention analogue que recouvre la même notion):

Contient FCC ID: S9NSPSGRFC
OU Ce produit contient FCC ID: S9NSPSGRFC

Le sous-traitant doit inclure les énoncés suivants sur l'étiquette extérieure du produit final à moins que le produit ne soit trop petit (par exemple moins de 4 x 4 pouces):

Cet appareil est en conformité avec la section 15 des règlements FCC. L'utilisation est soumise aux deux conditions suivantes:
(1) cet appareil ne doit pas causer d'interférences nocives, et
(2) Cet appareil doit supporter toute interférence reçue, y compris des interférences qui peuvent provoquer un fonctionnement non désiré.

### A.1.2 Instructions pour l’utilisation du produit

La présente section concerne les produits finis contenant le module SPSGRFC-915, assujettis aux normes FCC. Le manuel du produit final doit contenir la déclaration suivante (ou une mention analogue que recouvre la même notion):

*“ Avertissement: Les changements ou modifications non expressément approuvés par la partie responsable de la conformité pourraient annuler l'autorisation de l'utilisateur de faire fonctionner cet équipement. (Section 15.21)”*

Dans le cas où le produit finis d’un fabriquant OEM rentre dans les limites de la Classe B (résidentiel), les énoncés suivants doivent être inclus dans le manuel du produit finis:

*“Remarque : Cet équipement a été testé et déclaré conforme aux limitations prévues dans le cadre de la classe B des appareils numériques, définies par la section 15 du règlement de la FCC. Ces limites sont conçues pour fournir une protection raisonnable contre toute interférence dangereuse issue d'une installation résidentielle. Cet équipement produit, utilise et peut émettre de l'énergie radio électrique et, s'il n'est pas installé et utilisé conformément aux présentes instructions, peut causer des interférences nuisibles aux communications radio. Cependant, il se peut que des interférences se produisent dans une installation particulière. Si cet appareil cause des interférences nuisibles à la réception des signaux de radio ou de télévision, ce qui peut être déterminé en allumant et en éteignant l'appareil, on encourage l'utilisateur d'essayer de corriger ces interférences par l'un des moyens suivants:*

- *Réorienter ou repositionner l'antenne de réception.*
- *Augmenter la distance séparant l’équipement du récepteur.*
- *Connecter l’équipement à une prise appartenant à un circuit différent de celui sur lequel le récepteur est connecté.*
- *Consulter le revendeur ou un technicien radio/TV expérimenté pour obtenir de l’aide.”*

Dans le cas où le produit fini d’un sous-traitant rentre dans les limites imposées aux appareils numériques de classe A, les énoncés suivants doivent être inclus dans le manuel du produit finis:

*“REMARQUE : Cet appareil a été testé et certifié conforme aux spécifications d'un appareil électronique de classe A (class A digital device), conformément à la partie 15 du règlement de la FCC. Ces contraintes sont destinées à fournir une protection raisonnable contre les interférences nuisibles quand l'appareil est utilisé dans une installation commerciale. Cet équipement produit, utilise et peut émettre de l'énergie radio électrique et, s'il n'est pas installé et utilisé conformément aux présentes instructions, peut causer des interférences nuisibles aux communications radio. L'utilisation de cet appareil dans une installation résidentielle peut entraîner des interférences nuisibles et l'utilisateur devra corriger les interférences à ses propres frais.”*

## A.2 Certification IC [(a)]

Le module SPSGRFC-915 a été testé et déclaré conforme avec la Règlementation IC CNR-210. Ces limitations sont stipulées afin de procurer une protection raisonnable contre les interférences gênantes en installations approuvées. Cet appareil génère, utilise et diffuse des ondes radio et, s'il n'est pas installé et utilisé en conformité avec les instructions dont il fait l'objet, peut causer des interférences gênantes sur les communications radio.

Il n'y a cependant pas de garantie qu'une interférence ne se produira pas dans une installation particulière.

Ce produit répond aux exigences de la norme CNR-210 d'Industrie Canada. Son fonctionnement est soumis aux deux conditions suivantes:
(1) cet appareil ne doit pas causer d'interférences nocives, et
(2) Cet appareil doit supporter toute interférence reçue, y compris des interférences qui peuvent provoquer un fonctionnement non désiré.

Tout changement ou modification fait(e) à cet appareil et non expressément approuvé(e) par STMicroelectronics peut annuler l'autorisation pour l'utilisateur de faire fonctionner l'appareil.

### Approbation du module

IC: 8976C-SPSGRFC

Conformément à IC CNR-210, le module SPSGRFC-915 est répertorié comme un dispositif émetteur modulaire
Ce module n'est évalué que pour une utilisation autonome. Les produits finis incorporant plusieurs émetteurs doivent être conformes à la colocation et aux exigences d'exposition RF en concordance avec les procédures FCC multi-émetteurs. D'autres émetteurs fonctionnant dans des dispositifs portables exposés aux RF (par exemple, situés à moins de 20 cm des personnes avec dispositifs portatifs ou portés contre le corps) peuvent nécessiter d'une approbation séparée.

### A.2.1 Instructions d'étiquetage

Lors de l'intégration du module SPSGRFC-915 dans le produit final, le fabricant doit s'assurer que les exigences en matière d'étiquetage de la IC sont satisfaites. Une déclaration doit être placée sur l'étiquette extérieure du produit final indiquant que le produit comprend un module certifié. L'étiquette doit comporter les informations suivantes (ou une mention analogue que recouvre la même notion):

Contient IC ID: 8976C-SPSGRFC

OU Ce produit contient IC ID: 8976C-SPSGRFC

Le sous-traitant doit inclure les énoncés suivants sur l'étiquette extérieure du produit final à moins que le produit ne soit trop petit (par exemple moins de 4 x 4 pouces):

Cet appareil est en conformité aux normes IC. L'utilisation est soumise aux deux conditions suivantes:
(1) cet appareil ne doit pas causer d'interférences nocives, et
(2) Cet appareil doit supporter toute interférence reçue, y compris des interférences qui peuvent provoquer un fonctionnement non désiré

### A.2.2 Instructions pour l'utilisation du produit

La présente section concerne les produits finis contenant le module SPSGRFC-915, assujettis aux normes IC. Le manuel du produit final doit contenir la déclaration suivante (ou une mention analogue que recouvre la même notion):

*"Avertissement: Les changements ou modifications non expressément approuvés par la partie responsable de la conformité pourraient annuler l'autorisation de l'utilisateur de faire fonctionner cet équipement. (CNR-210)"*

Dans le cas où le produit finis d'un fabriquant OEM rentre dans les limites de la Classe B (résidentiel), les énoncés suivants doivent être inclus dans le manuel du produit finis:

*" Remarque : Cet équipement a été testé et déclaré conforme aux limitations prévues dans le cadre de la classe B des appareils numériques, définies par la norme CNR-210 d'Industrie Canada.*

*Ces limites sont conçues pour fournir une protection raisonnable contre toute interférence dangereuse issue d'une installation résidentielle. Cet équipement produit, utilise et peut émettre de l'énergie radio électrique et, s'il n'est pas installé et utilisé conformément aux présentes instructions, peut causer des interférences nuisibles aux communications radio. Cependant, il se peut que des interférences se produisent dans une installation particulière. Si cet appareil cause des interférences nuisibles à la réception des signaux de radio ou de télévision, ce qui peut être déterminé en allumant et en éteignant l'appareil, nous encourageons l'utilisateur à essayer de corriger ces interférences par l'un des moyens suivants:*

- *Réorienter ou repositionner l'antenne de réception.*
- *Augmenter la distance séparant l'équipement du récepteur.*
- *Connecter l'équipement à une prise appartenant à un circuit différent de celui sur lequel le récepteur est connecté.*
- *Consulter le revendeur ou un technicien radio/TV expérimenté pour obtenir de l'aide."*

Dans le cas où le produit finis d'un fabriquant OEM rentre dans le cadre des limites imposées aux appareils numériques de classe A, les énoncés suivants doivent être inclus dans le manuel du produit finis:

*" REMARQUE: Cet appareil a été testé et certifié conforme aux spécifications d'un appareil électronique de classe A (class A digital device), conformément à la norme CNR-210 d'Industrie Canada. Ces contraintes sont destinées à fournir une protection raisonnable contre les interférences nuisibles quand l'appareil est utilisé dans une installation commerciale. Cet équipement produit, utilise et peut émettre de l'énergie radio électrique et, s'il n'est pas installé et utilisé conformément aux présentes instructions, peut causer des interférences nuisibles aux communications radio. L'utilisation de cet appareil dans une installation résidentielle peut entraîner des interférences nuisibles et l'utilisateur devra corriger les interférences à ses propres frais."*

## A.3 Certification CE

Le module SPSGRFC a obtenu une certification de conformité aux normes suivantes:

- EN 300 328 V1.8.1 :2012
- EN 300 328 V1.9.1 :2015
- EN 301 489-17 V2.2.1 :2009
- EN 301 489-1 V1.9.2:2011
- EN 62479 :2010
- EN60950-1:2006 + A11:2009 + A1:2010 + A12:2011 + A2 :2013

Le module est certifié CE:

CE 0051

## A.4 Antennes certifiées

**Pour le module SPSGRF-915 l'antenne approuvée est le Taoglas TI.19.2113**

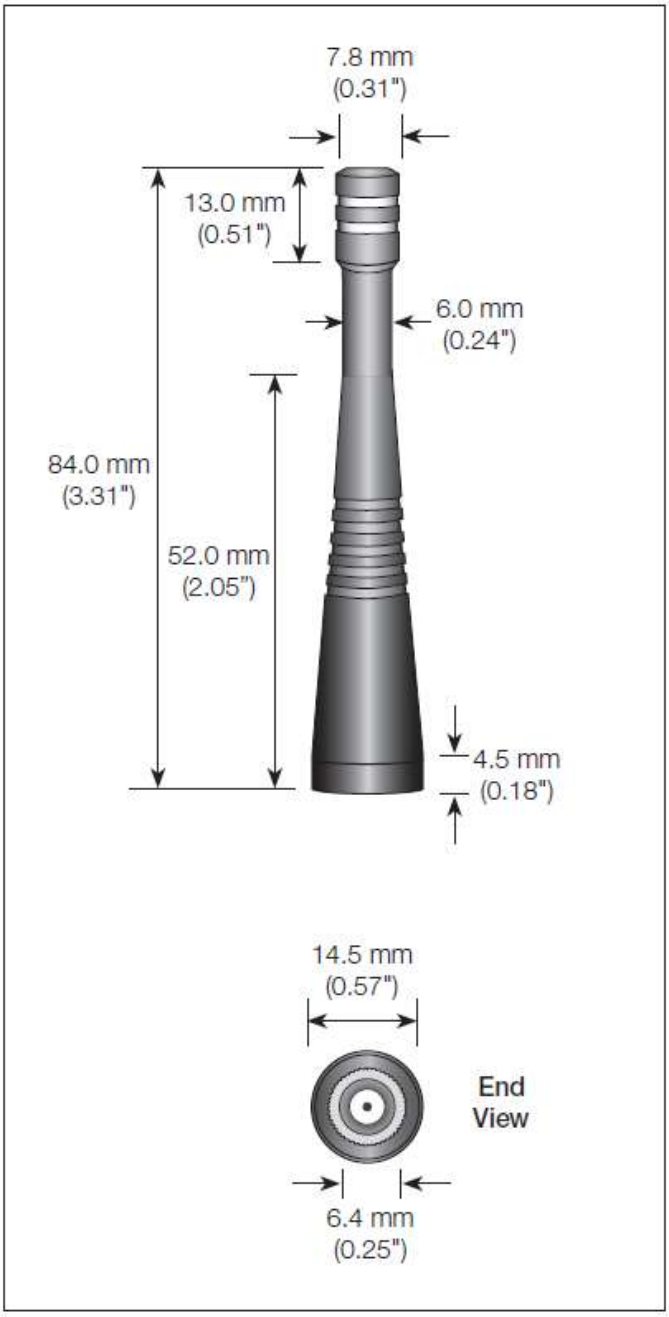
TI.19 est un 915MHz bande ISM dipôle antenne omnidirectionnelle haute performance. La conception permet à l'antenne articulée à être positionnée le plus approprié à son angle. Cette antenne dispose d'un SMA (M) de connecteur Fiche.
Pour un grand nombre d'applications d'antenne, telles que le Wi-Fi Hotspot ou Pico-cell cellulaire, le
l'antenne de l'appareil de l'opérateur et l'antenne du dispositif à distance de l'utilisateur ne sont pas sur le même plan horizontal. La TI.19 a été conçu avec un
diagramme de rayonnement en forme de papillon, pour aider à contrer cet effet.

**Spécifications de l'antenne**

| ELECTRICAL | |
|---|---|
| Frequency | 902 ~ 928MHz |
| Peak Gain (bend) | 2.5dBi |
| Peak Gain (straight) | 2.4dBi |
| Average Gain (bend) | -1.0dBi |
| Average Gain (straight) | -0.9dBi |
| Efficiency (bend) | 81% |
| Efficiency (straight) | 82% |
| Impedance | 50Ω |
| VSWR | < 1.9 : 1 |
| Polarization | Linear |
| Radiation Pattern | Omni |
| Input Power | 10 W |
| MECHANICAL | |
| Antenna Length | 389 ± 5 mm |
| Antenna Diameter | 13 ± 0.5 mm |
| Casing | TPU |
| Connector | SMA Male |
| ENVIRONMENTAL | |
| Temperature Range | -40°C to 85°C |
| Humidity | Non-condensing 65°C 95% RH |

**Pour le module SPSGRF-868 l'antenne approuvée est le LINX ANT-868-CW-QW**

Les antennes CW série ¼ d'onde offrent exceptionnelle
la performance dans un boîtier robuste et esthétiquement attrayant. Ces antennes sont disponibles avec SMA standard ou FCC Part 15 conformes connecteurs RP-SMA. connecteurs RP-SMA permettent le remplacement facile sur le terrain tout en respectant les exigences de la FCC. Une grande variété de connecteurs correspondant permet de nombreuses options de montage.



**Caractéristiques**

• À bas prix
• Performance excellente
• modèle Omni-directionnel
• Large bande passante
• Très faible ROS
• Entièrement intempérisés
• arbre principal flexible
• Robuste et résistante aux dommages
• SMA ou de la partie 15 connecteur RP-SMA conforme
• Utiliser avec du plastique * ou boîtiers métalliques

* Nécessite la proximité plan de masse

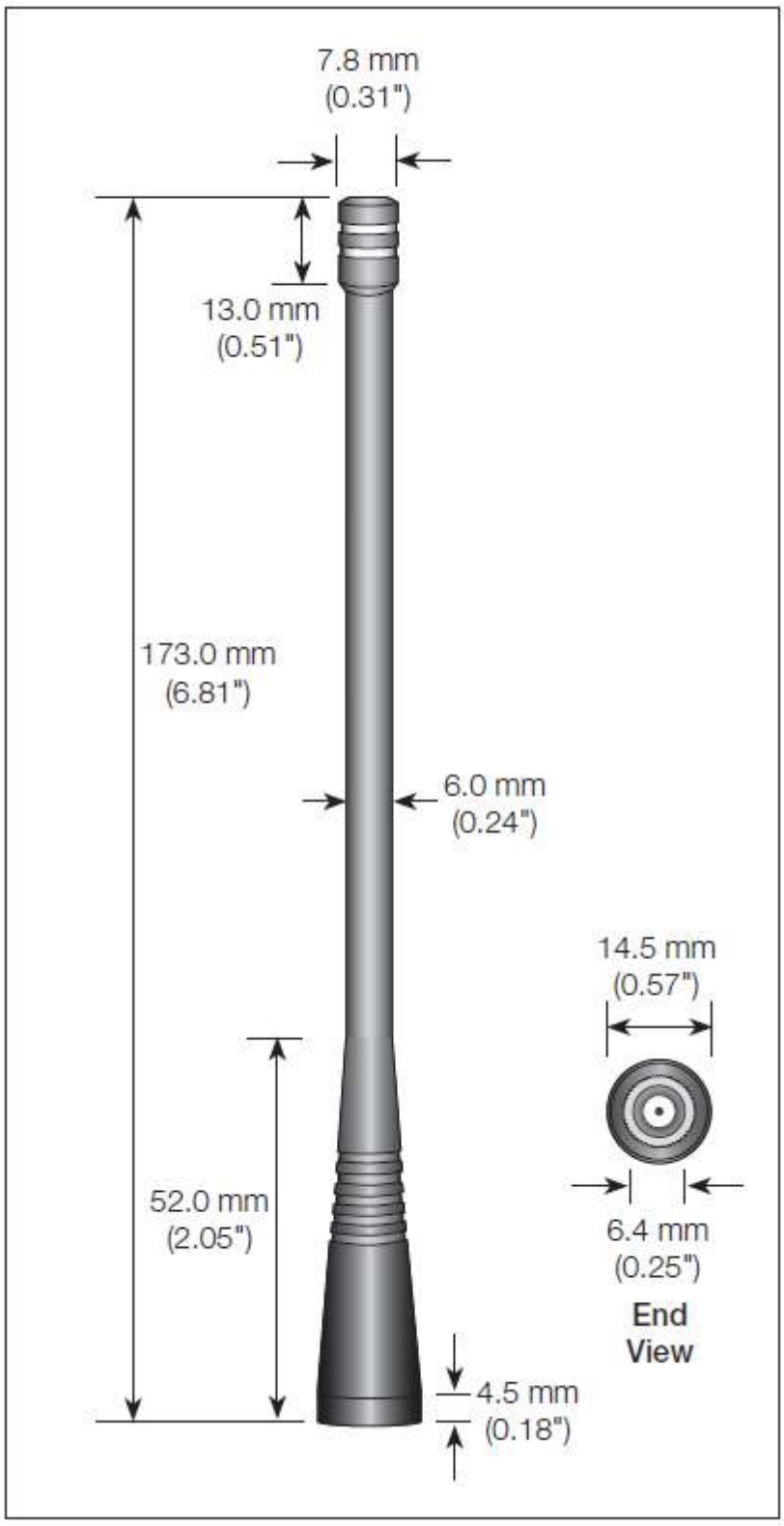
**Spécifications électriques**

Fréquence Centre: 868MHz
Recom. Fréq. Gamme: 750-950MHz
Wavelength: ¼ d'onde
Gain de crête: 1.6dBi
ROS: <1,9 typ. au centre
Impédance: 50 ohms
Connecteur: RP-SMA ou SMA
Oper. Temp. Plage: -40 ° C à + 90 ° C

les spécifications et les parcelles électriques mesurées sur 10,16 cm x 10,16 cm de plan de masse (4,00 "x 4,00") de référence

Informations de commande
ANT-868-CW-QW (avec connecteur RP-SMA)
ANT-868-CW-QW-SMA (avec connecteur SMA)

**Pour le module SPSGRF-433 l'antenne approuvée est le LINX ANT-433-CW-QW**



**Spécifications électriques**

Fréquence Centre: 433MHz
Recmd. Fréq. Gamme: 400-470MHz
Wavelength: ¼ d'onde
Gain de crête: 3.3dBi
ROS: <1,9 typ. au centre
Impédance: 50 ohms
Connecteur: RP-SMA ou SMA
Oper. Temp. Plage: -40 ° C à + 90 ° C

Caractéristiques électriques et les parcelles mesurées sur 10,16 cm x 10,16 cm (4,00 "x 4,00") plan de masse de référence

Informations de commande
ANT-433-CW-QW (avec connecteur RP-SMA)
ANT-433-CW-QW-SMA (avec connecteur SMA)

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