

532 SCHEMATICS

REV.: B.0

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P/N : 15-F56-010020
PCB M/B.532.V.B.318*173.8*1.6mm.6L YELLO



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Title

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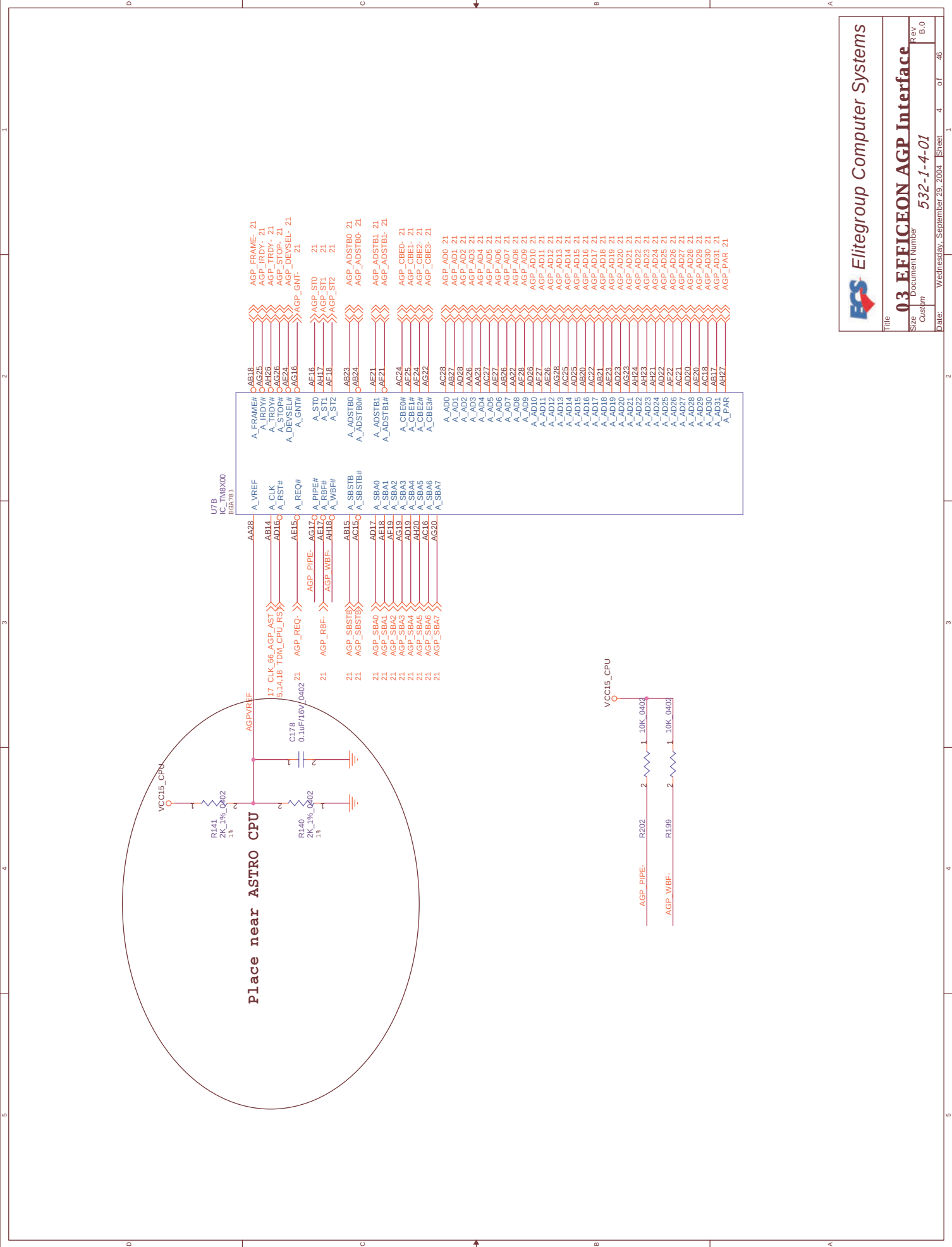
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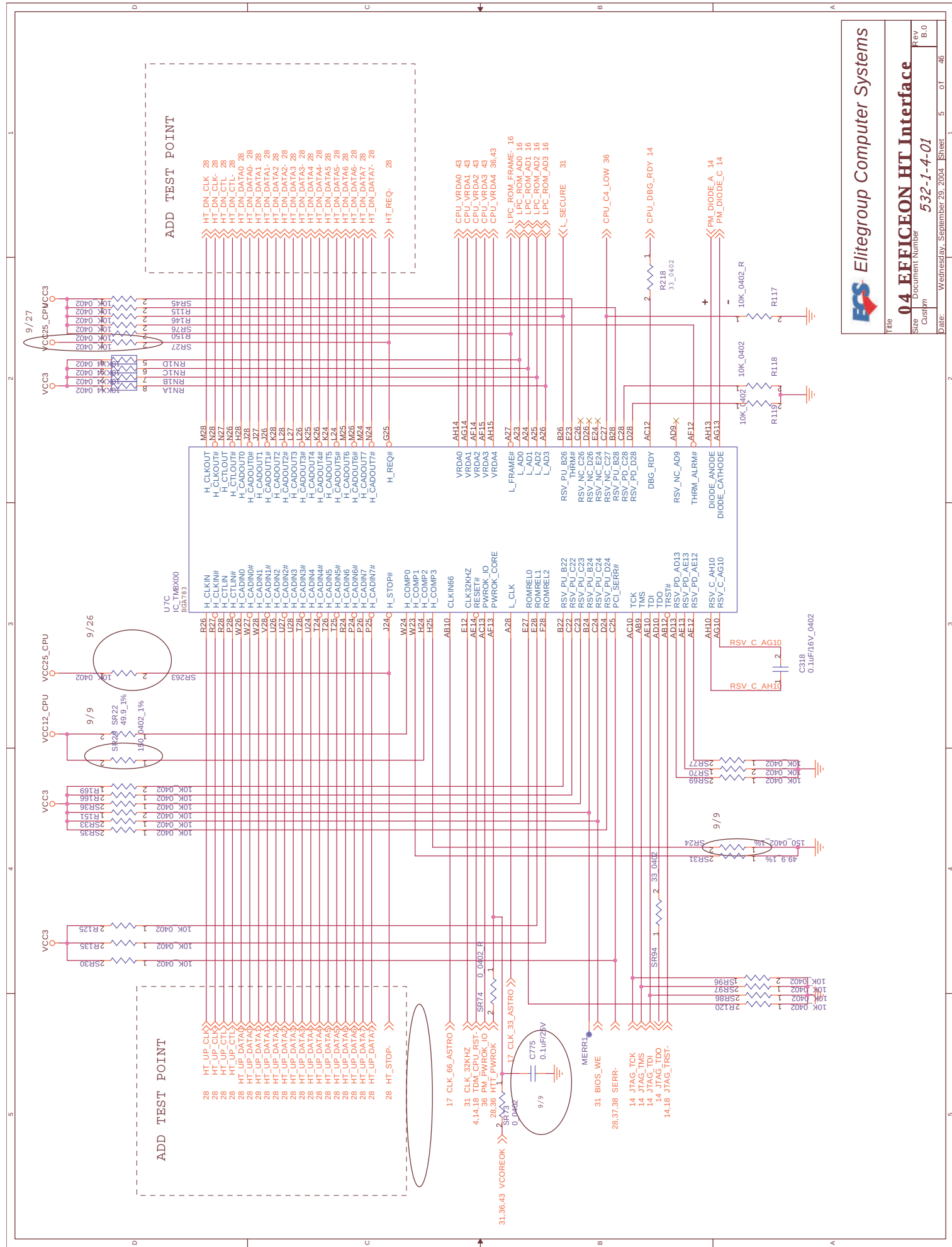
REVISION HISTORY

A.0 INITIAL RELEASE

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Revision History			
File			
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CH14A
200 SODIMM DDR

VCC_DIMM

QSI GA0115-20J0N01

DDR52_S

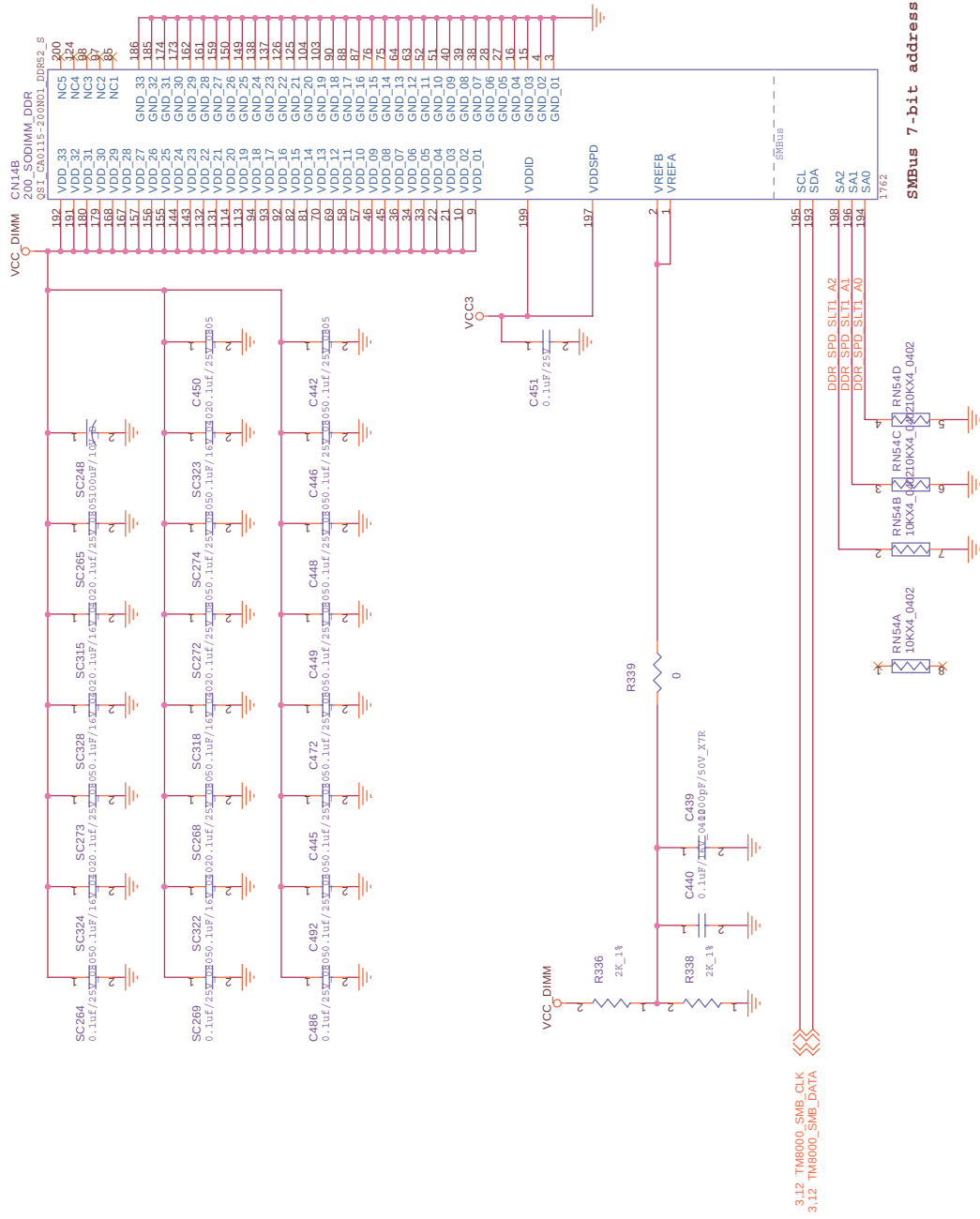
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3.13	DDR_CK0	95	CKE1	DQ_52	164	DDR_DQ52 3.11.13
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3.11.13	DDR_A10	123	A_13	DQ_49	182	DDR_DQ49 3.11.13
3.11.13	DDR_A10	99	A_12	DQ_48	163	DDR_DQ48 3.11.13
3.11.13	DDR_A10	100	A_11	DQ_47	154	DDR_DQ47 3.11.13
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3.11.13	DDR_A10	101	A_09	DQ_45	146	DDR_DQ45 3.11.13
3.11.13	DDR_A10	102	A_08	DQ_44	142	DDR_DQ44 3.11.13
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3.11.13	DDR_A10	106	A_06	DQ_42	145	DDR_DQ42 3.11.13
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3.11.13	DDR_A10	111	A_02	DQ_37	130	DDR_DQ37 3.11.13
3.11.13	DDR_A10	112	A_00	DQ_36	128	DDR_DQ36 3.11.13
3.11.13	DDR_BA0	116	BA1	DQ_35	135	DDR_DQ35 3.11.13
3.11.13	DDR_BA0	117	BA0	DQ_34	129	DDR_DQ34 3.11.13
3.13	DDR_CS0	122	S1#	DQ_33	127	DDR_DQ33 3.11.13
3.13	DDR_CS0	121	S1#	DQ_32	127	DDR_DQ32 3.11.13
3.11.13	DDR_RAS#	118	RAS#	DQ_31	68	DDR_DQ31 3.11.13
3.11.13	DDR_CAS#	120	CAS#	DQ_30	66	DDR_DQ30 3.11.13
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3.11.13	DDR_DM0	170	DM_6	DQ_27	65	DDR_DQ27 3.11.13
3.11.13	DDR_DM0	148	DM_5	DQ_26	59	DDR_DQ26 3.11.13
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3.11.13	DDR_DM0	169	DQS_6	DQ_18	43	DDR_DQ18 3.11.13
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3.11.13	DDR_DM0	11	DQS_0	DQ_05	8	DDR_DQ5 3.11.13
3.11.13	DDR_DM0	11	DQS_0	DQ_04	17	DDR_DQ4 3.11.13
3.11.13	DDR_DM0	11	DQS_0	DQ_03	13	DDR_DQ3 3.11.13
3.11.13	DDR_DM0	11	DQS_0	DQ_01	7	DDR_DQ1 3.11.13
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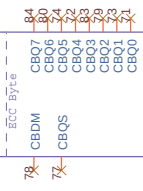
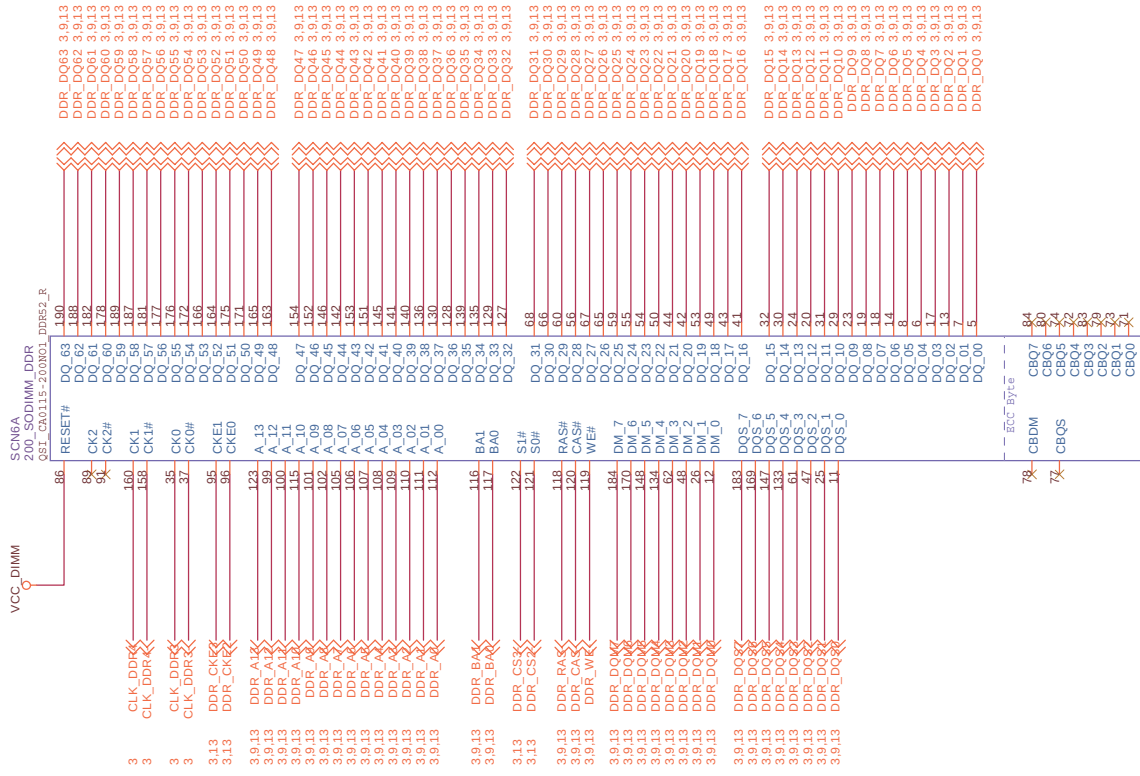
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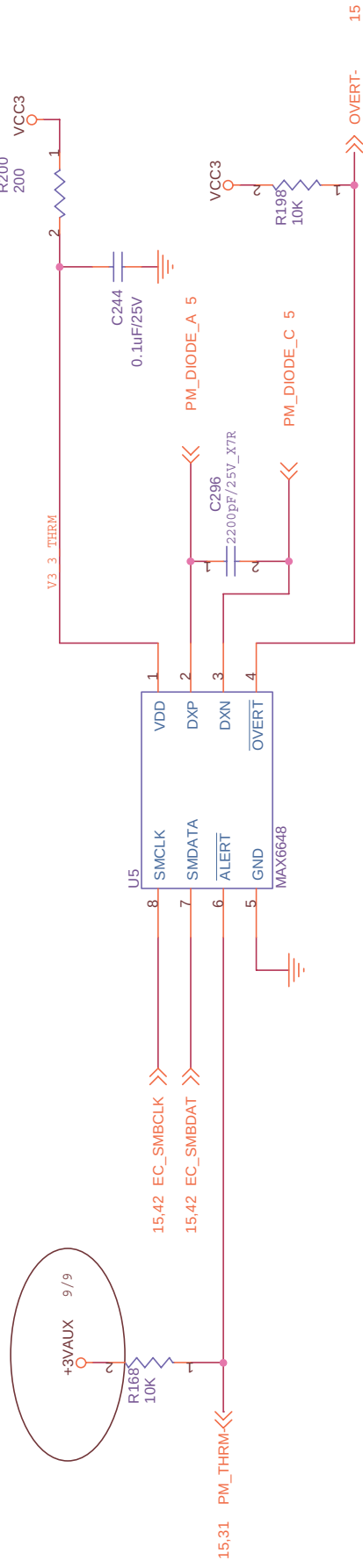
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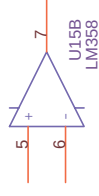
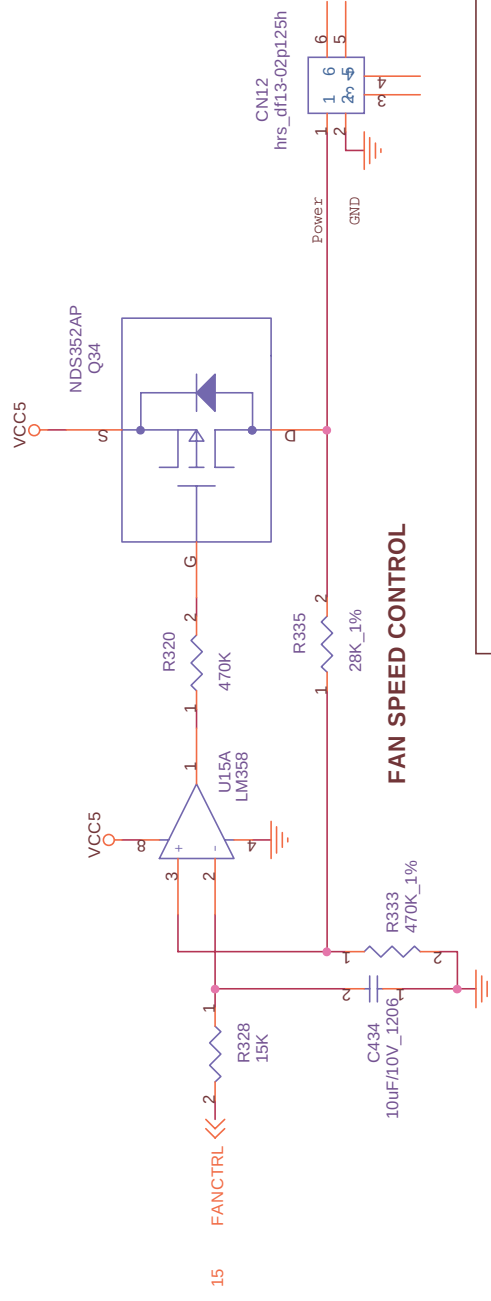
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08 DDR SO-DIMM 1 (1/2)			
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Place close to TM8600

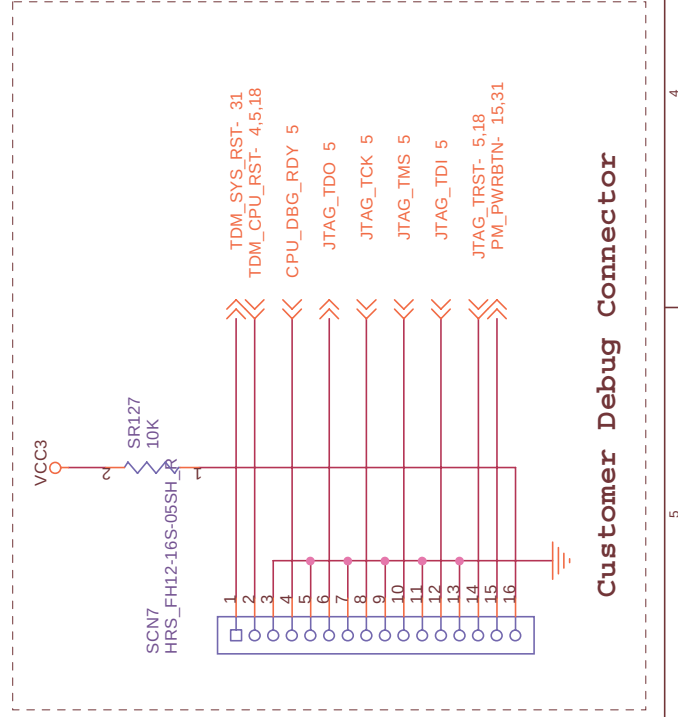


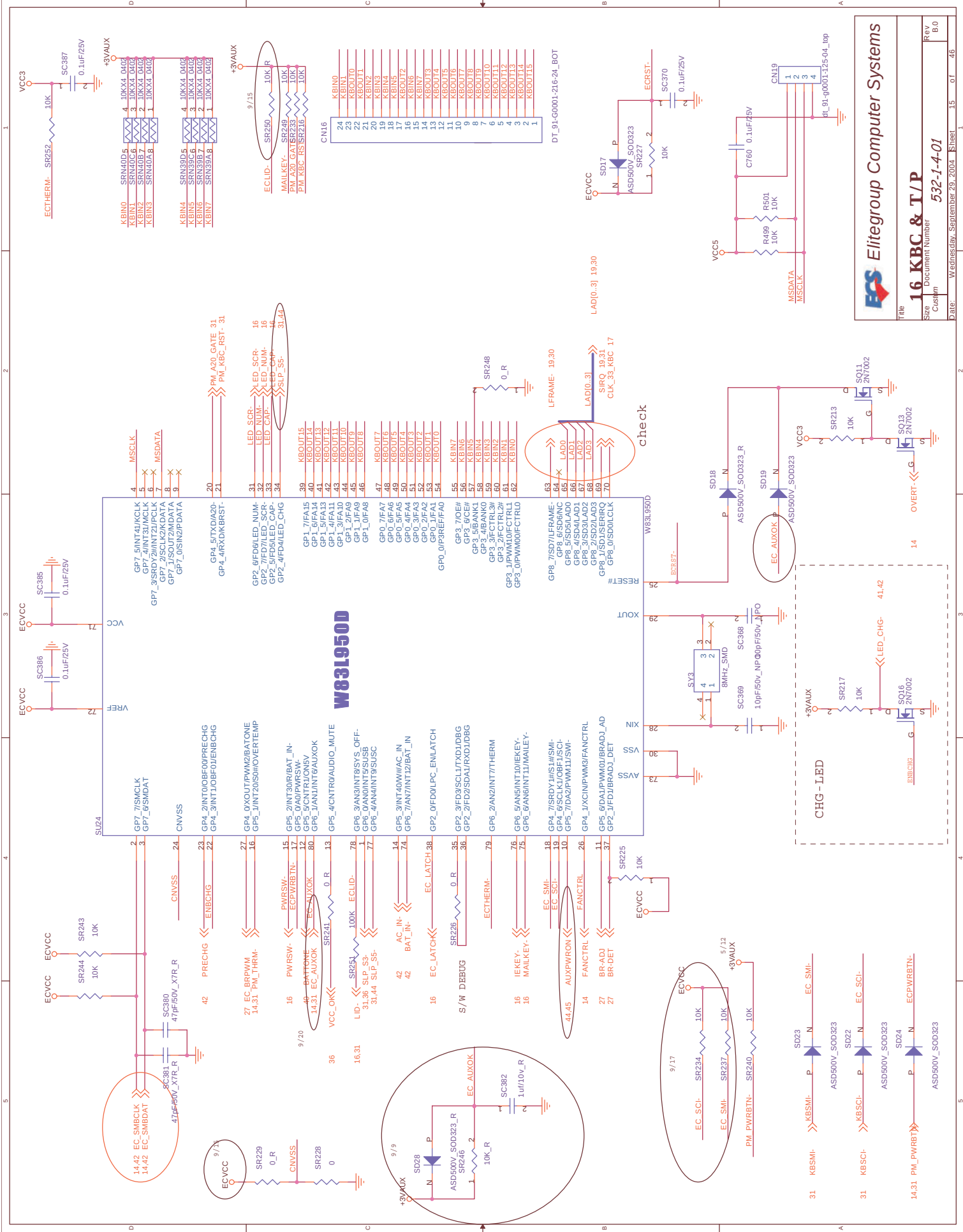
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Title
14 TDM-2 Conn & Thermal Sensor

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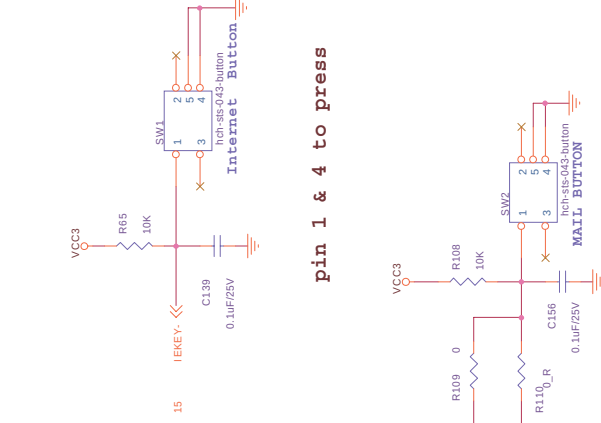
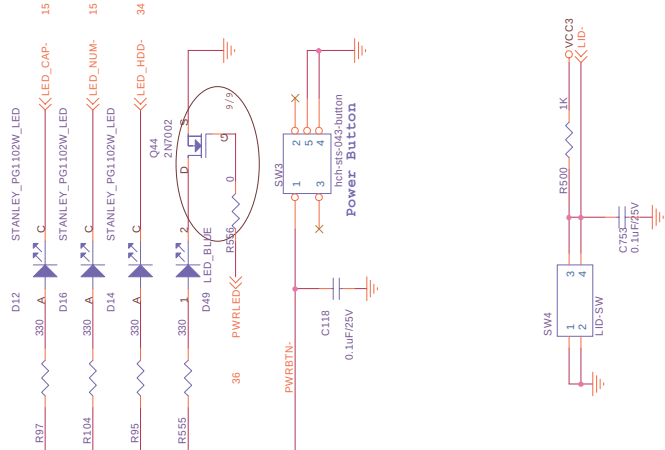
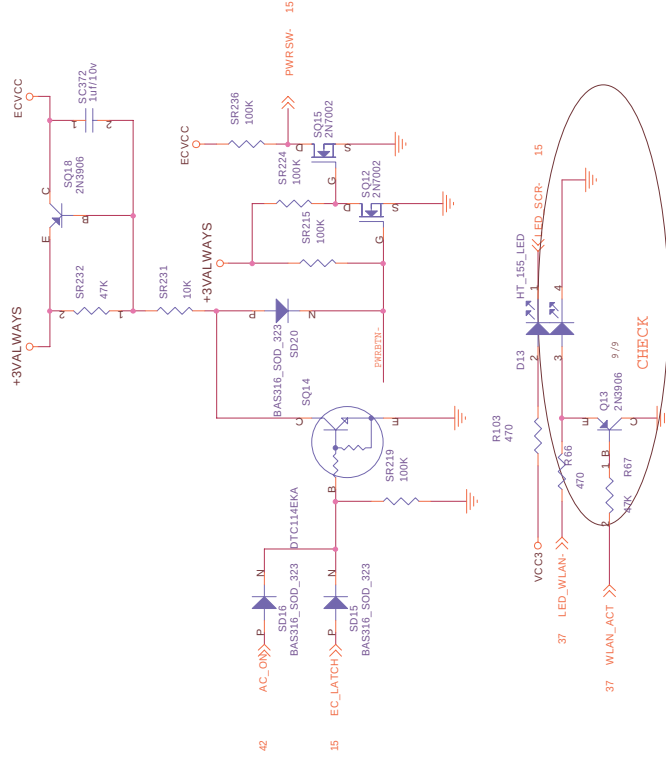




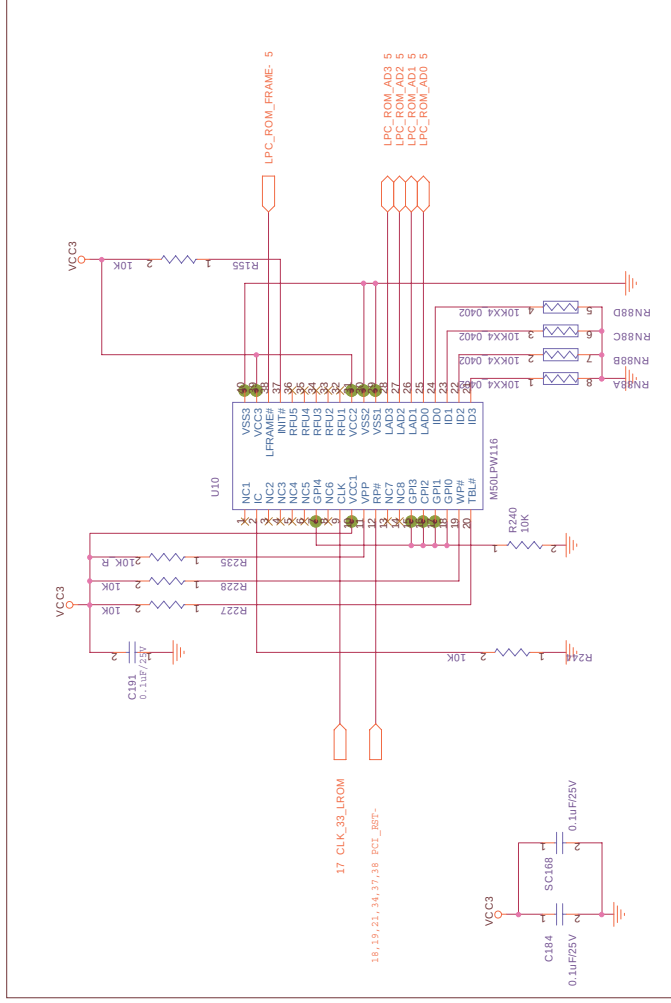
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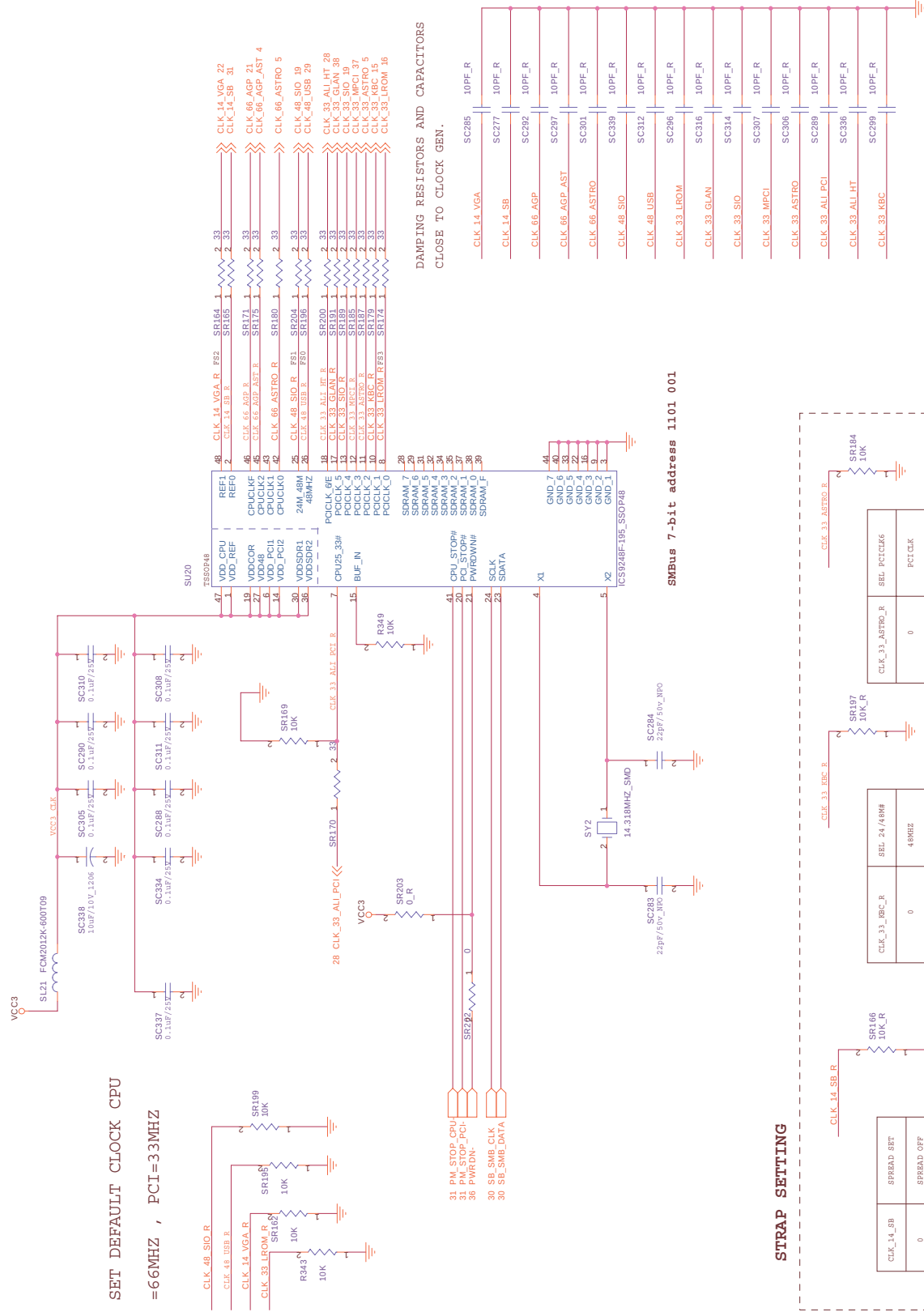
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EC LATCH CIRCUIT



pin 1 & 4 to press



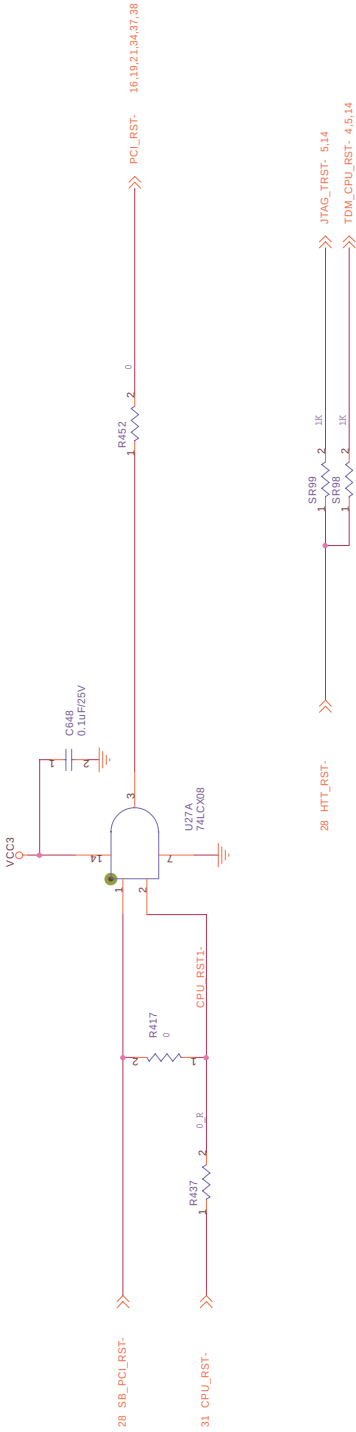


STRAP SETTING

CLK_14_SB	SPREAD SET
0	SPREAD OFF
1	SPREAD ON

CLK_33_KBC_R	SEL_24_48M#
0	48MHZ
1	24MHZ

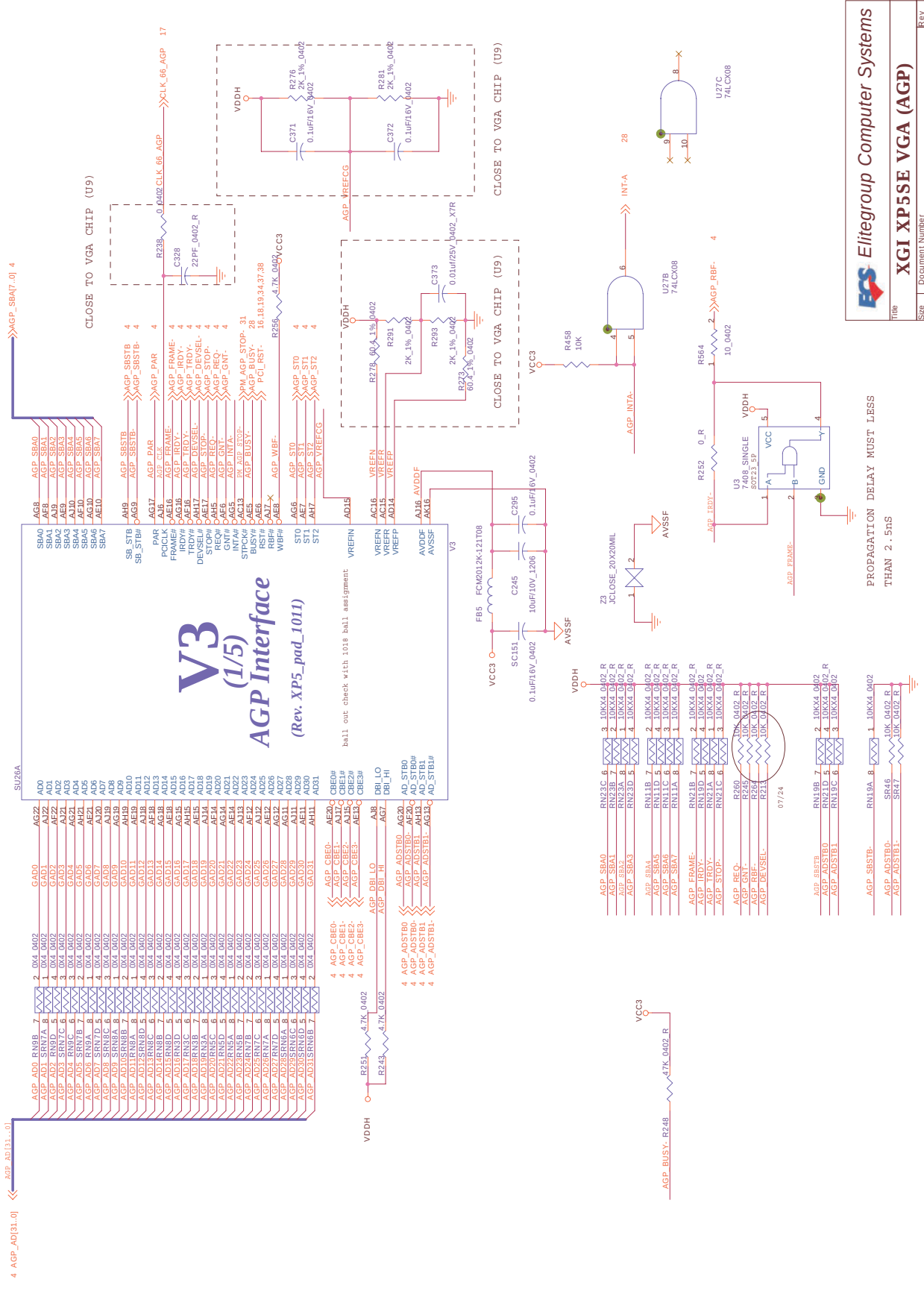
CLK_33_ASTRO_R	SEL PCICLK6
0	PCICLK
1	EARLY PCICLK





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Based on Volart V3 Dip Switch and Config.
Ver.2.0 Oct 03

PANEL ID

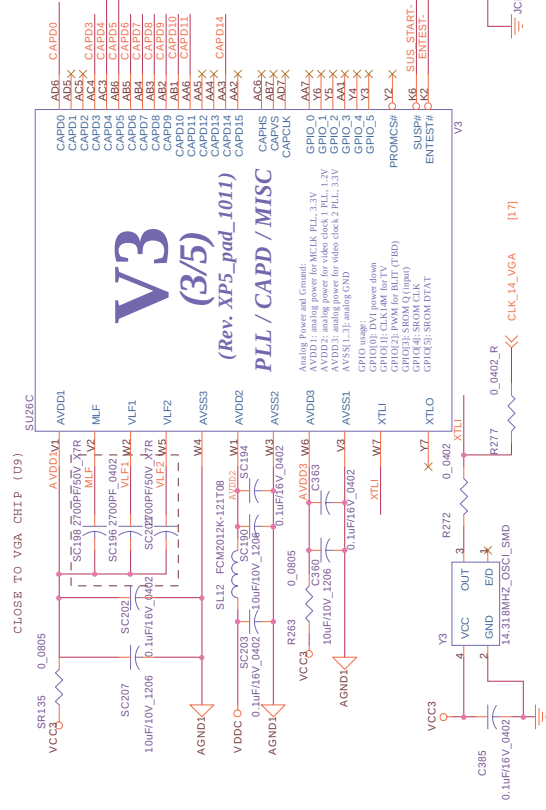
CAPD [11...9]

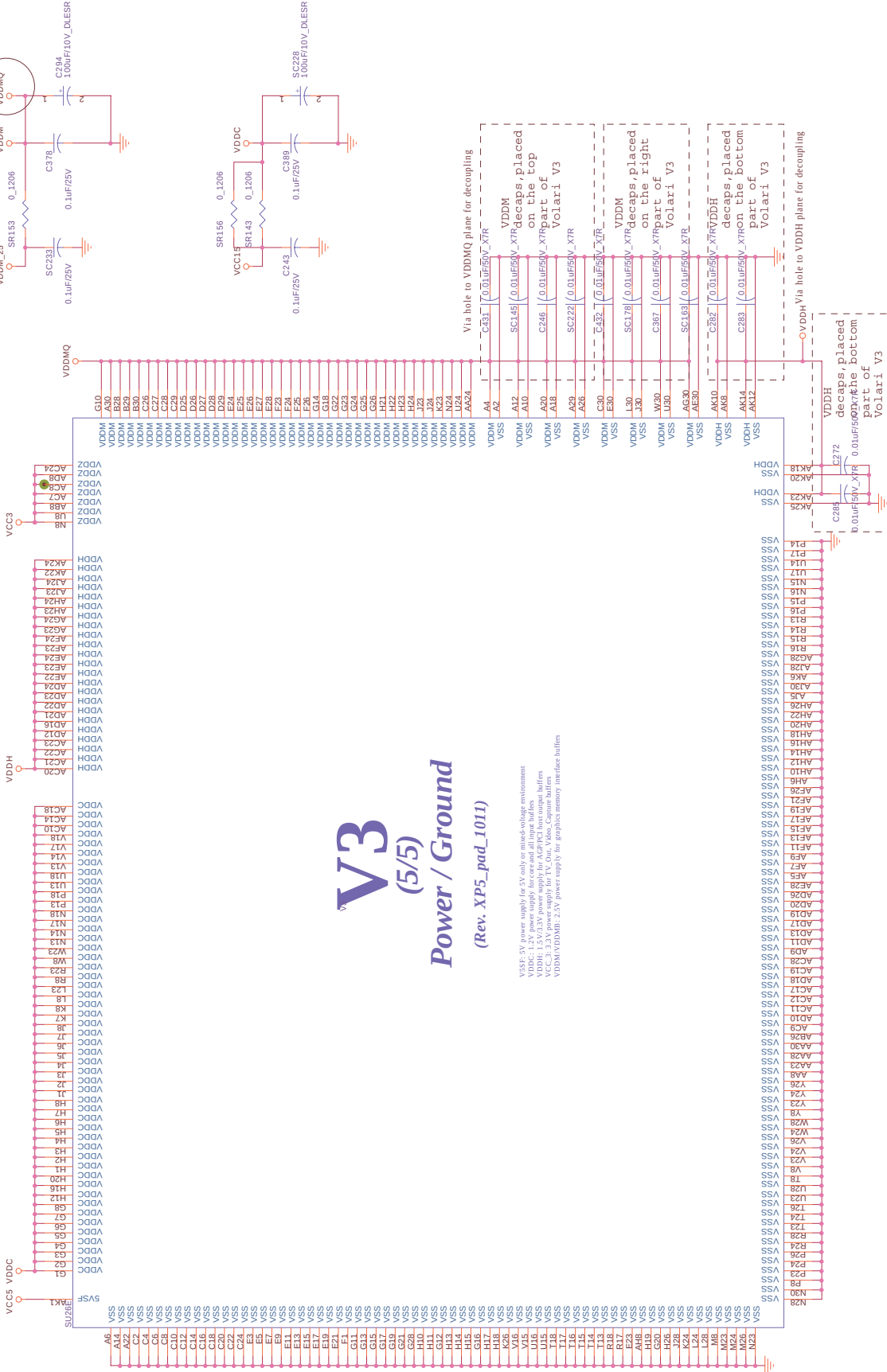
SYNC	PANEL TYPE
000	230MHz
001	125MHz
010	166MHz
011	215MHz
100	200MHz
101	250MHz
110	275MHz
111	300MHz

PANTID [1...01 : (CAPD [5...4])	PANEL TYPE
00	RESERVED
01	TFT 1024x768 - 18 QDII
10	TFT 1024x768 - 18
11	RESERVED

Configuration Table:

CAPD	FUNCTION	Config(Stuff R4.7K=0)	Default
0	CLOCK MODE	0: External, 1: Internal	1: Internal
1	BUS TYPE	0: RESERVED, 1: AGP	1: AGP
2	ID SELECT	0: AD17, 1: AD16	1: AD16
3	BIOS	0: Disable, 1: Enable	0: Disable
5,4	PANEL ID TYPE	See Panel Type Table	
6	RESERVED		
8	LCD ON/OFF	0: OFF, 1: ON	1: LCD ON
11,9	MEMORY CLOCK	See Table	100: 200MHz
12	VDDQ VOLTAGE	0: 3.3V, 1: 1.5V	1: 1.5V
13	DDR/SDR SELECT	0: SDR, 1: DDR	1: DDR
7	VIDEO RAM TYPE	0: 2MX32, 1: 4MX32	1: 4MX32
15	AGP Version	0: AGP 3.0, 1: AGP 2.0	1: AGP 2.0



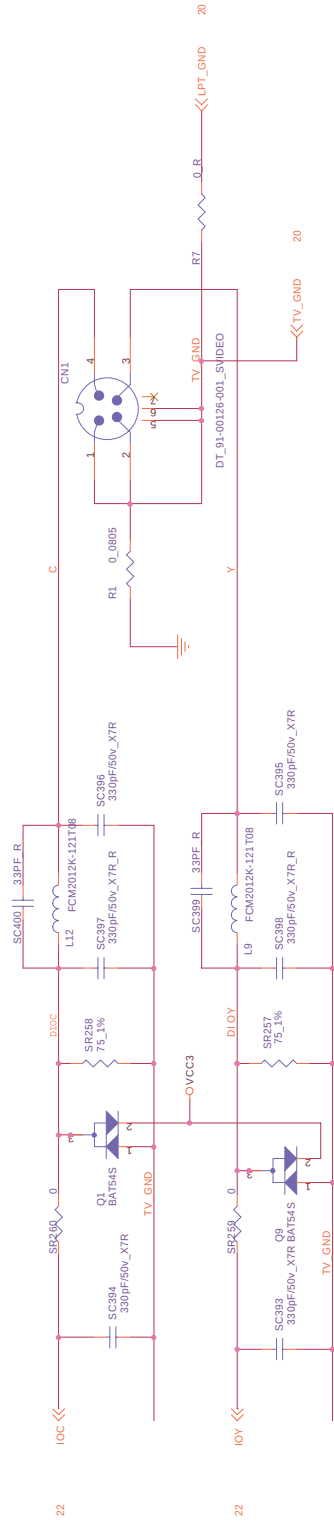
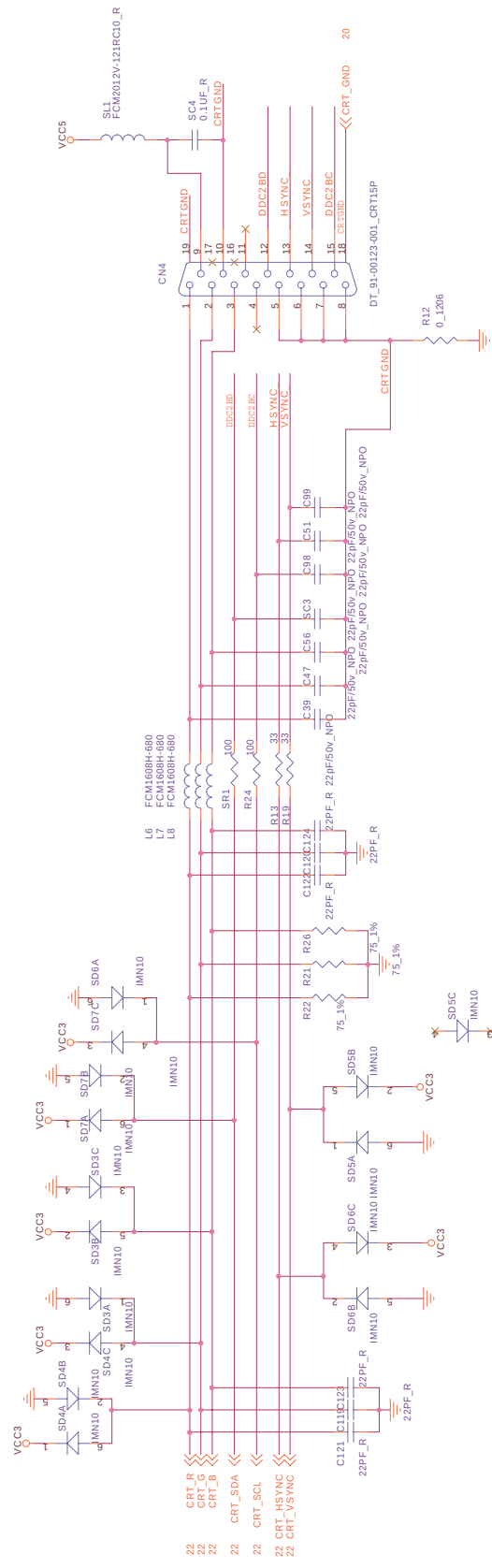


VDDH: 0V power supply for CPU and on-board voltage environment
VDDM: 1.2V power supply for core and all logic buffers
VDDH: 1.5V/1.3V power supply for AGP/PCI host output buffers
VDDH: 1.5V/1.3V power supply for TV-Out, Video Capture buffers
VDDM/VDDH: 2.5V power supply for graphics memory interface buffers

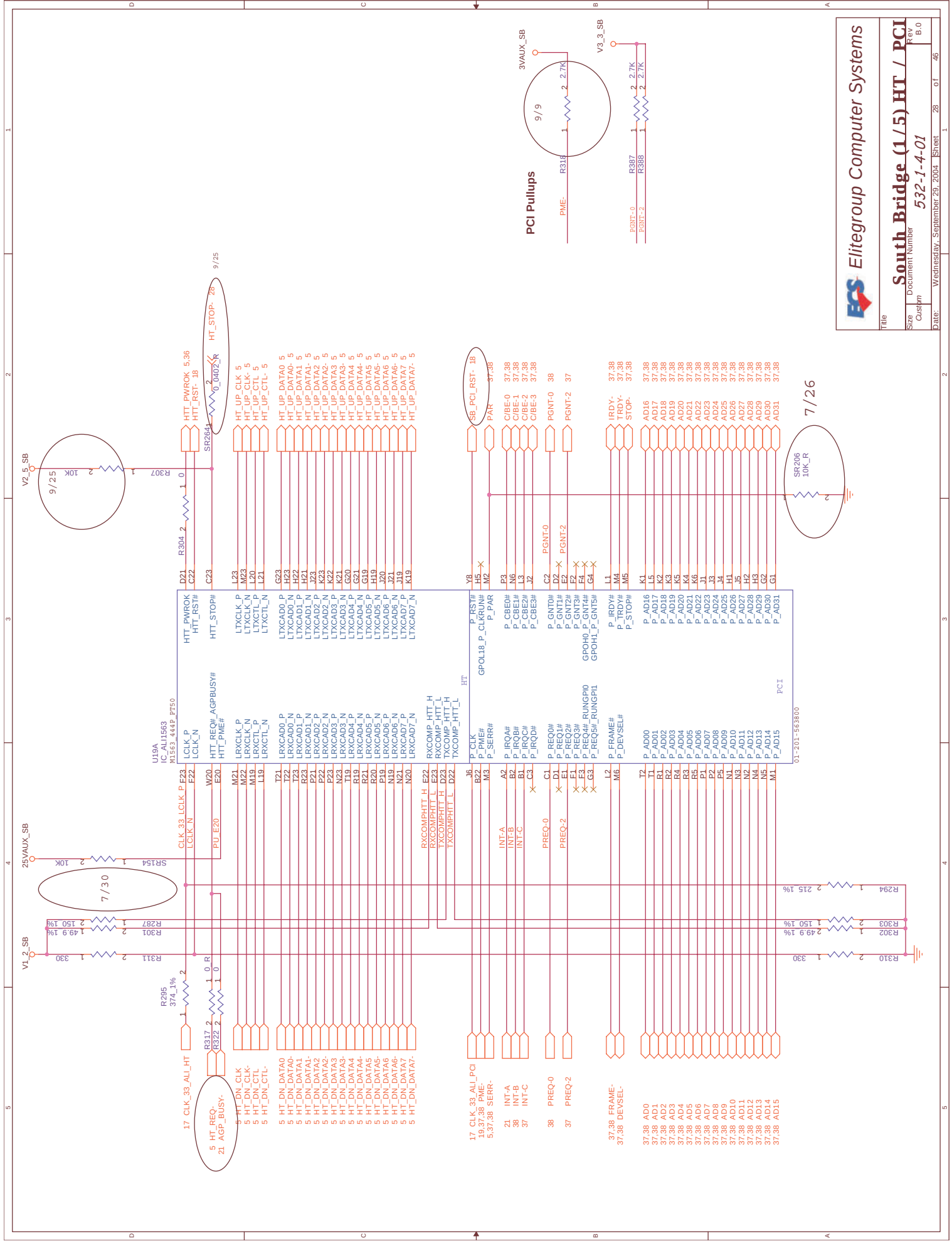


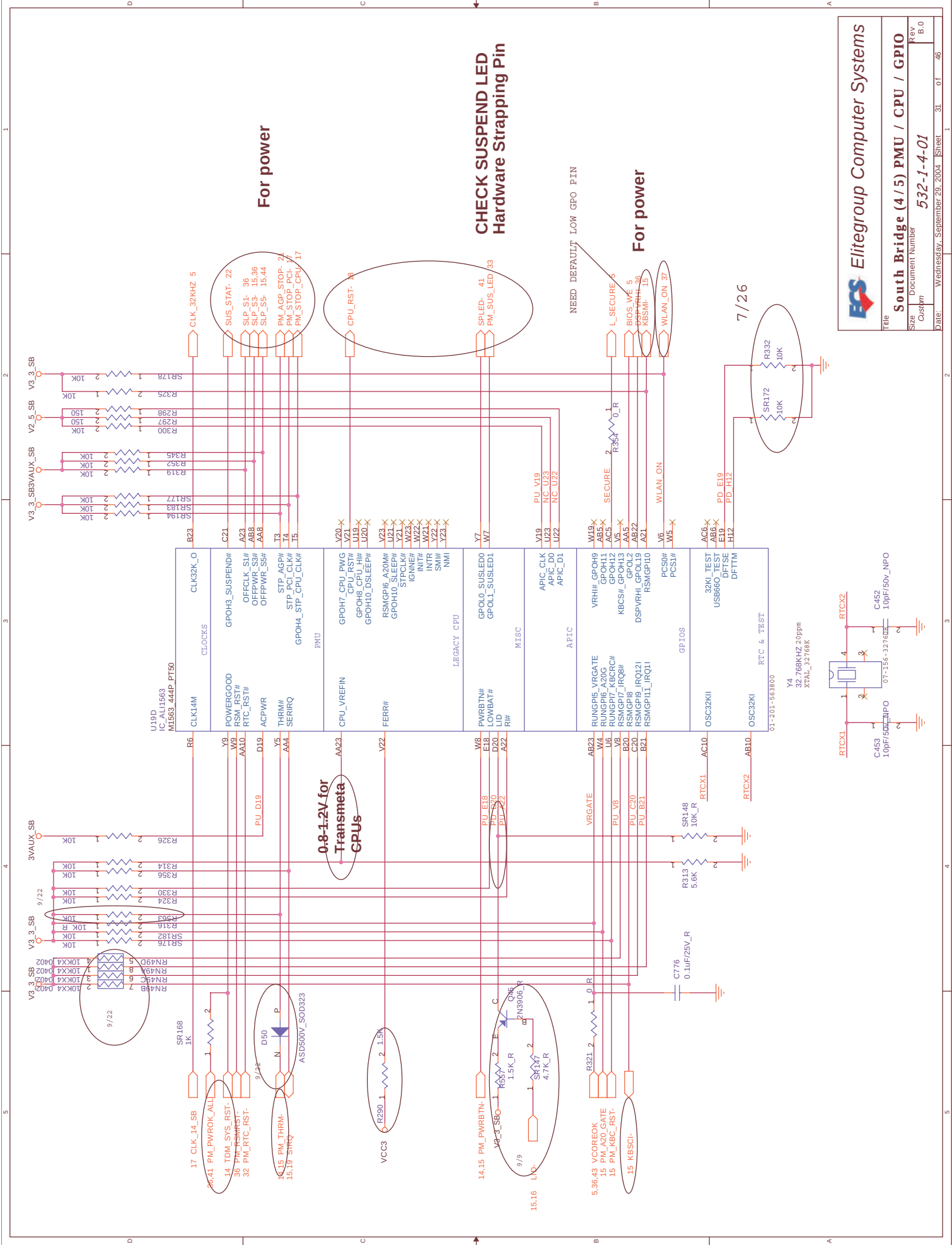
24	MAA[0..12]	24	CSA0	24	MCK0
24	DMA[0..7]	24	CSA0	24	MCK0

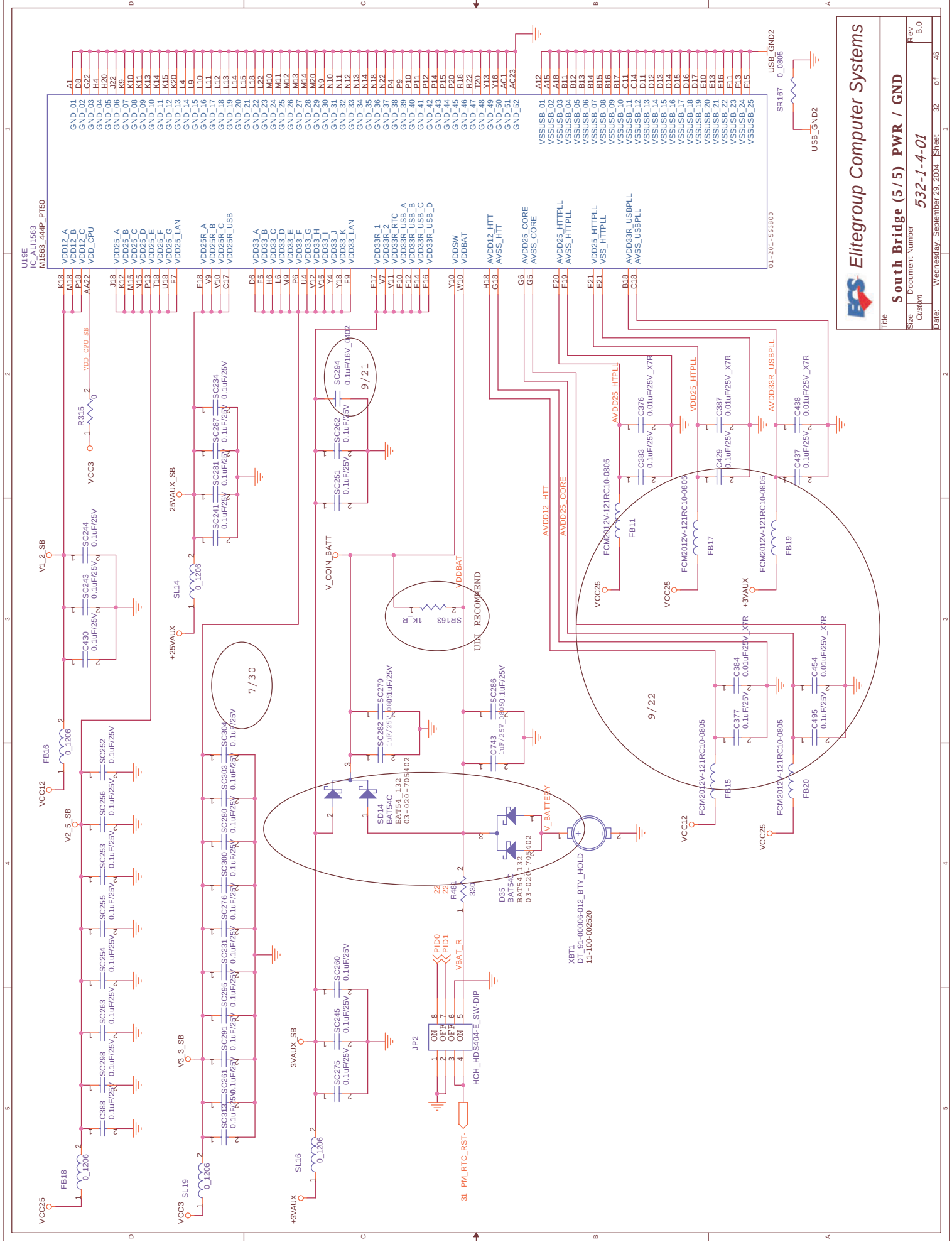




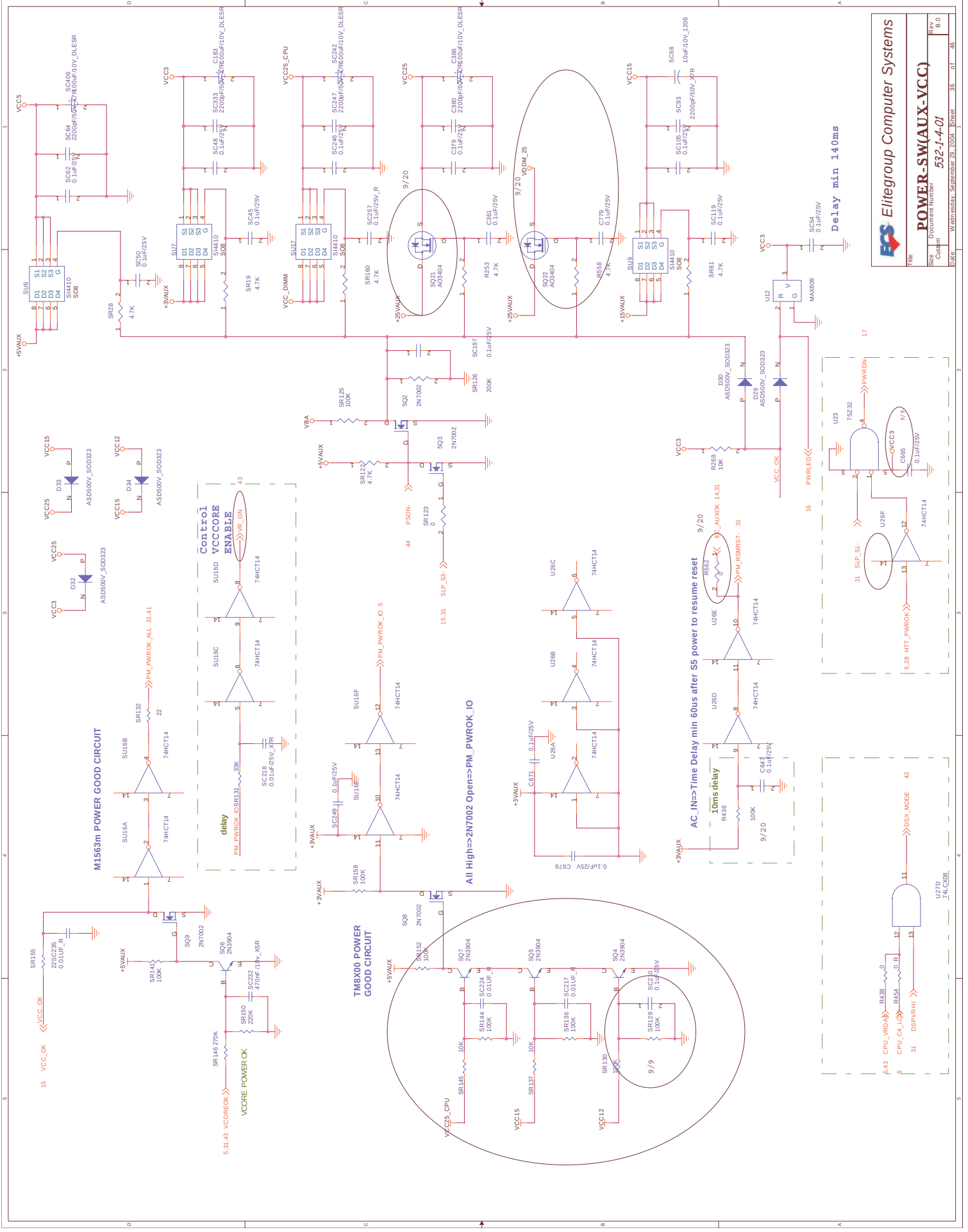


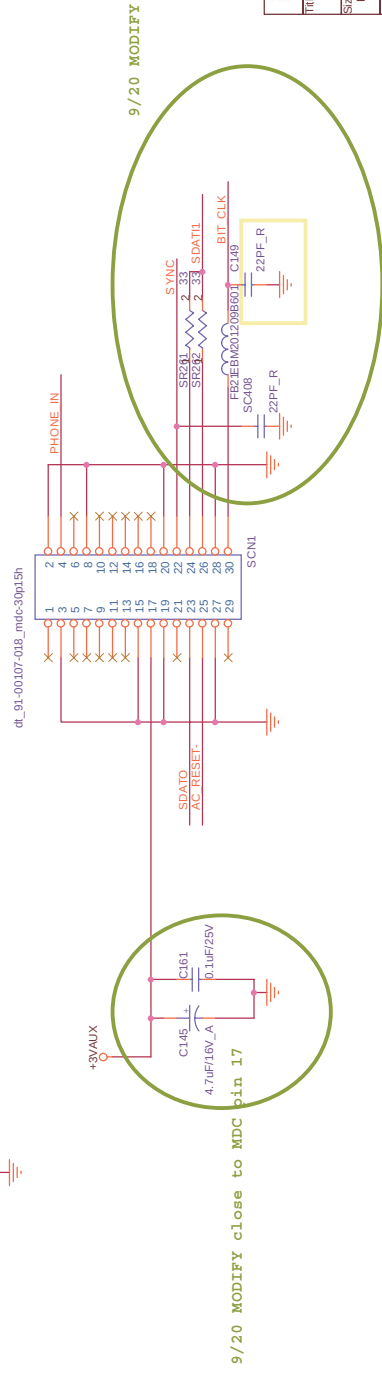
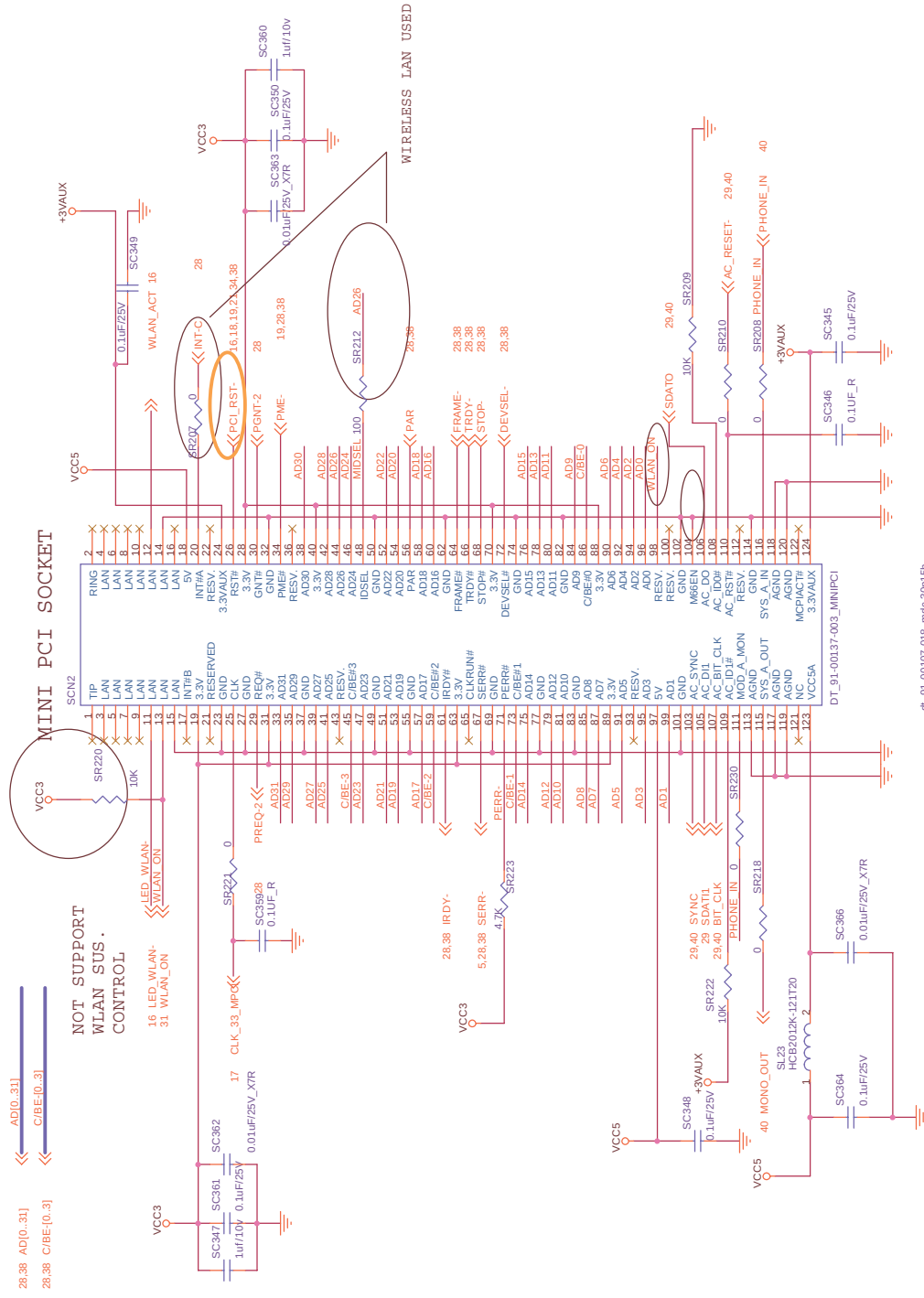


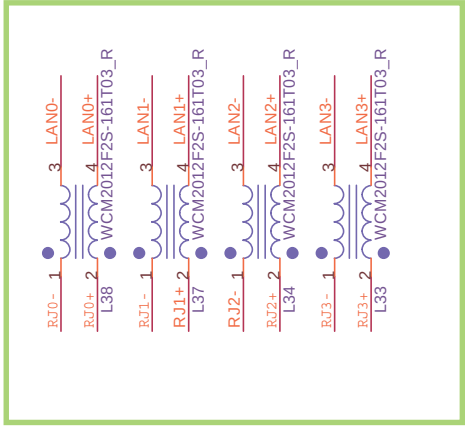
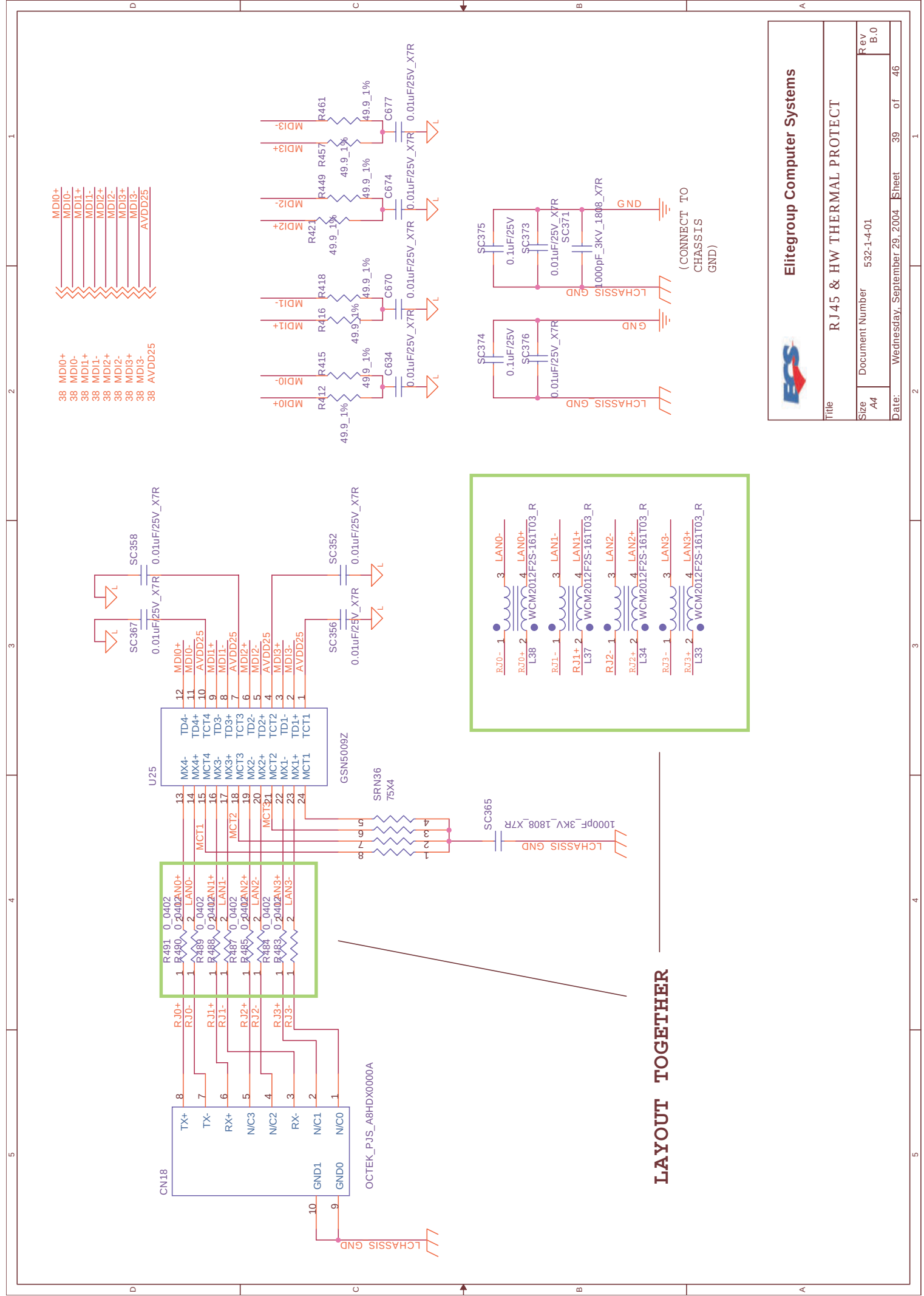




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D					C		B		A			

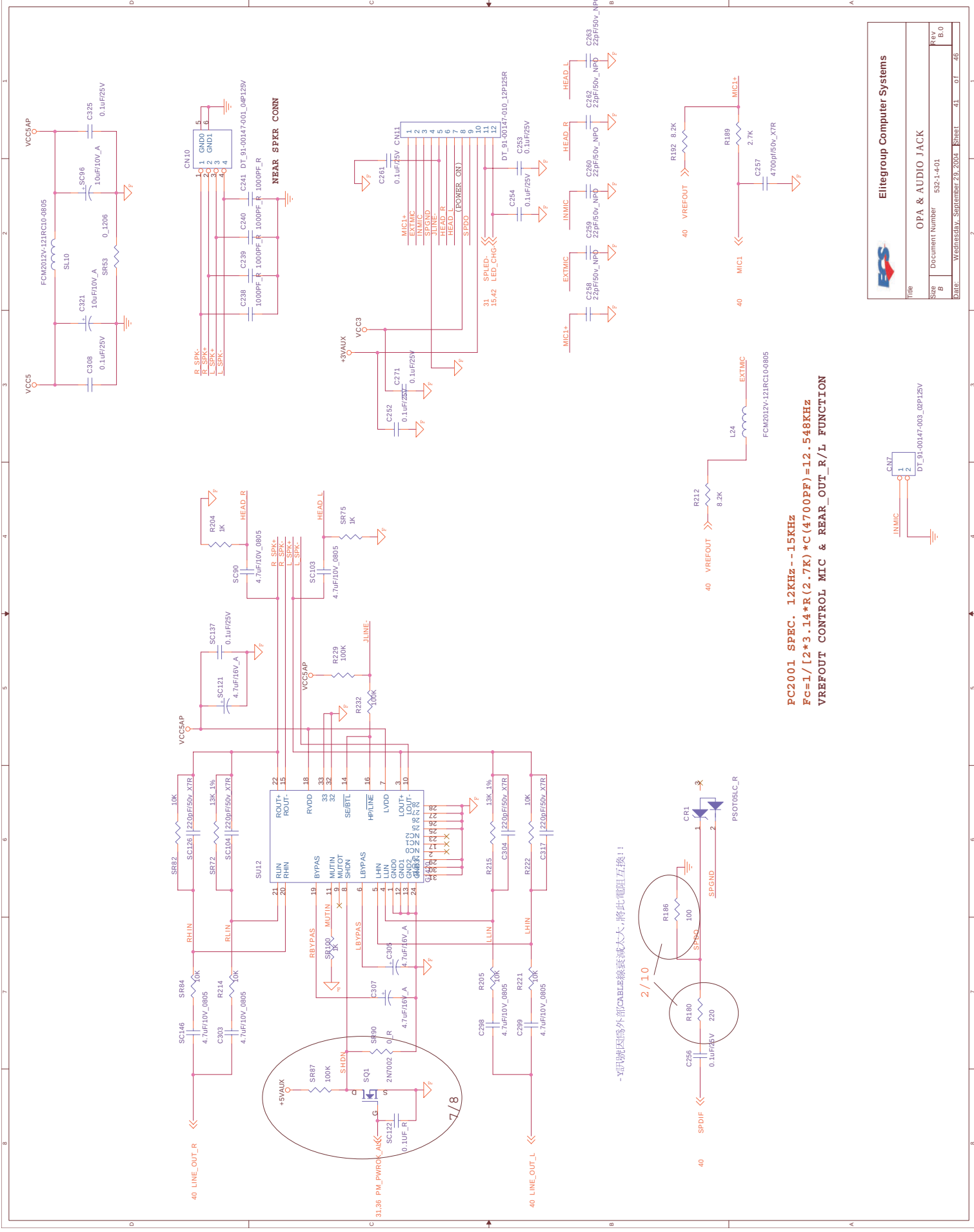






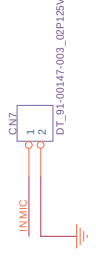
LAYOUT TOGETHER



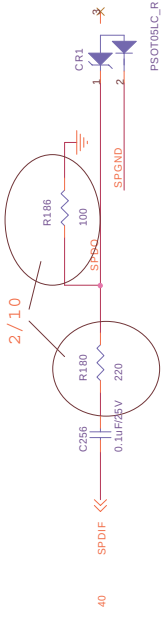


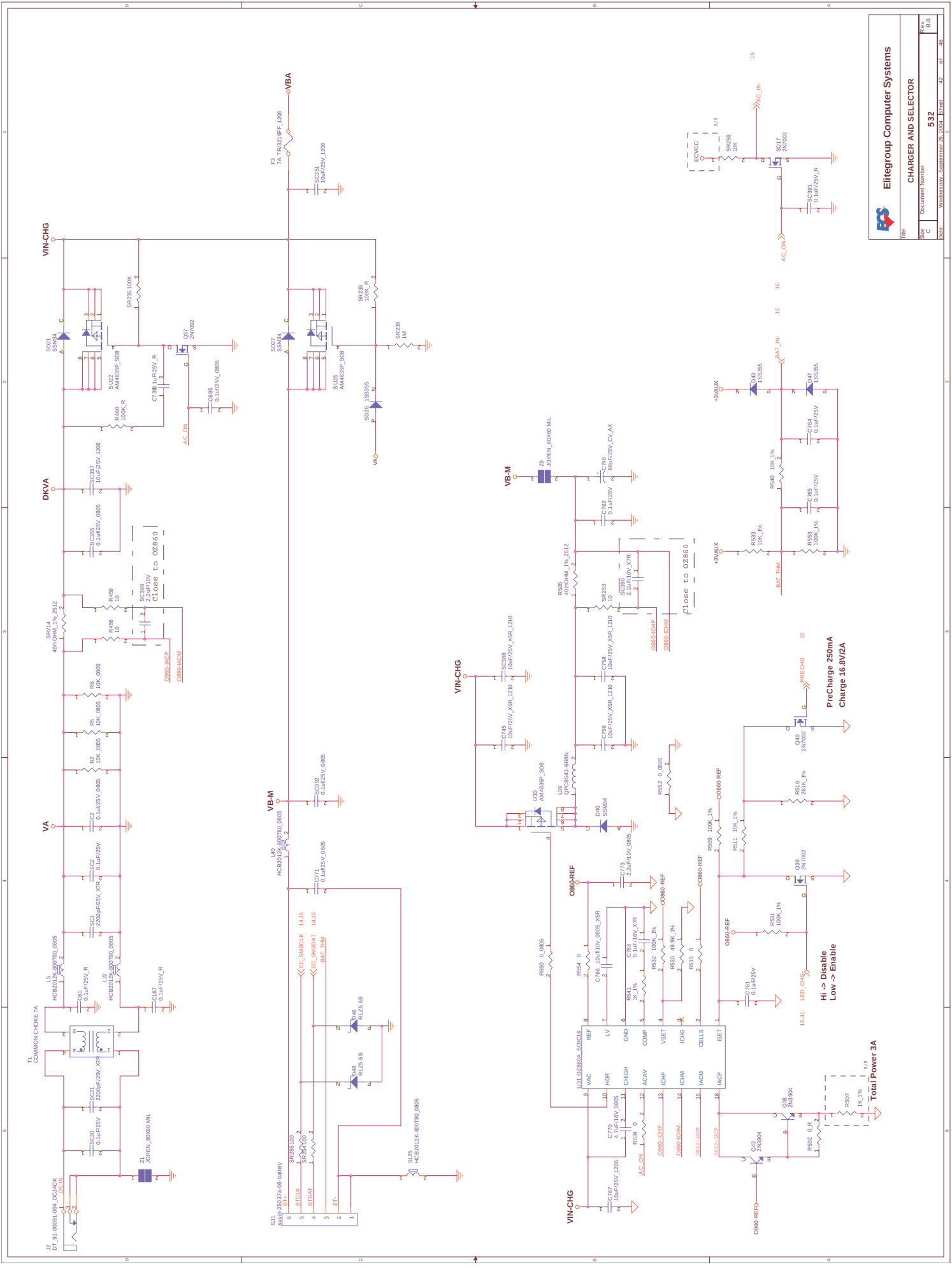
PC2001 SPEC. 12KHz--15KHz
 $F_c=1/[2*3.14*R(2.7K)*C(4700PF)]=12.548KHz$
VREFOUT CONTROL MIC & REAR_OUT_R/L FUNCTION

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Title OPA & AUDIO JACK			
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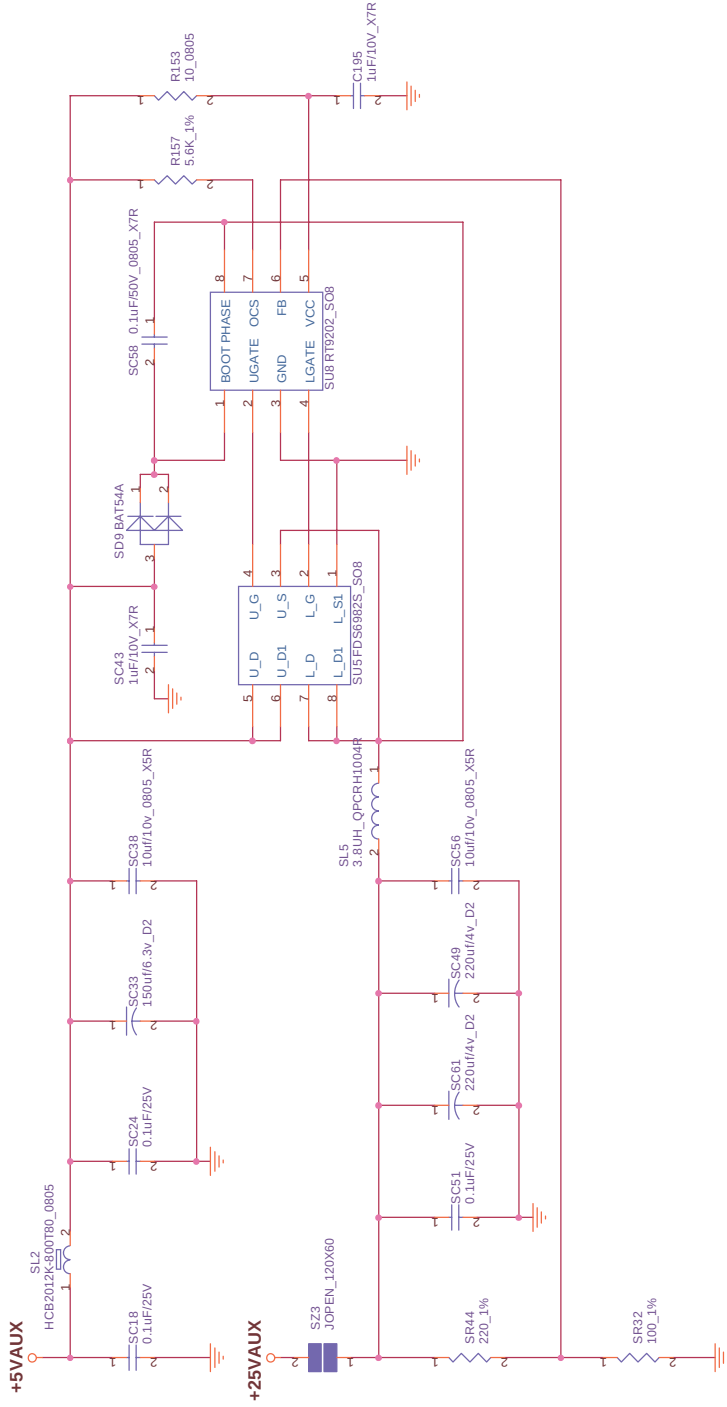
-VREFOUT因為外部CABLE線衰減太大,將此電阻互換!











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