

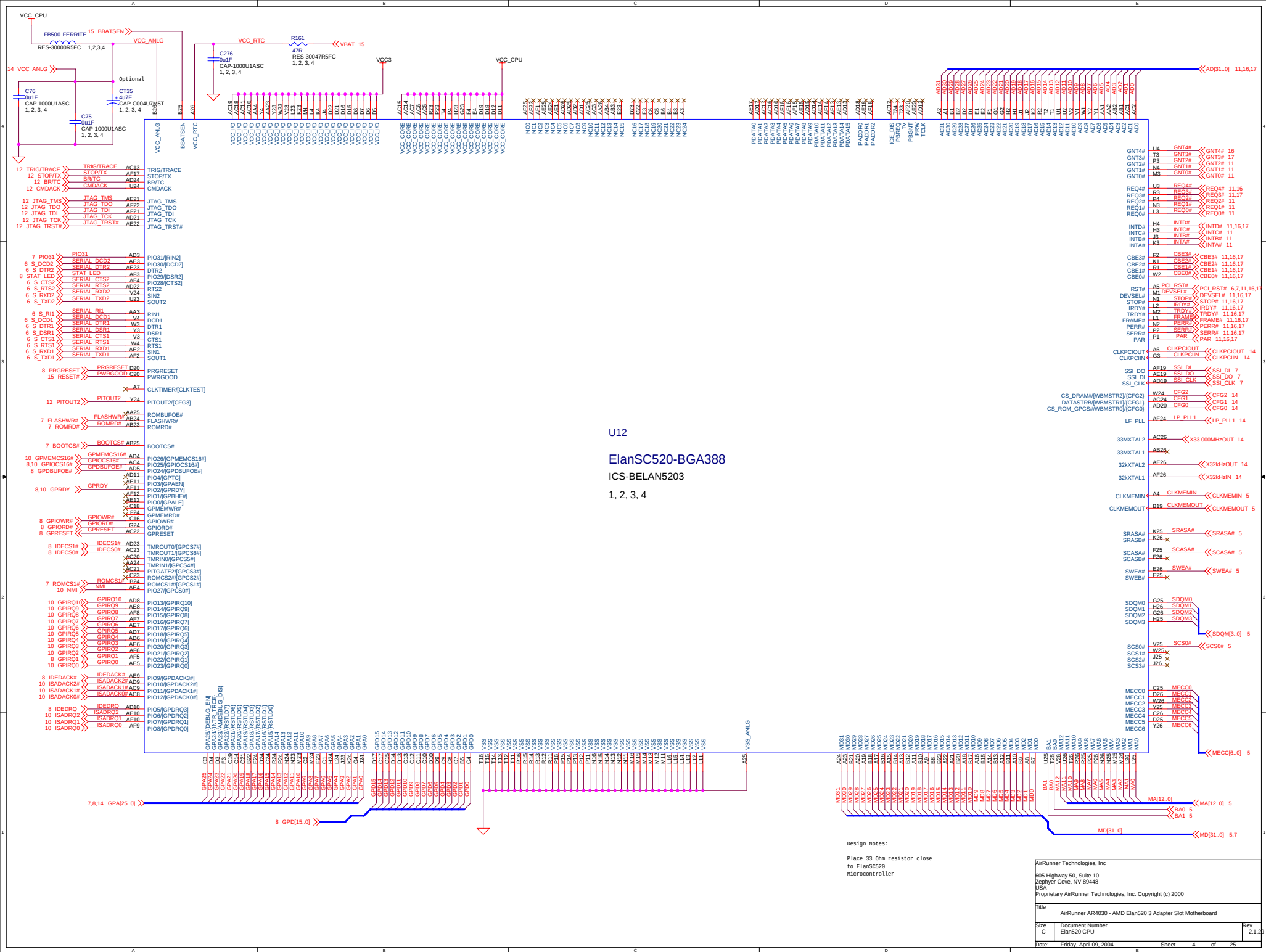
The logo for AirRunner Technologies features the word "Air" in a yellow sans-serif font, followed by "Runner" in a dark blue sans-serif font. A dark blue curved line arches over the word "Runner". Below "Runner" is the word "TECHNOLOGIES" in a smaller, dark blue, all-caps sans-serif font.

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AirRunner AR4030 - AMD Elan520 3 Adapter Slot Motherboard				
Size	Document Number			Rev
Customer	Revision History			2.1.29
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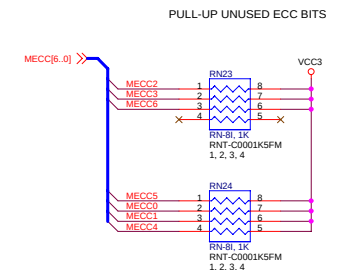
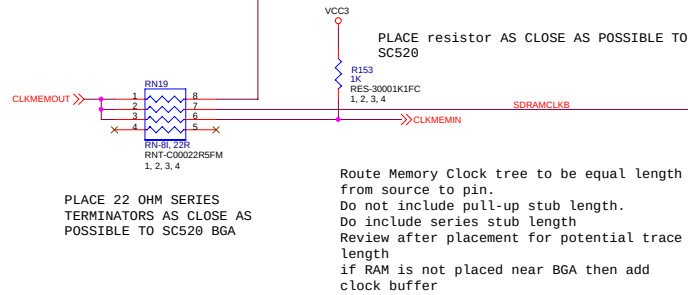
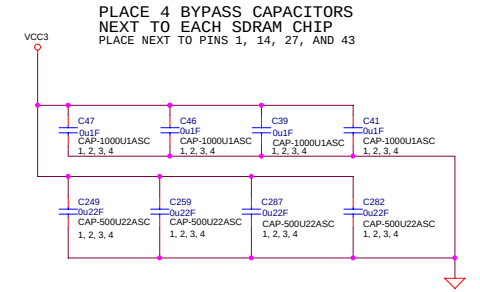
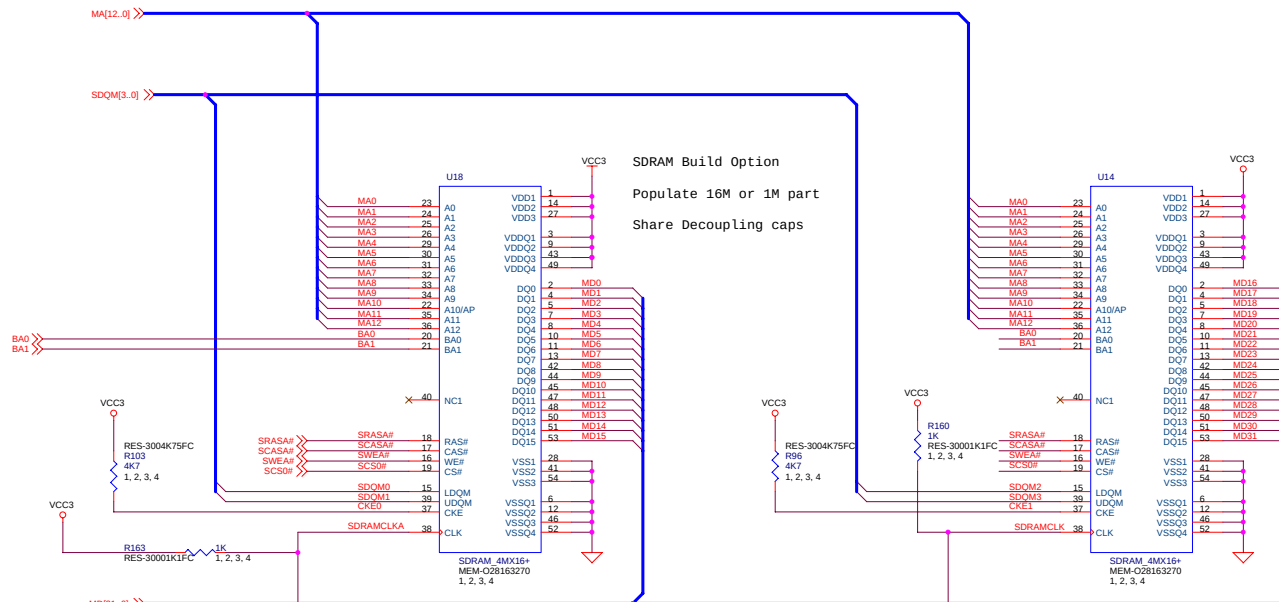
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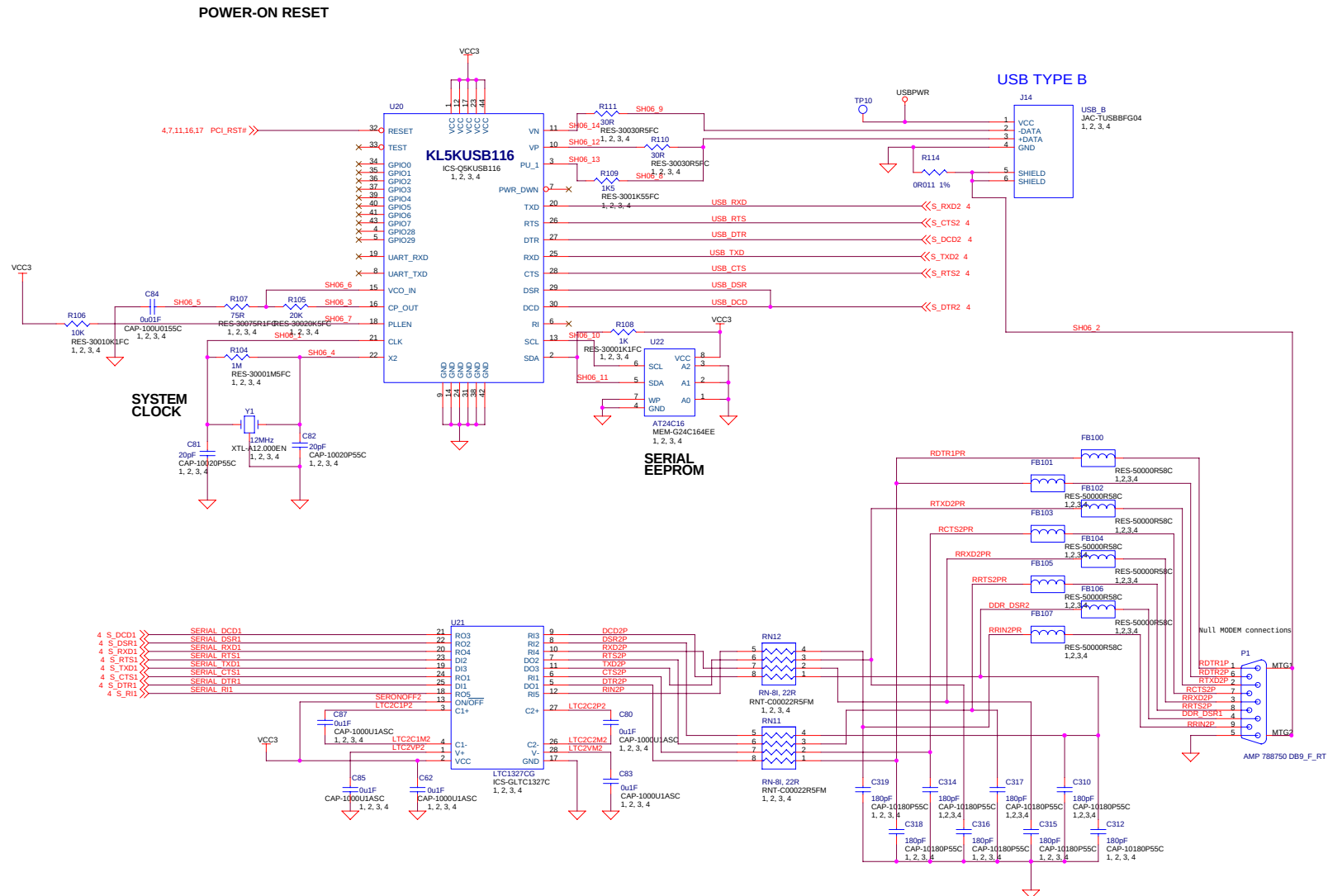
SDRAM MAIN MEMORY INTERFACE



16/32 SDRAM POPULATION OPTIONS

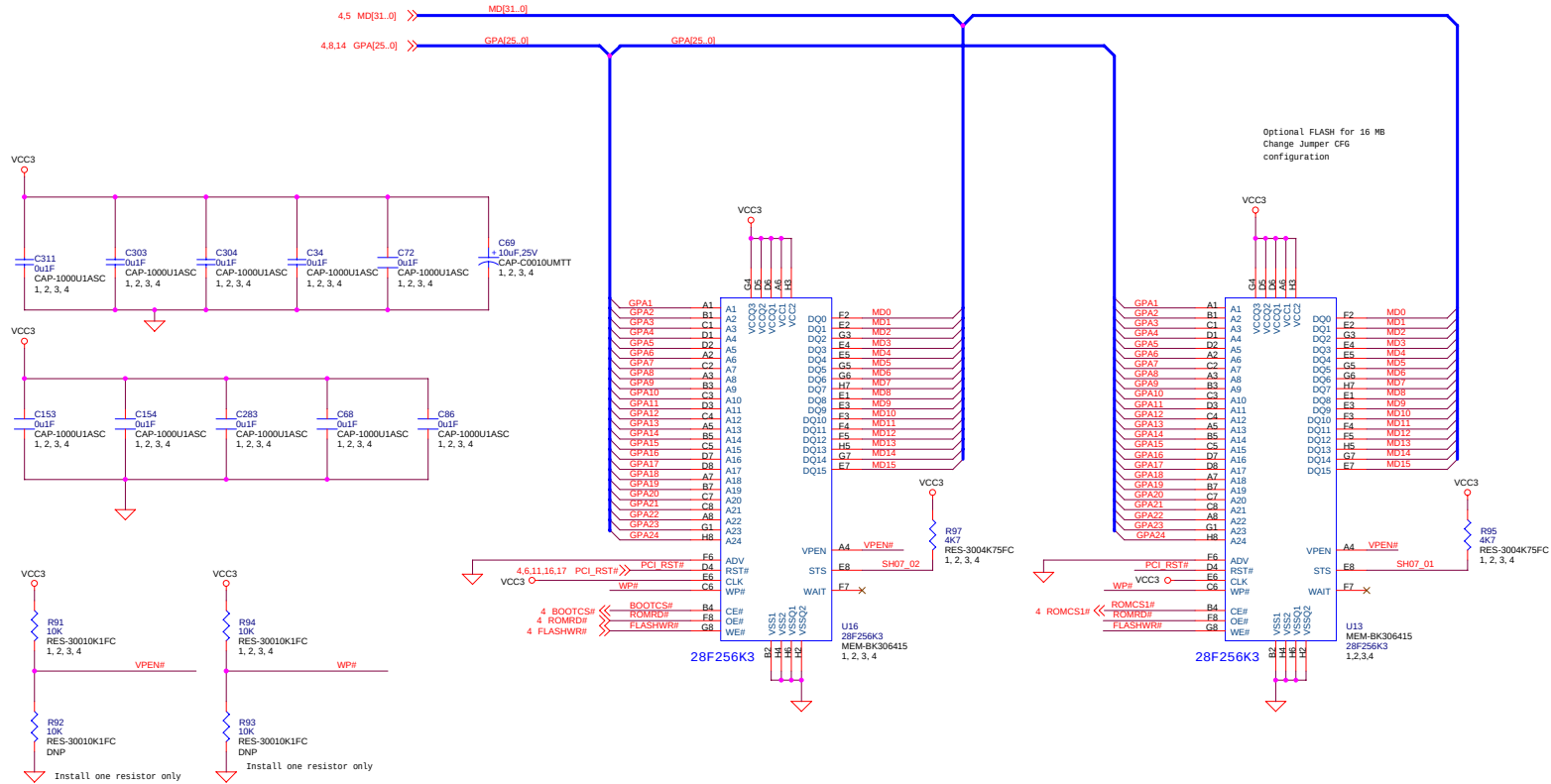
16MBYTE SDRAM	4MX16: SAMSUNG K4S641632C
32MBYTE SDRAM	8MX16: SAMSUNG K4S281632D

Serial & Serial to USB Ports (RS-232 & USB)



Execute in Place Flash Memory (8/16/32 MByte)

Note: FLASH is located on the SDRAM BUS



1Kbit Serial EEPROM (64x16)

Synchronous Serial Interface--Microwire SEEPROM

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IDE CONTROL CPLD

The schematic diagram illustrates the internal structure of the IDE Control CPLD. It features a central logic block with various inputs and outputs. The logic is implemented in Verilog, with signals like `pgreset`, `ided7rdrn`, `ided7wrn`, `idehoen`, `ideloen`, and `rstdrvna`. The diagram also shows the physical layout of the CPLD, including pins, pads, and connections to the JTAG interface.

Verilog Code:

```

pgreset <= not sresetn;

ided7rdrn <= '0' when (idecs0n = '0' and gpior0n = '0') or
              (idecs1n = '0' and gpi0a0 = '0' and gpior0n = '0')
              else '1';

ided7wrn <= '0' when (idecs0n = '0' and gpior0n = '0') or
              (idecs1n = '0' and gpi0a0 = '0' and gpior0n = '0')
              else '1';

idehoen <= '0' when (gpiorcs16n = '0' and idecs0n = '0' and (gpior0n = '0' or gpior0n = '0'))
              else '1';

ideloen <= '0' when (gpiorcs16n = '0' and idecs0n = '0' and (gpior0n = '0' or gpior0n = '0'))
              else '1';

-- add in gpiorcs16n to limit when OE can be asserted.

rstdrvna <= not pgregset;

```

External Components and Connections:

- Capacitors:** C48, C73, C53, C256 (all 0.1μF, CAP-1000U1ASC, 1.4).
- Resistors:** RN20, RN17, RN22, RN18, RN21, R88, R87, R85 (all 1K, RES-30001K5FC, 1.4).
- Connectors:** J15 (Xilinx CPLD JTAG ISP Interface), CON5 (CON-S00006GMN, 1).
- Power/Ground:** VCC3, GND1, GND2, GND3.

Logic Block Details:

- Inputs:** GPDBUF0E#, GPOR0E#, GPOR0W#, IDECS0#, IDECS1#, GPORCS16#, GPA0, SRESET#, PLDTCK, PLDTMS, PLDTDI, PLDTDO.
- Outputs:** IDELOE#, IDEHOE#, IDE7WR#, IDE7RDR#, PRGRESET, IDELOEN#, IDEHOEN#, IDE7WRN#, IDE7RDRN#, pgregset, rstdrvna.

INTERPLANE CAPACITORS

The diagram illustrates the placement of interplane capacitors between two power planes, VCC_CPU and VCC3. Five capacitors, labeled C225, C206, C216, C217, and C223, are connected in parallel between the two planes. Each capacitor is represented by a blue double-line symbol with the following specifications: 0u01F, CAP-100U0155C, and 1.4. The capacitors are positioned at regular intervals along the horizontal connection line. Below the diagram, a text label states: "Place amongst signals where they cross between power planes."

VCC_CPU

C225
0u01F
CAP-100U0155C
1.4

C206
0u01F
CAP-100U0155C
1.4

C216
0u01F
CAP-100U0155C
1.4

C217
0u01F
CAP-100U0155C
1.4

C223
0u01F
CAP-100U0155C
1.4

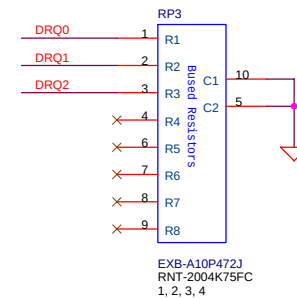
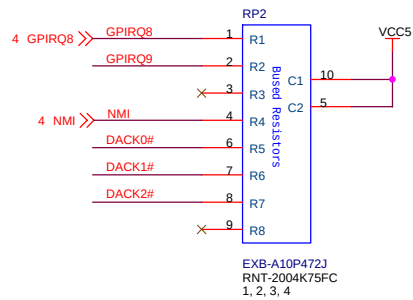
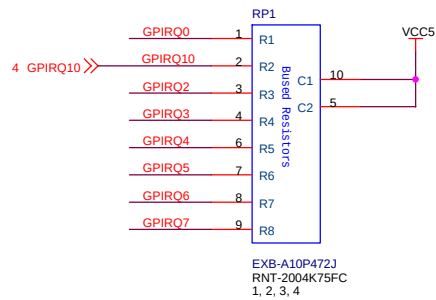
VCC3

Place amongst signals where they cross
between power planes.

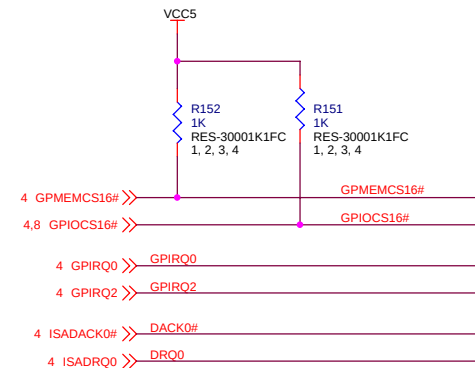
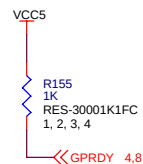
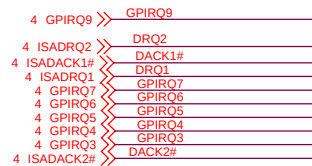
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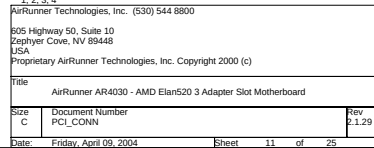


Design Notes:
Note: Pull-up Rs on IRQs

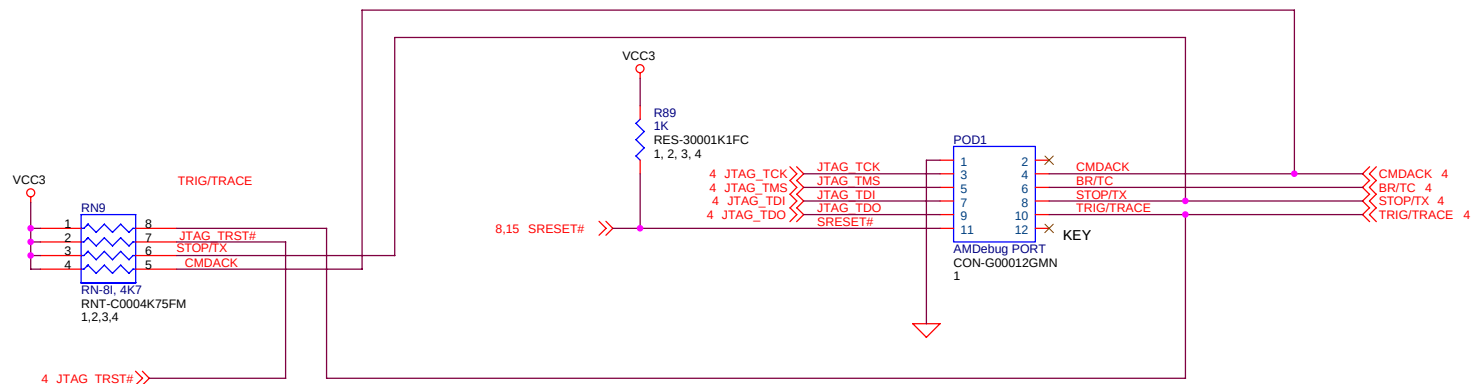


Remove ISA bus
Leave pull-ups for control signals from CPU

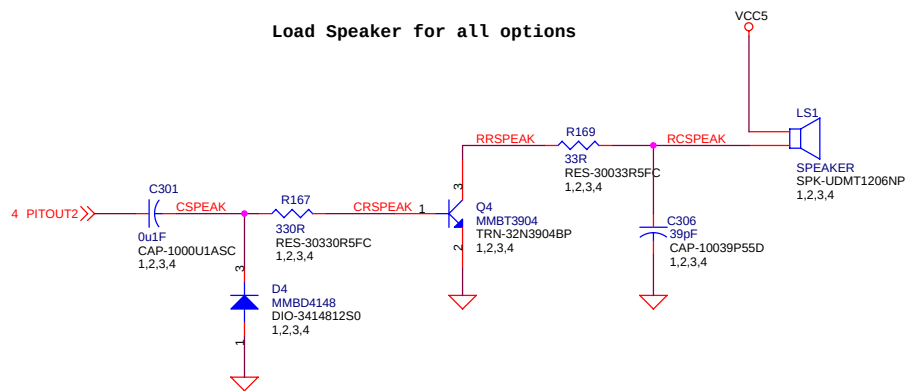
PCI Connectors



JTAG & AMDebug Port



Load Speaker for all options



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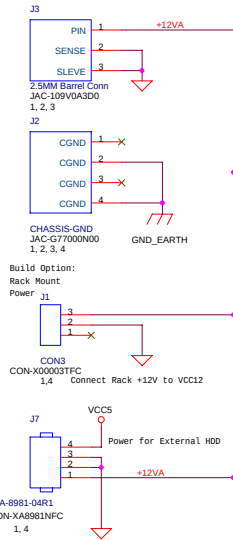
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Power Connector
Use 12V Power Cube
Mfg X/ Part Number
X

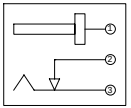
MAIN POWER

Build Option: Desktop Power



Follow Linear Technologies design notes and demo board layout for LT1374CR.

Build Option: Disk Drive
Powerex Order#: 15-24-4041



SOT-23 LED
(COMPONENT SIDE VIEW)

MRB0520LT1
CATHODE (2)



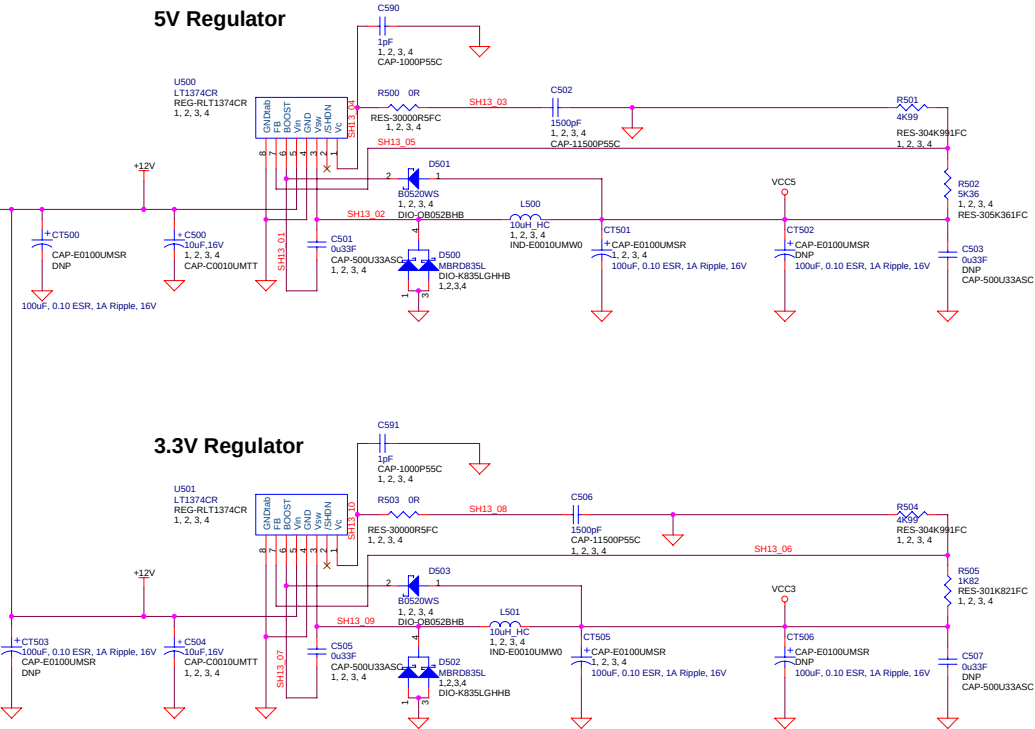
ANODE (1)

MRBS340T3
CATHODE (2)

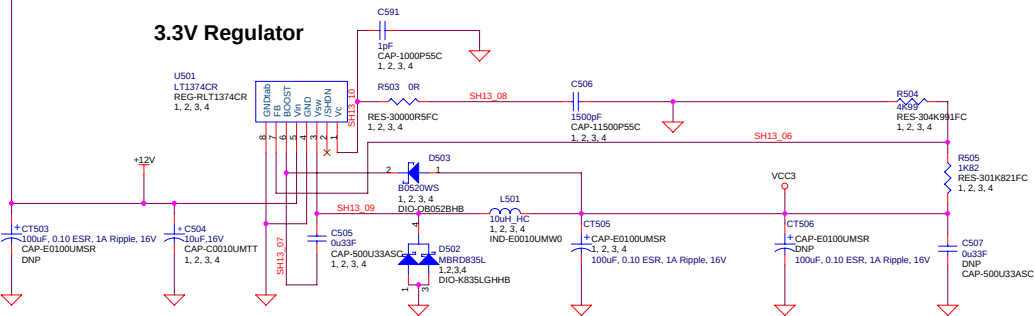


ANODE (1)

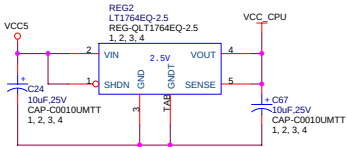
5V Regulator



3.3V Regulator

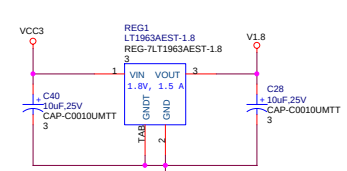


2.5V Regulator



3A 2.5V capability

1.8V Regulator

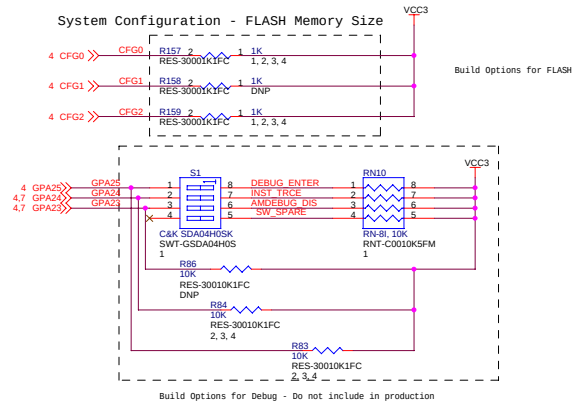


1.5A 1.8V capability

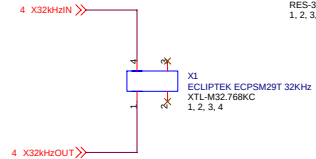
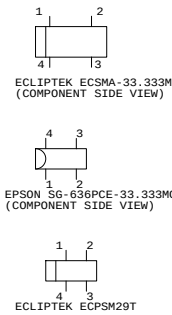
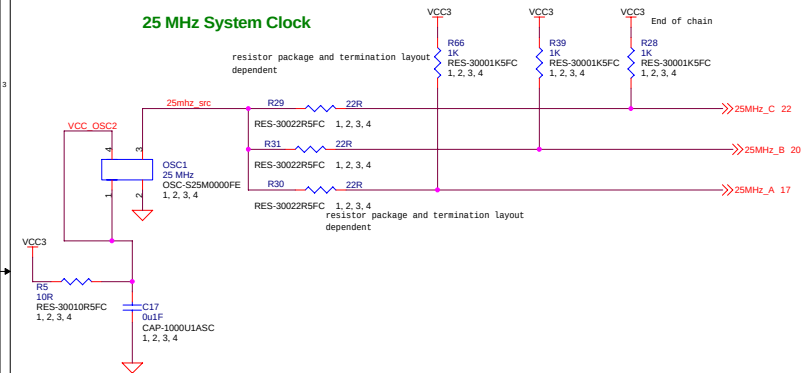
1.8V only loaded and used on 4-port build option

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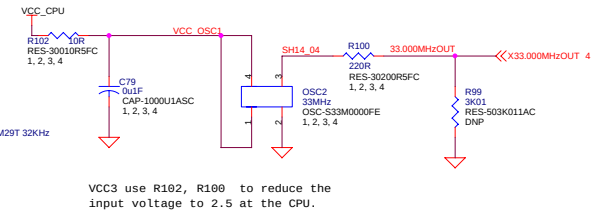
System Clocks & Boot Straps



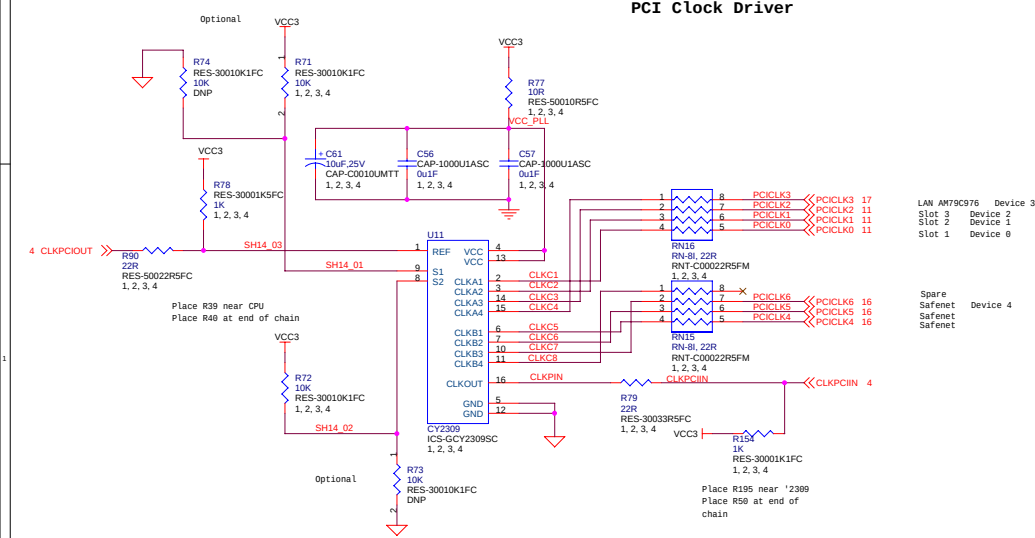
25 MHz System Clock



System Clock

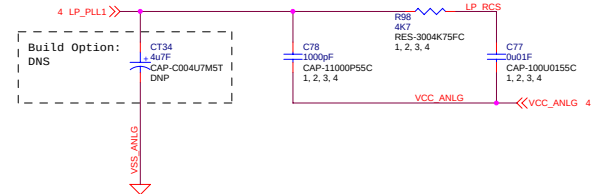


PCI Clock Driver



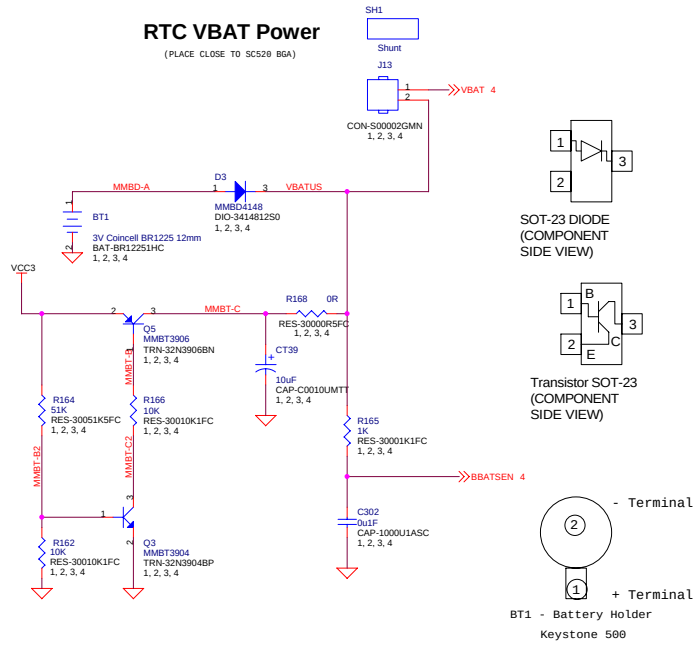
ISA Clocks Removed

PLL Loop Filter

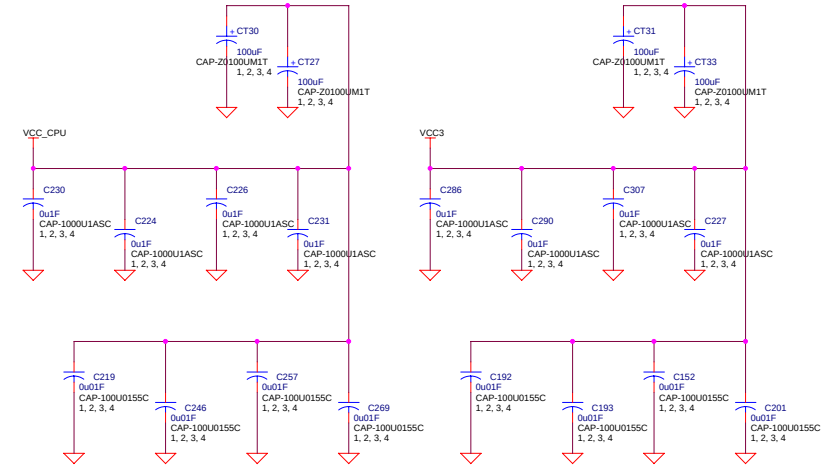


RTC VBAT Power

(PLACE CLOSE TO SC520 BGA)

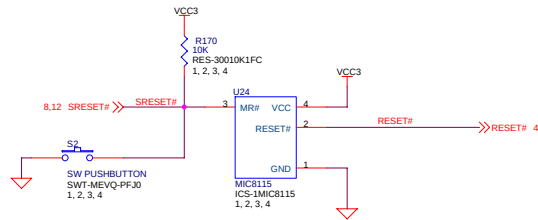


VCC_CPU Decoupling

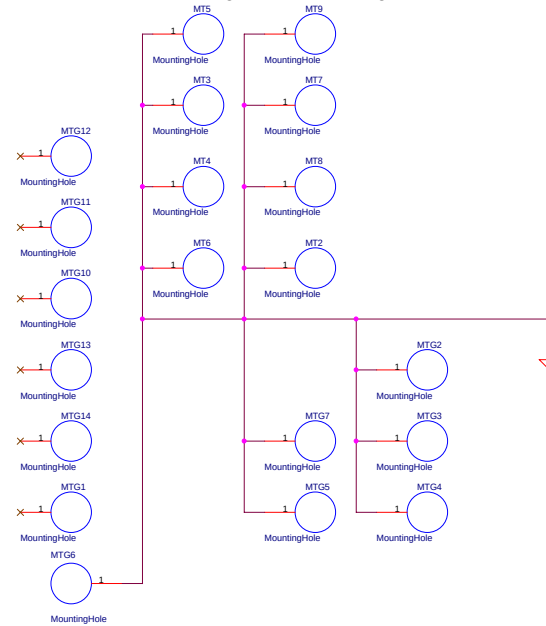


Place the above Caps under the
BGA (Back side of the board)
Check on tants about rear
placement - maybe height
restrictions

System Reset Control



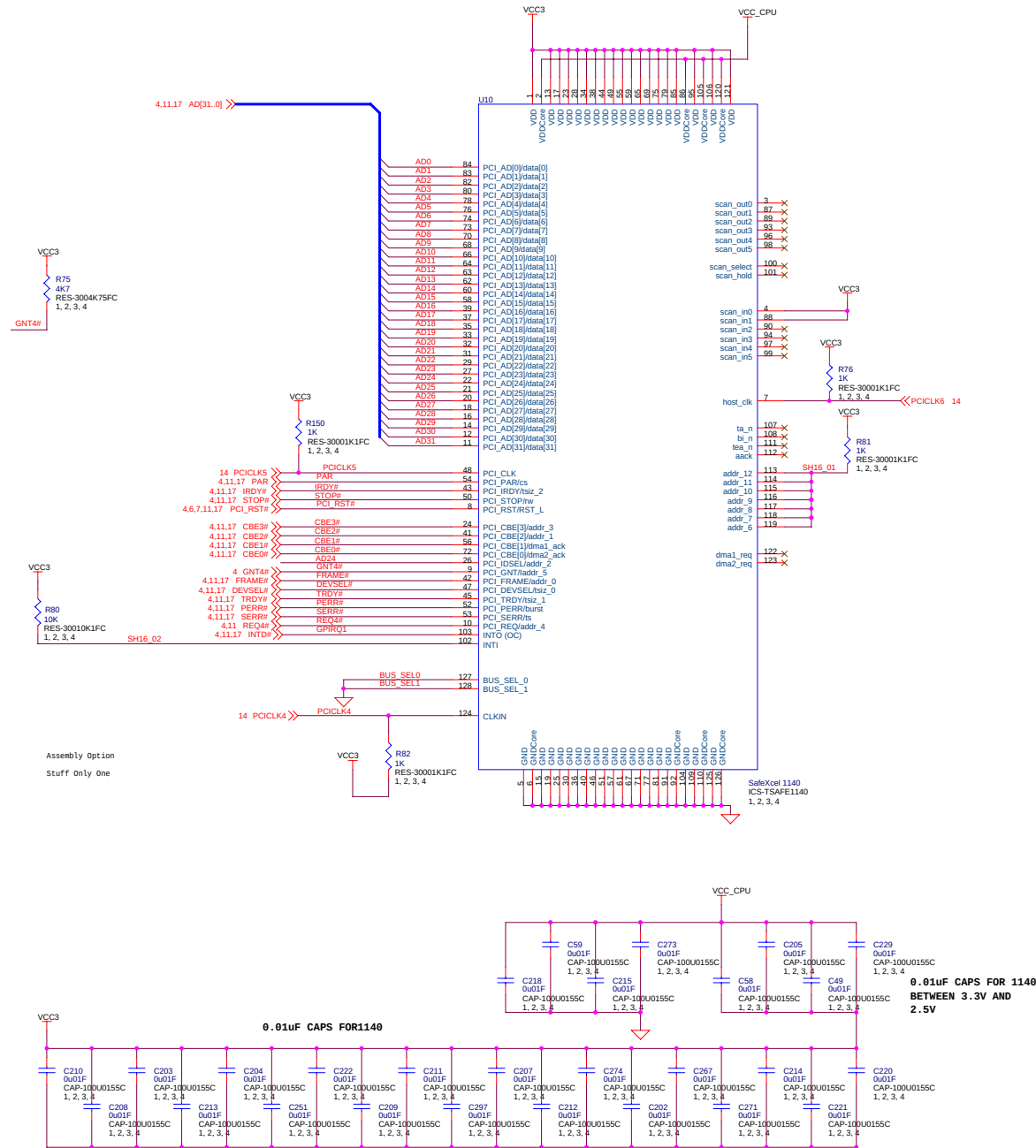
Mounting Hole Grounding

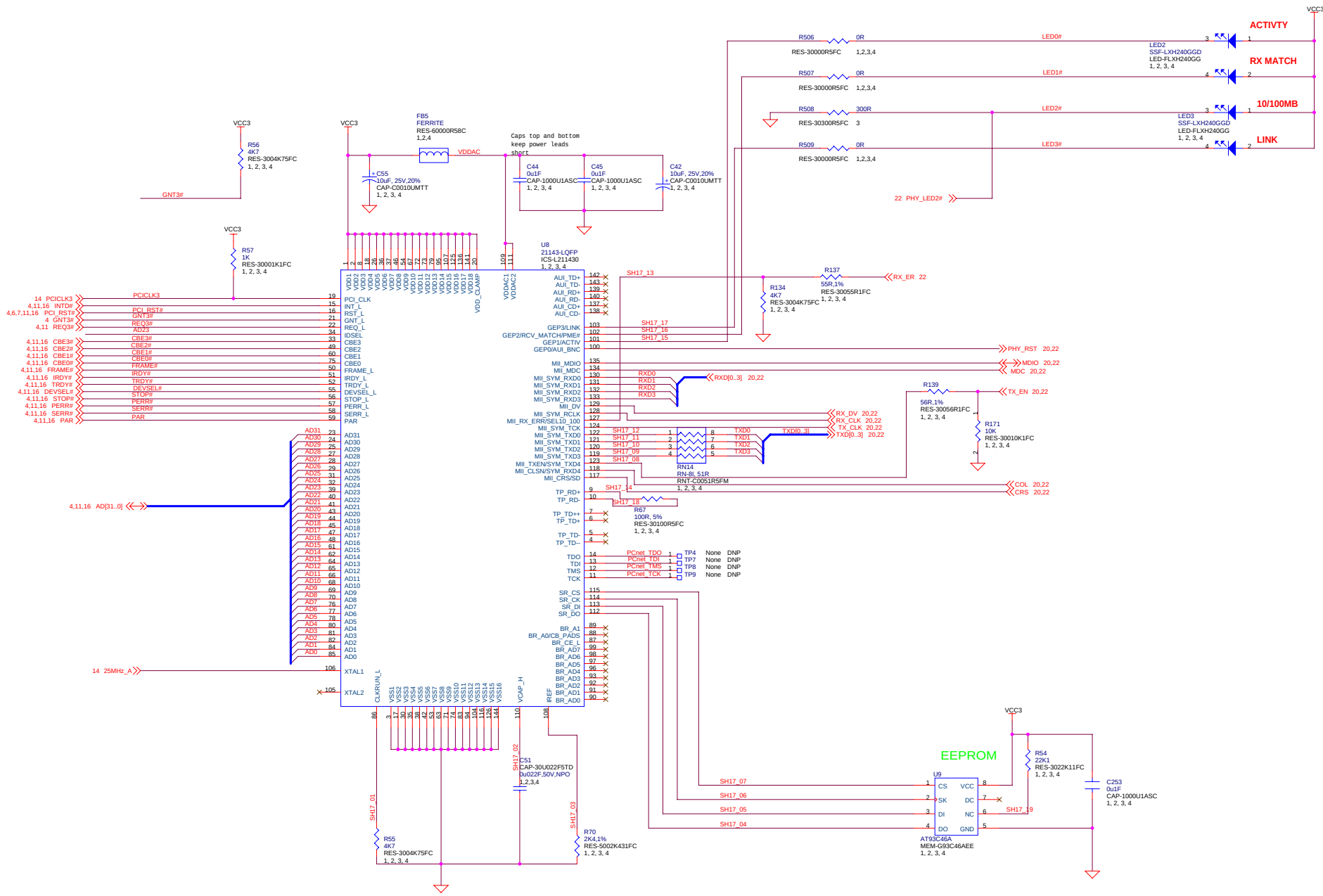


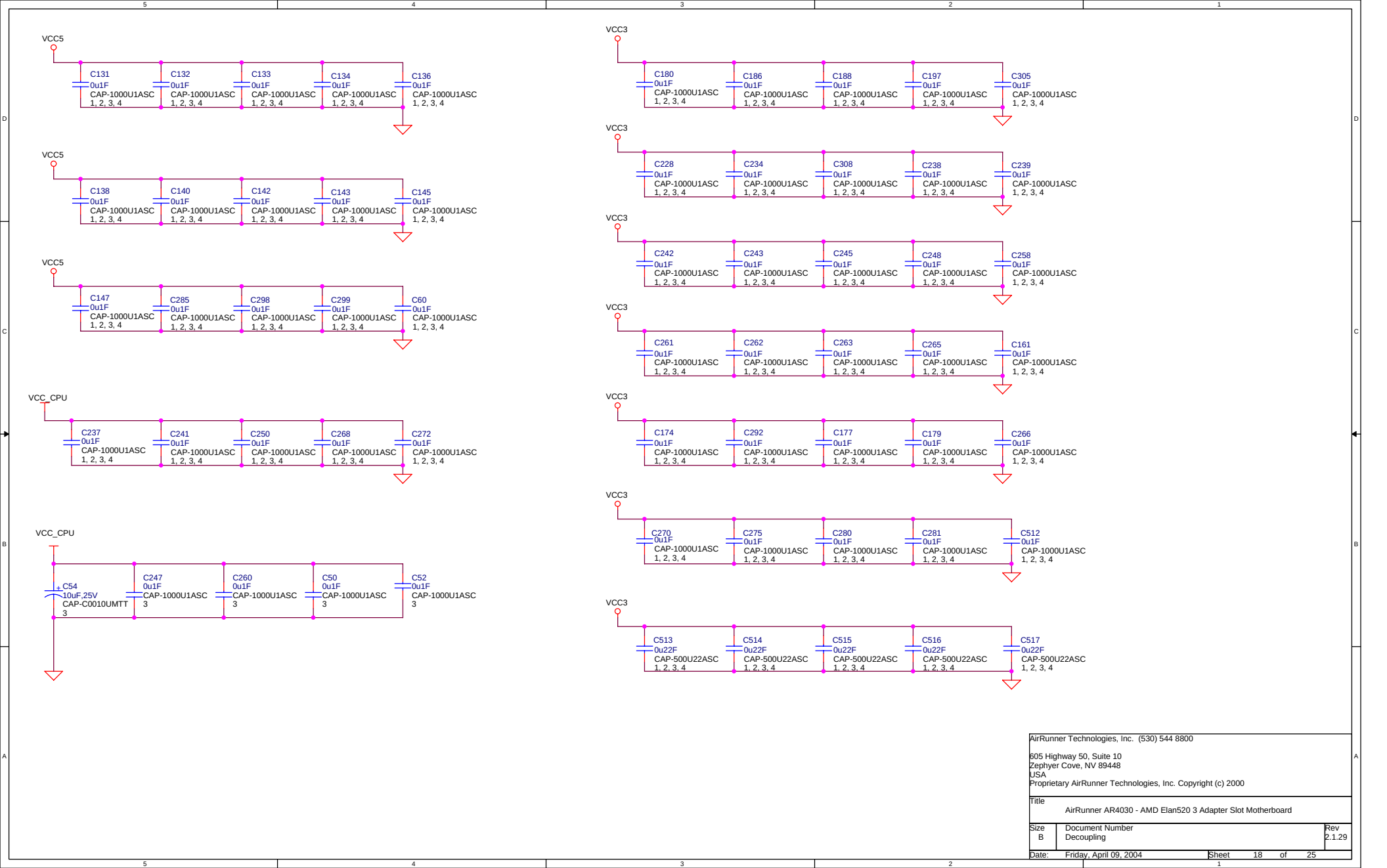
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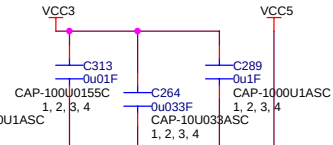
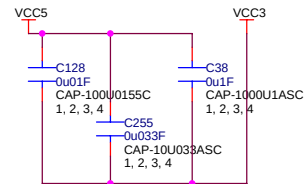
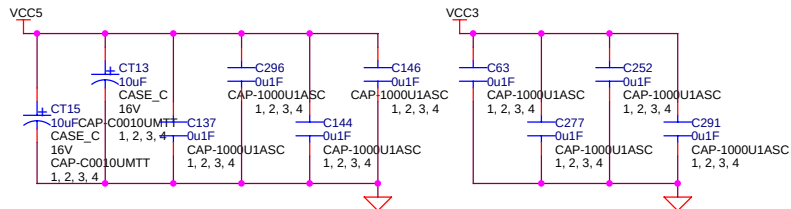
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SafeNet CRYPTO CORE

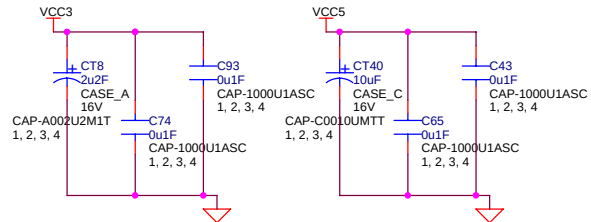
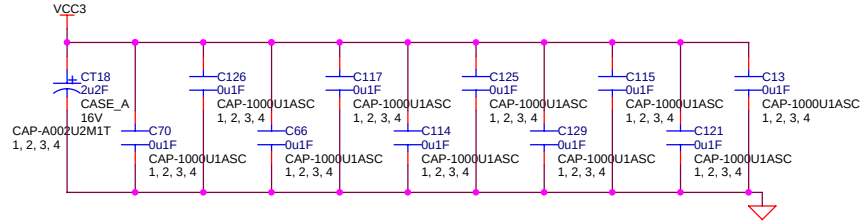
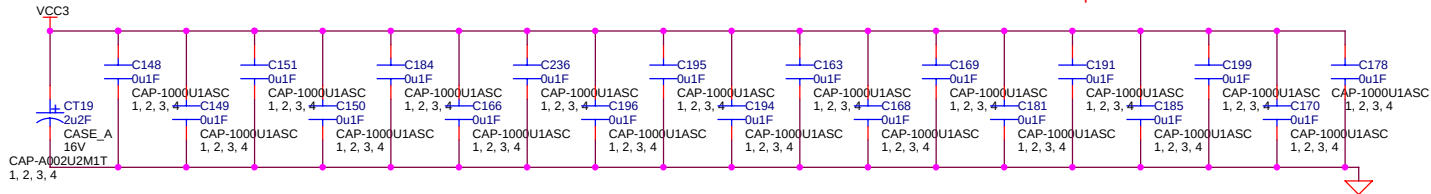




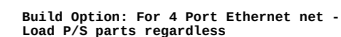




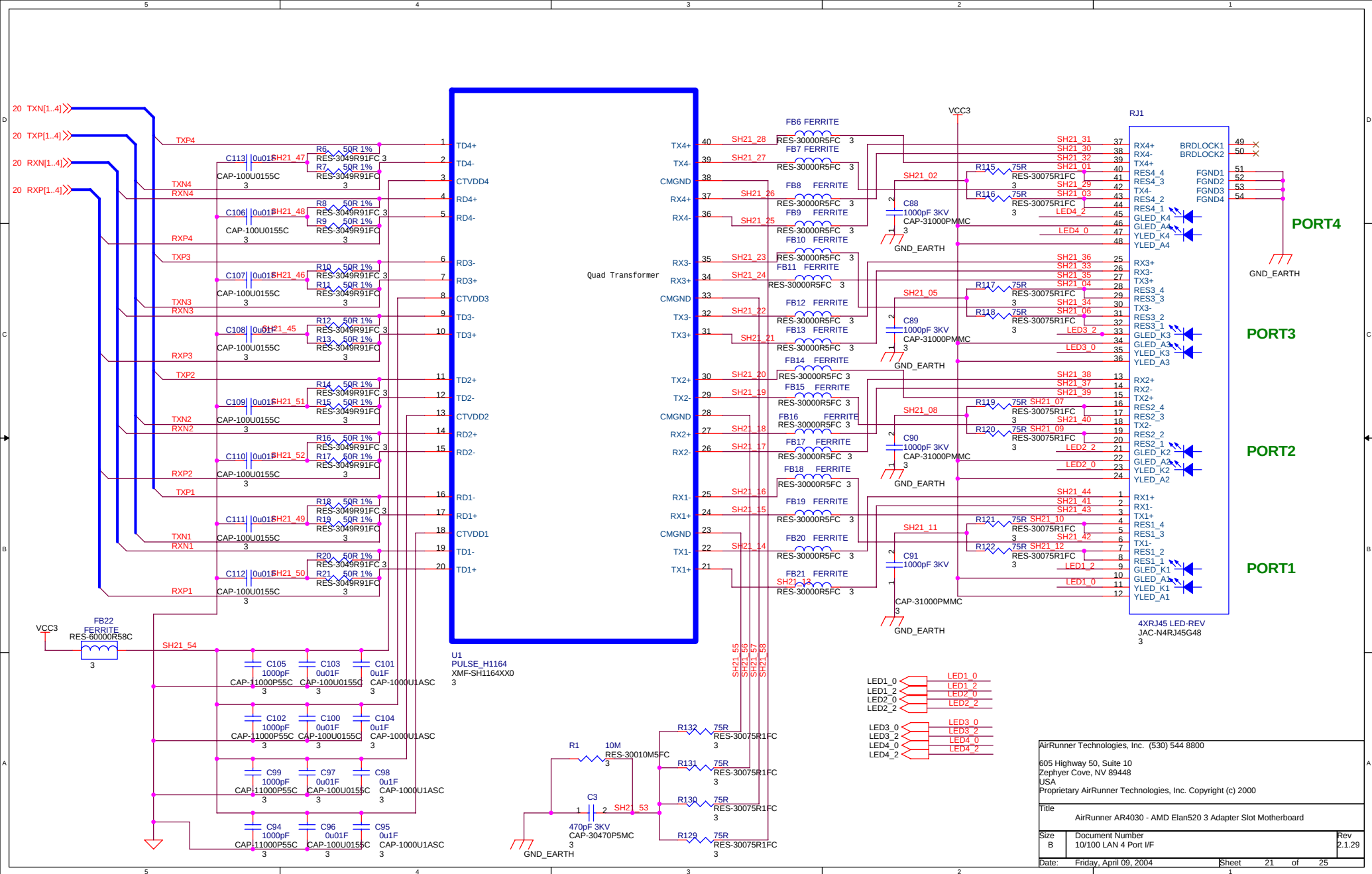
The schematic diagram illustrates a 10-bit DAC using a R-2R ladder network. The circuit is powered by VCC3 and has a common ground. The ladder consists of 10 stages, each with a 10k resistor (R1-R10) and a 100nF capacitor (C1-C10). The input voltages are V1 through V10, each connected to a 10k resistor (R1-R10) and a 100nF capacitor (C1-C10). The output of the ladder is connected to a 10k resistor (R11) and a 100nF capacitor (C11). The output voltage is VOUT.



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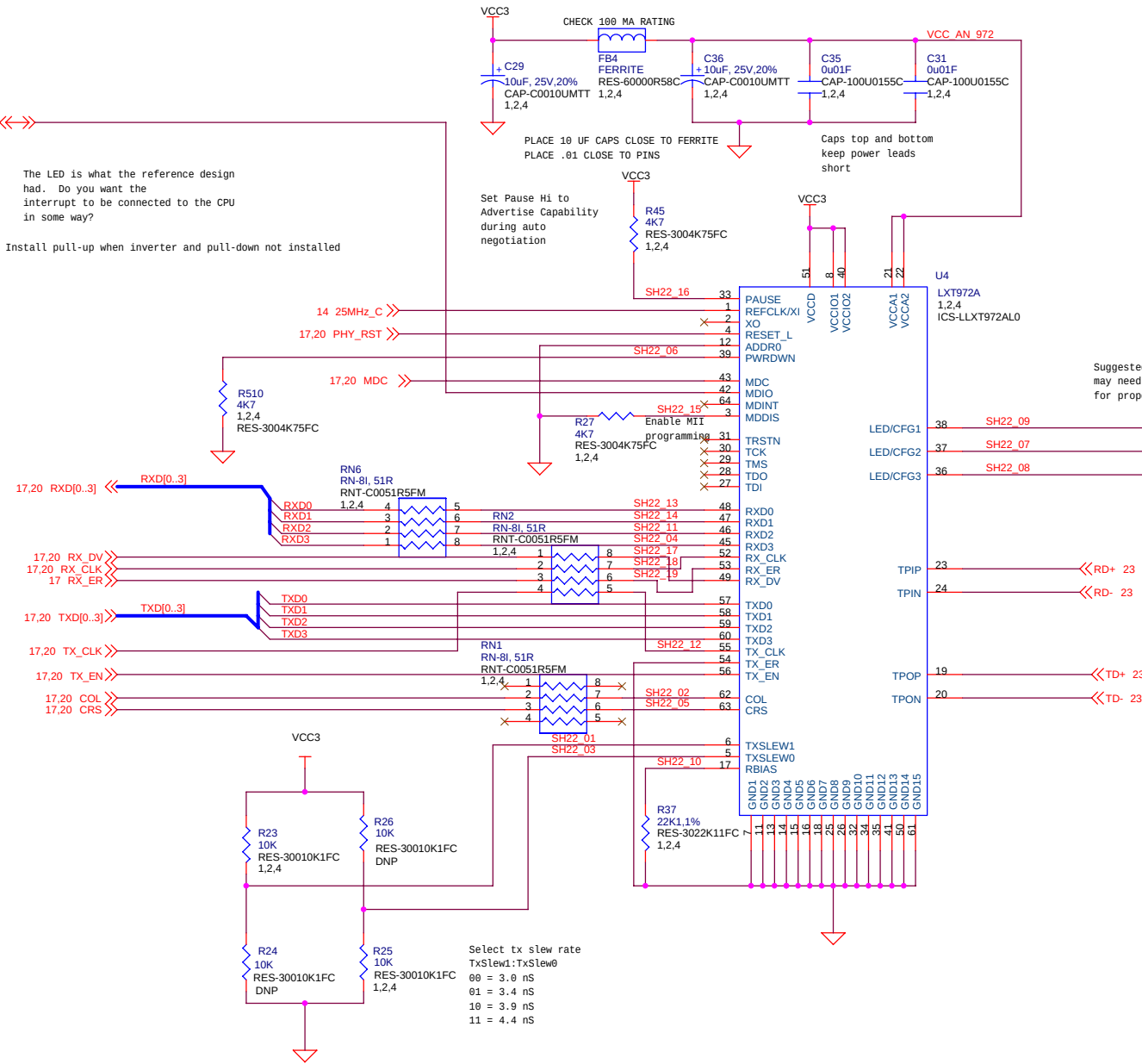
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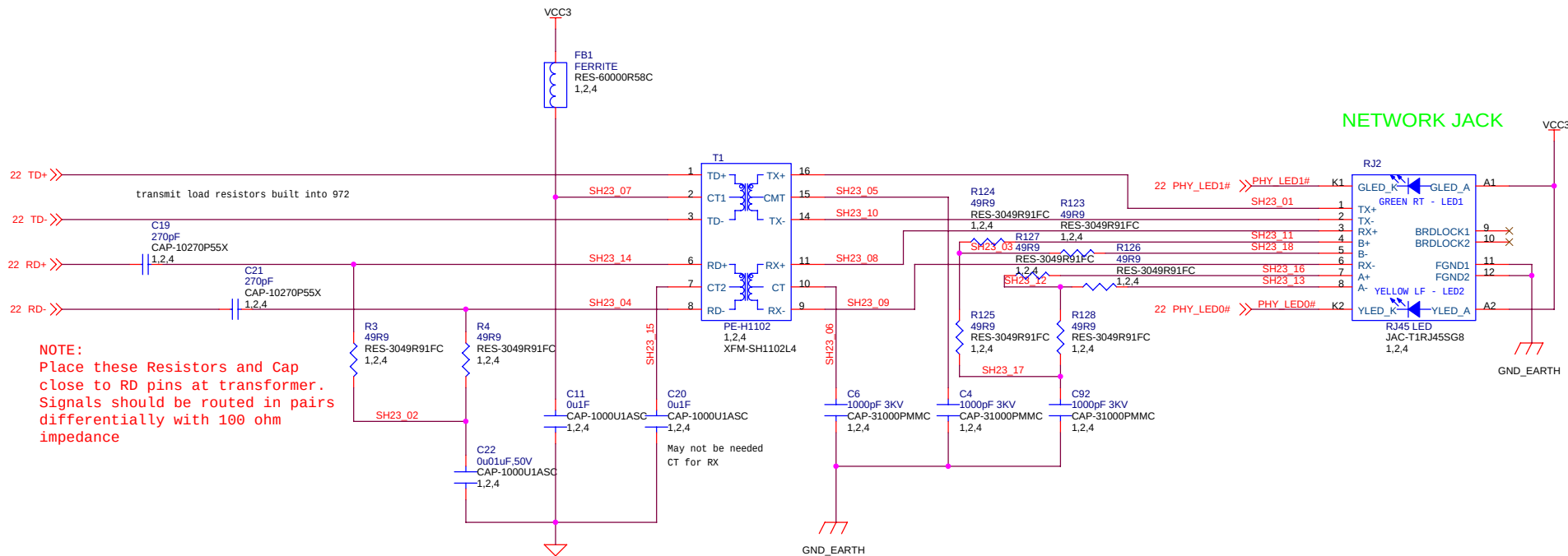
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Build Option 1, 2, 4

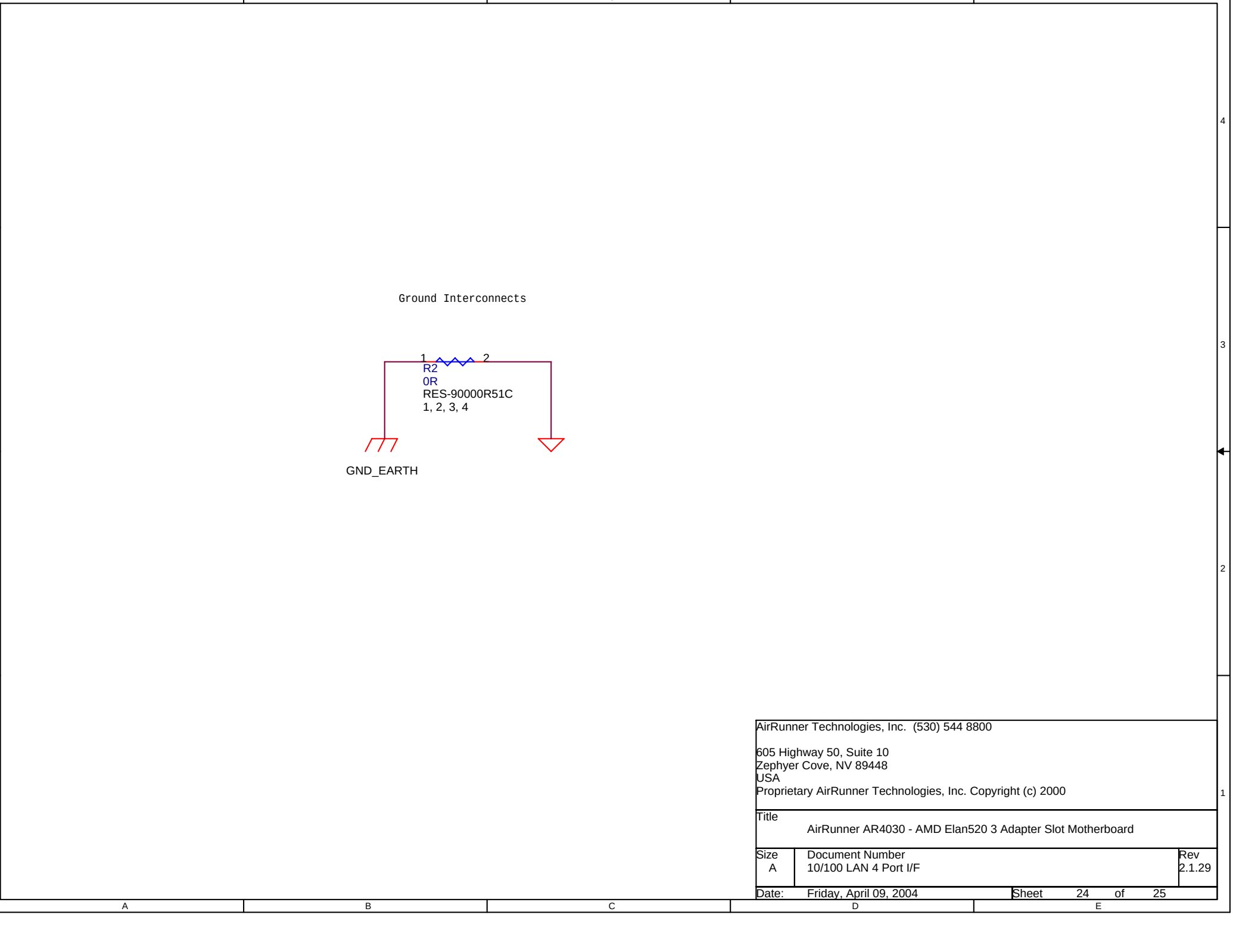
The LED is what the reference design had. Do you want the interrupt to be connected to the CPU in some way?
Install pull-up when inverter and pull-down not installed



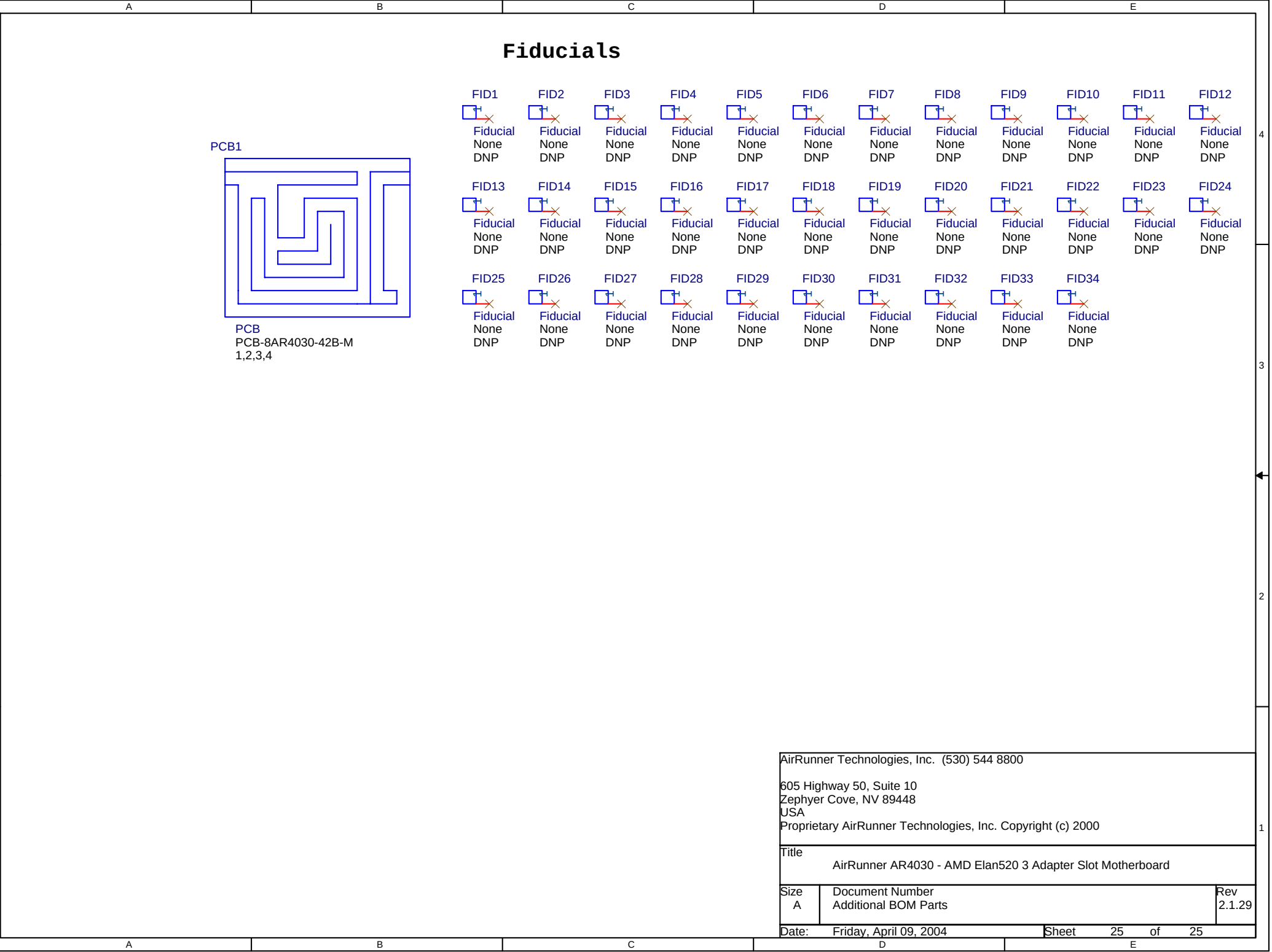
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Fiducials

FID1 Fiducial None DNP	FID2 Fiducial None DNP	FID3 Fiducial None DNP	FID4 Fiducial None DNP	FID5 Fiducial None DNP	FID6 Fiducial None DNP	FID7 Fiducial None DNP	FID8 Fiducial None DNP	FID9 Fiducial None DNP	FID10 Fiducial None DNP	FID11 Fiducial None DNP	FID12 Fiducial None DNP
FID13 Fiducial None DNP	FID14 Fiducial None DNP	FID15 Fiducial None DNP	FID16 Fiducial None DNP	FID17 Fiducial None DNP	FID18 Fiducial None DNP	FID19 Fiducial None DNP	FID20 Fiducial None DNP	FID21 Fiducial None DNP	FID22 Fiducial None DNP	FID23 Fiducial None DNP	FID24 Fiducial None DNP
FID25 Fiducial None DNP	FID26 Fiducial None DNP	FID27 Fiducial None DNP	FID28 Fiducial None DNP	FID29 Fiducial None DNP	FID30 Fiducial None DNP	FID31 Fiducial None DNP	FID32 Fiducial None DNP	FID33 Fiducial None DNP	FID34 Fiducial None DNP		

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